Electronics Workshop Project - 1

Audio Amplifier

Course Code: EC2.202
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Overview of the Project

The objective of this project was to design an audio amplifier which takes in a sound input via a mic and amplifies it to suitable level to drive an 10Ω load, within a power budget of 1.5W

Project Specifications –

1. Supply Voltage = -5 V to 5 V
2. Input small signal voltage = 10–20 mV peak-to-peak
3. Gain = $G_1 \times G_2 \geq 500$ (Pre-amp and Gain stage)
4. Frequency = Audible Range (20 Hz to 20 kHz)
5. Power $\geq$ 1.5 W
6. Filter **should not** attenuate the input signal
7. Power Amplifier **should not** provide voltage gain
8. Load = 10 Ω

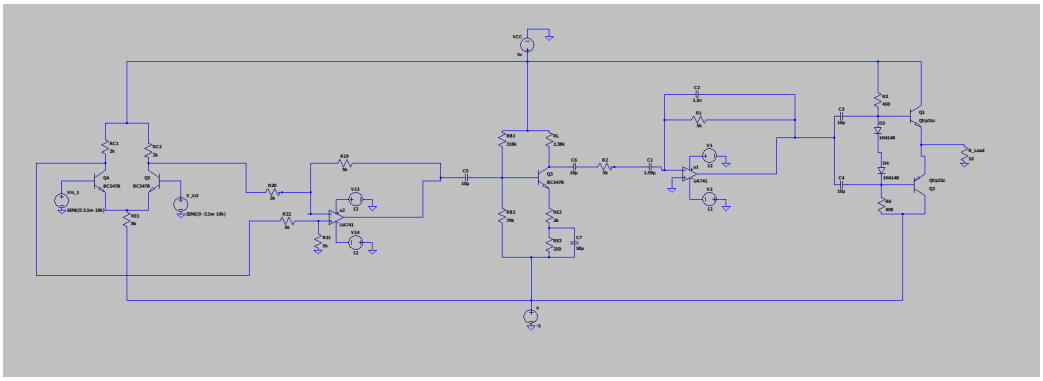

Figure 1: Amplifier Schematic - LTSpice

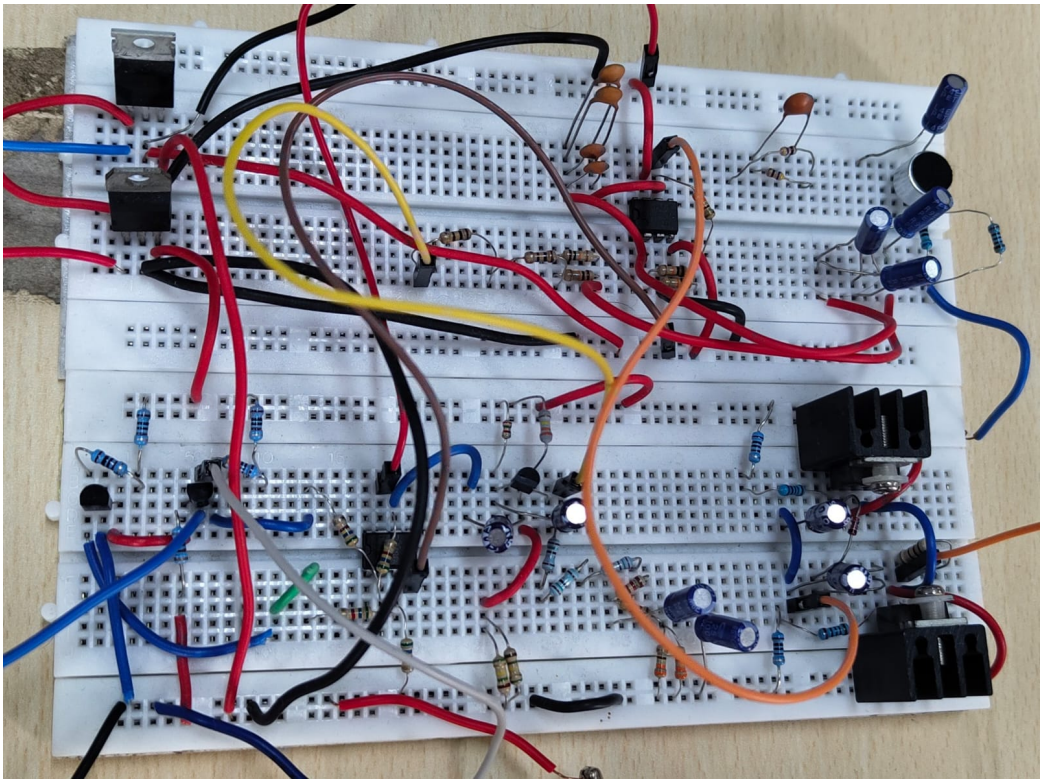

Figure 2: Hardware Implementation

The performance of an audio amplifier is based upon 4 major parameters:

- Frequency Response
- Noise
- Gain
- Distortion

This Project consists of 4 main stages. The first stage is the pre-amplifier which provides a minimal gain. The purpose of pre-amp is to eliminate noise. The second stage is the common emmiter amplifier (CE amp) stage which provides us the necessary voltage gain. The third stage is a band pass filter with a cuttoff frequency of 20Hz and 20kHz and the fourth stage is a class AB Power amplifier used to achieve the necessary power levels.

1 Pre-Amplifier

The input electrical signal cannot be directly fed into the common-emitter amplifier or power amplifier, as this would result in excessive noise, making it unsuitable for driving the load (speaker). Therefore, the signal must first be amplified to a sufficient level to withstand noise and reach line level. This is achieved in the pre-amplifier stage.

A pre-amplifier should have a high input impedance to minimize the current required for sensing the input signal and a low output impedance to prevent voltage drops at the output. This stage, known as the pre-amplifier stage, is implemented using a differential amplifier in a single-ended, unbalanced output configuration, where one input is connected to the microphone and the other is grounded.

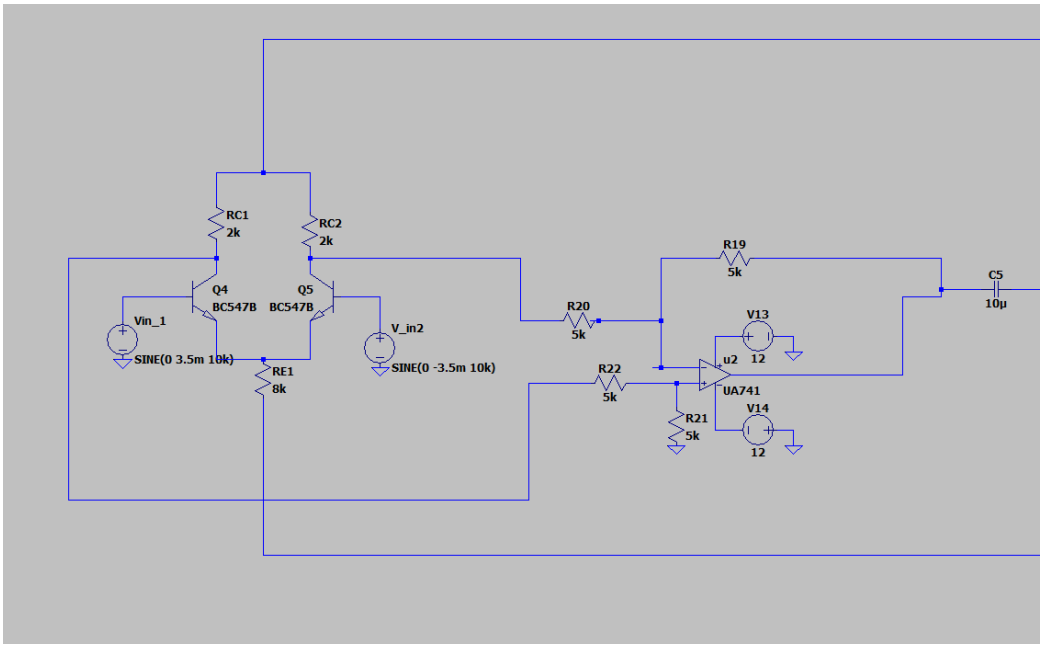

Figure 3: Differential Amplifier Schematic

The differential amplifier de-noises and amplifies an input signal of amplitude 10mV - 20 mV pp to an output signal of amplitude 140mV - 280mV pp, which is a gain of 14, close to the simulation gain of ≈ 15.

DC Analysis

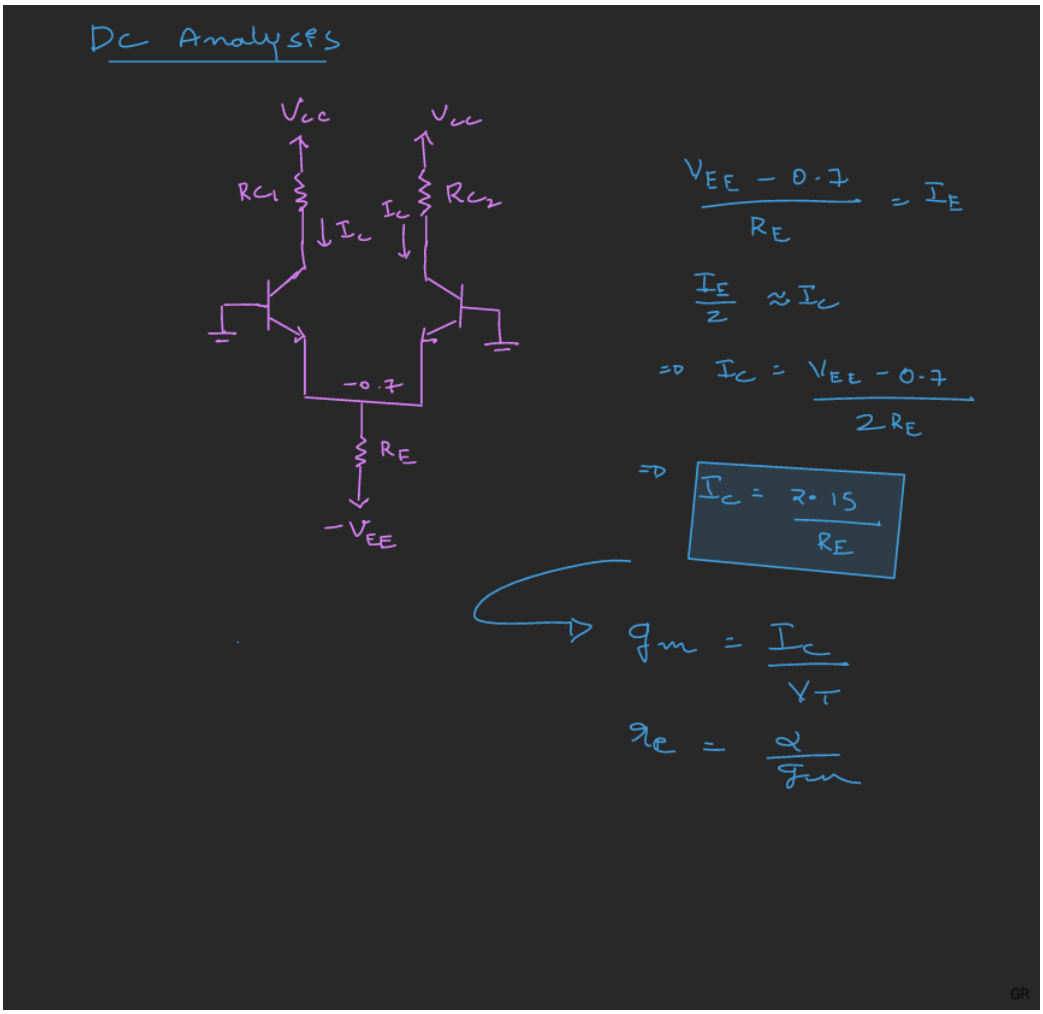

Figure 4: DC Analysis

AC Analysis:

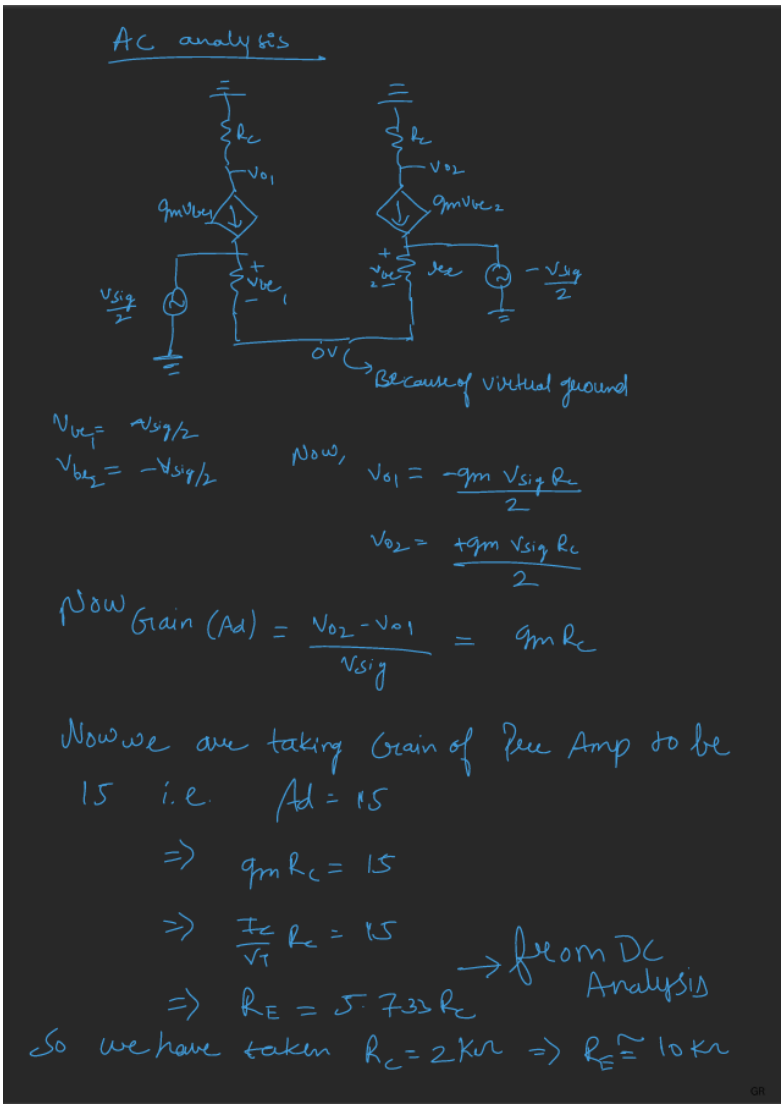

Figure 5: Differentaial Amp Small Signal Analysis

Common Mode Rejection Ratio CMRR
The CMRR is found using:

$$CMRR = 20 \log \left(\frac{A_d}{A_c} \right)$$

For our Differential Amplifier, the common mode gain is $A_c = 39.4 \times 10^{-6}$ and the differential gain is $A_d = 15$. The Common-Mode Rejection Ratio (CMRR) is given by:

$$CMRR = 20 \log \left(\frac{A_d}{A_c} \right)$$

Substituting the values:

$$CMRR = 20 \log \left(\frac{15}{39.4 \times 10^{-6}} \right)$$

$$CMRR = 20 \log(380456)$$

$$CMRR = 20 \times 5.58$$

$$CMRR = 111.6 \text{ dB}$$

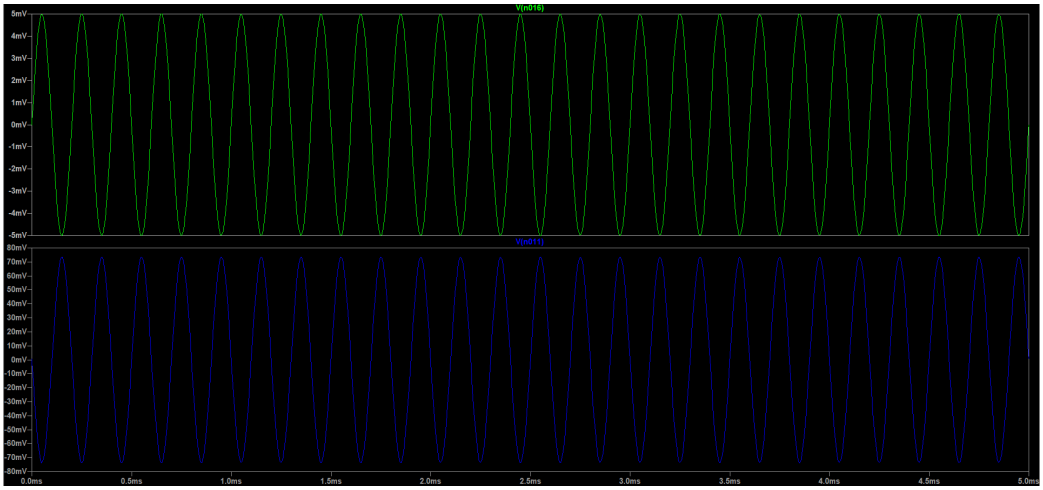

Figure 6: Simulation o/p for Pre-Amp stage

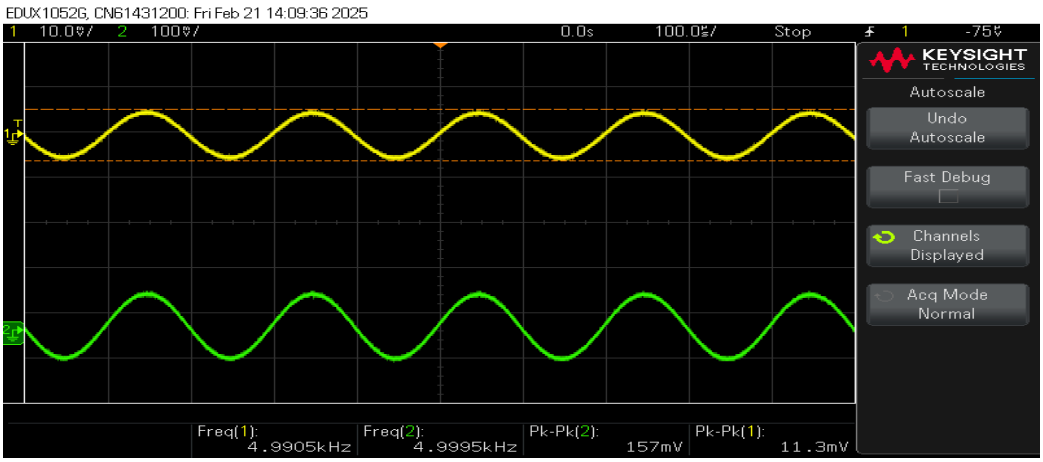

Figure 7: Pre Amp stage Hardware plots

2 Common Emitter Amplifier

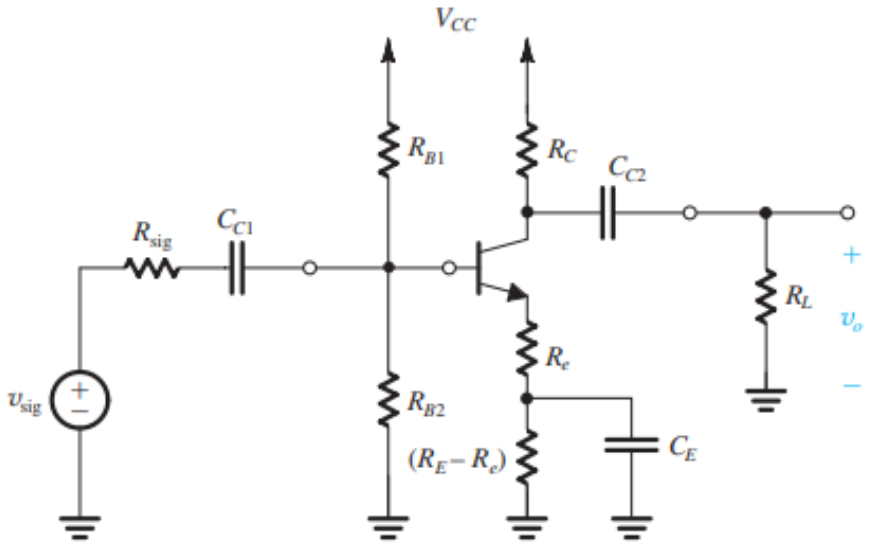

Figure 8: CE Amplifier

- **Input Capacitor C_1:**
  C_1 is used to block the DC components of the input signal, introducing a pole into the system. Since the frequency of interest lies between 20 Hz and 20 kHz, C_1 is chosen to allow frequencies below 20 kHz to pass. If C_1 is too small, the low-frequency components will be attenuated, resulting in a larger bias current I_B which decreases the current gain.

- **Emitter Capacitor C_E:**
  C_E blocks DC current from flowing to ground.

- **Coupling Capacitor C_2:**
  C_2 introduces a second pole into the system and provides AC coupling to the filtering stage.

- **Biasing Resistors R_{B1} and R_{B2}:**
  These resistors form a voltage divider with V_{CC} to bias the transistor, ensuring that the base-emitter junction is forward biased while the base-collector junction remains reverse biased.

- **Stability Factor:**
  The stability factor is given by:

$$S = \left.\frac{\delta I_C}{\delta I_{CBO}}\right|_{V_{BE},\beta}$$

  Specifically, since

$$I_C = \beta I_B + (\beta + 1) I_{CBO},$$

  differentiating with respect to I_C yields:

$$\frac{\delta I_C}{\delta I_C} = \beta \frac{\delta I_B}{\delta I_C} + \frac{\beta + 1}{S}.$$

Therefore, the stability factor can be expressed as:

$$S = \frac{\beta + 1}{1 - \beta \frac{\delta I_B}{\delta I_C}}.$$

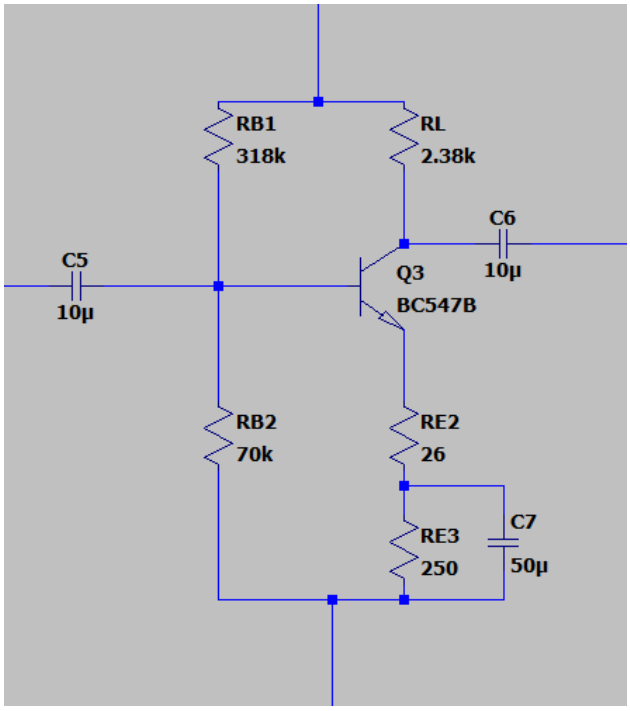

Figure 9: CE Amplifier Schematic

DC and AC Anaysis of CE Amplifier

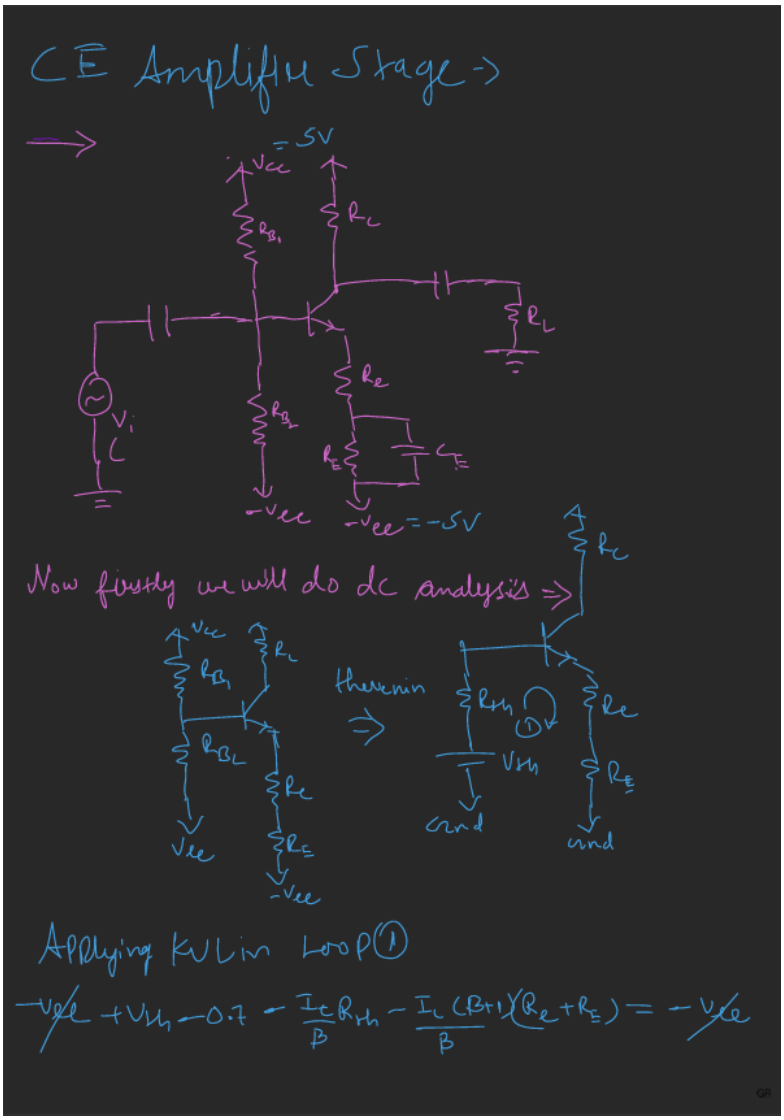

Figure 10:

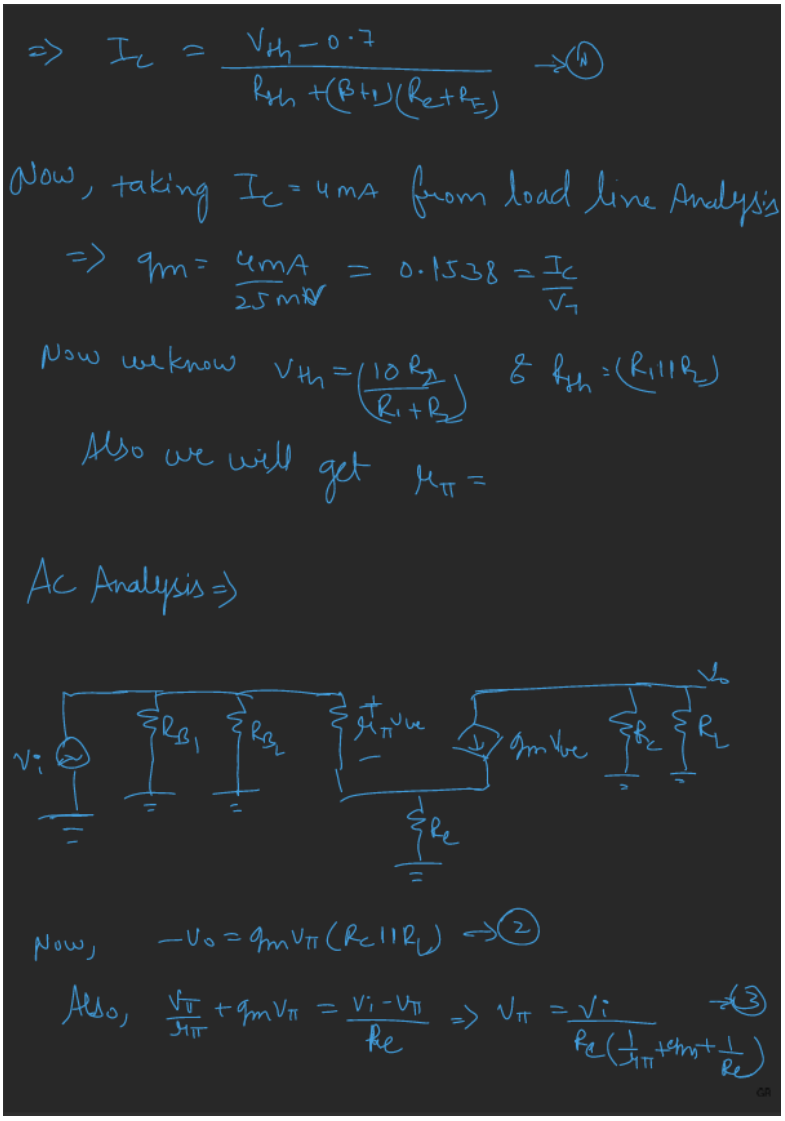
=> $I_C = \frac{V_{Th} - 0.7}{R_{th} + (\beta+1)(R_E + R_E)}$ → (1)
Now, taking $I_C = 4mA$ from load line Analysis
=> $g_m = \frac{4mA}{25mV} = 0.1538 = \frac{I_C}{V_T}$
Now we know $V_{Th} = \left(\frac{10 R_2}{R_1 + R_2}\right)$ & $R_{th} = (R_1 \| R_2)$
Also we will get $r_\pi =$
Ac Analysis =>
V_i
R_{B_1}
R_{B_2}
r_π
V_π
$g_m V_{be}$
R_C
R_L
V_o
R_E
Now, $-V_o = g_m V_\pi (R_C \| R_L)$ → (2)
Also, $\frac{V_\pi}{r_\pi} + g_m V_\pi = \frac{V_i - V_\pi}{R_E}$ => $V_\pi = \frac{V_i}{R_E\left(\frac{1}{r_\pi} + g_m + \frac{1}{R_E}\right)}$ → (3)

Figure 11:

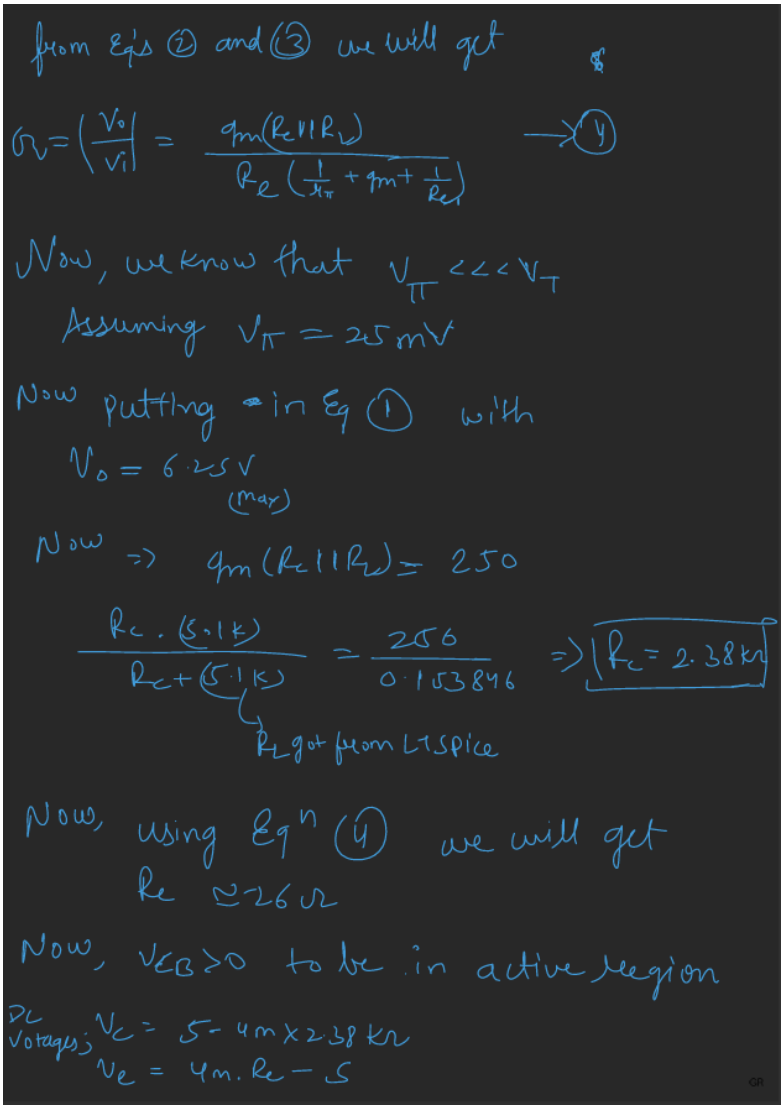
from Eqs ② and ③ we will get
$G_v = \left|\frac{V_o}{V_i}\right| = \frac{g_m(R_c \| R_L)}{R_E\left(\frac{1}{r_\pi} + g_m + \frac{1}{R_E}\right)}$ → ④
Now, we know that $V_\pi << V_T$
Assuming $V_\pi = 25\,mV$
Now putting in Eq ① with
$V_o = 6.25\,V$ (max)
Now ⇒ $g_m(R_c \| R_L) = 250$
$\frac{R_c \cdot (5.1k)}{R_c + (5.1k)} = \frac{250}{0.153846}$ ⇒ $R_c = 2.38\,k\Omega$
R_L got from LTSpice
Now, using Eqn ④ we will get
$R_E \simeq 26\,\Omega$
Now, $V_{CB} \geq 0$ to be in active region
DC Voltages; $V_C = 5 - 4m \times 2.38\,k\Omega$
$V_E = 4m \cdot R_E - 5$

Figure 12:

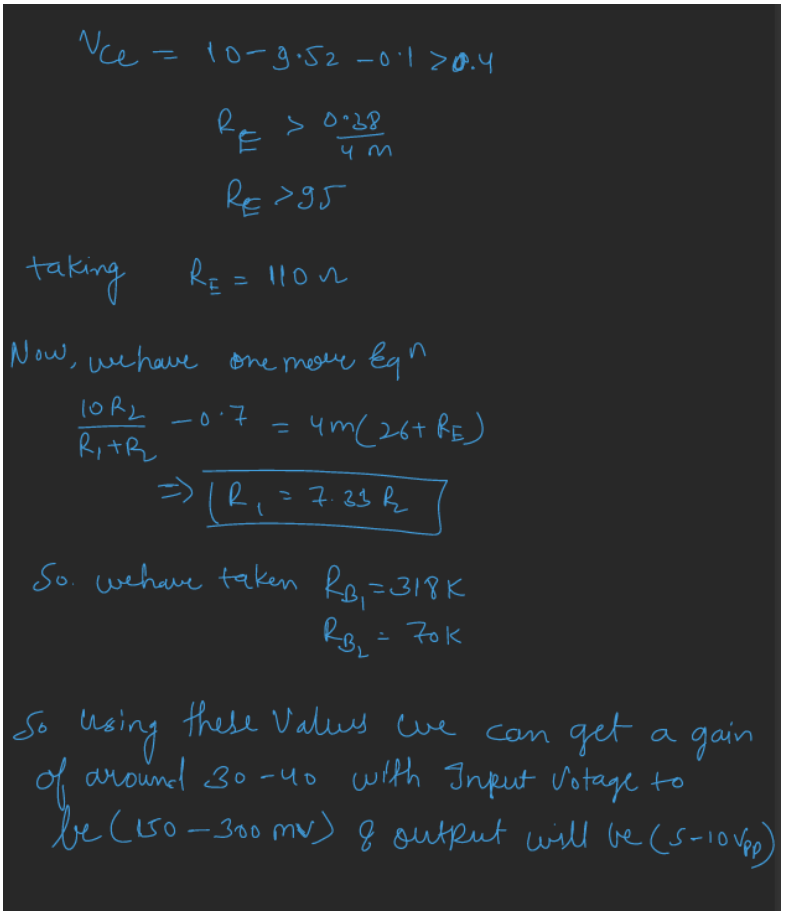
$V_{CE} = 10 - 9.52 - 0.1 > 0.4$
$R_E > \frac{0.38}{4m}$
$R_E > 95$
taking $R_E = 110\,\Omega$
Now, we have one more Eqn
$\frac{10R_2}{R_1+R_2} - 0.7 = 4m(26 + R_E)$
$\Rightarrow R_1 = 7.33 R_2$
So we have taken $R_{B_1} = 318K$
$R_{B_2} = 70K$
So using these values we can get a gain of around 30-40 with Input Votage to be (150 - 300 mV) & output will be (5-10 V_{pp})

Figure 13:

This stage takes in the output of the differential amplifier ($V_{pp} \approx 150mV$), and amplifies it further to $V_{pp} \approx 5.1V$, providing a voltage gain of 34 times for the CE stage.

Since, we have used a single common emitter amplifier stage, it introduces a phase shift. From the small signal model of a common emitter stage we know that its voltage gain is given by the following equation:

$$\text{Gain} = -\frac{R_C}{\frac{1}{g_m} + R_E}$$

which can be approximated as

$$-\frac{R_C}{R_E} \quad \text{for } R_E \gg \frac{1}{g_m}$$

The common emitter stage introduces a 180° phase shift because as the input increases i.e., the voltage at the base of the transistor increases, the current flowing through the base increases.

Since, $I_C = \beta \times I_B$, the collector current also increases which leads to more voltage being dropped across the collector resistor and hence less voltage at the output terminal; since $V_{\text{out}} = V_{CC} - I_C R_C$. This leads to an inverted output from the common emitter stage.

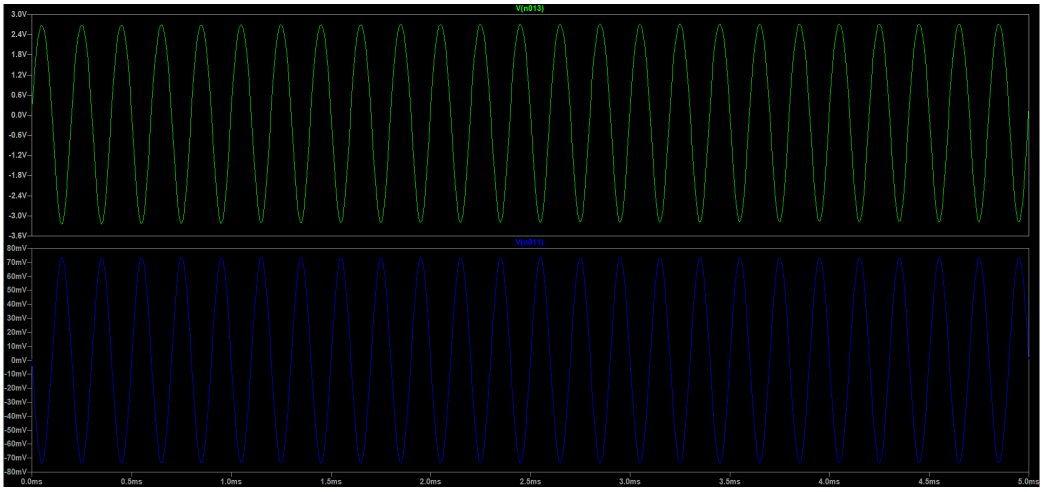

Figure 14: CE Amp Simulation

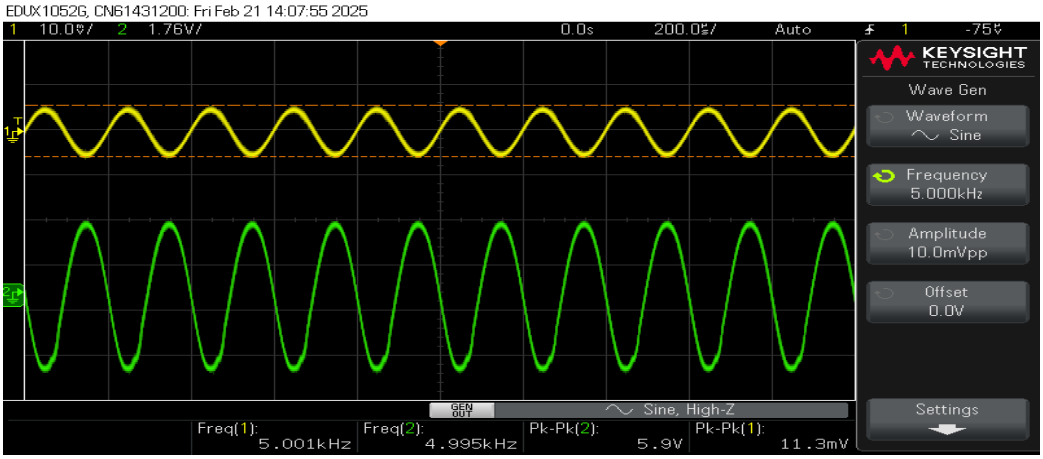

Figure 15: CE Amp Hardware o/p

3 Band-Pass Filter

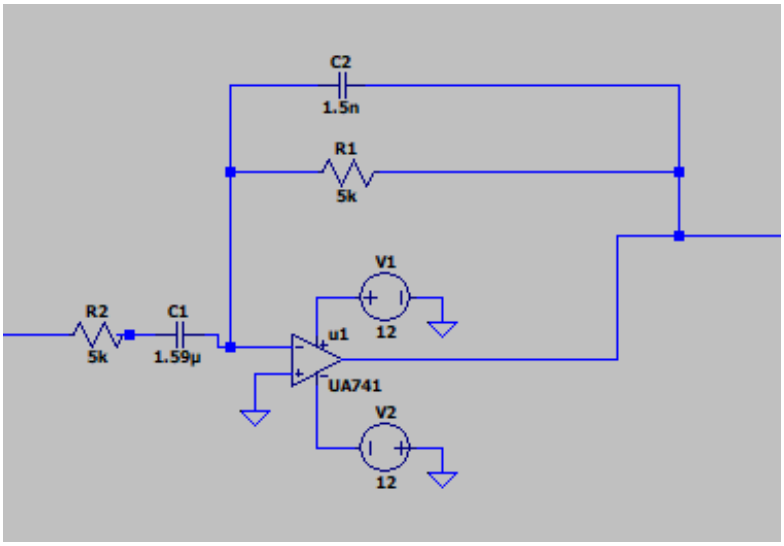

Figure 16: Band-Pass Filter Schematic

Filter Stage: Band-Pass Filter Implementation

The filter stage is typically used to adjust the balance of high and low frequencies, permitting the manual adjustment of the frequency response so that we can achieve frequency-selective amplification. This stage helps eliminate unwanted noise added in the previous stage of the system and improves the overall tone.

In our implementation, we wish to keep frequencies in the range of 20 Hz to 20 kHz (which is the ideal hearing range of a human) prominent while attenuating other frequencies. To achieve this, we have implemented a band-pass filter with a low cutoff frequency at 20 Hz and a high cutoff frequency at 20 kHz.

Gain of the Band-Pass Filter

The standard transfer function of a band-pass filter is given by:

$$H(s) = \frac{V_{\text{out}}(s)}{V_{\text{in}}(s)}$$

For the given circuit, the transfer function can be derived using impedance analysis.

1. The impedance of a capacitor is given by:

$$Z_C = \frac{1}{sC}$$

2. The circuit consists of a high-pass and low-pass combination. The impedance of the series capacitor and resistor at the input acts as a high-pass filter, while the feedback network acts as a low-pass filter.

The transfer function of an active band-pass filter is given by:

$$H(s) = \frac{\frac{s}{\omega_0}Q}{s^2 + \frac{s}{\omega_0}Q + 1}$$

where:

- $\omega_0 = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$ is the center frequency, - $Q = \frac{\sqrt{R_2/R_1}}{1+R_2/R_1}$ is the quality factor.

Gain at Resonance

At the resonant frequency ω_0, the gain of the band-pass filter is:

$$|H(j\omega_0)| = \frac{R_2}{R_1}$$

which depends on the resistor ratio.

Conclusion

The active band-pass filter amplifies signals within a certain frequency range and attenuates signals outside this range. The gain at resonance is determined by the resistor ratio, while the bandwidth and center frequency depend on the resistor and capacitor values.

For a passive band-pass filter, the gain at the center frequency f_0 is:

$$A_v = \frac{-R_2}{R_1}$$

To achieve a gain of 1, we choose:

$$R_1 = R_2 = 5k\Omega$$

Cutoff Frequency Calculations

The cutoff frequencies for a passive band-pass filter are given by:

$$f_{c,\text{low}} = \frac{1}{2\pi R C_1}$$

$$f_{c,\text{high}} = \frac{1}{2\pi R C_2}$$

where $R = 5k\Omega$ is the resistance used in both the high-pass and low-pass sections.

Solving for capacitances:

$$C_1 = \frac{1}{2\pi R f_{c,\text{low}}} = \frac{1}{2\pi \times 5 \times 10^3 \times 20} = 1.59 \times 10^{-6} \text{ F} = 1.59 \text{ µF}$$

$$C_2 = \frac{1}{2\pi R f_{c,\text{high}}} = \frac{1}{2\pi \times 5 \times 10^3 \times 20000} = 1.59 \times 10^{-9} \text{ F} = 1.59 \text{ nF}$$

Thus, the filter maintains a unity gain while allowing frequencies between 20 Hz and 20 kHz to pass and attenuating others.

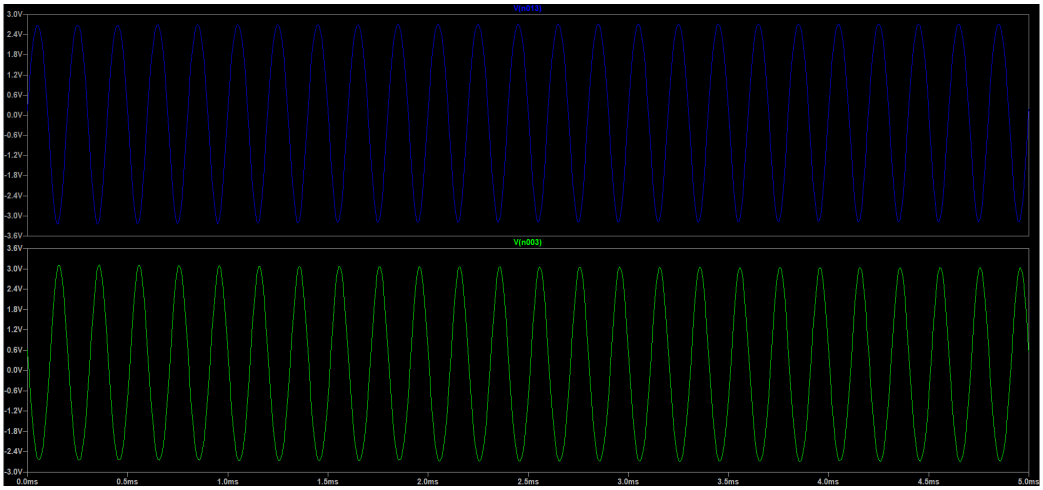

Figure 17: Band-Pass Filter Simulation o/p

We can see a 180 Degrees Phase shift from that of the CE Amp stage as the Band-Pass Filter has a negative gain.

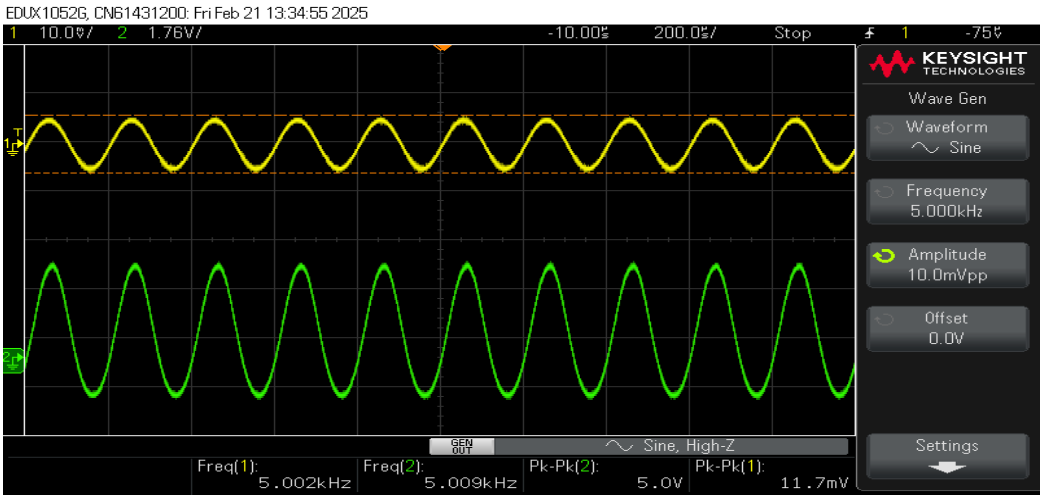

Figure 18: Band-Pass Filter Hardware o/p

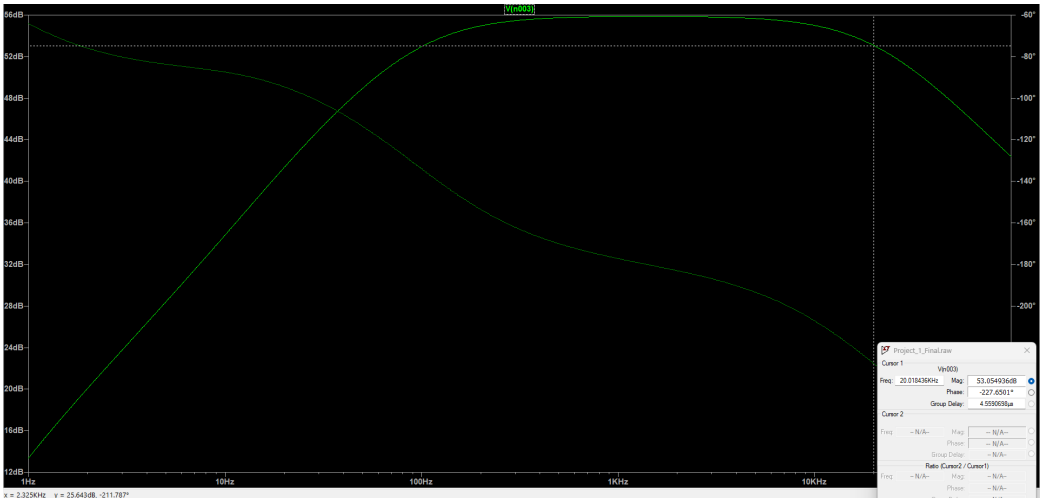

Figure 19: Filter Frequency response Plot - Simulation

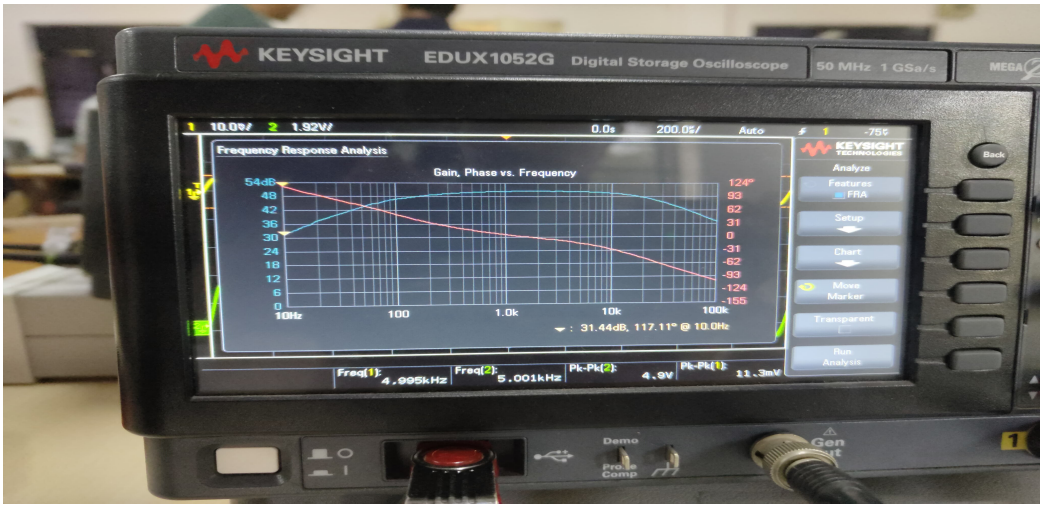

Figure 20: Filter Frequency response Plot - Hardware

We can see that there is a 3dB cutoff at both 20Hz and 20kHz. Therefore, this filter is designed in such a way that it passes only frequencies between 20Hz and 20kHz and rejects all the frequencies beyond the range.

4 Power Amplifier

Power amplifiers are used to increase the power level of a signal and are commonly classified intoClass-A, Class-B, and Class-AB based on their operating point, conduction angle, and efficiency.

4.1 Class - A Power Amplifier

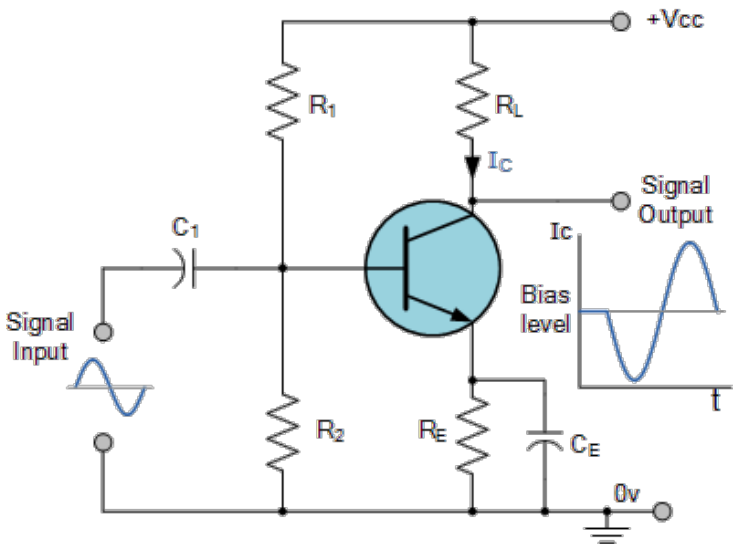

Figure 21: Class - A Power Amplifier

The transistor in a Class-A amplifier is biased so that it remains active (in the linear region) throughout the entire input signal cycle (360° conduction angle).

- **Operating Principle of Class A Amplifier:** The transistor in a Class-A amplifier is biased so that it remains active (in the linear region) throughout the entire input signal cycle (360° conduction angle).
- **Key Features:**
  - High linearity, making it suitable for low-distortion amplification.
  - Poor efficiency, typically around 25% – 30%.
  - High heat dissipation due to continuous current flow even without input signal.

4.2 Class - B Power Amplifier

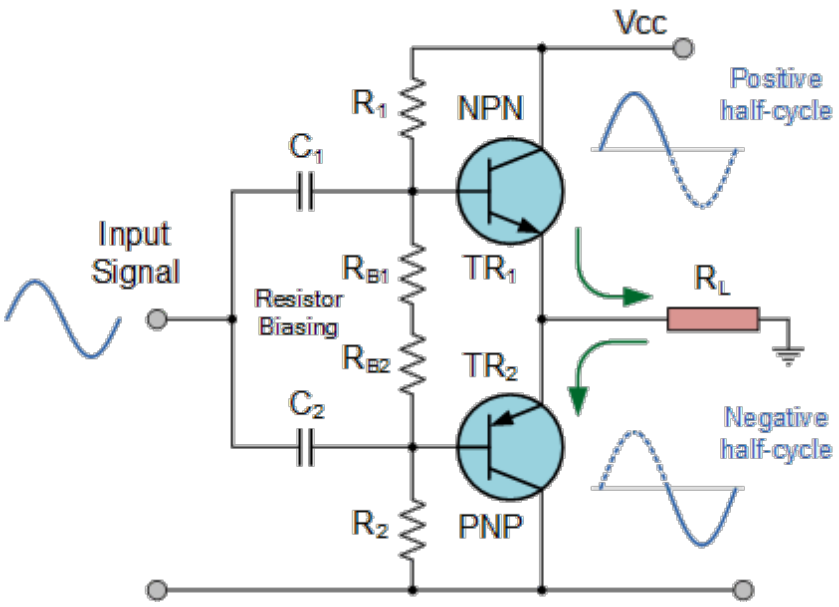

Figure 22: Class - B Power Amplifier

– **Operating Principle:** The transistor is biased at cutoff, and each transistor in a push-pull configuration conducts for half of the input signal cycle (180° conduction angle).

– **Key Features:**

  * Higher efficiency compared to Class-A, typically around 60% – 70%.
  * Introduces **crossover distortion** due to the transition between transistors.
  * Requires a complementary pair of transistors (NPN and PNP or MOSFETs).

4.3 Class - AB Power Amplifier

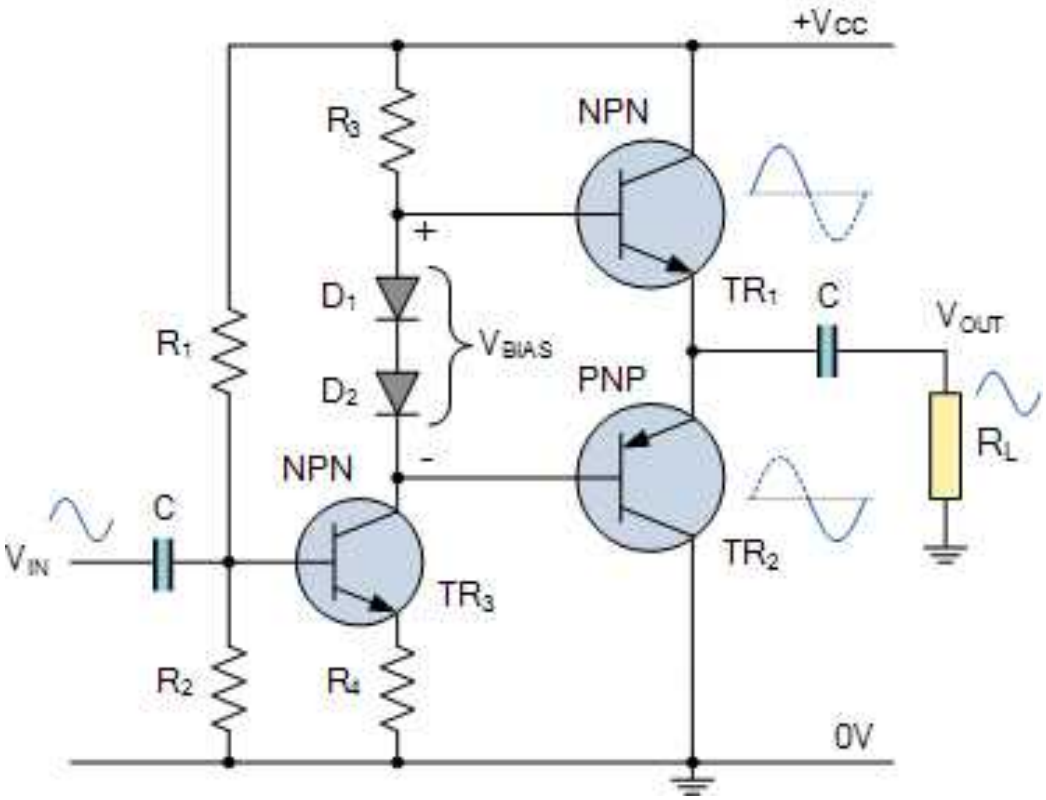

Figure 23: Enter Caption

- **Operating Principle:** Combines the features of Class-A and Class-B by biasing the transistors slightly above cutoff, allowing both transistors to conduct for slightly more than half of the signal cycle (greater than 180° but less than 360° conduction angle)
- **Key Features:**
  - Improved linearity compared to Class-B, reducing crossover distortion.
  - Higher efficiency than Class-A, typically around 50
  - Moderate heat dissipation, balancing efficiency and linearity.

In our circuit we are using **Class AB Power Amplifier**.

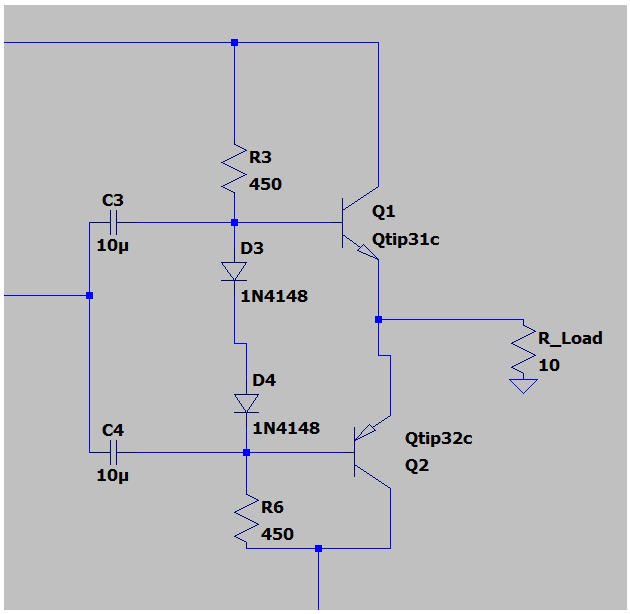

Figure 24: Power Amp Circut LTSpice

Note: For the power Amplifier we have used Resistance values greater than 1k(450 in the circuit Diagram here) because the the input waveform is getiing distorted as the output impedance is low.

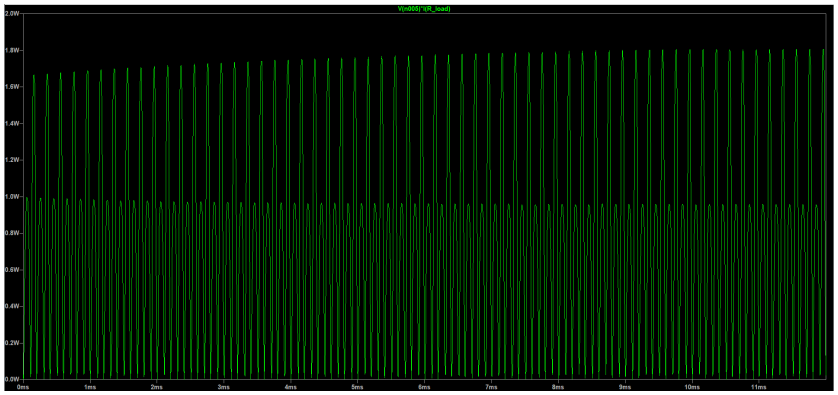

Figure 25: Power at the Load

We can see that we got the power output $1.5W$ as required.

MIC Circuit Used:

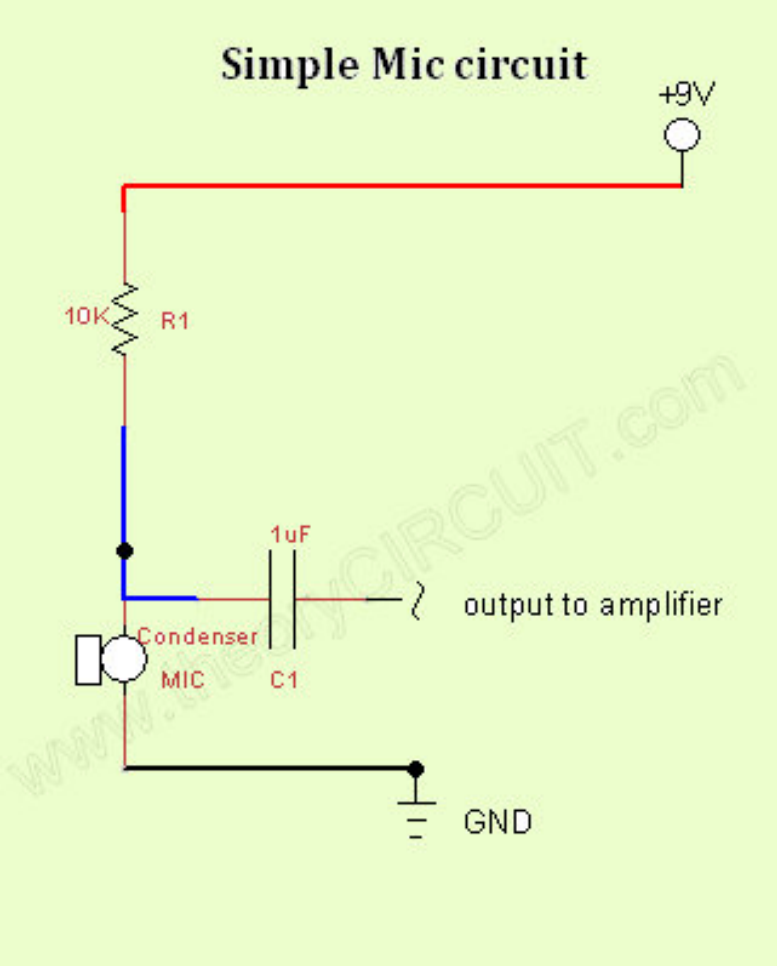

Figure 26: Mic Circuit

Capacitance Value Used $C = \mathbf{2.2}\,\mu\text{F}$

Resistance Value Used $R = \mathbf{6.7}\,\text{k}\mathbf{\Omega}$

Distortion Analysis

Distortion analysis helps determine the unwanted harmonic content in a signal's frequency spectrum. It provides insight into circuit behavior at different frequencies.

The total harmonic distortion (THD) is given by:

$$THD = \sqrt{\frac{\sum_{n=2}^{\infty} V_{n\_RMS}^2}{V_{f\_RMS}^2}}$$

where:

- THD is the total harmonic distortion.
- V_{n_RMS} is the RMS voltage of the nth harmonic.
- V_{f_RMS} is the RMS voltage of the fundamental frequency.

A high THD indicates signal distortion, which degrades audio quality. Lower THD improves signal amplification efficiency and output quality. Filters, such as resistive-capacitive (RC) networks, can reduce THD by eliminating higher-order harmonics.

Slew Rate

Slew rate is defined as the maximum rate of change of the output voltage with respect to time:

$$S.R. = \max\left(\frac{\delta V_{out}}{\delta t}\right)$$

A higher slew rate ensures that the circuit can handle high-frequency signals without distortion. If the slew rate is too low, the circuit may not respond quickly enough to changes in the input signal, leading to output distortion.

Slew rate can be improved by increasing the maximum operating voltage or by reducing the capacitive impedances of the circuit components.

Another expression for the slew rate is:

$$S = 2\pi f_m V_m, \quad V_m = 15mV, \quad f \text{ varies according to input audio.}$$

Observations

During the design and implementation of our audio amplifier, we made the following key observations:

1. **Impact of Transistor Matching:** A differential amplifier relies on well-matched transistors, as one of the fundamental assumptions in its analysis is that both transistors in the differential pair draw equal current. If the transistors are not closely matched, this assumption breaks down, leading to performance issues. We had to use BJTs instead of MOSFETs, which further increased mismatch issues. This problem is more pronounced in discrete components compared to integrated circuits (ICs).
2. **Importance of Proper Coupling and Biasing:** In discrete circuit designs, buffers and coupling capacitors are essential to prevent the output of one stage from disturbing the operating point of another. Alternatively, a DC-coupled amplifier could be implemented, but such designs are typically unsuitable for high-frequency applications.
3. **Managing Thermal Runaway:** Without proper heat dissipation, power amplifiers are prone to thermal runaway, which can lead to the failure of transistors, capacitors, and other components. Adequate thermal management is crucial for reliable operation.
4. **Effect of Cascaded Stages on Frequency Response:** Each stage in the amplifier contributes to the overall frequency response. Since the circuit consists of cascaded stages, the total frequency response is the product of individual stage responses. This can lead to undesirable frequency characteristics, making it essential to consider the high-frequency behavior of all components, not just filters.
5. **Use of Voltage Regulators:** The presence of voltage regulators introduces minor distortions in the output waveform. This distortion can be mitigated by using separate voltage sources for different power levels, such as a dedicated 5V supply and a separate 12V supply, to ensure cleaner power delivery.

Possible Improvements

To enhance our design, we propose the following improvements:

1. **Better Matched Transistors:** Instead of using multiple discrete transistors, employing transistor arrays in IC packages would help mitigate mismatch issues, reduce noise, and save PCB or breadboard space.
2. **Implementation of a Class-D Amplifier:** Replacing the Class-AB power amplifier with a Class-D amplifier could significantly improve power efficiency. However, achieving high fidelity with a Class-D amplifier presents design challenges.
3. **Higher-Order Active Filtering:** Instead of using a simple first-order passive low-pass filter, a higher-order active filter could be employed to achieve better frequency response and sharper cutoff frequencies. Additionally, an adjustable active filter could enable tone control, although trade-offs between magnitude and phase response must be considered.
4. **Use of Multiple Intermediate Gain Stages:** Increasing the number of gain stages can help achieve higher overall gain. Additionally, using an even number of gain stages would eliminate signal inversion introduced by those stages.
5. **Utilization of Positive Feedback Loops:** Incorporating positive feedback in amplifiers can enhance overall gain and help suppress noise in the system, leading to improved performance.