runse script run started on Tue Dec 1 21:26:03 2015

run on machine eecad50.engr.sjsu.edu

Run with a clock period of 4.0

student names

Aditya 8719

Shavinda 4891

options syn False gates False

VCS simulation worked

NCverilog simulation worked

Synthesis finished OK

Gate level simulation worked

Completed the se run for team