Design Compiler Graphical

DC Ultra (TM)

DFTMAX (TM)

Power Compiler (TM)

DesignWare (R)

DC Expert (TM)

Design Vision (TM)

HDL Compiler (TM)

VHDL Compiler (TM)

DFT Compiler

Library Compiler (TM)

Design Compiler(R)

Version I-2013.12-SP5 for RHEL32 -- Jul 20, 2014

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between you, or your company, and Synopsys, Inc.

Information: As of the J-2014.09 version of dc\_shell, the 32-bit

version of the product will not be delivered by default.

If you require a 32-bit version for any reason, please

contact Synopsys technical support.

Initializing...

set link\_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_NOMIN25 /apps/synopsys/I-2013.12-SP5/libraries/syn/dw\_foundation.sldb}

/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_NOMIN25 /apps/synopsys/I-2013.12-SP5/libraries/syn/dw\_foundation.sldb

set target\_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_NOMIN25}

/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_NOMIN25

analyze -format verilog primary\_lsfr15.v

Running PRESTO HDLC

Searching for ./primary\_lsfr15.v

Compiling source file ./primary\_lsfr15.v

Presto compilation completed successfully.

Loading db file '/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_NOMIN25'

Loading db file '/apps/synopsys/I-2013.12-SP5/libraries/syn/dw\_foundation.sldb'

1

elaborate primary\_lsfr15

Loading db file '/apps/synopsys/I-2013.12-SP5/libraries/syn/gtech.db'

Loading db file '/apps/synopsys/I-2013.12-SP5/libraries/syn/standard.sldb'

Loading link library 'tc240c'

Loading link library 'gtech'

Running PRESTO HDLC

Inferred memory devices in process

in routine primary\_lsfr15 line 19 in file

'./primary\_lsfr15.v'.

===============================================================================

| Register Name | Type | Width | Bus | MB | AR | AS | SR | SS | ST |

===============================================================================

| lfsr15\_reg | Flip-flop | 116 | Y | N | Y | N | N | N | N |

===============================================================================

Presto compilation completed successfully.

Elaborated 1 design.

Current design is now 'primary\_lsfr15'.

1

create\_clock clk -name clk -period 3.0

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_clock\_uncertainty 0.25 clk

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_output\_delay 0.5 -clock clk [all\_outputs]

1

set all\_inputs\_wo\_rst\_clk [remove\_from\_collection [remove\_from\_collection [all\_inputs] [get\_port clk]] [get\_port rst]]

Warning: Can't find port 'rst' in design 'primary\_lsfr15'. (UID-95)

{reset write pushin InitialData15[115] InitialData15[114] InitialData15[113] InitialData15[112] InitialData15[111] InitialData15[110] InitialData15[109] InitialData15[108] InitialData15[107] InitialData15[106] InitialData15[105] InitialData15[104] InitialData15[103] InitialData15[102] InitialData15[101] InitialData15[100] InitialData15[99] InitialData15[98] InitialData15[97] InitialData15[96] InitialData15[95] InitialData15[94] InitialData15[93] InitialData15[92] InitialData15[91] InitialData15[90] InitialData15[89] InitialData15[88] InitialData15[87] InitialData15[86] InitialData15[85] InitialData15[84] InitialData15[83] InitialData15[82] InitialData15[81] InitialData15[80] InitialData15[79] InitialData15[78] InitialData15[77] InitialData15[76] InitialData15[75] InitialData15[74] InitialData15[73] InitialData15[72] InitialData15[71] InitialData15[70] InitialData15[69] InitialData15[68] InitialData15[67] InitialData15[66] InitialData15[65] InitialData15[64] InitialData15[63] InitialData15[62] InitialData15[61] InitialData15[60] InitialData15[59] InitialData15[58] InitialData15[57] InitialData15[56] InitialData15[55] InitialData15[54] InitialData15[53] InitialData15[52] InitialData15[51] InitialData15[50] InitialData15[49] InitialData15[48] InitialData15[47] InitialData15[46] InitialData15[45] InitialData15[44] InitialData15[43] InitialData15[42] InitialData15[41] InitialData15[40] InitialData15[39] InitialData15[38] InitialData15[37] InitialData15[36] InitialData15[35] InitialData15[34] InitialData15[33] InitialData15[32] InitialData15[31] InitialData15[30] InitialData15[29] InitialData15[28] InitialData15[27] InitialData15[26] InitialData15[25] InitialData15[24] InitialData15[23] InitialData15[22] InitialData15[21] InitialData15[20] InitialData15[19] ...}

set\_driving\_cell -lib\_cell CND2X1 $all\_inputs\_wo\_rst\_clk

Warning: Design rule attributes from the driving cell will be

set on the port. (UID-401)

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set\_input\_delay 0.6 -clock clk $all\_inputs\_wo\_rst\_clk

1

set\_output\_delay 0.6 -clock clk [all\_outputs]

1

set\_fix\_hold [ get\_clocks clk ]

1

set\_output\_delay 0.3 -clock clk [all\_outputs]

1

set\_wire\_load\_model -name T8G00TW8

1

compile\_ultra

Alib files are up-to-date.

Information: Evaluating DesignWare library utilization. (UISN-27)

============================================================================

| DesignWare Building Block Library | Version | Available |

============================================================================

| Basic DW Building Blocks | I-2013.12-DWBB\_201312.5 | \* |

| Licensed DW Building Blocks | I-2013.12-DWBB\_201312.5 | \* |

============================================================================

Information: Sequential output inversion is enabled. SVF file must be used for formal verification. (OPT-1208)

Loaded alib file './alib-52/tc240c.db\_NOMIN25.alib'

Information: Ungrouping 0 of 1 hierarchies before Pass 1 (OPT-775)

Beginning Pass 1 Mapping

------------------------

Processing 'primary\_lsfr15'

Updating timing information

Information: Updating design information... (UID-85)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Mapping Optimizations (Ultra High effort)

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TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:02 1423.0 0.00 0.0 0.0 0.00

0:00:02 1423.0 0.00 0.0 0.0 0.00

0:00:02 1423.0 0.00 0.0 0.0 0.00

0:00:02 1423.0 0.00 0.0 0.0 0.00

Re-synthesis Optimization (Phase 1)

Re-synthesis Optimization (Phase 2)

Global Optimization (Phase 1)

Global Optimization (Phase 2)

Global Optimization (Phase 3)

Global Optimization (Phase 4)

Global Optimization (Phase 5)

Global Optimization (Phase 6)

Global Optimization (Phase 7)

Global Optimization (Phase 8)

Global Optimization (Phase 9)

Global Optimization (Phase 10)

Global Optimization (Phase 11)

Global Optimization (Phase 12)

Global Optimization (Phase 13)

Global Optimization (Phase 14)

Global Optimization (Phase 15)

Global Optimization (Phase 16)

Global Optimization (Phase 17)

Global Optimization (Phase 18)

Global Optimization (Phase 19)

Global Optimization (Phase 20)

Global Optimization (Phase 21)

Global Optimization (Phase 22)

Global Optimization (Phase 23)

Global Optimization (Phase 24)

Global Optimization (Phase 25)

Global Optimization (Phase 26)

Global Optimization (Phase 27)

Global Optimization (Phase 28)

Global Optimization (Phase 29)

Global Optimization (Phase 30)

Global Optimization (Phase 31)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Delay Optimization Phase

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TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:02 1162.0 0.00 0.0 1203.5 0.00

0:00:02 1162.0 0.00 0.0 1203.5 0.00

0:00:02 1162.0 0.00 0.0 1203.5 0.00

0:00:02 1162.0 0.00 0.0 1203.5 0.00

0:00:02 1162.0 0.00 0.0 1203.5 0.00

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0:00:02 1162.0 0.00 0.0 1203.5 0.00

0:00:02 1162.0 0.00 0.0 1203.5 0.00

0:00:02 1162.0 0.00 0.0 1203.5 0.00

Beginning Delay Optimization

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0:00:02 1162.0 0.00 0.0 1203.5 0.00

0:00:02 1162.0 0.00 0.0 1203.5 0.00

0:00:02 1162.0 0.00 0.0 1203.5 0.00

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0:00:02 1162.0 0.00 0.0 1203.5 0.00

0:00:02 1162.0 0.00 0.0 1203.5 0.00

Beginning Design Rule Fixing (max\_capacitance)

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TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

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0:00:02 1162.0 0.00 0.0 1203.5 0.00

Global Optimization (Phase 32)

Global Optimization (Phase 33)

Global Optimization (Phase 34)

0:00:02 1163.0 0.00 0.0 0.0 0.00

0:00:03 1159.0 0.00 0.0 0.0 0.00

0:00:03 1159.0 0.00 0.0 0.0 0.00

0:00:03 1159.0 0.00 0.0 0.0 0.00

0:00:03 1159.0 0.00 0.0 0.0 0.00

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:03 1159.0 0.00 0.0 0.0 0.00

0:00:04 1133.0 0.00 0.0 39.7 0.00

Beginning Area-Recovery Phase (max\_area 0)

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TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

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0:00:04 1133.0 0.00 0.0 39.7 0.00

Global Optimization (Phase 35)

Global Optimization (Phase 36)

Global Optimization (Phase 37)

Global Optimization (Phase 38)

Global Optimization (Phase 39)

Global Optimization (Phase 40)

Global Optimization (Phase 41)

Global Optimization (Phase 42)

Global Optimization (Phase 43)

Global Optimization (Phase 44)

Global Optimization (Phase 45)

Global Optimization (Phase 46)

Global Optimization (Phase 47)

Global Optimization (Phase 48)

Global Optimization (Phase 49)

Global Optimization (Phase 50)

0:00:04 1125.0 0.00 0.0 0.0 0.00

0:00:04 1125.0 0.00 0.0 0.0 0.00

0:00:04 1125.0 0.00 0.0 0.0 0.00

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Loading db file '/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_NOMIN25'

Optimization Complete

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1

create\_clock clk -name clk -period 4.0

1

update\_timing

Information: Updating design information... (UID-85)

1

report\_timing -max\_paths 3

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 3

Design : primary\_lsfr15

Version: I-2013.12-SP5

Date : Tue Dec 1 21:27:52 2015

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: NOMIN25 Library: tc240c

Wire Load Model Mode: top

Startpoint: write (input port clocked by clk)

Endpoint: lfsr15\_reg[100]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr15 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 r

write (in) 0.05 0.65 r

U363/Z (CNIVX12) 0.41 1.05 r

U361/Z (COR2X2) 0.44 1.49 r

U359/Z (CIVX3) 0.58 2.07 f

U366/Z (CANR2X1) 0.21 2.27 r

U367/Z (COND4CX1) 0.15 2.43 f

lfsr15\_reg[100]/D (CFD2XL) 0.00 2.43 f

data arrival time 2.43

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr15\_reg[100]/CP (CFD2XL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

-----------------------------------------------------------

data required time 3.53

data arrival time -2.43

-----------------------------------------------------------

slack (MET) 1.10

Startpoint: write (input port clocked by clk)

Endpoint: lfsr15\_reg[99]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr15 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 r

write (in) 0.05 0.65 r

U363/Z (CNIVX12) 0.41 1.05 r

U361/Z (COR2X2) 0.44 1.49 r

U359/Z (CIVX3) 0.58 2.07 f

U369/Z (CANR2X1) 0.21 2.27 r

U370/Z (COND4CX1) 0.15 2.43 f

lfsr15\_reg[99]/D (CFD2XL) 0.00 2.43 f

data arrival time 2.43

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr15\_reg[99]/CP (CFD2XL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

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data required time 3.53

data arrival time -2.43

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slack (MET) 1.10

Startpoint: write (input port clocked by clk)

Endpoint: lfsr15\_reg[98]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr15 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 r

write (in) 0.05 0.65 r

U363/Z (CNIVX12) 0.41 1.05 r

U361/Z (COR2X2) 0.44 1.49 r

U359/Z (CIVX3) 0.58 2.07 f

U372/Z (CANR2X1) 0.21 2.27 r

U373/Z (COND4CX1) 0.15 2.43 f

lfsr15\_reg[98]/D (CFD2XL) 0.00 2.43 f

data arrival time 2.43

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr15\_reg[98]/CP (CFD2XL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

-----------------------------------------------------------

data required time 3.53

data arrival time -2.43

-----------------------------------------------------------

slack (MET) 1.10

1

analyze -format verilog primary\_lsfr14.v

Running PRESTO HDLC

Searching for ./primary\_lsfr14.v

Compiling source file ./primary\_lsfr14.v

Presto compilation completed successfully.

1

elaborate primary\_lsfr14

Running PRESTO HDLC

Inferred memory devices in process

in routine primary\_lsfr14 line 20 in file

'./primary\_lsfr14.v'.

===============================================================================

| Register Name | Type | Width | Bus | MB | AR | AS | SR | SS | ST |

===============================================================================

| lfsr14\_reg | Flip-flop | 64 | Y | N | Y | N | N | N | N |

===============================================================================

Presto compilation completed successfully.

Elaborated 1 design.

Current design is now 'primary\_lsfr14'.

1

create\_clock clk -name clk -period 3.0

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_clock\_uncertainty 0.25 clk

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_output\_delay 0.5 -clock clk [all\_outputs]

1

set all\_inputs\_wo\_rst\_clk [remove\_from\_collection [remove\_from\_collection [all\_inputs] [get\_port clk]] [get\_port rst]]

Warning: Can't find port 'rst' in design 'primary\_lsfr14'. (UID-95)

{reset write pushin InitialData14[63] InitialData14[62] InitialData14[61] InitialData14[60] InitialData14[59] InitialData14[58] InitialData14[57] InitialData14[56] InitialData14[55] InitialData14[54] InitialData14[53] InitialData14[52] InitialData14[51] InitialData14[50] InitialData14[49] InitialData14[48] InitialData14[47] InitialData14[46] InitialData14[45] InitialData14[44] InitialData14[43] InitialData14[42] InitialData14[41] InitialData14[40] InitialData14[39] InitialData14[38] InitialData14[37] InitialData14[36] InitialData14[35] InitialData14[34] InitialData14[33] InitialData14[32] InitialData14[31] InitialData14[30] InitialData14[29] InitialData14[28] InitialData14[27] InitialData14[26] InitialData14[25] InitialData14[24] InitialData14[23] InitialData14[22] InitialData14[21] InitialData14[20] InitialData14[19] InitialData14[18] InitialData14[17] InitialData14[16] InitialData14[15] InitialData14[14] InitialData14[13] InitialData14[12] InitialData14[11] InitialData14[10] InitialData14[9] InitialData14[8] InitialData14[7] InitialData14[6] InitialData14[5] InitialData14[4] InitialData14[3] InitialData14[2] InitialData14[1] InitialData14[0]}

set\_driving\_cell -lib\_cell CND2X1 $all\_inputs\_wo\_rst\_clk

Warning: Design rule attributes from the driving cell will be

set on the port. (UID-401)

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set\_input\_delay 0.6 -clock clk $all\_inputs\_wo\_rst\_clk

1

set\_output\_delay 0.6 -clock clk [all\_outputs]

1

set\_fix\_hold [ get\_clocks clk ]

1

set\_output\_delay 0.3 -clock clk [all\_outputs]

1

set\_wire\_load\_model -name T8G00TW8

1

compile\_ultra

Alib files are up-to-date.

Information: Sequential output inversion is enabled. SVF file must be used for formal verification. (OPT-1208)

Information: Ungrouping 0 of 1 hierarchies before Pass 1 (OPT-775)

Beginning Pass 1 Mapping

------------------------

Processing 'primary\_lsfr14'

Updating timing information

Information: Updating design information... (UID-85)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Mapping Optimizations (Ultra High effort)

-------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:01 961.0 0.00 0.0 0.0 0.00

0:00:01 961.0 0.00 0.0 0.0 0.00

0:00:01 961.0 0.00 0.0 0.0 0.00

0:00:01 961.0 0.00 0.0 0.0 0.00

Re-synthesis Optimization (Phase 1)

Re-synthesis Optimization (Phase 2)

Global Optimization (Phase 1)

Global Optimization (Phase 2)

Global Optimization (Phase 3)

Global Optimization (Phase 4)

Global Optimization (Phase 5)

Global Optimization (Phase 6)

Global Optimization (Phase 7)

Global Optimization (Phase 8)

Global Optimization (Phase 9)

Global Optimization (Phase 10)

Global Optimization (Phase 11)

Global Optimization (Phase 12)

Global Optimization (Phase 13)

Global Optimization (Phase 14)

Global Optimization (Phase 15)

Global Optimization (Phase 16)

Global Optimization (Phase 17)

Global Optimization (Phase 18)

Global Optimization (Phase 19)

Global Optimization (Phase 20)

Global Optimization (Phase 21)

Global Optimization (Phase 22)

Global Optimization (Phase 23)

Global Optimization (Phase 24)

Global Optimization (Phase 25)

Global Optimization (Phase 26)

Global Optimization (Phase 27)

Global Optimization (Phase 28)

Global Optimization (Phase 29)

Global Optimization (Phase 30)

Global Optimization (Phase 31)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Delay Optimization Phase

----------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:01 700.5 0.00 0.0 333.8 0.00

0:00:01 700.5 0.00 0.0 333.8 0.00

0:00:01 700.5 0.00 0.0 333.8 0.00

0:00:01 700.5 0.00 0.0 333.8 0.00

0:00:01 700.5 0.00 0.0 333.8 0.00

0:00:01 700.5 0.00 0.0 333.8 0.00

0:00:01 700.5 0.00 0.0 333.8 0.00

0:00:01 700.5 0.00 0.0 333.8 0.00

0:00:01 700.5 0.00 0.0 333.8 0.00

0:00:01 700.5 0.00 0.0 333.8 0.00

0:00:01 700.5 0.00 0.0 333.8 0.00

Beginning Delay Optimization

----------------------------

0:00:01 700.5 0.00 0.0 333.8 0.00

0:00:01 700.5 0.00 0.0 333.8 0.00

0:00:01 700.5 0.00 0.0 333.8 0.00

0:00:01 700.5 0.00 0.0 333.8 0.00

0:00:01 700.5 0.00 0.0 333.8 0.00

0:00:01 700.5 0.00 0.0 333.8 0.00

0:00:01 700.5 0.00 0.0 333.8 0.00

0:00:01 700.5 0.00 0.0 333.8 0.00

Beginning Design Rule Fixing (min\_path) (max\_capacitance)

----------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:01 700.5 0.00 0.0 333.8 -0.01

Global Optimization (Phase 32)

Global Optimization (Phase 33)

Global Optimization (Phase 34)

0:00:01 701.0 0.00 0.0 0.0 0.00

0:00:01 700.0 0.00 0.0 0.0 -0.01

0:00:01 700.0 0.00 0.0 0.0 -0.01

Loaded alib file './alib-52/tc240c.db\_NOMIN25.alib'

0:00:02 700.0 0.00 0.0 0.0 -0.01

0:00:02 700.0 0.00 0.0 0.0 -0.01

0:00:02 700.0 0.00 0.0 0.0 0.00

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:02 700.0 0.00 0.0 0.0 0.00

0:00:02 700.0 0.00 0.0 0.0 0.00

Beginning Area-Recovery Phase (max\_area 0)

-----------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:02 700.0 0.00 0.0 0.0 0.00

Global Optimization (Phase 35)

Global Optimization (Phase 36)

Global Optimization (Phase 37)

Global Optimization (Phase 38)

Global Optimization (Phase 39)

Global Optimization (Phase 40)

Global Optimization (Phase 41)

Global Optimization (Phase 42)

Global Optimization (Phase 43)

Global Optimization (Phase 44)

Global Optimization (Phase 45)

Global Optimization (Phase 46)

Global Optimization (Phase 47)

Global Optimization (Phase 48)

Global Optimization (Phase 49)

0:00:02 698.0 0.00 0.0 0.0 0.00

0:00:02 698.0 0.00 0.0 0.0 0.00

0:00:02 698.0 0.00 0.0 0.0 0.00

0:00:02 698.0 0.00 0.0 0.0 0.00

0:00:02 698.0 0.00 0.0 0.0 0.00

0:00:02 698.0 0.00 0.0 0.0 0.00

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0:00:02 698.0 0.00 0.0 0.0 0.00

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0:00:02 698.0 0.00 0.0 0.0 0.00

0:00:02 698.0 0.00 0.0 0.0 0.00

0:00:02 698.0 0.00 0.0 0.0 0.00

0:00:02 698.0 0.00 0.0 0.0 0.00

0:00:02 698.0 0.00 0.0 0.0 0.00

Loading db file '/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_NOMIN25'

Optimization Complete

---------------------

1

create\_clock clk -name clk -period 4.0

1

update\_timing

Information: Updating design information... (UID-85)

1

report\_timing -max\_paths 3

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 3

Design : primary\_lsfr14

Version: I-2013.12-SP5

Date : Tue Dec 1 21:27:56 2015

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: NOMIN25 Library: tc240c

Wire Load Model Mode: top

Startpoint: write (input port clocked by clk)

Endpoint: lfsr14\_reg[8]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr14 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 f

write (in) 0.04 0.64 f

U219/Z (CNIVX8) 0.32 0.96 f

U220/Z (CNR2IX2) 0.29 1.25 r

U217/Z1 (CIVDX1) 0.79 2.04 r

U255/Z (COND1XL) 0.30 2.34 f

U257/Z (COND4CXL) 0.17 2.51 r

lfsr14\_reg[8]/D (CFD2QXL) 0.00 2.51 r

data arrival time 2.51

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr14\_reg[8]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.24 3.51

data required time 3.51

-----------------------------------------------------------

data required time 3.51

data arrival time -2.51

-----------------------------------------------------------

slack (MET) 1.01

Startpoint: write (input port clocked by clk)

Endpoint: lfsr14\_reg[37]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr14 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 f

write (in) 0.04 0.64 f

U219/Z (CNIVX8) 0.32 0.96 f

U220/Z (CNR2IX2) 0.29 1.25 r

U217/Z1 (CIVDX1) 0.79 2.04 r

U221/Z (COND1XL) 0.30 2.34 f

U224/Z (COND4CXL) 0.17 2.51 r

lfsr14\_reg[37]/D (CFD2QXL) 0.00 2.51 r

data arrival time 2.51

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr14\_reg[37]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.24 3.51

data required time 3.51

-----------------------------------------------------------

data required time 3.51

data arrival time -2.51

-----------------------------------------------------------

slack (MET) 1.01

Startpoint: lfsr14\_reg[57]

(rising edge-triggered flip-flop clocked by clk)

Endpoint: lfsr14\_reg[24]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr14 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

lfsr14\_reg[57]/CP (CFD2QXL) 0.00 0.00 r

lfsr14\_reg[57]/Q (CFD2QXL) 0.67 0.67 r

U263/Z (CENX1) 0.31 0.98 r

U264/Z (CENX1) 0.24 1.22 r

U265/Z (CEOX1) 0.32 1.54 r

U315/Z (CEOX1) 0.33 1.88 r

U316/Z (CENX1) 0.28 2.15 r

U363/Z (CENX1) 0.22 2.38 r

U365/Z (COND1XL) 0.12 2.49 f

lfsr14\_reg[24]/D (CFD2QXL) 0.00 2.49 f

data arrival time 2.49

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr14\_reg[24]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

-----------------------------------------------------------

data required time 3.53

data arrival time -2.49

-----------------------------------------------------------

slack (MET) 1.04

1

analyze -format verilog primary\_lsfr13.v

Running PRESTO HDLC

Searching for ./primary\_lsfr13.v

Compiling source file ./primary\_lsfr13.v

Presto compilation completed successfully.

1

elaborate primary\_lsfr13

Running PRESTO HDLC

Inferred memory devices in process

in routine primary\_lsfr13 line 20 in file

'./primary\_lsfr13.v'.

===============================================================================

| Register Name | Type | Width | Bus | MB | AR | AS | SR | SS | ST |

===============================================================================

| lfsr13\_reg | Flip-flop | 198 | Y | N | Y | N | N | N | N |

===============================================================================

Presto compilation completed successfully.

Elaborated 1 design.

Current design is now 'primary\_lsfr13'.

1

create\_clock clk -name clk -period 3.0

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_clock\_uncertainty 0.25 clk

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_output\_delay 0.5 -clock clk [all\_outputs]

1

set all\_inputs\_wo\_rst\_clk [remove\_from\_collection [remove\_from\_collection [all\_inputs] [get\_port clk]] [get\_port rst]]

Warning: Can't find port 'rst' in design 'primary\_lsfr13'. (UID-95)

{reset write pushin InitialData13[197] InitialData13[196] InitialData13[195] InitialData13[194] InitialData13[193] InitialData13[192] InitialData13[191] InitialData13[190] InitialData13[189] InitialData13[188] InitialData13[187] InitialData13[186] InitialData13[185] InitialData13[184] InitialData13[183] InitialData13[182] InitialData13[181] InitialData13[180] InitialData13[179] InitialData13[178] InitialData13[177] InitialData13[176] InitialData13[175] InitialData13[174] InitialData13[173] InitialData13[172] InitialData13[171] InitialData13[170] InitialData13[169] InitialData13[168] InitialData13[167] InitialData13[166] InitialData13[165] InitialData13[164] InitialData13[163] InitialData13[162] InitialData13[161] InitialData13[160] InitialData13[159] InitialData13[158] InitialData13[157] InitialData13[156] InitialData13[155] InitialData13[154] InitialData13[153] InitialData13[152] InitialData13[151] InitialData13[150] InitialData13[149] InitialData13[148] InitialData13[147] InitialData13[146] InitialData13[145] InitialData13[144] InitialData13[143] InitialData13[142] InitialData13[141] InitialData13[140] InitialData13[139] InitialData13[138] InitialData13[137] InitialData13[136] InitialData13[135] InitialData13[134] InitialData13[133] InitialData13[132] InitialData13[131] InitialData13[130] InitialData13[129] InitialData13[128] InitialData13[127] InitialData13[126] InitialData13[125] InitialData13[124] InitialData13[123] InitialData13[122] InitialData13[121] InitialData13[120] InitialData13[119] InitialData13[118] InitialData13[117] InitialData13[116] InitialData13[115] InitialData13[114] InitialData13[113] InitialData13[112] InitialData13[111] InitialData13[110] InitialData13[109] InitialData13[108] InitialData13[107] InitialData13[106] InitialData13[105] InitialData13[104] InitialData13[103] InitialData13[102] InitialData13[101] ...}

set\_driving\_cell -lib\_cell CND2X1 $all\_inputs\_wo\_rst\_clk

Warning: Design rule attributes from the driving cell will be

set on the port. (UID-401)

Warning: Design rule attributes from the driving cell will be

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set\_input\_delay 0.6 -clock clk $all\_inputs\_wo\_rst\_clk

1

set\_output\_delay 0.6 -clock clk [all\_outputs]

1

set\_fix\_hold [ get\_clocks clk ]

1

set\_output\_delay 0.3 -clock clk [all\_outputs]

1

set\_wire\_load\_model -name T8G00TW8

1

compile\_ultra

Alib files are up-to-date.

Information: Sequential output inversion is enabled. SVF file must be used for formal verification. (OPT-1208)

Information: Ungrouping 0 of 1 hierarchies before Pass 1 (OPT-775)

Beginning Pass 1 Mapping

------------------------

Processing 'primary\_lsfr13'

Updating timing information

Information: Updating design information... (UID-85)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Mapping Optimizations (Ultra High effort)

-------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:03 2438.5 0.00 -0.0 0.0 0.00

0:00:03 2438.5 0.00 -0.0 0.0 0.00

0:00:03 2438.5 0.00 -0.0 0.0 0.00

0:00:03 2438.5 0.00 -0.0 0.0 0.00

Re-synthesis Optimization (Phase 1)

Re-synthesis Optimization (Phase 2)

Global Optimization (Phase 1)

Global Optimization (Phase 2)

Global Optimization (Phase 3)

Global Optimization (Phase 4)

Global Optimization (Phase 5)

Global Optimization (Phase 6)

Global Optimization (Phase 7)

Global Optimization (Phase 8)

Global Optimization (Phase 9)

Global Optimization (Phase 10)

Global Optimization (Phase 11)

Global Optimization (Phase 12)

Global Optimization (Phase 13)

Global Optimization (Phase 14)

Global Optimization (Phase 15)

Global Optimization (Phase 16)

Global Optimization (Phase 17)

Global Optimization (Phase 18)

Global Optimization (Phase 19)

Global Optimization (Phase 20)

Global Optimization (Phase 21)

Global Optimization (Phase 22)

Global Optimization (Phase 23)

Global Optimization (Phase 24)

Global Optimization (Phase 25)

Global Optimization (Phase 26)

Global Optimization (Phase 27)

Global Optimization (Phase 28)

Global Optimization (Phase 29)

Global Optimization (Phase 30)

Global Optimization (Phase 31)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Delay Optimization Phase

----------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:03 1997.0 0.00 0.0 1227.3 0.00

0:00:03 1997.0 0.00 0.0 1227.3 0.00

0:00:03 1997.0 0.00 0.0 1227.3 0.00

0:00:03 1997.0 0.00 0.0 1227.3 0.00

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Beginning Delay Optimization

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0:00:03 1997.0 0.00 0.0 1227.3 0.00

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0:00:03 1997.0 0.00 0.0 1227.3 0.00

0:00:03 1997.0 0.00 0.0 1227.3 0.00

Beginning Design Rule Fixing (max\_capacitance)

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TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:03 1997.0 0.00 0.0 1227.3 0.00

Global Optimization (Phase 32)

Global Optimization (Phase 33)

Global Optimization (Phase 34)

0:00:03 1998.0 0.00 0.0 0.0 0.00

0:00:04 1951.5 0.00 0.0 0.0 0.00

0:00:04 1951.5 0.00 0.0 0.0 0.00

Loaded alib file './alib-52/tc240c.db\_NOMIN25.alib'

0:00:05 1951.5 0.00 0.0 0.0 0.00

0:00:05 1951.5 0.00 0.0 0.0 0.00

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:05 1951.5 0.00 0.0 0.0 0.00

0:00:05 1884.0 0.00 0.0 1732.5 0.00

0:00:05 2261.0 0.00 0.0 0.0 0.00

Beginning Area-Recovery Phase (max\_area 0)

-----------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:05 2261.0 0.00 0.0 0.0 0.00

Global Optimization (Phase 35)

Global Optimization (Phase 36)

Global Optimization (Phase 37)

Global Optimization (Phase 38)

Global Optimization (Phase 39)

Global Optimization (Phase 40)

Global Optimization (Phase 41)

Global Optimization (Phase 42)

Global Optimization (Phase 43)

Global Optimization (Phase 44)

Global Optimization (Phase 45)

Global Optimization (Phase 46)

Global Optimization (Phase 47)

Global Optimization (Phase 48)

Global Optimization (Phase 49)

Global Optimization (Phase 50)

0:00:05 1876.5 0.00 0.0 0.0 0.00

0:00:05 1876.5 0.00 0.0 0.0 0.00

0:00:05 1876.5 0.00 0.0 0.0 0.00

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0:00:05 1876.5 0.00 0.0 0.0 0.00

Loading db file '/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_NOMIN25'

Optimization Complete

---------------------

1

create\_clock clk -name clk -period 4.0

1

update\_timing

Information: Updating design information... (UID-85)

1

report\_timing -max\_paths 3

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 3

Design : primary\_lsfr13

Version: I-2013.12-SP5

Date : Tue Dec 1 21:28:02 2015

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: NOMIN25 Library: tc240c

Wire Load Model Mode: top

Startpoint: write (input port clocked by clk)

Endpoint: lfsr13\_reg[14]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr13 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 r

write (in) 0.05 0.65 r

U611/Z (CNIVX12) 0.58 1.23 r

U602/Z (COR2X4) 0.50 1.72 r

U604/Z (CIVX4) 0.44 2.17 f

U977/Z (CANR2X1) 0.18 2.35 r

U978/Z (COND1XL) 0.14 2.49 f

lfsr13\_reg[14]/D (CFD2XL) 0.00 2.49 f

data arrival time 2.49

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr13\_reg[14]/CP (CFD2XL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

-----------------------------------------------------------

data required time 3.53

data arrival time -2.49

-----------------------------------------------------------

slack (MET) 1.04

Startpoint: write (input port clocked by clk)

Endpoint: lfsr13\_reg[13]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr13 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 r

write (in) 0.05 0.65 r

U611/Z (CNIVX12) 0.58 1.23 r

U602/Z (COR2X4) 0.50 1.72 r

U604/Z (CIVX4) 0.44 2.17 f

U681/Z (CANR2X1) 0.18 2.35 r

U682/Z (COND1XL) 0.14 2.49 f

lfsr13\_reg[13]/D (CFD2XL) 0.00 2.49 f

data arrival time 2.49

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr13\_reg[13]/CP (CFD2XL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

-----------------------------------------------------------

data required time 3.53

data arrival time -2.49

-----------------------------------------------------------

slack (MET) 1.04

Startpoint: write (input port clocked by clk)

Endpoint: lfsr13\_reg[10]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr13 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 r

write (in) 0.05 0.65 r

U611/Z (CNIVX12) 0.58 1.23 r

U602/Z (COR2X4) 0.50 1.72 r

U604/Z (CIVX4) 0.44 2.17 f

U688/Z (CANR2X1) 0.18 2.35 r

U689/Z (COND1XL) 0.14 2.49 f

lfsr13\_reg[10]/D (CFD2XL) 0.00 2.49 f

data arrival time 2.49

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr13\_reg[10]/CP (CFD2XL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

-----------------------------------------------------------

data required time 3.53

data arrival time -2.49

-----------------------------------------------------------

slack (MET) 1.04

1

analyze -format verilog primary\_lsfr12.v

Running PRESTO HDLC

Searching for ./primary\_lsfr12.v

Compiling source file ./primary\_lsfr12.v

Presto compilation completed successfully.

1

elaborate primary\_lsfr12

Running PRESTO HDLC

Inferred memory devices in process

in routine primary\_lsfr12 line 19 in file

'./primary\_lsfr12.v'.

===============================================================================

| Register Name | Type | Width | Bus | MB | AR | AS | SR | SS | ST |

===============================================================================

| lfsr12\_reg | Flip-flop | 147 | Y | N | Y | N | N | N | N |

===============================================================================

Presto compilation completed successfully.

Elaborated 1 design.

Current design is now 'primary\_lsfr12'.

1

create\_clock clk -name clk -period 3.0

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_clock\_uncertainty 0.25 clk

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_output\_delay 0.5 -clock clk [all\_outputs]

1

set all\_inputs\_wo\_rst\_clk [remove\_from\_collection [remove\_from\_collection [all\_inputs] [get\_port clk]] [get\_port rst]]

Warning: Can't find port 'rst' in design 'primary\_lsfr12'. (UID-95)

{reset write pushin InitialData12[146] InitialData12[145] InitialData12[144] InitialData12[143] InitialData12[142] InitialData12[141] InitialData12[140] InitialData12[139] InitialData12[138] InitialData12[137] InitialData12[136] InitialData12[135] InitialData12[134] InitialData12[133] InitialData12[132] InitialData12[131] InitialData12[130] InitialData12[129] InitialData12[128] InitialData12[127] InitialData12[126] InitialData12[125] InitialData12[124] InitialData12[123] InitialData12[122] InitialData12[121] InitialData12[120] InitialData12[119] InitialData12[118] InitialData12[117] InitialData12[116] InitialData12[115] InitialData12[114] InitialData12[113] InitialData12[112] InitialData12[111] InitialData12[110] InitialData12[109] InitialData12[108] InitialData12[107] InitialData12[106] InitialData12[105] InitialData12[104] InitialData12[103] InitialData12[102] InitialData12[101] InitialData12[100] InitialData12[99] InitialData12[98] InitialData12[97] InitialData12[96] InitialData12[95] InitialData12[94] InitialData12[93] InitialData12[92] InitialData12[91] InitialData12[90] InitialData12[89] InitialData12[88] InitialData12[87] InitialData12[86] InitialData12[85] InitialData12[84] InitialData12[83] InitialData12[82] InitialData12[81] InitialData12[80] InitialData12[79] InitialData12[78] InitialData12[77] InitialData12[76] InitialData12[75] InitialData12[74] InitialData12[73] InitialData12[72] InitialData12[71] InitialData12[70] InitialData12[69] InitialData12[68] InitialData12[67] InitialData12[66] InitialData12[65] InitialData12[64] InitialData12[63] InitialData12[62] InitialData12[61] InitialData12[60] InitialData12[59] InitialData12[58] InitialData12[57] InitialData12[56] InitialData12[55] InitialData12[54] InitialData12[53] InitialData12[52] InitialData12[51] InitialData12[50] ...}

set\_driving\_cell -lib\_cell CND2X1 $all\_inputs\_wo\_rst\_clk

Warning: Design rule attributes from the driving cell will be

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1

set\_input\_delay 0.6 -clock clk $all\_inputs\_wo\_rst\_clk

1

set\_output\_delay 0.6 -clock clk [all\_outputs]

1

set\_fix\_hold [ get\_clocks clk ]

1

set\_output\_delay 0.3 -clock clk [all\_outputs]

1

set\_wire\_load\_model -name T8G00TW8

1

compile\_ultra

Alib files are up-to-date.

Information: Sequential output inversion is enabled. SVF file must be used for formal verification. (OPT-1208)

Information: Ungrouping 0 of 1 hierarchies before Pass 1 (OPT-775)

Beginning Pass 1 Mapping

------------------------

Processing 'primary\_lsfr12'

Updating timing information

Information: Updating design information... (UID-85)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Mapping Optimizations (Ultra High effort)

-------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:02 2170.5 0.00 0.0 0.0 0.00

0:00:02 2170.5 0.00 0.0 0.0 0.00

0:00:02 2170.5 0.00 0.0 0.0 0.00

0:00:02 2170.5 0.00 0.0 0.0 0.00

Re-synthesis Optimization (Phase 1)

Re-synthesis Optimization (Phase 2)

Global Optimization (Phase 1)

Global Optimization (Phase 2)

Global Optimization (Phase 3)

Global Optimization (Phase 4)

Global Optimization (Phase 5)

Global Optimization (Phase 6)

Global Optimization (Phase 7)

Global Optimization (Phase 8)

Global Optimization (Phase 9)

Global Optimization (Phase 10)

Global Optimization (Phase 11)

Global Optimization (Phase 12)

Global Optimization (Phase 13)

Global Optimization (Phase 14)

Global Optimization (Phase 15)

Global Optimization (Phase 16)

Global Optimization (Phase 17)

Global Optimization (Phase 18)

Global Optimization (Phase 19)

Global Optimization (Phase 20)

Global Optimization (Phase 21)

Global Optimization (Phase 22)

Global Optimization (Phase 23)

Global Optimization (Phase 24)

Global Optimization (Phase 25)

Global Optimization (Phase 26)

Global Optimization (Phase 27)

Global Optimization (Phase 28)

Global Optimization (Phase 29)

Global Optimization (Phase 30)

Global Optimization (Phase 31)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Delay Optimization Phase

----------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:02 1599.5 0.00 0.0 973.2 0.00

0:00:02 1599.5 0.00 0.0 973.2 0.00

0:00:02 1599.5 0.00 0.0 973.2 0.00

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Beginning Delay Optimization

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0:00:02 1599.5 0.00 0.0 973.2 0.00

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0:00:02 1599.5 0.00 0.0 973.2 0.00

Beginning Design Rule Fixing (max\_capacitance)

----------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

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0:00:02 1599.5 0.00 0.0 973.2 0.00

Global Optimization (Phase 32)

Global Optimization (Phase 33)

Global Optimization (Phase 34)

0:00:02 1600.5 0.00 0.0 0.0 0.00

0:00:02 1597.5 0.00 0.0 0.0 0.00

0:00:02 1597.5 0.00 0.0 0.0 0.00

Loaded alib file './alib-52/tc240c.db\_NOMIN25.alib'

0:00:03 1597.5 0.00 0.0 0.0 0.00

0:00:03 1597.5 0.00 0.0 0.0 0.00

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:03 1597.5 0.00 0.0 0.0 0.00

0:00:03 1597.5 0.00 0.0 0.0 0.00

Beginning Area-Recovery Phase (max\_area 0)

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TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

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0:00:03 1597.5 0.00 0.0 0.0 0.00

Global Optimization (Phase 35)

Global Optimization (Phase 36)

Global Optimization (Phase 37)

Global Optimization (Phase 38)

Global Optimization (Phase 39)

Global Optimization (Phase 40)

Global Optimization (Phase 41)

Global Optimization (Phase 42)

Global Optimization (Phase 43)

Global Optimization (Phase 44)

Global Optimization (Phase 45)

Global Optimization (Phase 46)

Global Optimization (Phase 47)

Global Optimization (Phase 48)

Global Optimization (Phase 49)

Global Optimization (Phase 50)

0:00:03 1572.5 0.00 0.0 0.0 0.00

0:00:03 1572.5 0.00 0.0 0.0 0.00

0:00:03 1572.5 0.00 0.0 0.0 0.00

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0:00:03 1572.5 0.00 0.0 0.0 0.00

Loading db file '/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_NOMIN25'

Optimization Complete

---------------------

1

create\_clock clk -name clk -period 4.0

1

update\_timing

Information: Updating design information... (UID-85)

1

report\_timing -max\_paths 3

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 3

Design : primary\_lsfr12

Version: I-2013.12-SP5

Date : Tue Dec 1 21:28:06 2015

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: NOMIN25 Library: tc240c

Wire Load Model Mode: top

Startpoint: lfsr12\_reg[144]

(rising edge-triggered flip-flop clocked by clk)

Endpoint: lfsr12\_reg[51]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr12 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

lfsr12\_reg[144]/CP (CFD2QXL) 0.00 0.00 r

lfsr12\_reg[144]/Q (CFD2QXL) 1.22 1.22 r

U594/Z (CEOX1) 0.37 1.60 r

U620/Z (CENX1) 0.25 1.85 r

U621/Z (CENX1) 0.23 2.07 r

U622/Z (CND2X1) 0.16 2.24 f

U672/Z (CIVX2) 0.07 2.30 r

U674/Z (CMXI2X1) 0.11 2.42 f

U675/Z (CND2X1) 0.07 2.49 r

lfsr12\_reg[51]/D (CFD2QXL) 0.00 2.49 r

data arrival time 2.49

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr12\_reg[51]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

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data required time 3.53

data arrival time -2.49

-----------------------------------------------------------

slack (MET) 1.05

Startpoint: lfsr12\_reg[144]

(rising edge-triggered flip-flop clocked by clk)

Endpoint: lfsr12\_reg[119]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr12 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

lfsr12\_reg[144]/CP (CFD2QXL) 0.00 0.00 r

lfsr12\_reg[144]/Q (CFD2QXL) 1.22 1.22 r

U594/Z (CEOX1) 0.37 1.60 r

U620/Z (CENX1) 0.25 1.85 r

U621/Z (CENX1) 0.23 2.07 r

U622/Z (CND2X1) 0.16 2.24 f

U672/Z (CIVX2) 0.07 2.30 r

U677/Z (CMXI2X1) 0.11 2.42 f

U678/Z (CND2X1) 0.07 2.49 r

lfsr12\_reg[119]/D (CFD2QXL) 0.00 2.49 r

data arrival time 2.49

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr12\_reg[119]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

-----------------------------------------------------------

data required time 3.53

data arrival time -2.49

-----------------------------------------------------------

slack (MET) 1.05

Startpoint: write (input port clocked by clk)

Endpoint: lfsr12\_reg[57]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr12 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 f

write (in) 0.09 0.69 f

U517/Z (CND2IX1) 0.17 0.86 f

U512/Z0 (CIVDX2) 0.40 1.27 r

U518/Z (CIVX2) 0.63 1.89 f

U629/Z (CNR2X1) 0.30 2.19 r

U630/Z (CMXI2X1) 0.17 2.36 f

U631/Z (CND2X1) 0.07 2.43 r

lfsr12\_reg[57]/D (CFD2QXL) 0.00 2.43 r

data arrival time 2.43

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr12\_reg[57]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

-----------------------------------------------------------

data required time 3.53

data arrival time -2.43

-----------------------------------------------------------

slack (MET) 1.10

1

analyze -format verilog primary\_lsfr11.v

Running PRESTO HDLC

Searching for ./primary\_lsfr11.v

Compiling source file ./primary\_lsfr11.v

Presto compilation completed successfully.

1

elaborate primary\_lsfr11

Running PRESTO HDLC

Inferred memory devices in process

in routine primary\_lsfr11 line 18 in file

'./primary\_lsfr11.v'.

===============================================================================

| Register Name | Type | Width | Bus | MB | AR | AS | SR | SS | ST |

===============================================================================

| lfsr11\_reg | Flip-flop | 53 | Y | N | Y | N | N | N | N |

===============================================================================

Presto compilation completed successfully.

Elaborated 1 design.

Current design is now 'primary\_lsfr11'.

1

create\_clock clk -name clk -period 3.0

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_clock\_uncertainty 0.25 clk

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_output\_delay 0.5 -clock clk [all\_outputs]

1

set all\_inputs\_wo\_rst\_clk [remove\_from\_collection [remove\_from\_collection [all\_inputs] [get\_port clk]] [get\_port rst]]

Warning: Can't find port 'rst' in design 'primary\_lsfr11'. (UID-95)

{reset write pushin InitialData11[52] InitialData11[51] InitialData11[50] InitialData11[49] InitialData11[48] InitialData11[47] InitialData11[46] InitialData11[45] InitialData11[44] InitialData11[43] InitialData11[42] InitialData11[41] InitialData11[40] InitialData11[39] InitialData11[38] InitialData11[37] InitialData11[36] InitialData11[35] InitialData11[34] InitialData11[33] InitialData11[32] InitialData11[31] InitialData11[30] InitialData11[29] InitialData11[28] InitialData11[27] InitialData11[26] InitialData11[25] InitialData11[24] InitialData11[23] InitialData11[22] InitialData11[21] InitialData11[20] InitialData11[19] InitialData11[18] InitialData11[17] InitialData11[16] InitialData11[15] InitialData11[14] InitialData11[13] InitialData11[12] InitialData11[11] InitialData11[10] InitialData11[9] InitialData11[8] InitialData11[7] InitialData11[6] InitialData11[5] InitialData11[4] InitialData11[3] InitialData11[2] InitialData11[1] InitialData11[0]}

set\_driving\_cell -lib\_cell CND2X1 $all\_inputs\_wo\_rst\_clk

Warning: Design rule attributes from the driving cell will be

set on the port. (UID-401)

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set on the port. (UID-401)

1

set\_input\_delay 0.6 -clock clk $all\_inputs\_wo\_rst\_clk

1

set\_output\_delay 0.6 -clock clk [all\_outputs]

1

set\_fix\_hold [ get\_clocks clk ]

1

set\_output\_delay 0.3 -clock clk [all\_outputs]

1

set\_wire\_load\_model -name T8G00TW8

1

compile\_ultra

Alib files are up-to-date.

Information: Sequential output inversion is enabled. SVF file must be used for formal verification. (OPT-1208)

Information: Ungrouping 0 of 1 hierarchies before Pass 1 (OPT-775)

Beginning Pass 1 Mapping

------------------------

Processing 'primary\_lsfr11'

Updating timing information

Information: Updating design information... (UID-85)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Mapping Optimizations (Ultra High effort)

-------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:01 828.0 0.00 0.0 0.0 0.00

0:00:01 828.0 0.00 0.0 0.0 0.00

0:00:01 828.0 0.00 0.0 0.0 0.00

0:00:01 828.0 0.00 0.0 0.0 0.00

Re-synthesis Optimization (Phase 1)

Re-synthesis Optimization (Phase 2)

Global Optimization (Phase 1)

Global Optimization (Phase 2)

Global Optimization (Phase 3)

Global Optimization (Phase 4)

Global Optimization (Phase 5)

Global Optimization (Phase 6)

Global Optimization (Phase 7)

Global Optimization (Phase 8)

Global Optimization (Phase 9)

Global Optimization (Phase 10)

Global Optimization (Phase 11)

Global Optimization (Phase 12)

Global Optimization (Phase 13)

Global Optimization (Phase 14)

Global Optimization (Phase 15)

Global Optimization (Phase 16)

Global Optimization (Phase 17)

Global Optimization (Phase 18)

Global Optimization (Phase 19)

Global Optimization (Phase 20)

Global Optimization (Phase 21)

Global Optimization (Phase 22)

Global Optimization (Phase 23)

Global Optimization (Phase 24)

Global Optimization (Phase 25)

Global Optimization (Phase 26)

Global Optimization (Phase 27)

Global Optimization (Phase 28)

Global Optimization (Phase 29)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Delay Optimization Phase

----------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:01 651.0 0.00 0.0 0.0 0.00

0:00:01 651.0 0.00 0.0 0.0 0.00

0:00:01 651.0 0.00 0.0 0.0 0.00

0:00:01 651.0 0.00 0.0 0.0 0.00

0:00:01 651.0 0.00 0.0 0.0 0.00

0:00:01 651.0 0.00 0.0 0.0 0.00

0:00:01 651.0 0.00 0.0 0.0 0.00

0:00:01 651.0 0.00 0.0 0.0 0.00

0:00:01 651.0 0.00 0.0 0.0 0.00

0:00:01 651.0 0.00 0.0 0.0 0.00

0:00:01 651.0 0.00 0.0 0.0 0.00

Beginning Delay Optimization

----------------------------

0:00:01 651.0 0.00 0.0 0.0 0.00

0:00:01 651.0 0.00 0.0 0.0 0.00

0:00:01 651.0 0.00 0.0 0.0 0.00

0:00:01 651.0 0.00 0.0 0.0 0.00

0:00:01 651.0 0.00 0.0 0.0 0.00

0:00:01 651.0 0.00 0.0 0.0 0.00

0:00:01 651.0 0.00 0.0 0.0 0.00

0:00:01 651.0 0.00 0.0 0.0 0.00

Beginning Design Rule Fixing (min\_path)

----------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:01 651.0 0.00 0.0 0.0 -0.01

Global Optimization (Phase 30)

Global Optimization (Phase 31)

Global Optimization (Phase 32)

0:00:01 649.0 0.00 0.0 0.0 0.00

0:00:01 638.5 0.00 0.0 0.0 0.00

0:00:01 638.5 0.00 0.0 0.0 0.00

Loaded alib file './alib-52/tc240c.db\_NOMIN25.alib'

0:00:02 638.5 0.00 0.0 0.0 0.00

0:00:02 638.5 0.00 0.0 0.0 0.00

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:02 638.5 0.00 0.0 0.0 0.00

0:00:02 638.5 0.00 0.0 0.0 0.00

Beginning Area-Recovery Phase (max\_area 0)

-----------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:02 638.5 0.00 0.0 0.0 0.00

Global Optimization (Phase 33)

Global Optimization (Phase 34)

Global Optimization (Phase 35)

Global Optimization (Phase 36)

Global Optimization (Phase 37)

Global Optimization (Phase 38)

Global Optimization (Phase 39)

Global Optimization (Phase 40)

Global Optimization (Phase 41)

Global Optimization (Phase 42)

Global Optimization (Phase 43)

Global Optimization (Phase 44)

Global Optimization (Phase 45)

Global Optimization (Phase 46)

Global Optimization (Phase 47)

0:00:02 634.0 0.00 0.0 0.0 0.00

0:00:02 634.0 0.00 0.0 0.0 0.00

0:00:02 634.0 0.00 0.0 0.0 0.00

0:00:02 634.0 0.00 0.0 0.0 0.00

0:00:02 634.0 0.00 0.0 0.0 0.00

0:00:02 634.0 0.00 0.0 0.0 0.00

0:00:02 634.0 0.00 0.0 0.0 0.00

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0:00:02 634.0 0.00 0.0 0.0 0.00

0:00:02 634.0 0.00 0.0 0.0 0.00

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0:00:02 634.0 0.00 0.0 0.0 0.00

0:00:02 634.0 0.00 0.0 0.0 0.00

0:00:02 634.0 0.00 0.0 0.0 0.00

0:00:02 634.0 0.00 0.0 0.0 0.00

0:00:02 634.0 0.00 0.0 0.0 0.00

Loading db file '/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_NOMIN25'

Optimization Complete

---------------------

1

create\_clock clk -name clk -period 4.0

1

update\_timing

Information: Updating design information... (UID-85)

1

report\_timing -max\_paths 3

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 3

Design : primary\_lsfr11

Version: I-2013.12-SP5

Date : Tue Dec 1 21:28:09 2015

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: NOMIN25 Library: tc240c

Wire Load Model Mode: top

Startpoint: lfsr11\_reg[52]

(rising edge-triggered flip-flop clocked by clk)

Endpoint: lfsr11\_reg[29]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr11 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

lfsr11\_reg[52]/CP (CFD2QX1) 0.00 0.00 r

lfsr11\_reg[52]/Q (CFD2QX1) 0.47 0.47 r

U247/Z (CEOX2) 0.38 0.85 r

U258/Z (CENX2) 0.29 1.14 r

U259/Z (CENX1) 0.33 1.47 r

U260/Z (CEOX1) 0.48 1.96 r

U272/Z (CEOX1) 0.27 2.22 r

U273/Z (CENX1) 0.18 2.40 r

U275/Z (COND1XL) 0.12 2.52 f

lfsr11\_reg[29]/D (CFD2QXL) 0.00 2.52 f

data arrival time 2.52

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr11\_reg[29]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

-----------------------------------------------------------

data required time 3.53

data arrival time -2.52

-----------------------------------------------------------

slack (MET) 1.01

Startpoint: write (input port clocked by clk)

Endpoint: lfsr11\_reg[50]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr11 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 r

write (in) 0.02 0.62 r

U191/Z (CNIVX2) 0.71 1.33 r

U195/Z (CND2IX2) 0.48 1.81 r

U190/Z (CIVX3) 0.34 2.15 f

U208/Z (CANR2X1) 0.18 2.33 r

U209/Z (COND1XL) 0.16 2.50 f

lfsr11\_reg[50]/D (CFD2QX1) 0.00 2.50 f

data arrival time 2.50

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr11\_reg[50]/CP (CFD2QX1) 0.00 3.75 r

library setup time -0.23 3.52

data required time 3.52

-----------------------------------------------------------

data required time 3.52

data arrival time -2.50

-----------------------------------------------------------

slack (MET) 1.02

Startpoint: write (input port clocked by clk)

Endpoint: lfsr11\_reg[5]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr11 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 r

write (in) 0.02 0.62 r

U191/Z (CNIVX2) 0.71 1.33 r

U195/Z (CND2IX2) 0.48 1.81 r

U190/Z (CIVX3) 0.34 2.15 f

U212/Z (CANR2X1) 0.18 2.33 r

U213/Z (COND1XL) 0.14 2.48 f

lfsr11\_reg[5]/D (CFD2QXL) 0.00 2.48 f

data arrival time 2.48

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr11\_reg[5]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

-----------------------------------------------------------

data required time 3.53

data arrival time -2.48

-----------------------------------------------------------

slack (MET) 1.05

1

analyze -format verilog primary\_lsfr10.v

Running PRESTO HDLC

Searching for ./primary\_lsfr10.v

Compiling source file ./primary\_lsfr10.v

Presto compilation completed successfully.

1

elaborate primary\_lsfr10

Running PRESTO HDLC

Inferred memory devices in process

in routine primary\_lsfr10 line 20 in file

'./primary\_lsfr10.v'.

===============================================================================

| Register Name | Type | Width | Bus | MB | AR | AS | SR | SS | ST |

===============================================================================

| lfsr10\_reg | Flip-flop | 50 | Y | N | Y | N | N | N | N |

===============================================================================

Presto compilation completed successfully.

Elaborated 1 design.

Current design is now 'primary\_lsfr10'.

1

create\_clock clk -name clk -period 3.0

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_clock\_uncertainty 0.25 clk

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_output\_delay 0.5 -clock clk [all\_outputs]

1

set all\_inputs\_wo\_rst\_clk [remove\_from\_collection [remove\_from\_collection [all\_inputs] [get\_port clk]] [get\_port rst]]

Warning: Can't find port 'rst' in design 'primary\_lsfr10'. (UID-95)

{reset write pushin InitialData10[49] InitialData10[48] InitialData10[47] InitialData10[46] InitialData10[45] InitialData10[44] InitialData10[43] InitialData10[42] InitialData10[41] InitialData10[40] InitialData10[39] InitialData10[38] InitialData10[37] InitialData10[36] InitialData10[35] InitialData10[34] InitialData10[33] InitialData10[32] InitialData10[31] InitialData10[30] InitialData10[29] InitialData10[28] InitialData10[27] InitialData10[26] InitialData10[25] InitialData10[24] InitialData10[23] InitialData10[22] InitialData10[21] InitialData10[20] InitialData10[19] InitialData10[18] InitialData10[17] InitialData10[16] InitialData10[15] InitialData10[14] InitialData10[13] InitialData10[12] InitialData10[11] InitialData10[10] InitialData10[9] InitialData10[8] InitialData10[7] InitialData10[6] InitialData10[5] InitialData10[4] InitialData10[3] InitialData10[2] InitialData10[1] InitialData10[0]}

set\_driving\_cell -lib\_cell CND2X1 $all\_inputs\_wo\_rst\_clk

Warning: Design rule attributes from the driving cell will be

set on the port. (UID-401)

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set\_input\_delay 0.6 -clock clk $all\_inputs\_wo\_rst\_clk

1

set\_output\_delay 0.6 -clock clk [all\_outputs]

1

set\_fix\_hold [ get\_clocks clk ]

1

set\_output\_delay 0.3 -clock clk [all\_outputs]

1

set\_wire\_load\_model -name T8G00TW8

1

compile\_ultra

Alib files are up-to-date.

Information: Sequential output inversion is enabled. SVF file must be used for formal verification. (OPT-1208)

Information: Ungrouping 0 of 1 hierarchies before Pass 1 (OPT-775)

Beginning Pass 1 Mapping

------------------------

Processing 'primary\_lsfr10'

Updating timing information

Information: Updating design information... (UID-85)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Mapping Optimizations (Ultra High effort)

-------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:01 761.5 0.00 0.0 0.0 0.00

0:00:01 761.5 0.00 0.0 0.0 0.00

0:00:01 761.5 0.00 0.0 0.0 0.00

0:00:01 761.5 0.00 0.0 0.0 0.00

Re-synthesis Optimization (Phase 1)

Re-synthesis Optimization (Phase 2)

Global Optimization (Phase 1)

Global Optimization (Phase 2)

Global Optimization (Phase 3)

Global Optimization (Phase 4)

Global Optimization (Phase 5)

Global Optimization (Phase 6)

Global Optimization (Phase 7)

Global Optimization (Phase 8)

Global Optimization (Phase 9)

Global Optimization (Phase 10)

Global Optimization (Phase 11)

Global Optimization (Phase 12)

Global Optimization (Phase 13)

Global Optimization (Phase 14)

Global Optimization (Phase 15)

Global Optimization (Phase 16)

Global Optimization (Phase 17)

Global Optimization (Phase 18)

Global Optimization (Phase 19)

Global Optimization (Phase 20)

Global Optimization (Phase 21)

Global Optimization (Phase 22)

Global Optimization (Phase 23)

Global Optimization (Phase 24)

Global Optimization (Phase 25)

Global Optimization (Phase 26)

Global Optimization (Phase 27)

Global Optimization (Phase 28)

Global Optimization (Phase 29)

Global Optimization (Phase 30)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Delay Optimization Phase

----------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:01 554.5 0.00 0.0 33.6 0.00

0:00:01 554.5 0.00 0.0 33.6 0.00

0:00:01 554.5 0.00 0.0 33.6 0.00

0:00:01 554.5 0.00 0.0 33.6 0.00

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0:00:01 554.5 0.00 0.0 33.6 0.00

Beginning Delay Optimization

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0:00:01 554.5 0.00 0.0 33.6 0.00

0:00:01 554.5 0.00 0.0 33.6 0.00

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0:00:01 554.5 0.00 0.0 33.6 0.00

0:00:01 554.5 0.00 0.0 33.6 0.00

Beginning Design Rule Fixing (max\_capacitance)

----------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:01 554.5 0.00 0.0 33.6 0.00

Global Optimization (Phase 31)

Global Optimization (Phase 32)

Global Optimization (Phase 33)

0:00:02 555.0 0.00 0.0 0.0 0.00

0:00:02 552.0 0.00 0.0 0.0 0.00

0:00:02 552.0 0.00 0.0 0.0 0.00

Loaded alib file './alib-52/tc240c.db\_NOMIN25.alib'

0:00:02 552.0 0.00 0.0 0.0 0.00

0:00:02 552.0 0.00 0.0 0.0 0.00

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:02 552.0 0.00 0.0 0.0 0.00

0:00:02 552.0 0.00 0.0 0.0 0.00

Beginning Area-Recovery Phase (max\_area 0)

-----------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:02 552.0 0.00 0.0 0.0 0.00

Global Optimization (Phase 34)

Global Optimization (Phase 35)

Global Optimization (Phase 36)

Global Optimization (Phase 37)

Global Optimization (Phase 38)

Global Optimization (Phase 39)

Global Optimization (Phase 40)

Global Optimization (Phase 41)

Global Optimization (Phase 42)

Global Optimization (Phase 43)

Global Optimization (Phase 44)

Global Optimization (Phase 45)

Global Optimization (Phase 46)

Global Optimization (Phase 47)

0:00:02 550.0 0.00 0.0 0.0 0.00

0:00:02 550.0 0.00 0.0 0.0 0.00

0:00:02 550.0 0.00 0.0 0.0 0.00

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0:00:02 550.0 0.00 0.0 0.0 0.00

0:00:02 550.0 0.00 0.0 0.0 0.00

Loading db file '/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_NOMIN25'

Optimization Complete

---------------------

1

create\_clock clk -name clk -period 4.0

1

update\_timing

Information: Updating design information... (UID-85)

1

report\_timing -max\_paths 3

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 3

Design : primary\_lsfr10

Version: I-2013.12-SP5

Date : Tue Dec 1 21:28:12 2015

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: NOMIN25 Library: tc240c

Wire Load Model Mode: top

Startpoint: write (input port clocked by clk)

Endpoint: lfsr10\_reg[7]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr10 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 f

write (in) 0.04 0.64 f

U171/Z (CNIVX4) 0.34 0.97 f

U172/Z (CNR2IX2) 0.52 1.49 r

U225/Z (CIVX2) 0.51 2.00 f

U236/Z (COND1XL) 0.17 2.17 r

lfsr10\_reg[7]/D (CFD2QXL) 0.00 2.17 r

data arrival time 2.17

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr10\_reg[7]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.23 3.52

data required time 3.52

-----------------------------------------------------------

data required time 3.52

data arrival time -2.17

-----------------------------------------------------------

slack (MET) 1.35

Startpoint: write (input port clocked by clk)

Endpoint: lfsr10\_reg[6]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr10 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 f

write (in) 0.04 0.64 f

U171/Z (CNIVX4) 0.34 0.97 f

U172/Z (CNR2IX2) 0.52 1.49 r

U225/Z (CIVX2) 0.51 2.00 f

U232/Z (COND1XL) 0.17 2.17 r

lfsr10\_reg[6]/D (CFD2QXL) 0.00 2.17 r

data arrival time 2.17

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr10\_reg[6]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.23 3.52

data required time 3.52

-----------------------------------------------------------

data required time 3.52

data arrival time -2.17

-----------------------------------------------------------

slack (MET) 1.35

Startpoint: write (input port clocked by clk)

Endpoint: lfsr10\_reg[5]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr10 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 f

write (in) 0.04 0.64 f

U171/Z (CNIVX4) 0.34 0.97 f

U172/Z (CNR2IX2) 0.52 1.49 r

U225/Z (CIVX2) 0.51 2.00 f

U228/Z (COND1XL) 0.17 2.17 r

lfsr10\_reg[5]/D (CFD2QXL) 0.00 2.17 r

data arrival time 2.17

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr10\_reg[5]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.23 3.52

data required time 3.52

-----------------------------------------------------------

data required time 3.52

data arrival time -2.17

-----------------------------------------------------------

slack (MET) 1.35

1

analyze -format verilog primary\_lsfr9.v

Running PRESTO HDLC

Searching for ./primary\_lsfr9.v

Compiling source file ./primary\_lsfr9.v

Presto compilation completed successfully.

1

elaborate primary\_lsfr9

Running PRESTO HDLC

Inferred memory devices in process

in routine primary\_lsfr9 line 18 in file

'./primary\_lsfr9.v'.

===============================================================================

| Register Name | Type | Width | Bus | MB | AR | AS | SR | SS | ST |

===============================================================================

| lfsr9\_reg | Flip-flop | 127 | Y | N | Y | N | N | N | N |

===============================================================================

Presto compilation completed successfully.

Elaborated 1 design.

Current design is now 'primary\_lsfr9'.

1

create\_clock clk -name clk -period 3.0

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_clock\_uncertainty 0.25 clk

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_output\_delay 0.5 -clock clk [all\_outputs]

1

set all\_inputs\_wo\_rst\_clk [remove\_from\_collection [remove\_from\_collection [all\_inputs] [get\_port clk]] [get\_port rst]]

Warning: Can't find port 'rst' in design 'primary\_lsfr9'. (UID-95)

{reset write pushin InitialData9[126] InitialData9[125] InitialData9[124] InitialData9[123] InitialData9[122] InitialData9[121] InitialData9[120] InitialData9[119] InitialData9[118] InitialData9[117] InitialData9[116] InitialData9[115] InitialData9[114] InitialData9[113] InitialData9[112] InitialData9[111] InitialData9[110] InitialData9[109] InitialData9[108] InitialData9[107] InitialData9[106] InitialData9[105] InitialData9[104] InitialData9[103] InitialData9[102] InitialData9[101] InitialData9[100] InitialData9[99] InitialData9[98] InitialData9[97] InitialData9[96] InitialData9[95] InitialData9[94] InitialData9[93] InitialData9[92] InitialData9[91] InitialData9[90] InitialData9[89] InitialData9[88] InitialData9[87] InitialData9[86] InitialData9[85] InitialData9[84] InitialData9[83] InitialData9[82] InitialData9[81] InitialData9[80] InitialData9[79] InitialData9[78] InitialData9[77] InitialData9[76] InitialData9[75] InitialData9[74] InitialData9[73] InitialData9[72] InitialData9[71] InitialData9[70] InitialData9[69] InitialData9[68] InitialData9[67] InitialData9[66] InitialData9[65] InitialData9[64] InitialData9[63] InitialData9[62] InitialData9[61] InitialData9[60] InitialData9[59] InitialData9[58] InitialData9[57] InitialData9[56] InitialData9[55] InitialData9[54] InitialData9[53] InitialData9[52] InitialData9[51] InitialData9[50] InitialData9[49] InitialData9[48] InitialData9[47] InitialData9[46] InitialData9[45] InitialData9[44] InitialData9[43] InitialData9[42] InitialData9[41] InitialData9[40] InitialData9[39] InitialData9[38] InitialData9[37] InitialData9[36] InitialData9[35] InitialData9[34] InitialData9[33] InitialData9[32] InitialData9[31] InitialData9[30] ...}

set\_driving\_cell -lib\_cell CND2X1 $all\_inputs\_wo\_rst\_clk

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1

set\_input\_delay 0.6 -clock clk $all\_inputs\_wo\_rst\_clk

1

set\_output\_delay 0.6 -clock clk [all\_outputs]

1

set\_fix\_hold [ get\_clocks clk ]

1

set\_output\_delay 0.3 -clock clk [all\_outputs]

1

set\_wire\_load\_model -name T8G00TW8

1

compile\_ultra

Alib files are up-to-date.

Information: Sequential output inversion is enabled. SVF file must be used for formal verification. (OPT-1208)

Information: Ungrouping 0 of 1 hierarchies before Pass 1 (OPT-775)

Beginning Pass 1 Mapping

------------------------

Processing 'primary\_lsfr9'

Updating timing information

Information: Updating design information... (UID-85)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Mapping Optimizations (Ultra High effort)

-------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:02 1624.0 0.00 0.0 0.0 0.00

0:00:02 1624.0 0.00 0.0 0.0 0.00

0:00:02 1624.0 0.00 0.0 0.0 0.00

0:00:02 1624.0 0.00 0.0 0.0 0.00

Re-synthesis Optimization (Phase 1)

Re-synthesis Optimization (Phase 2)

Global Optimization (Phase 1)

Global Optimization (Phase 2)

Global Optimization (Phase 3)

Global Optimization (Phase 4)

Global Optimization (Phase 5)

Global Optimization (Phase 6)

Global Optimization (Phase 7)

Global Optimization (Phase 8)

Global Optimization (Phase 9)

Global Optimization (Phase 10)

Global Optimization (Phase 11)

Global Optimization (Phase 12)

Global Optimization (Phase 13)

Global Optimization (Phase 14)

Global Optimization (Phase 15)

Global Optimization (Phase 16)

Global Optimization (Phase 17)

Global Optimization (Phase 18)

Global Optimization (Phase 19)

Global Optimization (Phase 20)

Global Optimization (Phase 21)

Global Optimization (Phase 22)

Global Optimization (Phase 23)

Global Optimization (Phase 24)

Global Optimization (Phase 25)

Global Optimization (Phase 26)

Global Optimization (Phase 27)

Global Optimization (Phase 28)

Global Optimization (Phase 29)

Global Optimization (Phase 30)

Global Optimization (Phase 31)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Delay Optimization Phase

----------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:03 1284.0 0.00 0.0 1244.7 0.00

0:00:03 1284.0 0.00 0.0 1244.7 0.00

0:00:03 1284.0 0.00 0.0 1244.7 0.00

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0:00:03 1284.0 0.00 0.0 1244.7 0.00

Beginning Delay Optimization

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0:00:03 1284.0 0.00 0.0 1244.7 0.00

0:00:03 1284.0 0.00 0.0 1244.7 0.00

0:00:03 1284.0 0.00 0.0 1244.7 0.00

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0:00:03 1284.0 0.00 0.0 1244.7 0.00

0:00:03 1284.0 0.00 0.0 1244.7 0.00

0:00:03 1284.0 0.00 0.0 1244.7 0.00

Beginning Design Rule Fixing (max\_capacitance)

----------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:03 1284.0 0.00 0.0 1244.7 0.00

Global Optimization (Phase 32)

Global Optimization (Phase 33)

Global Optimization (Phase 34)

0:00:03 1285.0 0.00 0.0 0.0 0.00

0:00:03 1284.0 0.00 0.0 0.0 0.00

0:00:03 1284.0 0.00 0.0 0.0 0.00

Loaded alib file './alib-52/tc240c.db\_NOMIN25.alib'

0:00:03 1284.0 0.00 0.0 0.0 0.00

0:00:03 1284.0 0.00 0.0 0.0 0.00

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:03 1284.0 0.00 0.0 0.0 0.00

0:00:04 1271.5 0.00 0.0 115.6 0.00

Beginning Area-Recovery Phase (max\_area 0)

-----------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:04 1271.5 0.00 0.0 115.6 0.00

Global Optimization (Phase 35)

Global Optimization (Phase 36)

Global Optimization (Phase 37)

Global Optimization (Phase 38)

Global Optimization (Phase 39)

Global Optimization (Phase 40)

Global Optimization (Phase 41)

Global Optimization (Phase 42)

Global Optimization (Phase 43)

Global Optimization (Phase 44)

Global Optimization (Phase 45)

Global Optimization (Phase 46)

Global Optimization (Phase 47)

Global Optimization (Phase 48)

Global Optimization (Phase 49)

0:00:04 1261.5 0.00 0.0 0.0 0.00

0:00:04 1261.5 0.00 0.0 0.0 0.00

0:00:04 1261.5 0.00 0.0 0.0 0.00

0:00:04 1261.5 0.00 0.0 0.0 0.00

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0:00:04 1261.5 0.00 0.0 0.0 0.00

0:00:04 1261.5 0.00 0.0 0.0 0.00

Loading db file '/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_NOMIN25'

Optimization Complete

---------------------

1

create\_clock clk -name clk -period 4.0

1

update\_timing

Information: Updating design information... (UID-85)

1

report\_timing -max\_paths 3

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 3

Design : primary\_lsfr9

Version: I-2013.12-SP5

Date : Tue Dec 1 21:28:16 2015

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: NOMIN25 Library: tc240c

Wire Load Model Mode: top

Startpoint: write (input port clocked by clk)

Endpoint: lfsr9\_reg[47]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr9 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 r

write (in) 0.06 0.66 r

U400/Z (CNIVX8) 0.36 1.02 r

U395/Z (COR2X2) 0.44 1.46 r

U396/Z (CIVX3) 0.64 2.10 f

U450/Z (CANR2X1) 0.21 2.31 r

U451/Z (COND4CX1) 0.15 2.46 f

lfsr9\_reg[47]/D (CFD2XL) 0.00 2.46 f

data arrival time 2.46

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr9\_reg[47]/CP (CFD2XL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

-----------------------------------------------------------

data required time 3.53

data arrival time -2.46

-----------------------------------------------------------

slack (MET) 1.07

Startpoint: write (input port clocked by clk)

Endpoint: lfsr9\_reg[46]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr9 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 r

write (in) 0.06 0.66 r

U400/Z (CNIVX8) 0.36 1.02 r

U395/Z (COR2X2) 0.44 1.46 r

U396/Z (CIVX3) 0.64 2.10 f

U447/Z (CANR2X1) 0.21 2.31 r

U448/Z (COND4CX1) 0.15 2.46 f

lfsr9\_reg[46]/D (CFD2XL) 0.00 2.46 f

data arrival time 2.46

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr9\_reg[46]/CP (CFD2XL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

-----------------------------------------------------------

data required time 3.53

data arrival time -2.46

-----------------------------------------------------------

slack (MET) 1.07

Startpoint: write (input port clocked by clk)

Endpoint: lfsr9\_reg[45]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr9 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 r

write (in) 0.06 0.66 r

U400/Z (CNIVX8) 0.36 1.02 r

U395/Z (COR2X2) 0.44 1.46 r

U396/Z (CIVX3) 0.64 2.10 f

U444/Z (CANR2X1) 0.21 2.31 r

U445/Z (COND4CX1) 0.15 2.46 f

lfsr9\_reg[45]/D (CFD2XL) 0.00 2.46 f

data arrival time 2.46

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr9\_reg[45]/CP (CFD2XL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

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data required time 3.53

data arrival time -2.46

-----------------------------------------------------------

slack (MET) 1.07

1

analyze -format verilog primary\_lsfr8.v

Running PRESTO HDLC

Searching for ./primary\_lsfr8.v

Compiling source file ./primary\_lsfr8.v

Presto compilation completed successfully.

1

elaborate primary\_lsfr8

Running PRESTO HDLC

Inferred memory devices in process

in routine primary\_lsfr8 line 20 in file

'./primary\_lsfr8.v'.

===============================================================================

| Register Name | Type | Width | Bus | MB | AR | AS | SR | SS | ST |

===============================================================================

| lfsr8\_reg | Flip-flop | 70 | Y | N | Y | N | N | N | N |

===============================================================================

Presto compilation completed successfully.

Elaborated 1 design.

Current design is now 'primary\_lsfr8'.

1

create\_clock clk -name clk -period 3.0

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_clock\_uncertainty 0.25 clk

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_output\_delay 0.5 -clock clk [all\_outputs]

1

set all\_inputs\_wo\_rst\_clk [remove\_from\_collection [remove\_from\_collection [all\_inputs] [get\_port clk]] [get\_port rst]]

Warning: Can't find port 'rst' in design 'primary\_lsfr8'. (UID-95)

{reset write pushin InitialData8[69] InitialData8[68] InitialData8[67] InitialData8[66] InitialData8[65] InitialData8[64] InitialData8[63] InitialData8[62] InitialData8[61] InitialData8[60] InitialData8[59] InitialData8[58] InitialData8[57] InitialData8[56] InitialData8[55] InitialData8[54] InitialData8[53] InitialData8[52] InitialData8[51] InitialData8[50] InitialData8[49] InitialData8[48] InitialData8[47] InitialData8[46] InitialData8[45] InitialData8[44] InitialData8[43] InitialData8[42] InitialData8[41] InitialData8[40] InitialData8[39] InitialData8[38] InitialData8[37] InitialData8[36] InitialData8[35] InitialData8[34] InitialData8[33] InitialData8[32] InitialData8[31] InitialData8[30] InitialData8[29] InitialData8[28] InitialData8[27] InitialData8[26] InitialData8[25] InitialData8[24] InitialData8[23] InitialData8[22] InitialData8[21] InitialData8[20] InitialData8[19] InitialData8[18] InitialData8[17] InitialData8[16] InitialData8[15] InitialData8[14] InitialData8[13] InitialData8[12] InitialData8[11] InitialData8[10] InitialData8[9] InitialData8[8] InitialData8[7] InitialData8[6] InitialData8[5] InitialData8[4] InitialData8[3] InitialData8[2] InitialData8[1] InitialData8[0]}

set\_driving\_cell -lib\_cell CND2X1 $all\_inputs\_wo\_rst\_clk

Warning: Design rule attributes from the driving cell will be

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1

set\_input\_delay 0.6 -clock clk $all\_inputs\_wo\_rst\_clk

1

set\_output\_delay 0.6 -clock clk [all\_outputs]

1

set\_fix\_hold [ get\_clocks clk ]

1

set\_output\_delay 0.3 -clock clk [all\_outputs]

1

set\_wire\_load\_model -name T8G00TW8

1

compile\_ultra

Alib files are up-to-date.

Information: Sequential output inversion is enabled. SVF file must be used for formal verification. (OPT-1208)

Information: Ungrouping 0 of 1 hierarchies before Pass 1 (OPT-775)

Beginning Pass 1 Mapping

------------------------

Processing 'primary\_lsfr8'

Updating timing information

Information: Updating design information... (UID-85)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Mapping Optimizations (Ultra High effort)

-------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:01 1030.0 0.00 0.0 0.0 0.00

0:00:01 1030.0 0.00 0.0 0.0 0.00

0:00:01 1030.0 0.00 0.0 0.0 0.00

0:00:01 1030.0 0.00 0.0 0.0 0.00

Re-synthesis Optimization (Phase 1)

Re-synthesis Optimization (Phase 2)

Global Optimization (Phase 1)

Global Optimization (Phase 2)

Global Optimization (Phase 3)

Global Optimization (Phase 4)

Global Optimization (Phase 5)

Global Optimization (Phase 6)

Global Optimization (Phase 7)

Global Optimization (Phase 8)

Global Optimization (Phase 9)

Global Optimization (Phase 10)

Global Optimization (Phase 11)

Global Optimization (Phase 12)

Global Optimization (Phase 13)

Global Optimization (Phase 14)

Global Optimization (Phase 15)

Global Optimization (Phase 16)

Global Optimization (Phase 17)

Global Optimization (Phase 18)

Global Optimization (Phase 19)

Global Optimization (Phase 20)

Global Optimization (Phase 21)

Global Optimization (Phase 22)

Global Optimization (Phase 23)

Global Optimization (Phase 24)

Global Optimization (Phase 25)

Global Optimization (Phase 26)

Global Optimization (Phase 27)

Global Optimization (Phase 28)

Global Optimization (Phase 29)

Global Optimization (Phase 30)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Delay Optimization Phase

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TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:01 773.0 0.00 0.0 0.0 0.00

0:00:01 773.0 0.00 0.0 0.0 0.00

0:00:01 773.0 0.00 0.0 0.0 0.00

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Beginning Delay Optimization

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0:00:01 773.0 0.00 0.0 0.0 0.00

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0:00:01 773.0 0.00 0.0 0.0 0.00

0:00:01 770.0 0.00 0.0 0.0 0.00

0:00:01 770.0 0.00 0.0 0.0 0.00

Loaded alib file './alib-52/tc240c.db\_NOMIN25.alib'

0:00:03 770.0 0.00 0.0 0.0 0.00

0:00:03 770.0 0.00 0.0 0.0 0.00

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:03 770.0 0.00 0.0 0.0 0.00

0:00:03 769.5 0.00 0.0 0.0 0.00

Beginning Area-Recovery Phase (max\_area 0)

-----------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:03 769.5 0.00 0.0 0.0 0.00

Global Optimization (Phase 31)

Global Optimization (Phase 32)

Global Optimization (Phase 33)

Global Optimization (Phase 34)

Global Optimization (Phase 35)

Global Optimization (Phase 36)

Global Optimization (Phase 37)

Global Optimization (Phase 38)

Global Optimization (Phase 39)

Global Optimization (Phase 40)

Global Optimization (Phase 41)

Global Optimization (Phase 42)

Global Optimization (Phase 43)

Global Optimization (Phase 44)

Global Optimization (Phase 45)

0:00:03 765.5 0.00 0.0 0.0 0.00

0:00:03 765.5 0.00 0.0 0.0 0.00

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0:00:03 765.5 0.00 0.0 0.0 0.00

Loading db file '/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_NOMIN25'

Optimization Complete

---------------------

1

create\_clock clk -name clk -period 4.0

1

update\_timing

Information: Updating design information... (UID-85)

1

report\_timing -max\_paths 3

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 3

Design : primary\_lsfr8

Version: I-2013.12-SP5

Date : Tue Dec 1 21:28:20 2015

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: NOMIN25 Library: tc240c

Wire Load Model Mode: top

Startpoint: write (input port clocked by clk)

Endpoint: lfsr8\_reg[18]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr8 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 r

write (in) 0.03 0.63 r

U234/Z (CNIVX8) 0.32 0.95 r

U235/Z (CND2IX1) 0.64 1.59 r

U267/Z0 (CIVDX1) 0.52 2.11 f

U332/Z (CANR2XL) 0.24 2.34 r

U333/Z (COND1XL) 0.17 2.51 f

lfsr8\_reg[18]/D (CFD2QXL) 0.00 2.51 f

data arrival time 2.51

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr8\_reg[18]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

-----------------------------------------------------------

data required time 3.53

data arrival time -2.51

-----------------------------------------------------------

slack (MET) 1.02

Startpoint: write (input port clocked by clk)

Endpoint: lfsr8\_reg[17]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr8 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 r

write (in) 0.03 0.63 r

U234/Z (CNIVX8) 0.32 0.95 r

U235/Z (CND2IX1) 0.64 1.59 r

U267/Z0 (CIVDX1) 0.52 2.11 f

U329/Z (CANR2XL) 0.24 2.34 r

U330/Z (COND1XL) 0.17 2.51 f

lfsr8\_reg[17]/D (CFD2QXL) 0.00 2.51 f

data arrival time 2.51

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr8\_reg[17]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

-----------------------------------------------------------

data required time 3.53

data arrival time -2.51

-----------------------------------------------------------

slack (MET) 1.02

Startpoint: write (input port clocked by clk)

Endpoint: lfsr8\_reg[19]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr8 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 r

write (in) 0.03 0.63 r

U234/Z (CNIVX8) 0.32 0.95 r

U235/Z (CND2IX1) 0.64 1.59 r

U267/Z0 (CIVDX1) 0.52 2.11 f

U335/Z (CANR2XL) 0.24 2.34 r

U336/Z (COND1XL) 0.17 2.51 f

lfsr8\_reg[19]/D (CFD2QXL) 0.00 2.51 f

data arrival time 2.51

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr8\_reg[19]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

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data required time 3.53

data arrival time -2.51

-----------------------------------------------------------

slack (MET) 1.02

1

analyze -format verilog primary\_lsfr7.v

Running PRESTO HDLC

Searching for ./primary\_lsfr7.v

Compiling source file ./primary\_lsfr7.v

Presto compilation completed successfully.

1

elaborate primary\_lsfr7

Running PRESTO HDLC

Inferred memory devices in process

in routine primary\_lsfr7 line 20 in file

'./primary\_lsfr7.v'.

===============================================================================

| Register Name | Type | Width | Bus | MB | AR | AS | SR | SS | ST |

===============================================================================

| lfsr7\_reg | Flip-flop | 212 | Y | N | Y | N | N | N | N |

===============================================================================

Presto compilation completed successfully.

Elaborated 1 design.

Current design is now 'primary\_lsfr7'.

1

create\_clock clk -name clk -period 3.0

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_clock\_uncertainty 0.25 clk

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_output\_delay 0.5 -clock clk [all\_outputs]

1

set all\_inputs\_wo\_rst\_clk [remove\_from\_collection [remove\_from\_collection [all\_inputs] [get\_port clk]] [get\_port rst]]

Warning: Can't find port 'rst' in design 'primary\_lsfr7'. (UID-95)

{reset write pushin InitialData7[211] InitialData7[210] InitialData7[209] InitialData7[208] InitialData7[207] InitialData7[206] InitialData7[205] InitialData7[204] InitialData7[203] InitialData7[202] InitialData7[201] InitialData7[200] InitialData7[199] InitialData7[198] InitialData7[197] InitialData7[196] InitialData7[195] InitialData7[194] InitialData7[193] InitialData7[192] InitialData7[191] InitialData7[190] InitialData7[189] InitialData7[188] InitialData7[187] InitialData7[186] InitialData7[185] InitialData7[184] InitialData7[183] InitialData7[182] InitialData7[181] InitialData7[180] InitialData7[179] InitialData7[178] InitialData7[177] InitialData7[176] InitialData7[175] InitialData7[174] InitialData7[173] InitialData7[172] InitialData7[171] InitialData7[170] InitialData7[169] InitialData7[168] InitialData7[167] InitialData7[166] InitialData7[165] InitialData7[164] InitialData7[163] InitialData7[162] InitialData7[161] InitialData7[160] InitialData7[159] InitialData7[158] InitialData7[157] InitialData7[156] InitialData7[155] InitialData7[154] InitialData7[153] InitialData7[152] InitialData7[151] InitialData7[150] InitialData7[149] InitialData7[148] InitialData7[147] InitialData7[146] InitialData7[145] InitialData7[144] InitialData7[143] InitialData7[142] InitialData7[141] InitialData7[140] InitialData7[139] InitialData7[138] InitialData7[137] InitialData7[136] InitialData7[135] InitialData7[134] InitialData7[133] InitialData7[132] InitialData7[131] InitialData7[130] InitialData7[129] InitialData7[128] InitialData7[127] InitialData7[126] InitialData7[125] InitialData7[124] InitialData7[123] InitialData7[122] InitialData7[121] InitialData7[120] InitialData7[119] InitialData7[118] InitialData7[117] InitialData7[116] InitialData7[115] ...}

set\_driving\_cell -lib\_cell CND2X1 $all\_inputs\_wo\_rst\_clk

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set\_input\_delay 0.6 -clock clk $all\_inputs\_wo\_rst\_clk

1

set\_output\_delay 0.6 -clock clk [all\_outputs]

1

set\_fix\_hold [ get\_clocks clk ]

1

set\_output\_delay 0.3 -clock clk [all\_outputs]

1

set\_wire\_load\_model -name T8G00TW8

1

compile\_ultra

Alib files are up-to-date.

Information: Sequential output inversion is enabled. SVF file must be used for formal verification. (OPT-1208)

Information: Ungrouping 0 of 1 hierarchies before Pass 1 (OPT-775)

Beginning Pass 1 Mapping

------------------------

Processing 'primary\_lsfr7'

Updating timing information

Information: Updating design information... (UID-85)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Mapping Optimizations (Ultra High effort)

-------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:02 3036.5 0.00 0.0 0.0 0.00

0:00:02 3036.5 0.00 0.0 0.0 0.00

0:00:02 3036.5 0.00 0.0 0.0 0.00

0:00:02 3036.5 0.00 0.0 0.0 0.00

Re-synthesis Optimization (Phase 1)

Re-synthesis Optimization (Phase 2)

Global Optimization (Phase 1)

Global Optimization (Phase 2)

Global Optimization (Phase 3)

Global Optimization (Phase 4)

Global Optimization (Phase 5)

Global Optimization (Phase 6)

Global Optimization (Phase 7)

Global Optimization (Phase 8)

Global Optimization (Phase 9)

Global Optimization (Phase 10)

Global Optimization (Phase 11)

Global Optimization (Phase 12)

Global Optimization (Phase 13)

Global Optimization (Phase 14)

Global Optimization (Phase 15)

Global Optimization (Phase 16)

Global Optimization (Phase 17)

Global Optimization (Phase 18)

Global Optimization (Phase 19)

Global Optimization (Phase 20)

Global Optimization (Phase 21)

Global Optimization (Phase 22)

Global Optimization (Phase 23)

Global Optimization (Phase 24)

Global Optimization (Phase 25)

Global Optimization (Phase 26)

Global Optimization (Phase 27)

Global Optimization (Phase 28)

Global Optimization (Phase 29)

Global Optimization (Phase 30)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Delay Optimization Phase

----------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:03 2104.5 0.00 0.0 1010.0 0.00

0:00:03 2104.5 0.00 0.0 1010.0 0.00

0:00:03 2104.5 0.00 0.0 1010.0 0.00

0:00:03 2104.5 0.00 0.0 1010.0 0.00

0:00:03 2104.5 0.00 0.0 1010.0 0.00

0:00:03 2104.5 0.00 0.0 1010.0 0.00

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0:00:03 2104.5 0.00 0.0 1010.0 0.00

Beginning Delay Optimization

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0:00:03 2104.5 0.00 0.0 1010.0 0.00

0:00:03 2104.5 0.00 0.0 1010.0 0.00

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0:00:03 2104.5 0.00 0.0 1010.0 0.00

0:00:03 2104.5 0.00 0.0 1010.0 0.00

Beginning Design Rule Fixing (max\_capacitance)

----------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:03 2104.5 0.00 0.0 1010.0 0.00

Global Optimization (Phase 31)

Global Optimization (Phase 32)

Global Optimization (Phase 33)

0:00:03 2105.5 0.00 0.0 0.0 0.00

0:00:03 2101.5 0.00 0.0 0.0 0.00

0:00:03 2101.5 0.00 0.0 0.0 0.00

Loaded alib file './alib-52/tc240c.db\_NOMIN25.alib'

0:00:04 2101.5 0.00 0.0 0.0 0.00

0:00:04 2101.5 0.00 0.0 0.0 0.00

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:04 2101.5 0.00 0.0 0.0 0.00

0:00:04 2028.0 0.00 0.0 2021.5 0.00

0:00:04 2431.0 0.00 0.0 0.0 0.00

Beginning Area-Recovery Phase (max\_area 0)

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TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:04 2431.0 0.00 0.0 0.0 0.00

Global Optimization (Phase 34)

Global Optimization (Phase 35)

Global Optimization (Phase 36)

Global Optimization (Phase 37)

Global Optimization (Phase 38)

Global Optimization (Phase 39)

Global Optimization (Phase 40)

Global Optimization (Phase 41)

Global Optimization (Phase 42)

Global Optimization (Phase 43)

Global Optimization (Phase 44)

Global Optimization (Phase 45)

Global Optimization (Phase 46)

Global Optimization (Phase 47)

Global Optimization (Phase 48)

0:00:04 2020.0 0.00 0.0 0.0 0.00

0:00:04 2020.0 0.00 0.0 0.0 0.00

0:00:04 2020.0 0.00 0.0 0.0 0.00

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0:00:04 2020.0 0.00 0.0 0.0 0.00

Loading db file '/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_NOMIN25'

Optimization Complete

---------------------

1

create\_clock clk -name clk -period 4.0

1

update\_timing

Information: Updating design information... (UID-85)

1

report\_timing -max\_paths 3

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 3

Design : primary\_lsfr7

Version: I-2013.12-SP5

Date : Tue Dec 1 21:28:26 2015

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: NOMIN25 Library: tc240c

Wire Load Model Mode: top

Startpoint: write (input port clocked by clk)

Endpoint: lfsr7\_reg[15]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr7 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 r

write (in) 0.05 0.65 r

U649/Z (CNIVX12) 0.50 1.15 r

U652/Z (CNR2X1) 0.19 1.34 f

U665/Z0 (CIVDX2) 0.43 1.78 r

U659/Z (CIVX16) 0.32 2.10 f

U903/Z (CANR2XL) 0.23 2.33 r

U904/Z (COND1XL) 0.17 2.49 f

lfsr7\_reg[15]/D (CFD2XL) 0.00 2.49 f

data arrival time 2.49

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr7\_reg[15]/CP (CFD2XL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

-----------------------------------------------------------

data required time 3.53

data arrival time -2.49

-----------------------------------------------------------

slack (MET) 1.04

Startpoint: write (input port clocked by clk)

Endpoint: lfsr7\_reg[14]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr7 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 r

write (in) 0.05 0.65 r

U649/Z (CNIVX12) 0.50 1.15 r

U652/Z (CNR2X1) 0.19 1.34 f

U665/Z0 (CIVDX2) 0.43 1.78 r

U659/Z (CIVX16) 0.32 2.10 f

U879/Z (CANR2XL) 0.23 2.33 r

U880/Z (COND1XL) 0.17 2.49 f

lfsr7\_reg[14]/D (CFD2XL) 0.00 2.49 f

data arrival time 2.49

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr7\_reg[14]/CP (CFD2XL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

-----------------------------------------------------------

data required time 3.53

data arrival time -2.49

-----------------------------------------------------------

slack (MET) 1.04

Startpoint: write (input port clocked by clk)

Endpoint: lfsr7\_reg[13]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr7 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 r

write (in) 0.05 0.65 r

U649/Z (CNIVX12) 0.50 1.15 r

U652/Z (CNR2X1) 0.19 1.34 f

U665/Z0 (CIVDX2) 0.43 1.78 r

U659/Z (CIVX16) 0.32 2.10 f

U859/Z (CANR2XL) 0.23 2.33 r

U860/Z (COND1XL) 0.17 2.49 f

lfsr7\_reg[13]/D (CFD2XL) 0.00 2.49 f

data arrival time 2.49

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr7\_reg[13]/CP (CFD2XL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

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data required time 3.53

data arrival time -2.49

-----------------------------------------------------------

slack (MET) 1.04

1

analyze -format verilog primary\_lsfr6.v

Running PRESTO HDLC

Searching for ./primary\_lsfr6.v

Compiling source file ./primary\_lsfr6.v

Presto compilation completed successfully.

1

elaborate primary\_lsfr6

Running PRESTO HDLC

Inferred memory devices in process

in routine primary\_lsfr6 line 19 in file

'./primary\_lsfr6.v'.

===============================================================================

| Register Name | Type | Width | Bus | MB | AR | AS | SR | SS | ST |

===============================================================================

| lfsr6\_reg | Flip-flop | 528 | Y | N | Y | N | N | N | N |

===============================================================================

Presto compilation completed successfully.

Elaborated 1 design.

Current design is now 'primary\_lsfr6'.

1

create\_clock clk -name clk -period 3.0

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_clock\_uncertainty 0.25 clk

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_output\_delay 0.5 -clock clk [all\_outputs]

1

set all\_inputs\_wo\_rst\_clk [remove\_from\_collection [remove\_from\_collection [all\_inputs] [get\_port clk]] [get\_port rst]]

Warning: Can't find port 'rst' in design 'primary\_lsfr6'. (UID-95)

{reset write pushin InitialData6[527] InitialData6[526] InitialData6[525] InitialData6[524] InitialData6[523] InitialData6[522] InitialData6[521] InitialData6[520] InitialData6[519] InitialData6[518] InitialData6[517] InitialData6[516] InitialData6[515] InitialData6[514] InitialData6[513] InitialData6[512] InitialData6[511] InitialData6[510] InitialData6[509] InitialData6[508] InitialData6[507] InitialData6[506] InitialData6[505] InitialData6[504] InitialData6[503] InitialData6[502] InitialData6[501] InitialData6[500] InitialData6[499] InitialData6[498] InitialData6[497] InitialData6[496] InitialData6[495] InitialData6[494] InitialData6[493] InitialData6[492] InitialData6[491] InitialData6[490] InitialData6[489] InitialData6[488] InitialData6[487] InitialData6[486] InitialData6[485] InitialData6[484] InitialData6[483] InitialData6[482] InitialData6[481] InitialData6[480] InitialData6[479] InitialData6[478] InitialData6[477] InitialData6[476] InitialData6[475] InitialData6[474] InitialData6[473] InitialData6[472] InitialData6[471] InitialData6[470] InitialData6[469] InitialData6[468] InitialData6[467] InitialData6[466] InitialData6[465] InitialData6[464] InitialData6[463] InitialData6[462] InitialData6[461] InitialData6[460] InitialData6[459] InitialData6[458] InitialData6[457] InitialData6[456] InitialData6[455] InitialData6[454] InitialData6[453] InitialData6[452] InitialData6[451] InitialData6[450] InitialData6[449] InitialData6[448] InitialData6[447] InitialData6[446] InitialData6[445] InitialData6[444] InitialData6[443] InitialData6[442] InitialData6[441] InitialData6[440] InitialData6[439] InitialData6[438] InitialData6[437] InitialData6[436] InitialData6[435] InitialData6[434] InitialData6[433] InitialData6[432] InitialData6[431] ...}

set\_driving\_cell -lib\_cell CND2X1 $all\_inputs\_wo\_rst\_clk

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set\_input\_delay 0.6 -clock clk $all\_inputs\_wo\_rst\_clk

1

set\_output\_delay 0.6 -clock clk [all\_outputs]

1

set\_fix\_hold [ get\_clocks clk ]

1

set\_output\_delay 0.3 -clock clk [all\_outputs]

1

set\_wire\_load\_model -name T8G00TW8

1

compile\_ultra

Alib files are up-to-date.

Information: Sequential output inversion is enabled. SVF file must be used for formal verification. (OPT-1208)

Information: Ungrouping 0 of 1 hierarchies before Pass 1 (OPT-775)

Beginning Pass 1 Mapping

------------------------

Processing 'primary\_lsfr6'

Updating timing information

Information: Updating design information... (UID-85)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Mapping Optimizations (Ultra High effort)

-------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:03 7278.0 0.00 0.0 0.0 0.00

0:00:03 7278.0 0.00 0.0 0.0 0.00

0:00:03 7278.0 0.00 0.0 0.0 0.00

0:00:03 7278.0 0.00 0.0 0.0 0.00

Re-synthesis Optimization (Phase 1)

Re-synthesis Optimization (Phase 2)

Global Optimization (Phase 1)

Global Optimization (Phase 2)

Global Optimization (Phase 3)

Global Optimization (Phase 4)

Global Optimization (Phase 5)

Global Optimization (Phase 6)

Global Optimization (Phase 7)

Global Optimization (Phase 8)

Global Optimization (Phase 9)

Global Optimization (Phase 10)

Global Optimization (Phase 11)

Global Optimization (Phase 12)

Global Optimization (Phase 13)

Global Optimization (Phase 14)

Global Optimization (Phase 15)

Global Optimization (Phase 16)

Global Optimization (Phase 17)

Global Optimization (Phase 18)

Global Optimization (Phase 19)

Global Optimization (Phase 20)

Global Optimization (Phase 21)

Global Optimization (Phase 22)

Global Optimization (Phase 23)

Global Optimization (Phase 24)

Global Optimization (Phase 25)

Global Optimization (Phase 26)

Global Optimization (Phase 27)

Global Optimization (Phase 28)

Global Optimization (Phase 29)

Global Optimization (Phase 30)

Global Optimization (Phase 31)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Delay Optimization Phase

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TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:04 5424.5 0.00 0.0 64.5 0.00

0:00:04 5424.5 0.00 0.0 64.5 0.00

0:00:04 5424.5 0.00 0.0 64.5 0.00

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Beginning Delay Optimization

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0:00:04 5424.5 0.00 0.0 64.5 0.00

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0:00:04 5424.5 0.00 0.0 64.5 0.00

Beginning Design Rule Fixing (min\_path) (max\_capacitance)

----------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:04 5424.5 0.00 0.0 64.5 -3.44

Global Optimization (Phase 32)

Global Optimization (Phase 33)

Global Optimization (Phase 34)

0:00:05 5507.5 0.00 0.0 0.0 0.00

0:00:05 5395.5 0.00 0.0 0.0 -1.08

0:00:05 5395.5 0.00 0.0 0.0 -1.08

Loaded alib file './alib-52/tc240c.db\_NOMIN25.alib'

0:00:06 5395.5 0.00 0.0 0.0 -1.08

0:00:06 5395.5 0.00 0.0 0.0 -1.08

0:00:06 5411.5 0.00 0.0 0.0 0.00

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:06 5411.5 0.00 0.0 0.0 0.00

0:00:07 4942.0 0.00 0.0 8545.0 0.00

0:00:07 5930.0 0.00 0.0 0.0 0.00

Beginning Area-Recovery Phase (max\_area 0)

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TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:07 5930.0 0.00 0.0 0.0 0.00

Global Optimization (Phase 35)

Global Optimization (Phase 36)

Global Optimization (Phase 37)

Global Optimization (Phase 38)

Global Optimization (Phase 39)

Global Optimization (Phase 40)

Global Optimization (Phase 41)

Global Optimization (Phase 42)

Global Optimization (Phase 43)

Global Optimization (Phase 44)

Global Optimization (Phase 45)

Global Optimization (Phase 46)

Global Optimization (Phase 47)

Global Optimization (Phase 48)

Global Optimization (Phase 49)

Global Optimization (Phase 50)

Global Optimization (Phase 51)

0:00:08 4930.5 0.00 0.0 0.0 0.00

0:00:08 4930.5 0.00 0.0 0.0 0.00

0:00:08 4930.5 0.00 0.0 0.0 0.00

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Loading db file '/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_NOMIN25'

Optimization Complete

---------------------

1

create\_clock clk -name clk -period 4.0

1

update\_timing

Information: Updating design information... (UID-85)

1

report\_timing -max\_paths 3

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 3

Design : primary\_lsfr6

Version: I-2013.12-SP5

Date : Tue Dec 1 21:28:36 2015

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: NOMIN25 Library: tc240c

Wire Load Model Mode: top

Startpoint: write (input port clocked by clk)

Endpoint: lfsr6\_reg[521]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr6 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 f

write (in) 0.15 0.75 f

U1637/Z (CNIVX8) 0.47 1.22 f

U1651/Z (CNR2IX2) 0.14 1.36 r

U1653/Z1 (CIVDX2) 0.19 1.56 r

U1603/Z (CNIVX2) 0.41 1.96 r

U1680/Z (CND2X1) 0.37 2.33 f

U1768/Z (COND3XL) 0.19 2.51 r

lfsr6\_reg[521]/D (CFD2XL) 0.00 2.51 r

data arrival time 2.51

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr6\_reg[521]/CP (CFD2XL) 0.00 3.75 r

library setup time -0.24 3.51

data required time 3.51

-----------------------------------------------------------

data required time 3.51

data arrival time -2.51

-----------------------------------------------------------

slack (MET) 1.00

Startpoint: write (input port clocked by clk)

Endpoint: lfsr6\_reg[401]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr6 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 f

write (in) 0.15 0.75 f

U1637/Z (CNIVX8) 0.47 1.22 f

U1651/Z (CNR2IX2) 0.14 1.36 r

U1653/Z1 (CIVDX2) 0.19 1.56 r

U1603/Z (CNIVX2) 0.41 1.96 r

U1673/Z (CND2X1) 0.37 2.33 f

U1677/Z (COND3XL) 0.19 2.51 r

lfsr6\_reg[401]/D (CFD2XL) 0.00 2.51 r

data arrival time 2.51

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr6\_reg[401]/CP (CFD2XL) 0.00 3.75 r

library setup time -0.24 3.51

data required time 3.51

-----------------------------------------------------------

data required time 3.51

data arrival time -2.51

-----------------------------------------------------------

slack (MET) 1.00

Startpoint: write (input port clocked by clk)

Endpoint: lfsr6\_reg[518]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr6 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 f

write (in) 0.15 0.75 f

U1637/Z (CNIVX8) 0.47 1.22 f

U1651/Z (CNR2IX2) 0.14 1.36 r

U1653/Z1 (CIVDX2) 0.19 1.56 r

U1606/Z (CNIVX2) 0.40 1.95 r

U1687/Z (CND2X1) 0.36 2.32 f

U1691/Z (COND3XL) 0.19 2.50 r

lfsr6\_reg[518]/D (CFD2XL) 0.00 2.50 r

data arrival time 2.50

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr6\_reg[518]/CP (CFD2XL) 0.00 3.75 r

library setup time -0.24 3.51

data required time 3.51

-----------------------------------------------------------

data required time 3.51

data arrival time -2.50

-----------------------------------------------------------

slack (MET) 1.01

1

analyze -format verilog primary\_lsfr5.v

Running PRESTO HDLC

Searching for ./primary\_lsfr5.v

Compiling source file ./primary\_lsfr5.v

Presto compilation completed successfully.

1

elaborate primary\_lsfr5

Running PRESTO HDLC

Inferred memory devices in process

in routine primary\_lsfr5 line 18 in file

'./primary\_lsfr5.v'.

===============================================================================

| Register Name | Type | Width | Bus | MB | AR | AS | SR | SS | ST |

===============================================================================

| lfsr5\_reg | Flip-flop | 301 | Y | N | Y | N | N | N | N |

===============================================================================

Presto compilation completed successfully.

Elaborated 1 design.

Current design is now 'primary\_lsfr5'.

1

create\_clock clk -name clk -period 3.0

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_clock\_uncertainty 0.25 clk

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_output\_delay 0.5 -clock clk [all\_outputs]

1

set all\_inputs\_wo\_rst\_clk [remove\_from\_collection [remove\_from\_collection [all\_inputs] [get\_port clk]] [get\_port rst]]

Warning: Can't find port 'rst' in design 'primary\_lsfr5'. (UID-95)

{reset pushin write InitialData5[300] InitialData5[299] InitialData5[298] InitialData5[297] InitialData5[296] InitialData5[295] InitialData5[294] InitialData5[293] InitialData5[292] InitialData5[291] InitialData5[290] InitialData5[289] InitialData5[288] InitialData5[287] InitialData5[286] InitialData5[285] InitialData5[284] InitialData5[283] InitialData5[282] InitialData5[281] InitialData5[280] InitialData5[279] InitialData5[278] InitialData5[277] InitialData5[276] InitialData5[275] InitialData5[274] InitialData5[273] InitialData5[272] InitialData5[271] InitialData5[270] InitialData5[269] InitialData5[268] InitialData5[267] InitialData5[266] InitialData5[265] InitialData5[264] InitialData5[263] InitialData5[262] InitialData5[261] InitialData5[260] InitialData5[259] InitialData5[258] InitialData5[257] InitialData5[256] InitialData5[255] InitialData5[254] InitialData5[253] InitialData5[252] InitialData5[251] InitialData5[250] InitialData5[249] InitialData5[248] InitialData5[247] InitialData5[246] InitialData5[245] InitialData5[244] InitialData5[243] InitialData5[242] InitialData5[241] InitialData5[240] InitialData5[239] InitialData5[238] InitialData5[237] InitialData5[236] InitialData5[235] InitialData5[234] InitialData5[233] InitialData5[232] InitialData5[231] InitialData5[230] InitialData5[229] InitialData5[228] InitialData5[227] InitialData5[226] InitialData5[225] InitialData5[224] InitialData5[223] InitialData5[222] InitialData5[221] InitialData5[220] InitialData5[219] InitialData5[218] InitialData5[217] InitialData5[216] InitialData5[215] InitialData5[214] InitialData5[213] InitialData5[212] InitialData5[211] InitialData5[210] InitialData5[209] InitialData5[208] InitialData5[207] InitialData5[206] InitialData5[205] InitialData5[204] ...}

set\_driving\_cell -lib\_cell CND2X1 $all\_inputs\_wo\_rst\_clk

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set\_input\_delay 0.6 -clock clk $all\_inputs\_wo\_rst\_clk

1

set\_output\_delay 0.6 -clock clk [all\_outputs]

1

set\_fix\_hold [ get\_clocks clk ]

1

set\_output\_delay 0.3 -clock clk [all\_outputs]

1

set\_wire\_load\_model -name T8G00TW8

1

compile\_ultra

Alib files are up-to-date.

Information: Sequential output inversion is enabled. SVF file must be used for formal verification. (OPT-1208)

Information: Ungrouping 0 of 1 hierarchies before Pass 1 (OPT-775)

Beginning Pass 1 Mapping

------------------------

Processing 'primary\_lsfr5'

Updating timing information

Information: Updating design information... (UID-85)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Mapping Optimizations (Ultra High effort)

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TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

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0:00:02 4105.5 0.00 -0.0 0.0 0.00

0:00:02 4105.5 0.00 -0.0 0.0 0.00

0:00:02 4105.5 0.00 -0.0 0.0 0.00

0:00:02 4105.5 0.00 -0.0 0.0 0.00

Re-synthesis Optimization (Phase 1)

Re-synthesis Optimization (Phase 2)

Global Optimization (Phase 1)

Global Optimization (Phase 2)

Global Optimization (Phase 3)

Global Optimization (Phase 4)

Global Optimization (Phase 5)

Global Optimization (Phase 6)

Global Optimization (Phase 7)

Global Optimization (Phase 8)

Global Optimization (Phase 9)

Global Optimization (Phase 10)

Global Optimization (Phase 11)

Global Optimization (Phase 12)

Global Optimization (Phase 13)

Global Optimization (Phase 14)

Global Optimization (Phase 15)

Global Optimization (Phase 16)

Global Optimization (Phase 17)

Global Optimization (Phase 18)

Global Optimization (Phase 19)

Global Optimization (Phase 20)

Global Optimization (Phase 21)

Global Optimization (Phase 22)

Global Optimization (Phase 23)

Global Optimization (Phase 24)

Global Optimization (Phase 25)

Global Optimization (Phase 26)

Global Optimization (Phase 27)

Global Optimization (Phase 28)

Global Optimization (Phase 29)

Global Optimization (Phase 30)

Global Optimization (Phase 31)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Delay Optimization Phase

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TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

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0:00:02 2997.0 0.00 0.0 2842.7 0.00

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Beginning Delay Optimization

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0:00:02 2997.0 0.00 0.0 2842.7 0.00

Beginning Design Rule Fixing (max\_capacitance)

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TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

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0:00:02 2997.0 0.00 0.0 2842.7 0.00

Global Optimization (Phase 32)

Global Optimization (Phase 33)

Global Optimization (Phase 34)

0:00:02 2999.5 0.00 0.0 0.0 0.00

0:00:03 2995.5 0.00 0.0 0.0 0.00

0:00:03 2995.5 0.00 0.0 0.0 0.00

Loaded alib file './alib-52/tc240c.db\_NOMIN25.alib'

0:00:03 2995.5 0.00 0.0 0.0 0.00

0:00:03 2995.5 0.00 0.0 0.0 0.00

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

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0:00:03 2995.5 0.00 0.0 0.0 0.00

0:00:04 2913.5 0.00 0.0 1559.8 0.00

0:00:04 3472.5 0.00 0.0 0.0 0.00

Beginning Area-Recovery Phase (max\_area 0)

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TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:04 3472.5 0.00 0.0 0.0 0.00

Global Optimization (Phase 35)

Global Optimization (Phase 36)

Global Optimization (Phase 37)

Global Optimization (Phase 38)

Global Optimization (Phase 39)

Global Optimization (Phase 40)

Global Optimization (Phase 41)

Global Optimization (Phase 42)

Global Optimization (Phase 43)

Global Optimization (Phase 44)

Global Optimization (Phase 45)

Global Optimization (Phase 46)

Global Optimization (Phase 47)

Global Optimization (Phase 48)

Global Optimization (Phase 49)

Global Optimization (Phase 50)

0:00:04 2880.5 0.00 0.0 0.0 0.00

0:00:04 2880.5 0.00 0.0 0.0 0.00

0:00:04 2880.5 0.00 0.0 0.0 0.00

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0:00:04 2880.5 0.00 0.0 0.0 0.00

Loading db file '/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_NOMIN25'

Optimization Complete

---------------------

1

create\_clock clk -name clk -period 4.0

1

update\_timing

Information: Updating design information... (UID-85)

1

report\_timing -max\_paths 3

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 3

Design : primary\_lsfr5

Version: I-2013.12-SP5

Date : Tue Dec 1 21:28:42 2015

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: NOMIN25 Library: tc240c

Wire Load Model Mode: top

Startpoint: write (input port clocked by clk)

Endpoint: lfsr5\_reg[55]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr5 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 r

write (in) 0.11 0.71 r

U931/Z (CNIVX12) 0.55 1.26 r

U927/Z (CNR2X2) 0.26 1.52 f

U928/Z (CIVX8) 0.20 1.72 r

U1380/Z (CIVX2) 0.38 2.10 f

U1261/Z (CANR2XL) 0.24 2.34 r

U1262/Z (COND1XL) 0.17 2.51 f

lfsr5\_reg[55]/D (CFD2XL) 0.00 2.51 f

data arrival time 2.51

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr5\_reg[55]/CP (CFD2XL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

-----------------------------------------------------------

data required time 3.53

data arrival time -2.51

-----------------------------------------------------------

slack (MET) 1.02

Startpoint: write (input port clocked by clk)

Endpoint: lfsr5\_reg[52]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr5 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 r

write (in) 0.11 0.71 r

U931/Z (CNIVX12) 0.55 1.26 r

U927/Z (CNR2X2) 0.26 1.52 f

U928/Z (CIVX8) 0.20 1.72 r

U1380/Z (CIVX2) 0.38 2.10 f

U1255/Z (CANR2XL) 0.24 2.34 r

U1256/Z (COND1XL) 0.17 2.51 f

lfsr5\_reg[52]/D (CFD2XL) 0.00 2.51 f

data arrival time 2.51

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr5\_reg[52]/CP (CFD2XL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

-----------------------------------------------------------

data required time 3.53

data arrival time -2.51

-----------------------------------------------------------

slack (MET) 1.02

Startpoint: write (input port clocked by clk)

Endpoint: lfsr5\_reg[68]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr5 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 r

write (in) 0.11 0.71 r

U931/Z (CNIVX12) 0.55 1.26 r

U927/Z (CNR2X2) 0.26 1.52 f

U928/Z (CIVX8) 0.20 1.72 r

U1380/Z (CIVX2) 0.38 2.10 f

U1287/Z (CANR2XL) 0.24 2.34 r

U1288/Z (COND1XL) 0.17 2.51 f

lfsr5\_reg[68]/D (CFD2XL) 0.00 2.51 f

data arrival time 2.51

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr5\_reg[68]/CP (CFD2XL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

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data required time 3.53

data arrival time -2.51

-----------------------------------------------------------

slack (MET) 1.02

1

analyze -format verilog primary\_lsfr4.v

Running PRESTO HDLC

Searching for ./primary\_lsfr4.v

Compiling source file ./primary\_lsfr4.v

Presto compilation completed successfully.

1

elaborate primary\_lsfr4

Running PRESTO HDLC

Inferred memory devices in process

in routine primary\_lsfr4 line 21 in file

'./primary\_lsfr4.v'.

===============================================================================

| Register Name | Type | Width | Bus | MB | AR | AS | SR | SS | ST |

===============================================================================

| lfsr4\_reg | Flip-flop | 86 | Y | N | Y | N | N | N | N |

===============================================================================

Presto compilation completed successfully.

Elaborated 1 design.

Current design is now 'primary\_lsfr4'.

1

create\_clock clk -name clk -period 3.0

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_clock\_uncertainty 0.25 clk

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_output\_delay 0.5 -clock clk [all\_outputs]

1

set all\_inputs\_wo\_rst\_clk [remove\_from\_collection [remove\_from\_collection [all\_inputs] [get\_port clk]] [get\_port rst]]

Warning: Can't find port 'rst' in design 'primary\_lsfr4'. (UID-95)

{reset write pushin InitialData4[85] InitialData4[84] InitialData4[83] InitialData4[82] InitialData4[81] InitialData4[80] InitialData4[79] InitialData4[78] InitialData4[77] InitialData4[76] InitialData4[75] InitialData4[74] InitialData4[73] InitialData4[72] InitialData4[71] InitialData4[70] InitialData4[69] InitialData4[68] InitialData4[67] InitialData4[66] InitialData4[65] InitialData4[64] InitialData4[63] InitialData4[62] InitialData4[61] InitialData4[60] InitialData4[59] InitialData4[58] InitialData4[57] InitialData4[56] InitialData4[55] InitialData4[54] InitialData4[53] InitialData4[52] InitialData4[51] InitialData4[50] InitialData4[49] InitialData4[48] InitialData4[47] InitialData4[46] InitialData4[45] InitialData4[44] InitialData4[43] InitialData4[42] InitialData4[41] InitialData4[40] InitialData4[39] InitialData4[38] InitialData4[37] InitialData4[36] InitialData4[35] InitialData4[34] InitialData4[33] InitialData4[32] InitialData4[31] InitialData4[30] InitialData4[29] InitialData4[28] InitialData4[27] InitialData4[26] InitialData4[25] InitialData4[24] InitialData4[23] InitialData4[22] InitialData4[21] InitialData4[20] InitialData4[19] InitialData4[18] InitialData4[17] InitialData4[16] InitialData4[15] InitialData4[14] InitialData4[13] InitialData4[12] InitialData4[11] InitialData4[10] InitialData4[9] InitialData4[8] InitialData4[7] InitialData4[6] InitialData4[5] InitialData4[4] InitialData4[3] InitialData4[2] InitialData4[1] InitialData4[0]}

set\_driving\_cell -lib\_cell CND2X1 $all\_inputs\_wo\_rst\_clk

Warning: Design rule attributes from the driving cell will be

set on the port. (UID-401)

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1

set\_input\_delay 0.6 -clock clk $all\_inputs\_wo\_rst\_clk

1

set\_output\_delay 0.6 -clock clk [all\_outputs]

1

set\_fix\_hold [ get\_clocks clk ]

1

set\_output\_delay 0.3 -clock clk [all\_outputs]

1

set\_wire\_load\_model -name T8G00TW8

1

compile\_ultra

Alib files are up-to-date.

Information: Sequential output inversion is enabled. SVF file must be used for formal verification. (OPT-1208)

Information: Ungrouping 0 of 1 hierarchies before Pass 1 (OPT-775)

Beginning Pass 1 Mapping

------------------------

Processing 'primary\_lsfr4'

Updating timing information

Information: Updating design information... (UID-85)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Mapping Optimizations (Ultra High effort)

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TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

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0:00:01 1346.5 0.00 -0.0 0.0 0.00

0:00:01 1346.5 0.00 -0.0 0.0 0.00

0:00:01 1346.5 0.00 -0.0 0.0 0.00

0:00:01 1346.5 0.00 -0.0 0.0 0.00

Re-synthesis Optimization (Phase 1)

Re-synthesis Optimization (Phase 2)

Global Optimization (Phase 1)

Global Optimization (Phase 2)

Global Optimization (Phase 3)

Global Optimization (Phase 4)

Global Optimization (Phase 5)

Global Optimization (Phase 6)

Global Optimization (Phase 7)

Global Optimization (Phase 8)

Global Optimization (Phase 9)

Global Optimization (Phase 10)

Global Optimization (Phase 11)

Global Optimization (Phase 12)

Global Optimization (Phase 13)

Global Optimization (Phase 14)

Global Optimization (Phase 15)

Global Optimization (Phase 16)

Global Optimization (Phase 17)

Global Optimization (Phase 18)

Global Optimization (Phase 19)

Global Optimization (Phase 20)

Global Optimization (Phase 21)

Global Optimization (Phase 22)

Global Optimization (Phase 23)

Global Optimization (Phase 24)

Global Optimization (Phase 25)

Global Optimization (Phase 26)

Global Optimization (Phase 27)

Global Optimization (Phase 28)

Global Optimization (Phase 29)

Global Optimization (Phase 30)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Delay Optimization Phase

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TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

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0:00:02 919.5 0.00 0.0 774.9 0.00

0:00:02 919.5 0.00 0.0 774.9 0.00

0:00:02 919.5 0.00 0.0 774.9 0.00

0:00:02 919.5 0.00 0.0 774.9 0.00

0:00:02 919.5 0.00 0.0 774.9 0.00

0:00:02 919.5 0.00 0.0 774.9 0.00

0:00:02 919.5 0.00 0.0 774.9 0.00

0:00:02 919.5 0.00 0.0 774.9 0.00

0:00:02 919.5 0.00 0.0 774.9 0.00

0:00:02 919.5 0.00 0.0 774.9 0.00

0:00:02 919.5 0.00 0.0 774.9 0.00

Beginning Delay Optimization

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0:00:02 919.5 0.00 0.0 774.9 0.00

0:00:02 919.5 0.00 0.0 774.9 0.00

0:00:02 919.5 0.00 0.0 774.9 0.00

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0:00:02 919.5 0.00 0.0 774.9 0.00

0:00:02 919.5 0.00 0.0 774.9 0.00

0:00:02 919.5 0.00 0.0 774.9 0.00

Beginning Design Rule Fixing (max\_capacitance)

----------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:02 919.5 0.00 0.0 774.9 0.00

Global Optimization (Phase 31)

Global Optimization (Phase 32)

Global Optimization (Phase 33)

0:00:02 920.5 0.00 0.0 0.0 0.00

0:00:02 905.0 0.00 0.0 0.0 0.00

0:00:02 905.0 0.00 0.0 0.0 0.00

Loaded alib file './alib-52/tc240c.db\_NOMIN25.alib'

0:00:02 905.0 0.00 0.0 0.0 0.00

0:00:02 905.0 0.00 0.0 0.0 0.00

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:02 905.0 0.00 0.0 0.0 0.00

0:00:03 905.0 0.00 0.0 0.0 0.00

Beginning Area-Recovery Phase (max\_area 0)

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TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

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0:00:03 905.0 0.00 0.0 0.0 0.00

Global Optimization (Phase 34)

Global Optimization (Phase 35)

Global Optimization (Phase 36)

Global Optimization (Phase 37)

Global Optimization (Phase 38)

Global Optimization (Phase 39)

Global Optimization (Phase 40)

Global Optimization (Phase 41)

Global Optimization (Phase 42)

Global Optimization (Phase 43)

Global Optimization (Phase 44)

Global Optimization (Phase 45)

Global Optimization (Phase 46)

Global Optimization (Phase 47)

Global Optimization (Phase 48)

0:00:03 895.5 0.00 0.0 0.0 0.00

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0:00:03 895.5 0.00 0.0 0.0 0.00

Loading db file '/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_NOMIN25'

Optimization Complete

---------------------

1

create\_clock clk -name clk -period 4.0

1

update\_timing

Information: Updating design information... (UID-85)

1

report\_timing -max\_paths 3

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 3

Design : primary\_lsfr4

Version: I-2013.12-SP5

Date : Tue Dec 1 21:28:45 2015

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: NOMIN25 Library: tc240c

Wire Load Model Mode: top

Startpoint: write (input port clocked by clk)

Endpoint: lfsr4\_reg[72]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr4 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 f

write (in) 0.04 0.64 f

U276/Z (CNIVX8) 0.34 0.98 f

U275/Z (CNR2X4) 0.35 1.33 r

U272/Z0 (CIVDX1) 0.28 1.62 f

U274/Z (CIVX2) 0.47 2.09 r

U540/Z (CANR2XL) 0.32 2.40 f

U541/Z (COND1XL) 0.11 2.52 r

lfsr4\_reg[72]/D (CFD2QXL) 0.00 2.52 r

data arrival time 2.52

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr4\_reg[72]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.23 3.52

data required time 3.52

-----------------------------------------------------------

data required time 3.52

data arrival time -2.52

-----------------------------------------------------------

slack (MET) 1.00

Startpoint: write (input port clocked by clk)

Endpoint: lfsr4\_reg[78]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr4 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 f

write (in) 0.04 0.64 f

U276/Z (CNIVX8) 0.34 0.98 f

U275/Z (CNR2X4) 0.35 1.33 r

U272/Z0 (CIVDX1) 0.28 1.62 f

U274/Z (CIVX2) 0.47 2.09 r

U546/Z (CANR2XL) 0.32 2.40 f

U547/Z (COND1XL) 0.11 2.52 r

lfsr4\_reg[78]/D (CFD2QXL) 0.00 2.52 r

data arrival time 2.52

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr4\_reg[78]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.23 3.52

data required time 3.52

-----------------------------------------------------------

data required time 3.52

data arrival time -2.52

-----------------------------------------------------------

slack (MET) 1.00

Startpoint: write (input port clocked by clk)

Endpoint: lfsr4\_reg[84]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr4 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 f

write (in) 0.04 0.64 f

U276/Z (CNIVX8) 0.34 0.98 f

U275/Z (CNR2X4) 0.35 1.33 r

U272/Z0 (CIVDX1) 0.28 1.62 f

U274/Z (CIVX2) 0.47 2.09 r

U555/Z (CANR2XL) 0.32 2.40 f

U556/Z (COND1XL) 0.11 2.52 r

lfsr4\_reg[84]/D (CFD2QXL) 0.00 2.52 r

data arrival time 2.52

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr4\_reg[84]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.23 3.52

data required time 3.52

-----------------------------------------------------------

data required time 3.52

data arrival time -2.52

-----------------------------------------------------------

slack (MET) 1.00

1

analyze -format verilog primary\_lsfr3.v

Running PRESTO HDLC

Searching for ./primary\_lsfr3.v

Compiling source file ./primary\_lsfr3.v

Presto compilation completed successfully.

1

elaborate primary\_lsfr3

Running PRESTO HDLC

Inferred memory devices in process

in routine primary\_lsfr3 line 21 in file

'./primary\_lsfr3.v'.

===============================================================================

| Register Name | Type | Width | Bus | MB | AR | AS | SR | SS | ST |

===============================================================================

| lfsr1\_reg | Flip-flop | 73 | Y | N | Y | N | N | N | N |

===============================================================================

Presto compilation completed successfully.

Elaborated 1 design.

Current design is now 'primary\_lsfr3'.

1

create\_clock clk -name clk -period 3.0

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_clock\_uncertainty 0.25 clk

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_output\_delay 0.5 -clock clk [all\_outputs]

1

set all\_inputs\_wo\_rst\_clk [remove\_from\_collection [remove\_from\_collection [all\_inputs] [get\_port clk]] [get\_port rst]]

Warning: Can't find port 'rst' in design 'primary\_lsfr3'. (UID-95)

{reset write pushin InitialData3[72] InitialData3[71] InitialData3[70] InitialData3[69] InitialData3[68] InitialData3[67] InitialData3[66] InitialData3[65] InitialData3[64] InitialData3[63] InitialData3[62] InitialData3[61] InitialData3[60] InitialData3[59] InitialData3[58] InitialData3[57] InitialData3[56] InitialData3[55] InitialData3[54] InitialData3[53] InitialData3[52] InitialData3[51] InitialData3[50] InitialData3[49] InitialData3[48] InitialData3[47] InitialData3[46] InitialData3[45] InitialData3[44] InitialData3[43] InitialData3[42] InitialData3[41] InitialData3[40] InitialData3[39] InitialData3[38] InitialData3[37] InitialData3[36] InitialData3[35] InitialData3[34] InitialData3[33] InitialData3[32] InitialData3[31] InitialData3[30] InitialData3[29] InitialData3[28] InitialData3[27] InitialData3[26] InitialData3[25] InitialData3[24] InitialData3[23] InitialData3[22] InitialData3[21] InitialData3[20] InitialData3[19] InitialData3[18] InitialData3[17] InitialData3[16] InitialData3[15] InitialData3[14] InitialData3[13] InitialData3[12] InitialData3[11] InitialData3[10] InitialData3[9] InitialData3[8] InitialData3[7] InitialData3[6] InitialData3[5] InitialData3[4] InitialData3[3] InitialData3[2] InitialData3[1] InitialData3[0]}

set\_driving\_cell -lib\_cell CND2X1 $all\_inputs\_wo\_rst\_clk

Warning: Design rule attributes from the driving cell will be

set on the port. (UID-401)

Warning: Design rule attributes from the driving cell will be

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set on the port. (UID-401)

1

set\_input\_delay 0.6 -clock clk $all\_inputs\_wo\_rst\_clk

1

set\_output\_delay 0.6 -clock clk [all\_outputs]

1

set\_fix\_hold [ get\_clocks clk ]

1

set\_output\_delay 0.3 -clock clk [all\_outputs]

1

set\_wire\_load\_model -name T8G00TW8

1

compile\_ultra

Alib files are up-to-date.

Information: Sequential output inversion is enabled. SVF file must be used for formal verification. (OPT-1208)

Information: Ungrouping 0 of 1 hierarchies before Pass 1 (OPT-775)

Beginning Pass 1 Mapping

------------------------

Processing 'primary\_lsfr3'

Updating timing information

Information: Updating design information... (UID-85)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Mapping Optimizations (Ultra High effort)

-------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:02 920.0 0.00 0.0 0.0 0.00

0:00:02 920.0 0.00 0.0 0.0 0.00

0:00:02 920.0 0.00 0.0 0.0 0.00

0:00:02 920.0 0.00 0.0 0.0 0.00

Re-synthesis Optimization (Phase 1)

Re-synthesis Optimization (Phase 2)

Global Optimization (Phase 1)

Global Optimization (Phase 2)

Global Optimization (Phase 3)

Global Optimization (Phase 4)

Global Optimization (Phase 5)

Global Optimization (Phase 6)

Global Optimization (Phase 7)

Global Optimization (Phase 8)

Global Optimization (Phase 9)

Global Optimization (Phase 10)

Global Optimization (Phase 11)

Global Optimization (Phase 12)

Global Optimization (Phase 13)

Global Optimization (Phase 14)

Global Optimization (Phase 15)

Global Optimization (Phase 16)

Global Optimization (Phase 17)

Global Optimization (Phase 18)

Global Optimization (Phase 19)

Global Optimization (Phase 20)

Global Optimization (Phase 21)

Global Optimization (Phase 22)

Global Optimization (Phase 23)

Global Optimization (Phase 24)

Global Optimization (Phase 25)

Global Optimization (Phase 26)

Global Optimization (Phase 27)

Global Optimization (Phase 28)

Global Optimization (Phase 29)

Global Optimization (Phase 30)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Delay Optimization Phase

----------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:02 740.5 0.00 0.0 574.9 0.00

0:00:02 740.5 0.00 0.0 574.9 0.00

0:00:02 740.5 0.00 0.0 574.9 0.00

0:00:02 740.5 0.00 0.0 574.9 0.00

0:00:02 740.5 0.00 0.0 574.9 0.00

0:00:02 740.5 0.00 0.0 574.9 0.00

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0:00:02 740.5 0.00 0.0 574.9 0.00

0:00:02 740.5 0.00 0.0 574.9 0.00

0:00:02 740.5 0.00 0.0 574.9 0.00

Beginning Delay Optimization

----------------------------

0:00:02 740.5 0.00 0.0 574.9 0.00

0:00:02 740.5 0.00 0.0 574.9 0.00

0:00:02 740.5 0.00 0.0 574.9 0.00

0:00:02 740.5 0.00 0.0 574.9 0.00

0:00:02 740.5 0.00 0.0 574.9 0.00

0:00:02 740.5 0.00 0.0 574.9 0.00

0:00:02 740.5 0.00 0.0 574.9 0.00

0:00:02 740.5 0.00 0.0 574.9 0.00

Beginning Design Rule Fixing (max\_capacitance)

----------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:02 740.5 0.00 0.0 574.9 0.00

Global Optimization (Phase 31)

Global Optimization (Phase 32)

Global Optimization (Phase 33)

0:00:02 742.0 0.00 0.0 0.0 0.00

0:00:02 751.5 0.00 0.0 0.0 0.00

0:00:02 751.5 0.00 0.0 0.0 0.00

Loaded alib file './alib-52/tc240c.db\_NOMIN25.alib'

0:00:03 751.5 0.00 0.0 0.0 0.00

0:00:03 751.5 0.00 0.0 0.0 0.00

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:03 751.5 0.00 0.0 0.0 0.00

0:00:03 751.0 0.00 0.0 0.0 0.00

Beginning Area-Recovery Phase (max\_area 0)

-----------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:03 751.0 0.00 0.0 0.0 0.00

Global Optimization (Phase 34)

Global Optimization (Phase 35)

Global Optimization (Phase 36)

Global Optimization (Phase 37)

Global Optimization (Phase 38)

Global Optimization (Phase 39)

Global Optimization (Phase 40)

Global Optimization (Phase 41)

Global Optimization (Phase 42)

Global Optimization (Phase 43)

Global Optimization (Phase 44)

Global Optimization (Phase 45)

Global Optimization (Phase 46)

Global Optimization (Phase 47)

Global Optimization (Phase 48)

Global Optimization (Phase 49)

Global Optimization (Phase 50)

Global Optimization (Phase 51)

0:00:03 734.5 0.00 0.0 0.0 0.00

0:00:03 734.5 0.00 0.0 0.0 0.00

0:00:03 734.5 0.00 0.0 0.0 0.00

0:00:03 734.5 0.00 0.0 0.0 0.00

0:00:03 734.5 0.00 0.0 0.0 0.00

0:00:03 734.5 0.00 0.0 0.0 0.00

0:00:03 734.5 0.00 0.0 0.0 0.00

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0:00:03 734.5 0.00 0.0 0.0 0.00

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0:00:03 734.5 0.00 0.0 0.0 0.00

0:00:03 734.5 0.00 0.0 0.0 0.00

0:00:03 734.5 0.00 0.0 0.0 0.00

0:00:03 734.5 0.00 0.0 0.0 0.00

Loading db file '/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_NOMIN25'

Optimization Complete

---------------------

1

create\_clock clk -name clk -period 4.0

1

update\_timing

Information: Updating design information... (UID-85)

1

report\_timing -max\_paths 3

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 3

Design : primary\_lsfr3

Version: I-2013.12-SP5

Date : Tue Dec 1 21:28:49 2015

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: NOMIN25 Library: tc240c

Wire Load Model Mode: top

Startpoint: write (input port clocked by clk)

Endpoint: lfsr1\_reg[12]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr3 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 r

write (in) 0.07 0.67 r

U232/Z (CNIVX2) 0.99 1.66 r

U253/Z (CANR2X1) 0.36 2.02 f

U254/Z (COND1XL) 0.11 2.13 r

lfsr1\_reg[12]/D (CFD2QXL) 0.00 2.13 r

data arrival time 2.13

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr1\_reg[12]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.23 3.52

data required time 3.52

-----------------------------------------------------------

data required time 3.52

data arrival time -2.13

-----------------------------------------------------------

slack (MET) 1.39

Startpoint: write (input port clocked by clk)

Endpoint: lfsr1\_reg[13]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr3 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 r

write (in) 0.07 0.67 r

U232/Z (CNIVX2) 0.99 1.66 r

U250/Z (CANR2X1) 0.36 2.02 f

U251/Z (COND1XL) 0.11 2.13 r

lfsr1\_reg[13]/D (CFD2QXL) 0.00 2.13 r

data arrival time 2.13

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr1\_reg[13]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.23 3.52

data required time 3.52

-----------------------------------------------------------

data required time 3.52

data arrival time -2.13

-----------------------------------------------------------

slack (MET) 1.39

Startpoint: write (input port clocked by clk)

Endpoint: lfsr1\_reg[11]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr3 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 r

write (in) 0.07 0.67 r

U232/Z (CNIVX2) 0.99 1.66 r

U238/Z (CANR2X1) 0.36 2.02 f

U239/Z (COND1XL) 0.11 2.13 r

lfsr1\_reg[11]/D (CFD2QXL) 0.00 2.13 r

data arrival time 2.13

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr1\_reg[11]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.23 3.52

data required time 3.52

-----------------------------------------------------------

data required time 3.52

data arrival time -2.13

-----------------------------------------------------------

slack (MET) 1.39

1

analyze -format verilog primary\_lsfr2.v

Running PRESTO HDLC

Searching for ./primary\_lsfr2.v

Compiling source file ./primary\_lsfr2.v

Presto compilation completed successfully.

1

elaborate primary\_lsfr2

Running PRESTO HDLC

Inferred memory devices in process

in routine primary\_lsfr2 line 16 in file

'./primary\_lsfr2.v'.

===============================================================================

| Register Name | Type | Width | Bus | MB | AR | AS | SR | SS | ST |

===============================================================================

| lfsr2\_reg | Flip-flop | 43 | Y | N | Y | N | N | N | N |

===============================================================================

Presto compilation completed successfully.

Elaborated 1 design.

Current design is now 'primary\_lsfr2'.

1

create\_clock clk -name clk -period 3.0

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_clock\_uncertainty 0.25 clk

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_output\_delay 0.5 -clock clk [all\_outputs]

1

set all\_inputs\_wo\_rst\_clk [remove\_from\_collection [remove\_from\_collection [all\_inputs] [get\_port clk]] [get\_port rst]]

Warning: Can't find port 'rst' in design 'primary\_lsfr2'. (UID-95)

{reset write pushin InitialData2[42] InitialData2[41] InitialData2[40] InitialData2[39] InitialData2[38] InitialData2[37] InitialData2[36] InitialData2[35] InitialData2[34] InitialData2[33] InitialData2[32] InitialData2[31] InitialData2[30] InitialData2[29] InitialData2[28] InitialData2[27] InitialData2[26] InitialData2[25] InitialData2[24] InitialData2[23] InitialData2[22] InitialData2[21] InitialData2[20] InitialData2[19] InitialData2[18] InitialData2[17] InitialData2[16] InitialData2[15] InitialData2[14] InitialData2[13] InitialData2[12] InitialData2[11] InitialData2[10] InitialData2[9] InitialData2[8] InitialData2[7] InitialData2[6] InitialData2[5] InitialData2[4] InitialData2[3] InitialData2[2] InitialData2[1] InitialData2[0]}

set\_driving\_cell -lib\_cell CND2X1 $all\_inputs\_wo\_rst\_clk

Warning: Design rule attributes from the driving cell will be

set on the port. (UID-401)

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set\_input\_delay 0.6 -clock clk $all\_inputs\_wo\_rst\_clk

1

set\_output\_delay 0.6 -clock clk [all\_outputs]

1

set\_fix\_hold [ get\_clocks clk ]

1

set\_output\_delay 0.3 -clock clk [all\_outputs]

1

set\_wire\_load\_model -name T8G00TW8

1

compile\_ultra

Alib files are up-to-date.

Information: Sequential output inversion is enabled. SVF file must be used for formal verification. (OPT-1208)

Information: Ungrouping 0 of 1 hierarchies before Pass 1 (OPT-775)

Beginning Pass 1 Mapping

------------------------

Processing 'primary\_lsfr2'

Updating timing information

Information: Updating design information... (UID-85)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Mapping Optimizations (Ultra High effort)

-------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:01 688.0 0.00 0.0 0.0 0.00

0:00:01 688.0 0.00 0.0 0.0 0.00

0:00:01 688.0 0.00 0.0 0.0 0.00

0:00:01 688.0 0.00 0.0 0.0 0.00

Re-synthesis Optimization (Phase 1)

Re-synthesis Optimization (Phase 2)

Global Optimization (Phase 1)

Global Optimization (Phase 2)

Global Optimization (Phase 3)

Global Optimization (Phase 4)

Global Optimization (Phase 5)

Global Optimization (Phase 6)

Global Optimization (Phase 7)

Global Optimization (Phase 8)

Global Optimization (Phase 9)

Global Optimization (Phase 10)

Global Optimization (Phase 11)

Global Optimization (Phase 12)

Global Optimization (Phase 13)

Global Optimization (Phase 14)

Global Optimization (Phase 15)

Global Optimization (Phase 16)

Global Optimization (Phase 17)

Global Optimization (Phase 18)

Global Optimization (Phase 19)

Global Optimization (Phase 20)

Global Optimization (Phase 21)

Global Optimization (Phase 22)

Global Optimization (Phase 23)

Global Optimization (Phase 24)

Global Optimization (Phase 25)

Global Optimization (Phase 26)

Global Optimization (Phase 27)

Global Optimization (Phase 28)

Global Optimization (Phase 29)

Global Optimization (Phase 30)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Delay Optimization Phase

----------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:01 517.0 0.00 0.0 0.0 0.00

0:00:01 517.0 0.00 0.0 0.0 0.00

0:00:01 517.0 0.00 0.0 0.0 0.00

0:00:01 517.0 0.00 0.0 0.0 0.00

0:00:01 517.0 0.00 0.0 0.0 0.00

0:00:01 517.0 0.00 0.0 0.0 0.00

0:00:01 517.0 0.00 0.0 0.0 0.00

0:00:01 517.0 0.00 0.0 0.0 0.00

0:00:01 517.0 0.00 0.0 0.0 0.00

0:00:01 517.0 0.00 0.0 0.0 0.00

0:00:01 517.0 0.00 0.0 0.0 0.00

Beginning Delay Optimization

----------------------------

0:00:01 517.0 0.00 0.0 0.0 0.00

0:00:01 517.0 0.00 0.0 0.0 0.00

0:00:01 517.0 0.00 0.0 0.0 0.00

0:00:01 517.0 0.00 0.0 0.0 0.00

0:00:01 517.0 0.00 0.0 0.0 0.00

0:00:01 517.0 0.00 0.0 0.0 0.00

0:00:01 517.0 0.00 0.0 0.0 0.00

0:00:01 517.0 0.00 0.0 0.0 0.00

0:00:01 517.0 0.00 0.0 0.0 0.00

0:00:01 516.0 0.00 0.0 0.0 0.00

0:00:01 516.0 0.00 0.0 0.0 0.00

Loaded alib file './alib-52/tc240c.db\_NOMIN25.alib'

0:00:02 516.0 0.00 0.0 0.0 0.00

0:00:02 516.0 0.00 0.0 0.0 0.00

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:02 516.0 0.00 0.0 0.0 0.00

0:00:02 515.5 0.00 0.0 0.0 0.00

Beginning Area-Recovery Phase (max\_area 0)

-----------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:02 515.5 0.00 0.0 0.0 0.00

Global Optimization (Phase 31)

Global Optimization (Phase 32)

Global Optimization (Phase 33)

Global Optimization (Phase 34)

Global Optimization (Phase 35)

Global Optimization (Phase 36)

Global Optimization (Phase 37)

Global Optimization (Phase 38)

Global Optimization (Phase 39)

Global Optimization (Phase 40)

Global Optimization (Phase 41)

Global Optimization (Phase 42)

Global Optimization (Phase 43)

Global Optimization (Phase 44)

0:00:02 512.5 0.00 0.0 0.0 0.00

0:00:02 512.5 0.00 0.0 0.0 0.00

0:00:02 512.5 0.00 0.0 0.0 0.00

0:00:02 512.5 0.00 0.0 0.0 0.00

0:00:02 512.5 0.00 0.0 0.0 0.00

0:00:02 512.5 0.00 0.0 0.0 0.00

0:00:02 512.5 0.00 0.0 0.0 0.00

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0:00:02 512.5 0.00 0.0 0.0 0.00

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0:00:02 512.5 0.00 0.0 0.0 0.00

0:00:02 512.5 0.00 0.0 0.0 0.00

0:00:02 512.5 0.00 0.0 0.0 0.00

0:00:02 512.5 0.00 0.0 0.0 0.00

Loading db file '/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_NOMIN25'

Optimization Complete

---------------------

1

create\_clock clk -name clk -period 4.0

1

update\_timing

Information: Updating design information... (UID-85)

1

report\_timing -max\_paths 3

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 3

Design : primary\_lsfr2

Version: I-2013.12-SP5

Date : Tue Dec 1 21:28:52 2015

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: NOMIN25 Library: tc240c

Wire Load Model Mode: top

Startpoint: write (input port clocked by clk)

Endpoint: lfsr2\_reg[42]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr2 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 f

write (in) 0.06 0.66 f

U173/Z (CNIVX2) 0.59 1.25 f

U174/Z (CNR2X1) 0.17 1.42 r

U170/Z (CNIVX2) 0.64 2.06 r

U335/Z (CANR2XL) 0.34 2.40 f

U336/Z (COND1XL) 0.11 2.51 r

lfsr2\_reg[42]/D (CFD2QXL) 0.00 2.51 r

data arrival time 2.51

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr2\_reg[42]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.23 3.52

data required time 3.52

-----------------------------------------------------------

data required time 3.52

data arrival time -2.51

-----------------------------------------------------------

slack (MET) 1.01

Startpoint: write (input port clocked by clk)

Endpoint: lfsr2\_reg[11]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr2 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 f

write (in) 0.06 0.66 f

U173/Z (CNIVX2) 0.59 1.25 f

U174/Z (CNR2X1) 0.17 1.42 r

U170/Z (CNIVX2) 0.64 2.06 r

U276/Z (CANR2X1) 0.28 2.35 f

U277/Z (COND1XL) 0.11 2.45 r

lfsr2\_reg[11]/D (CFD2QXL) 0.00 2.45 r

data arrival time 2.45

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr2\_reg[11]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.23 3.52

data required time 3.52

-----------------------------------------------------------

data required time 3.52

data arrival time -2.45

-----------------------------------------------------------

slack (MET) 1.07

Startpoint: write (input port clocked by clk)

Endpoint: lfsr2\_reg[40]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr2 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 f

write (in) 0.06 0.66 f

U173/Z (CNIVX2) 0.59 1.25 f

U174/Z (CNR2X1) 0.17 1.42 r

U170/Z (CNIVX2) 0.64 2.06 r

U328/Z (CANR2X1) 0.28 2.35 f

U329/Z (COND1XL) 0.11 2.45 r

lfsr2\_reg[40]/D (CFD2QXL) 0.00 2.45 r

data arrival time 2.45

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr2\_reg[40]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.23 3.52

data required time 3.52

-----------------------------------------------------------

data required time 3.52

data arrival time -2.45

-----------------------------------------------------------

slack (MET) 1.07

1

analyze -format verilog primary\_lsfr1.v

Running PRESTO HDLC

Searching for ./primary\_lsfr1.v

Compiling source file ./primary\_lsfr1.v

Presto compilation completed successfully.

1

elaborate primary\_lsfr1

Running PRESTO HDLC

Inferred memory devices in process

in routine primary\_lsfr1 line 18 in file

'./primary\_lsfr1.v'.

===============================================================================

| Register Name | Type | Width | Bus | MB | AR | AS | SR | SS | ST |

===============================================================================

| lfsr1\_reg | Flip-flop | 185 | Y | N | Y | N | N | N | N |

===============================================================================

Presto compilation completed successfully.

Elaborated 1 design.

Current design is now 'primary\_lsfr1'.

1

create\_clock clk -name clk -period 3.0

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_clock\_uncertainty 0.25 clk

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_output\_delay 0.5 -clock clk [all\_outputs]

1

set all\_inputs\_wo\_rst\_clk [remove\_from\_collection [remove\_from\_collection [all\_inputs] [get\_port clk]] [get\_port rst]]

Warning: Can't find port 'rst' in design 'primary\_lsfr1'. (UID-95)

{reset write pushin InitialData1[184] InitialData1[183] InitialData1[182] InitialData1[181] InitialData1[180] InitialData1[179] InitialData1[178] InitialData1[177] InitialData1[176] InitialData1[175] InitialData1[174] InitialData1[173] InitialData1[172] InitialData1[171] InitialData1[170] InitialData1[169] InitialData1[168] InitialData1[167] InitialData1[166] InitialData1[165] InitialData1[164] InitialData1[163] InitialData1[162] InitialData1[161] InitialData1[160] InitialData1[159] InitialData1[158] InitialData1[157] InitialData1[156] InitialData1[155] InitialData1[154] InitialData1[153] InitialData1[152] InitialData1[151] InitialData1[150] InitialData1[149] InitialData1[148] InitialData1[147] InitialData1[146] InitialData1[145] InitialData1[144] InitialData1[143] InitialData1[142] InitialData1[141] InitialData1[140] InitialData1[139] InitialData1[138] InitialData1[137] InitialData1[136] InitialData1[135] InitialData1[134] InitialData1[133] InitialData1[132] InitialData1[131] InitialData1[130] InitialData1[129] InitialData1[128] InitialData1[127] InitialData1[126] InitialData1[125] InitialData1[124] InitialData1[123] InitialData1[122] InitialData1[121] InitialData1[120] InitialData1[119] InitialData1[118] InitialData1[117] InitialData1[116] InitialData1[115] InitialData1[114] InitialData1[113] InitialData1[112] InitialData1[111] InitialData1[110] InitialData1[109] InitialData1[108] InitialData1[107] InitialData1[106] InitialData1[105] InitialData1[104] InitialData1[103] InitialData1[102] InitialData1[101] InitialData1[100] InitialData1[99] InitialData1[98] InitialData1[97] InitialData1[96] InitialData1[95] InitialData1[94] InitialData1[93] InitialData1[92] InitialData1[91] InitialData1[90] InitialData1[89] InitialData1[88] ...}

set\_driving\_cell -lib\_cell CND2X1 $all\_inputs\_wo\_rst\_clk

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1

set\_input\_delay 0.6 -clock clk $all\_inputs\_wo\_rst\_clk

1

set\_output\_delay 0.6 -clock clk [all\_outputs]

1

set\_fix\_hold [ get\_clocks clk ]

1

set\_output\_delay 0.3 -clock clk [all\_outputs]

1

set\_wire\_load\_model -name T8G00TW8

1

compile\_ultra

Alib files are up-to-date.

Information: Sequential output inversion is enabled. SVF file must be used for formal verification. (OPT-1208)

Information: Ungrouping 0 of 1 hierarchies before Pass 1 (OPT-775)

Beginning Pass 1 Mapping

------------------------

Processing 'primary\_lsfr1'

Updating timing information

Information: Updating design information... (UID-85)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Mapping Optimizations (Ultra High effort)

-------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:02 2592.0 0.00 0.0 0.0 0.00

0:00:02 2592.0 0.00 0.0 0.0 0.00

0:00:02 2592.0 0.00 0.0 0.0 0.00

0:00:02 2592.0 0.00 0.0 0.0 0.00

Re-synthesis Optimization (Phase 1)

Re-synthesis Optimization (Phase 2)

Global Optimization (Phase 1)

Global Optimization (Phase 2)

Global Optimization (Phase 3)

Global Optimization (Phase 4)

Global Optimization (Phase 5)

Global Optimization (Phase 6)

Global Optimization (Phase 7)

Global Optimization (Phase 8)

Global Optimization (Phase 9)

Global Optimization (Phase 10)

Global Optimization (Phase 11)

Global Optimization (Phase 12)

Global Optimization (Phase 13)

Global Optimization (Phase 14)

Global Optimization (Phase 15)

Global Optimization (Phase 16)

Global Optimization (Phase 17)

Global Optimization (Phase 18)

Global Optimization (Phase 19)

Global Optimization (Phase 20)

Global Optimization (Phase 21)

Global Optimization (Phase 22)

Global Optimization (Phase 23)

Global Optimization (Phase 24)

Global Optimization (Phase 25)

Global Optimization (Phase 26)

Global Optimization (Phase 27)

Global Optimization (Phase 28)

Global Optimization (Phase 29)

Global Optimization (Phase 30)

Global Optimization (Phase 31)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Delay Optimization Phase

----------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:02 1888.0 0.00 0.0 0.0 0.00

0:00:02 1888.0 0.00 0.0 0.0 0.00

0:00:02 1888.0 0.00 0.0 0.0 0.00

0:00:02 1888.0 0.00 0.0 0.0 0.00

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Beginning Delay Optimization

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0:00:02 1888.0 0.00 0.0 0.0 0.00

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0:00:02 1888.0 0.00 0.0 0.0 0.00

0:00:02 1865.0 0.00 0.0 0.0 0.00

0:00:02 1865.0 0.00 0.0 0.0 0.00

Loaded alib file './alib-52/tc240c.db\_NOMIN25.alib'

0:00:03 1865.0 0.00 0.0 0.0 0.00

0:00:03 1865.0 0.00 0.0 0.0 0.00

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:03 1865.0 0.00 0.0 0.0 0.00

0:00:03 1850.5 0.00 0.0 0.0 0.00

Beginning Area-Recovery Phase (max\_area 0)

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TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:03 1850.5 0.00 0.0 0.0 0.00

Global Optimization (Phase 32)

Global Optimization (Phase 33)

Global Optimization (Phase 34)

Global Optimization (Phase 35)

Global Optimization (Phase 36)

Global Optimization (Phase 37)

Global Optimization (Phase 38)

Global Optimization (Phase 39)

Global Optimization (Phase 40)

Global Optimization (Phase 41)

Global Optimization (Phase 42)

Global Optimization (Phase 43)

Global Optimization (Phase 44)

Global Optimization (Phase 45)

Global Optimization (Phase 46)

Global Optimization (Phase 47)

0:00:03 1827.0 0.00 0.0 0.0 0.00

0:00:03 1827.0 0.00 0.0 0.0 0.00

0:00:03 1827.0 0.00 0.0 0.0 0.00

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Loading db file '/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_NOMIN25'

Optimization Complete

---------------------

1

create\_clock clk -name clk -period 4.0

1

update\_timing

Information: Updating design information... (UID-85)

1

report\_timing -max\_paths 3

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 3

Design : primary\_lsfr1

Version: I-2013.12-SP5

Date : Tue Dec 1 21:28:56 2015

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: NOMIN25 Library: tc240c

Wire Load Model Mode: top

Startpoint: write (input port clocked by clk)

Endpoint: lfsr1\_reg[14]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr1 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 f

write (in) 0.05 0.65 f

U577/Z (CNIVX12) 0.47 1.12 f

U581/Z (CNR2IX1) 0.20 1.32 r

U580/Z1 (CIVDX2) 0.71 2.03 r

U732/Z (COND1XL) 0.29 2.32 f

U734/Z (COND4CXL) 0.17 2.48 r

lfsr1\_reg[14]/D (CFD2QXL) 0.00 2.48 r

data arrival time 2.48

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr1\_reg[14]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.24 3.51

data required time 3.51

-----------------------------------------------------------

data required time 3.51

data arrival time -2.48

-----------------------------------------------------------

slack (MET) 1.03

Startpoint: write (input port clocked by clk)

Endpoint: lfsr1\_reg[15]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr1 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 f

write (in) 0.05 0.65 f

U577/Z (CNIVX12) 0.47 1.12 f

U581/Z (CNR2IX1) 0.20 1.32 r

U580/Z1 (CIVDX2) 0.71 2.03 r

U705/Z (COND1XL) 0.29 2.32 f

U707/Z (COND4CXL) 0.17 2.48 r

lfsr1\_reg[15]/D (CFD2QXL) 0.00 2.48 r

data arrival time 2.48

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr1\_reg[15]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.24 3.51

data required time 3.51

-----------------------------------------------------------

data required time 3.51

data arrival time -2.48

-----------------------------------------------------------

slack (MET) 1.03

Startpoint: write (input port clocked by clk)

Endpoint: lfsr1\_reg[16]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr1 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 f

write (in) 0.05 0.65 f

U577/Z (CNIVX12) 0.47 1.12 f

U581/Z (CNR2IX1) 0.20 1.32 r

U580/Z1 (CIVDX2) 0.71 2.03 r

U714/Z (COND1XL) 0.29 2.32 f

U716/Z (COND4CXL) 0.17 2.48 r

lfsr1\_reg[16]/D (CFD2QXL) 0.00 2.48 r

data arrival time 2.48

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr1\_reg[16]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.24 3.51

data required time 3.51

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data required time 3.51

data arrival time -2.48

-----------------------------------------------------------

slack (MET) 1.03

1

analyze -format verilog primary\_lsfr0.v

Running PRESTO HDLC

Searching for ./primary\_lsfr0.v

Compiling source file ./primary\_lsfr0.v

Presto compilation completed successfully.

1

elaborate primary\_lsfr0

Running PRESTO HDLC

Inferred memory devices in process

in routine primary\_lsfr0 line 16 in file

'./primary\_lsfr0.v'.

===============================================================================

| Register Name | Type | Width | Bus | MB | AR | AS | SR | SS | ST |

===============================================================================

| lfsr0\_reg | Flip-flop | 450 | Y | N | Y | N | N | N | N |

===============================================================================

Presto compilation completed successfully.

Elaborated 1 design.

Current design is now 'primary\_lsfr0'.

1

create\_clock clk -name clk -period 3.0

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_clock\_uncertainty 0.25 clk

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_output\_delay 0.5 -clock clk [all\_outputs]

1

set all\_inputs\_wo\_rst\_clk [remove\_from\_collection [remove\_from\_collection [all\_inputs] [get\_port clk]] [get\_port rst]]

Warning: Can't find port 'rst' in design 'primary\_lsfr0'. (UID-95)

{reset write pushin InitialData0[449] InitialData0[448] InitialData0[447] InitialData0[446] InitialData0[445] InitialData0[444] InitialData0[443] InitialData0[442] InitialData0[441] InitialData0[440] InitialData0[439] InitialData0[438] InitialData0[437] InitialData0[436] InitialData0[435] InitialData0[434] InitialData0[433] InitialData0[432] InitialData0[431] InitialData0[430] InitialData0[429] InitialData0[428] InitialData0[427] InitialData0[426] InitialData0[425] InitialData0[424] InitialData0[423] InitialData0[422] InitialData0[421] InitialData0[420] InitialData0[419] InitialData0[418] InitialData0[417] InitialData0[416] InitialData0[415] InitialData0[414] InitialData0[413] InitialData0[412] InitialData0[411] InitialData0[410] InitialData0[409] InitialData0[408] InitialData0[407] InitialData0[406] InitialData0[405] InitialData0[404] InitialData0[403] InitialData0[402] InitialData0[401] InitialData0[400] InitialData0[399] InitialData0[398] InitialData0[397] InitialData0[396] InitialData0[395] InitialData0[394] InitialData0[393] InitialData0[392] InitialData0[391] InitialData0[390] InitialData0[389] InitialData0[388] InitialData0[387] InitialData0[386] InitialData0[385] InitialData0[384] InitialData0[383] InitialData0[382] InitialData0[381] InitialData0[380] InitialData0[379] InitialData0[378] InitialData0[377] InitialData0[376] InitialData0[375] InitialData0[374] InitialData0[373] InitialData0[372] InitialData0[371] InitialData0[370] InitialData0[369] InitialData0[368] InitialData0[367] InitialData0[366] InitialData0[365] InitialData0[364] InitialData0[363] InitialData0[362] InitialData0[361] InitialData0[360] InitialData0[359] InitialData0[358] InitialData0[357] InitialData0[356] InitialData0[355] InitialData0[354] InitialData0[353] ...}

set\_driving\_cell -lib\_cell CND2X1 $all\_inputs\_wo\_rst\_clk

Warning: Design rule attributes from the driving cell will be

set on the port. (UID-401)

Warning: Design rule attributes from the driving cell will be

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1

set\_input\_delay 0.6 -clock clk $all\_inputs\_wo\_rst\_clk

1

set\_output\_delay 0.6 -clock clk [all\_outputs]

1

set\_fix\_hold [ get\_clocks clk ]

1

set\_output\_delay 0.3 -clock clk [all\_outputs]

1

set\_wire\_load\_model -name T8G00TW8

1

compile\_ultra

Alib files are up-to-date.

Information: Sequential output inversion is enabled. SVF file must be used for formal verification. (OPT-1208)

Information: Ungrouping 0 of 1 hierarchies before Pass 1 (OPT-775)

Beginning Pass 1 Mapping

------------------------

Processing 'primary\_lsfr0'

Updating timing information

Information: Updating design information... (UID-85)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Mapping Optimizations (Ultra High effort)

-------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:03 6375.5 0.00 -0.0 0.0 0.00

0:00:03 6375.5 0.00 -0.0 0.0 0.00

0:00:03 6375.5 0.00 -0.0 0.0 0.00

0:00:03 6375.5 0.00 -0.0 0.0 0.00

Re-synthesis Optimization (Phase 1)

Re-synthesis Optimization (Phase 2)

Global Optimization (Phase 1)

Global Optimization (Phase 2)

Global Optimization (Phase 3)

Global Optimization (Phase 4)

Global Optimization (Phase 5)

Global Optimization (Phase 6)

Global Optimization (Phase 7)

Global Optimization (Phase 8)

Global Optimization (Phase 9)

Global Optimization (Phase 10)

Global Optimization (Phase 11)

Global Optimization (Phase 12)

Global Optimization (Phase 13)

Global Optimization (Phase 14)

Global Optimization (Phase 15)

Global Optimization (Phase 16)

Global Optimization (Phase 17)

Global Optimization (Phase 18)

Global Optimization (Phase 19)

Global Optimization (Phase 20)

Global Optimization (Phase 21)

Global Optimization (Phase 22)

Global Optimization (Phase 23)

Global Optimization (Phase 24)

Global Optimization (Phase 25)

Global Optimization (Phase 26)

Global Optimization (Phase 27)

Global Optimization (Phase 28)

Global Optimization (Phase 29)

Global Optimization (Phase 30)

Global Optimization (Phase 31)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Delay Optimization Phase

----------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:04 4495.0 0.00 0.0 98.6 0.00

0:00:04 4495.0 0.00 0.0 98.6 0.00

0:00:04 4495.0 0.00 0.0 98.6 0.00

0:00:04 4495.0 0.00 0.0 98.6 0.00

0:00:04 4495.0 0.00 0.0 98.6 0.00

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0:00:04 4495.0 0.00 0.0 98.6 0.00

0:00:04 4495.0 0.00 0.0 98.6 0.00

Beginning Delay Optimization

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0:00:04 4495.0 0.00 0.0 98.6 0.00

0:00:04 4495.0 0.00 0.0 98.6 0.00

0:00:04 4495.0 0.00 0.0 98.6 0.00

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0:00:04 4495.0 0.00 0.0 98.6 0.00

0:00:04 4495.0 0.00 0.0 98.6 0.00

Beginning Design Rule Fixing (min\_path) (max\_capacitance)

----------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:04 4495.0 0.00 0.0 98.6 -0.25

Global Optimization (Phase 32)

Global Optimization (Phase 33)

Global Optimization (Phase 34)

0:00:04 4497.0 0.00 0.0 0.0 0.00

0:00:05 4460.5 0.00 0.0 0.0 -0.03

0:00:05 4460.5 0.00 0.0 0.0 -0.03

Loaded alib file './alib-52/tc240c.db\_NOMIN25.alib'

0:00:05 4460.5 0.00 0.0 0.0 -0.03

0:00:05 4460.5 0.00 0.0 0.0 -0.03

0:00:05 4461.5 0.00 0.0 0.0 0.00

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:05 4461.5 0.00 0.0 0.0 0.00

0:00:06 4302.5 0.00 0.0 8293.7 0.00

0:00:06 5147.5 0.00 0.0 0.0 0.00

Beginning Area-Recovery Phase (max\_area 0)

-----------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:06 5147.5 0.00 0.0 0.0 0.00

Global Optimization (Phase 35)

Global Optimization (Phase 36)

Global Optimization (Phase 37)

Global Optimization (Phase 38)

Global Optimization (Phase 39)

Global Optimization (Phase 40)

Global Optimization (Phase 41)

Global Optimization (Phase 42)

Global Optimization (Phase 43)

Global Optimization (Phase 44)

Global Optimization (Phase 45)

Global Optimization (Phase 46)

Global Optimization (Phase 47)

Global Optimization (Phase 48)

Global Optimization (Phase 49)

Global Optimization (Phase 50)

Global Optimization (Phase 51)

0:00:07 4304.0 0.00 0.0 0.0 0.00

0:00:07 4304.0 0.00 0.0 0.0 0.00

0:00:07 4304.0 0.00 0.0 0.0 0.00

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0:00:07 4304.0 0.00 0.0 0.0 0.00

Loading db file '/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_NOMIN25'

Optimization Complete

---------------------

1

create\_clock clk -name clk -period 4.0

1

update\_timing

Information: Updating design information... (UID-85)

1

report\_timing -max\_paths 3

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 3

Design : primary\_lsfr0

Version: I-2013.12-SP5

Date : Tue Dec 1 21:29:04 2015

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: NOMIN25 Library: tc240c

Wire Load Model Mode: top

Startpoint: write (input port clocked by clk)

Endpoint: lfsr0\_reg[60]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr0 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 f

write (in) 0.05 0.65 f

U1415/Z (CNIVX1) 0.26 0.91 f

U1412/Z (CNR2IX4) 0.35 1.26 r

U1385/Z (CIVX3) 0.65 1.91 f

U1694/Z (CNR2X1) 0.37 2.28 r

U1695/Z (CND2X1) 0.16 2.44 f

U1697/Z (COND3X1) 0.08 2.52 r

lfsr0\_reg[60]/D (CFD2QXL) 0.00 2.52 r

data arrival time 2.52

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr0\_reg[60]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

-----------------------------------------------------------

data required time 3.53

data arrival time -2.52

-----------------------------------------------------------

slack (MET) 1.00

Startpoint: write (input port clocked by clk)

Endpoint: lfsr0\_reg[19]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr0 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 f

write (in) 0.05 0.65 f

U1415/Z (CNIVX1) 0.26 0.91 f

U1412/Z (CNR2IX4) 0.35 1.26 r

U1385/Z (CIVX3) 0.65 1.91 f

U1518/Z (CNR2X1) 0.37 2.28 r

U1561/Z (CND2X1) 0.16 2.44 f

U1563/Z (COND3X1) 0.08 2.52 r

lfsr0\_reg[19]/D (CFD2XL) 0.00 2.52 r

data arrival time 2.52

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr0\_reg[19]/CP (CFD2XL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

-----------------------------------------------------------

data required time 3.53

data arrival time -2.52

-----------------------------------------------------------

slack (MET) 1.00

Startpoint: write (input port clocked by clk)

Endpoint: lfsr0\_reg[18]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

primary\_lsfr0 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 f

write (in) 0.05 0.65 f

U1415/Z (CNIVX1) 0.26 0.91 f

U1412/Z (CNR2IX4) 0.35 1.26 r

U1385/Z (CIVX3) 0.65 1.91 f

U1649/Z (CNR2X1) 0.37 2.28 r

U1666/Z (CND2X1) 0.16 2.44 f

U1668/Z (COND3X1) 0.08 2.52 r

lfsr0\_reg[18]/D (CFD2XL) 0.00 2.52 r

data arrival time 2.52

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

lfsr0\_reg[18]/CP (CFD2XL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

-----------------------------------------------------------

data required time 3.53

data arrival time -2.52

-----------------------------------------------------------

slack (MET) 1.00

1

analyze -format verilog dataSelectLFSR.v

Running PRESTO HDLC

Searching for ./dataSelectLFSR.v

Compiling source file ./dataSelectLFSR.v

Warning: ./dataSelectLFSR.v:74: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./dataSelectLFSR.v:75: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./dataSelectLFSR.v:76: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./dataSelectLFSR.v:78: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./dataSelectLFSR.v:124: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./dataSelectLFSR.v:128: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./dataSelectLFSR.v:129: Intraassignment delays for blocking assignments are ignored. (VER-129)

Presto compilation completed successfully.

1

elaborate dataSelectLFSR

Running PRESTO HDLC

Inferred memory devices in process

in routine dataSelectLFSR line 18 in file

'./dataSelectLFSR.v'.

===============================================================================

| Register Name | Type | Width | Bus | MB | AR | AS | SR | SS | ST |

===============================================================================

| dataSelect\_reg | Flip-flop | 64 | Y | N | Y | N | N | N | N |

===============================================================================

Presto compilation completed successfully.

Elaborated 1 design.

Current design is now 'dataSelectLFSR'.

1

create\_clock clk -name clk -period 3.0

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_clock\_uncertainty 0.25 clk

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_output\_delay 0.5 -clock clk [all\_outputs]

1

set all\_inputs\_wo\_rst\_clk [remove\_from\_collection [remove\_from\_collection [all\_inputs] [get\_port clk]] [get\_port rst]]

Warning: Can't find port 'rst' in design 'dataSelectLFSR'. (UID-95)

{reset write pushin data[6] data[5] data[4] data[3] data[2] data[1] data[0] initialData[63] initialData[62] initialData[61] initialData[60] initialData[59] initialData[58] initialData[57] initialData[56] initialData[55] initialData[54] initialData[53] initialData[52] initialData[51] initialData[50] initialData[49] initialData[48] initialData[47] initialData[46] initialData[45] initialData[44] initialData[43] initialData[42] initialData[41] initialData[40] initialData[39] initialData[38] initialData[37] initialData[36] initialData[35] initialData[34] initialData[33] initialData[32] initialData[31] initialData[30] initialData[29] initialData[28] initialData[27] initialData[26] initialData[25] initialData[24] initialData[23] initialData[22] initialData[21] initialData[20] initialData[19] initialData[18] initialData[17] initialData[16] initialData[15] initialData[14] initialData[13] initialData[12] initialData[11] initialData[10] initialData[9] initialData[8] initialData[7] initialData[6] initialData[5] initialData[4] initialData[3] initialData[2] initialData[1] initialData[0]}

set\_driving\_cell -lib\_cell CND2X1 $all\_inputs\_wo\_rst\_clk

Warning: Design rule attributes from the driving cell will be

set on the port. (UID-401)

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1

set\_input\_delay 0.6 -clock clk $all\_inputs\_wo\_rst\_clk

1

set\_output\_delay 0.6 -clock clk [all\_outputs]

1

set\_fix\_hold [ get\_clocks clk ]

1

set\_output\_delay 0.3 -clock clk [all\_outputs]

1

set\_wire\_load\_model -name T8G00TW8

1

compile\_ultra

Alib files are up-to-date.

Information: Sequential output inversion is enabled. SVF file must be used for formal verification. (OPT-1208)

Information: Ungrouping 0 of 1 hierarchies before Pass 1 (OPT-775)

Beginning Pass 1 Mapping

------------------------

Processing 'dataSelectLFSR'

Updating timing information

Information: Updating design information... (UID-85)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Mapping Optimizations (Ultra High effort)

-------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:01 961.5 0.00 0.0 0.0 0.00

0:00:01 961.5 0.00 0.0 0.0 0.00

0:00:01 961.5 0.00 0.0 0.0 0.00

0:00:01 961.5 0.00 0.0 0.0 0.00

Re-synthesis Optimization (Phase 1)

Re-synthesis Optimization (Phase 2)

Global Optimization (Phase 1)

Global Optimization (Phase 2)

Global Optimization (Phase 3)

Global Optimization (Phase 4)

Global Optimization (Phase 5)

Global Optimization (Phase 6)

Global Optimization (Phase 7)

Global Optimization (Phase 8)

Global Optimization (Phase 9)

Global Optimization (Phase 10)

Global Optimization (Phase 11)

Global Optimization (Phase 12)

Global Optimization (Phase 13)

Global Optimization (Phase 14)

Global Optimization (Phase 15)

Global Optimization (Phase 16)

Global Optimization (Phase 17)

Global Optimization (Phase 18)

Global Optimization (Phase 19)

Global Optimization (Phase 20)

Global Optimization (Phase 21)

Global Optimization (Phase 22)

Global Optimization (Phase 23)

Global Optimization (Phase 24)

Global Optimization (Phase 25)

Global Optimization (Phase 26)

Global Optimization (Phase 27)

Global Optimization (Phase 28)

Global Optimization (Phase 29)

Global Optimization (Phase 30)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Delay Optimization Phase

----------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:01 817.5 0.00 0.0 345.8 0.00

0:00:01 817.5 0.00 0.0 345.8 0.00

0:00:01 817.5 0.00 0.0 345.8 0.00

0:00:01 817.5 0.00 0.0 345.8 0.00

0:00:01 817.5 0.00 0.0 345.8 0.00

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Beginning Delay Optimization

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0:00:01 817.5 0.00 0.0 345.8 0.00

0:00:01 817.5 0.00 0.0 345.8 0.00

0:00:01 817.5 0.00 0.0 345.8 0.00

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0:00:01 817.5 0.00 0.0 345.8 0.00

0:00:01 817.5 0.00 0.0 345.8 0.00

Beginning Design Rule Fixing (max\_capacitance)

----------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:01 817.5 0.00 0.0 345.8 0.00

Global Optimization (Phase 31)

Global Optimization (Phase 32)

Global Optimization (Phase 33)

0:00:01 818.0 0.00 0.0 0.0 0.00

0:00:02 815.5 0.00 0.0 0.0 0.00

0:00:02 815.5 0.00 0.0 0.0 0.00

Loaded alib file './alib-52/tc240c.db\_NOMIN25.alib'

0:00:02 815.5 0.00 0.0 0.0 0.00

0:00:02 815.5 0.00 0.0 0.0 0.00

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:02 815.5 0.00 0.0 0.0 0.00

0:00:02 815.5 0.00 0.0 0.0 0.00

Beginning Area-Recovery Phase (max\_area 0)

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TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:02 815.5 0.00 0.0 0.0 0.00

Global Optimization (Phase 34)

Global Optimization (Phase 35)

Global Optimization (Phase 36)

Global Optimization (Phase 37)

Global Optimization (Phase 38)

Global Optimization (Phase 39)

Global Optimization (Phase 40)

Global Optimization (Phase 41)

Global Optimization (Phase 42)

Global Optimization (Phase 43)

Global Optimization (Phase 44)

Global Optimization (Phase 45)

Global Optimization (Phase 46)

Global Optimization (Phase 47)

Global Optimization (Phase 48)

Global Optimization (Phase 49)

0:00:02 812.0 0.00 0.0 0.0 0.00

0:00:02 812.0 0.00 0.0 0.0 0.00

0:00:02 812.0 0.00 0.0 0.0 0.00

0:00:02 812.0 0.00 0.0 0.0 0.00

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0:00:02 812.0 0.00 0.0 0.0 0.00

0:00:02 812.0 0.00 0.0 0.0 0.00

Loading db file '/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_NOMIN25'

Optimization Complete

---------------------

1

create\_clock clk -name clk -period 4.0

1

update\_timing

Information: Updating design information... (UID-85)

1

report\_timing -max\_paths 3

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 3

Design : dataSelectLFSR

Version: I-2013.12-SP5

Date : Tue Dec 1 21:29:08 2015

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: NOMIN25 Library: tc240c

Wire Load Model Mode: top

Startpoint: dataSelect\_reg[59]

(rising edge-triggered flip-flop clocked by clk)

Endpoint: dataSelect\_reg[62]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

dataSelectLFSR T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

dataSelect\_reg[59]/CP (CFD2QX1) 0.00 0.00 r

dataSelect\_reg[59]/Q (CFD2QX1) 0.52 0.52 r

U298/Z (CEOX1) 0.61 1.13 r

U299/Z (CENX1) 0.64 1.77 f

U300/Z (CEOXL) 0.33 2.09 r

U301/Z (CENX1) 0.21 2.31 r

U303/Z (COND1XL) 0.14 2.44 f

dataSelect\_reg[62]/D (CFD2QX1) 0.00 2.44 f

data arrival time 2.44

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

dataSelect\_reg[62]/CP (CFD2QX1) 0.00 3.75 r

library setup time -0.23 3.52

data required time 3.52

-----------------------------------------------------------

data required time 3.52

data arrival time -2.44

-----------------------------------------------------------

slack (MET) 1.07

Startpoint: dataSelect\_reg[59]

(rising edge-triggered flip-flop clocked by clk)

Endpoint: dataSelect\_reg[22]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

dataSelectLFSR T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

dataSelect\_reg[59]/CP (CFD2QX1) 0.00 0.00 r

dataSelect\_reg[59]/Q (CFD2QX1) 0.52 0.52 r

U298/Z (CEOX1) 0.61 1.13 r

U299/Z (CENX1) 0.55 1.68 r

U389/Z (CENX1) 0.38 2.06 r

U444/Z (CENX1) 0.21 2.26 r

U446/Z (COND1XL) 0.12 2.38 f

dataSelect\_reg[22]/D (CFD2QXL) 0.00 2.38 f

data arrival time 2.38

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

dataSelect\_reg[22]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

-----------------------------------------------------------

data required time 3.53

data arrival time -2.38

-----------------------------------------------------------

slack (MET) 1.15

Startpoint: dataSelect\_reg[59]

(rising edge-triggered flip-flop clocked by clk)

Endpoint: dataSelect\_reg[32]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

dataSelectLFSR T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

dataSelect\_reg[59]/CP (CFD2QX1) 0.00 0.00 r

dataSelect\_reg[59]/Q (CFD2QX1) 0.52 0.52 r

U298/Z (CEOX1) 0.61 1.13 r

U299/Z (CENX1) 0.55 1.68 r

U389/Z (CENX1) 0.38 2.06 r

U390/Z (CENX1) 0.21 2.26 r

U392/Z (COND1XL) 0.12 2.38 f

dataSelect\_reg[32]/D (CFD2QXL) 0.00 2.38 f

data arrival time 2.38

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

dataSelect\_reg[32]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

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data required time 3.53

data arrival time -2.38

-----------------------------------------------------------

slack (MET) 1.15

1

analyze -format verilog initialize\_scrambler.v

Running PRESTO HDLC

Searching for ./initialize\_scrambler.v

Compiling source file ./initialize\_scrambler.v

Presto compilation completed successfully.

1

elaborate initialize\_scrambler

Running PRESTO HDLC

$display output: I am inside

$display output: address is ???

$display output: data is ????????

Statistics for case statements in always block at line 50 in file

'./initialize\_scrambler.v'

===============================================

| Line | full/ parallel |

===============================================

| 159 | no/auto |

===============================================

Inferred memory devices in process

in routine initialize\_scrambler line 50 in file

'./initialize\_scrambler.v'.

===============================================================================

| Register Name | Type | Width | Bus | MB | AR | AS | SR | SS | ST |

===============================================================================

| Poly14\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly14\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly4\_reg | Flip-flop | 22 | Y | N | Y | N | N | N | N |

| Poly4\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly4\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly7\_reg | Flip-flop | 20 | Y | N | Y | N | N | N | N |

| Poly7\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly7\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly7\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly7\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly7\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly7\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly11\_reg | Flip-flop | 21 | Y | N | Y | N | N | N | N |

| Poly11\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly5\_reg | Flip-flop | 13 | Y | N | Y | N | N | N | N |

| Poly5\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly5\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly5\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly5\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly5\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly5\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly5\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly5\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly5\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly6\_reg | Flip-flop | 16 | Y | N | Y | N | N | N | N |

| Poly6\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly6\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly6\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly6\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly6\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly6\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly6\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly6\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly6\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly6\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly6\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly6\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly6\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly6\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly6\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly6\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly12\_reg | Flip-flop | 19 | Y | N | Y | N | N | N | N |

| Poly12\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly12\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly12\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly12\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly15\_reg | Flip-flop | 20 | Y | N | Y | N | N | N | N |

| Poly15\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly15\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly15\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly3\_reg | Flip-flop | 9 | Y | N | Y | N | N | N | N |

| Poly3\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly3\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly13\_reg | Flip-flop | 6 | Y | N | Y | N | N | N | N |

| Poly13\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly13\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly13\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly13\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly13\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly13\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly2\_reg | Flip-flop | 11 | Y | N | Y | N | N | N | N |

| Poly2\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly9\_reg | Flip-flop | 31 | Y | N | Y | N | N | N | N |

| Poly9\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly9\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly9\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly1\_reg | Flip-flop | 25 | Y | N | Y | N | N | N | N |

| Poly1\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly1\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly1\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly1\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly1\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly10\_reg | Flip-flop | 18 | Y | N | Y | N | N | N | N |

| Poly10\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly0\_reg | Flip-flop | 2 | Y | N | Y | N | N | N | N |

| Poly0\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly0\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly0\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly0\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly0\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly0\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly0\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly0\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly0\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly0\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly0\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly0\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly0\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly0\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly8\_reg | Flip-flop | 6 | Y | N | Y | N | N | N | N |

| Poly8\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| Poly8\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| dataselector\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| dataselector\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

===============================================================================

Presto compilation completed successfully.

Elaborated 1 design.

Current design is now 'initialize\_scrambler'.

1

create\_clock clk -name clk -period 3.0

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_clock\_uncertainty 0.25 clk

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_output\_delay 0.5 -clock clk [all\_outputs]

1

set all\_inputs\_wo\_rst\_clk [remove\_from\_collection [remove\_from\_collection [all\_inputs] [get\_port clk]] [get\_port rst]]

Warning: Can't find port 'rst' in design 'initialize\_scrambler'. (UID-95)

{reset write lfsrdin[31] lfsrdin[30] lfsrdin[29] lfsrdin[28] lfsrdin[27] lfsrdin[26] lfsrdin[25] lfsrdin[24] lfsrdin[23] lfsrdin[22] lfsrdin[21] lfsrdin[20] lfsrdin[19] lfsrdin[18] lfsrdin[17] lfsrdin[16] lfsrdin[15] lfsrdin[14] lfsrdin[13] lfsrdin[12] lfsrdin[11] lfsrdin[10] lfsrdin[9] lfsrdin[8] lfsrdin[7] lfsrdin[6] lfsrdin[5] lfsrdin[4] lfsrdin[3] lfsrdin[2] lfsrdin[1] lfsrdin[0] addr[11] addr[10] addr[9] addr[8] addr[7] addr[6] addr[5] addr[4] addr[3] addr[2] addr[1] addr[0]}

set\_driving\_cell -lib\_cell CND2X1 $all\_inputs\_wo\_rst\_clk

Warning: Design rule attributes from the driving cell will be

set on the port. (UID-401)

Warning: Design rule attributes from the driving cell will be

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1

set\_input\_delay 0.6 -clock clk $all\_inputs\_wo\_rst\_clk

1

set\_output\_delay 0.6 -clock clk [all\_outputs]

1

set\_fix\_hold [ get\_clocks clk ]

1

set\_output\_delay 0.3 -clock clk [all\_outputs]

1

set\_wire\_load\_model -name T8G00TW8

1

compile\_ultra

Alib files are up-to-date.

Information: Sequential output inversion is enabled. SVF file must be used for formal verification. (OPT-1208)

Information: Ungrouping 0 of 1 hierarchies before Pass 1 (OPT-775)

Beginning Pass 1 Mapping

------------------------

Processing 'initialize\_scrambler'

Updating timing information

Information: Updating design information... (UID-85)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Mapping Optimizations (Ultra High effort)

-------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:12 35178.0 0.32 55.8 0.0 0.00

0:00:12 35178.0 0.32 55.8 0.0 0.00

0:00:12 35178.0 0.32 55.8 0.0 0.00

0:00:12 35178.0 0.32 55.8 0.0 0.00

Re-synthesis Optimization (Phase 1)

Re-synthesis Optimization (Phase 2)

Global Optimization (Phase 1)

Global Optimization (Phase 2)

Global Optimization (Phase 3)

Global Optimization (Phase 4)

Global Optimization (Phase 5)

Global Optimization (Phase 6)

Global Optimization (Phase 7)

Global Optimization (Phase 8)

Global Optimization (Phase 9)

Global Optimization (Phase 10)

Global Optimization (Phase 11)

Global Optimization (Phase 12)

Global Optimization (Phase 13)

Global Optimization (Phase 14)

Global Optimization (Phase 15)

Global Optimization (Phase 16)

Global Optimization (Phase 17)

Global Optimization (Phase 18)

Global Optimization (Phase 19)

Global Optimization (Phase 20)

Global Optimization (Phase 21)

Global Optimization (Phase 22)

Global Optimization (Phase 23)

Global Optimization (Phase 24)

Global Optimization (Phase 25)

Global Optimization (Phase 26)

Global Optimization (Phase 27)

Global Optimization (Phase 28)

Global Optimization (Phase 29)

Global Optimization (Phase 30)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Delay Optimization Phase

----------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:15 21951.5 0.00 0.0 4410.6 0.00

0:00:15 21951.5 0.00 0.0 4410.6 0.00

0:00:15 21951.5 0.00 0.0 4410.6 0.00

0:00:15 21951.5 0.00 0.0 4410.6 0.00

0:00:15 21951.5 0.00 0.0 4410.6 0.00

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0:00:15 21951.5 0.00 0.0 4410.6 0.00

Beginning Delay Optimization

----------------------------

0:00:15 21951.5 0.00 0.0 4410.6 0.00

0:00:15 21951.5 0.00 0.0 4410.6 0.00

0:00:15 21951.5 0.00 0.0 4410.6 0.00

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0:00:15 21951.5 0.00 0.0 4410.6 0.00

0:00:15 21951.5 0.00 0.0 4410.6 0.00

0:00:15 21951.5 0.00 0.0 4410.6 0.00

0:00:15 21951.5 0.00 0.0 4410.6 0.00

Beginning Design Rule Fixing (max\_capacitance)

----------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:15 21951.5 0.00 0.0 4410.6 0.00

Global Optimization (Phase 31)

Global Optimization (Phase 32)

Global Optimization (Phase 33)

0:00:15 21955.5 0.00 0.0 0.0 0.00

0:00:16 21918.5 0.00 0.0 0.0 0.00

0:00:16 21918.5 0.00 0.0 0.0 0.00

Loaded alib file './alib-52/tc240c.db\_NOMIN25.alib'

0:00:17 21918.5 0.00 0.0 0.0 0.00

0:00:17 21918.5 0.00 0.0 0.0 0.00

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:17 21918.5 0.00 0.0 0.0 0.00

0:00:17 21918.5 0.00 0.0 0.0 0.00

Beginning Area-Recovery Phase (max\_area 0)

-----------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:17 21918.5 0.00 0.0 0.0 0.00

Global Optimization (Phase 34)

Global Optimization (Phase 35)

Global Optimization (Phase 36)

Global Optimization (Phase 37)

Global Optimization (Phase 38)

Global Optimization (Phase 39)

Global Optimization (Phase 40)

Global Optimization (Phase 41)

Global Optimization (Phase 42)

Global Optimization (Phase 43)

Global Optimization (Phase 44)

Global Optimization (Phase 45)

Global Optimization (Phase 46)

Global Optimization (Phase 47)

Global Optimization (Phase 48)

Global Optimization (Phase 49)

Global Optimization (Phase 50)

Global Optimization (Phase 51)

0:00:23 21300.5 0.00 0.0 0.0 0.00

0:00:23 21300.5 0.00 0.0 0.0 0.00

0:00:23 21300.5 0.00 0.0 0.0 0.00

0:00:23 21300.5 0.00 0.0 0.0 0.00

0:00:23 21300.5 0.00 0.0 0.0 0.00

0:00:23 21300.5 0.00 0.0 0.0 0.00

0:00:23 21300.5 0.00 0.0 0.0 0.00

0:00:23 21300.5 0.00 0.0 0.0 0.00

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0:00:23 21300.5 0.00 0.0 0.0 0.00

0:00:23 21300.5 0.00 0.0 0.0 0.00

Loading db file '/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_NOMIN25'

Optimization Complete

---------------------

Warning: Design 'initialize\_scrambler' contains 1 high-fanout nets. A fanout number of 1000 will be used for delay calculations involving these nets. (TIM-134)

Net 'clk': 2767 load(s), 1 driver(s)

1

create\_clock clk -name clk -period 4.0

1

update\_timing

Information: Updating design information... (UID-85)

Warning: Design 'initialize\_scrambler' contains 1 high-fanout nets. A fanout number of 1000 will be used for delay calculations involving these nets. (TIM-134)

1

report\_timing -max\_paths 3

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 3

Design : initialize\_scrambler

Version: I-2013.12-SP5

Date : Tue Dec 1 21:29:36 2015

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

# A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: NOMIN25 Library: tc240c

Wire Load Model Mode: top

Startpoint: addr[6] (input port clocked by clk)

Endpoint: Poly15\_reg[66]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

initialize\_scrambler

T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 f

addr[6] (in) 0.08 0.68 f

U2932/Z (CIVX2) 0.11 0.79 r

U2935/Z (CND2X1) 0.17 0.96 f

U3043/Z (CNR2X2) 0.16 1.12 r

U3352/Z (CND2X2) 0.27 1.39 f

U3034/Z (CNR2X4) 0.40 1.80 r

U3035/Z (CNIVX1) 0.43 2.23 r

U3382/Z (CMX2XL) 0.30 2.53 f

Poly15\_reg[66]/D (CFD2QXL) 0.00 2.53 f

data arrival time 2.53

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

Poly15\_reg[66]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

-----------------------------------------------------------

data required time 3.53

data arrival time -2.53

-----------------------------------------------------------

slack (MET) 1.00

Startpoint: addr[6] (input port clocked by clk)

Endpoint: Poly15\_reg[65]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

initialize\_scrambler

T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 f

addr[6] (in) 0.08 0.68 f

U2932/Z (CIVX2) 0.11 0.79 r

U2935/Z (CND2X1) 0.17 0.96 f

U3043/Z (CNR2X2) 0.16 1.12 r

U3352/Z (CND2X2) 0.27 1.39 f

U3034/Z (CNR2X4) 0.40 1.80 r

U3035/Z (CNIVX1) 0.43 2.23 r

U3380/Z (CMX2XL) 0.30 2.53 f

Poly15\_reg[65]/D (CFD2QXL) 0.00 2.53 f

data arrival time 2.53

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

Poly15\_reg[65]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

-----------------------------------------------------------

data required time 3.53

data arrival time -2.53

-----------------------------------------------------------

slack (MET) 1.00

Startpoint: addr[6] (input port clocked by clk)

Endpoint: Poly15\_reg[64]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

initialize\_scrambler

T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 f

addr[6] (in) 0.08 0.68 f

U2932/Z (CIVX2) 0.11 0.79 r

U2935/Z (CND2X1) 0.17 0.96 f

U3043/Z (CNR2X2) 0.16 1.12 r

U3352/Z (CND2X2) 0.27 1.39 f

U3034/Z (CNR2X4) 0.40 1.80 r

U3035/Z (CNIVX1) 0.43 2.23 r

U3385/Z (CMX2XL) 0.30 2.53 f

Poly15\_reg[64]/D (CFD2QXL) 0.00 2.53 f

data arrival time 2.53

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

Poly15\_reg[64]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

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data required time 3.53

data arrival time -2.53

-----------------------------------------------------------

slack (MET) 1.00

1

analyze -format verilog scramblerLFSR.v

Running PRESTO HDLC

Searching for ./scramblerLFSR.v

Compiling source file ./scramblerLFSR.v

Presto compilation completed successfully.

1

elaborate scramblerLFSR

Running PRESTO HDLC

Inferred memory devices in process

in routine scramblerLFSR line 13 in file

'./scramblerLFSR.v'.

===============================================================================

| Register Name | Type | Width | Bus | MB | AR | AS | SR | SS | ST |

===============================================================================

| s\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| data\_d1\_reg | Flip-flop | 16 | Y | N | N | N | N | N | N |

===============================================================================

Presto compilation completed successfully.

Elaborated 1 design.

Current design is now 'scramblerLFSR'.

1

create\_clock clk -name clk -period 3.0

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_clock\_uncertainty 0.25 clk

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_output\_delay 0.5 -clock clk [all\_outputs]

1

set all\_inputs\_wo\_rst\_clk [remove\_from\_collection [remove\_from\_collection [all\_inputs] [get\_port clk]] [get\_port rst]]

Warning: Can't find port 'rst' in design 'scramblerLFSR'. (UID-95)

{reset pushin data[15] data[14] data[13] data[12] data[11] data[10] data[9] data[8] data[7] data[6] data[5] data[4] data[3] data[2] data[1] data[0] initialData[31] initialData[30] initialData[29] initialData[28] initialData[27] initialData[26] initialData[25] initialData[24] initialData[23] initialData[22] initialData[21] initialData[20] initialData[19] initialData[18] initialData[17] initialData[16] initialData[15] initialData[14] initialData[13] initialData[12] initialData[11] initialData[10] initialData[9] initialData[8] initialData[7] initialData[6] initialData[5] initialData[4] initialData[3] initialData[2] initialData[1] initialData[0]}

set\_driving\_cell -lib\_cell CND2X1 $all\_inputs\_wo\_rst\_clk

Warning: Design rule attributes from the driving cell will be

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set on the port. (UID-401)

Warning: Design rule attributes from the driving cell will be

set on the port. (UID-401)

Warning: Design rule attributes from the driving cell will be

set on the port. (UID-401)

Warning: Design rule attributes from the driving cell will be

set on the port. (UID-401)

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set on the port. (UID-401)

Warning: Design rule attributes from the driving cell will be

set on the port. (UID-401)

Warning: Design rule attributes from the driving cell will be

set on the port. (UID-401)

1

set\_input\_delay 0.6 -clock clk $all\_inputs\_wo\_rst\_clk

1

set\_output\_delay 0.6 -clock clk [all\_outputs]

1

set\_fix\_hold [ get\_clocks clk ]

1

set\_output\_delay 0.3 -clock clk [all\_outputs]

1

set\_wire\_load\_model -name T8G00TW8

1

compile\_ultra

Alib files are up-to-date.

Information: Sequential output inversion is enabled. SVF file must be used for formal verification. (OPT-1208)

Information: Ungrouping 0 of 1 hierarchies before Pass 1 (OPT-775)

Beginning Pass 1 Mapping

------------------------

Processing 'scramblerLFSR'

Updating timing information

Information: Updating design information... (UID-85)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Mapping Optimizations (Ultra High effort)

-------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:01 767.5 0.00 0.0 0.0 0.00

0:00:01 767.5 0.00 0.0 0.0 0.00

0:00:01 767.5 0.00 0.0 0.0 0.00

0:00:01 767.5 0.00 0.0 0.0 0.00

Re-synthesis Optimization (Phase 1)

Re-synthesis Optimization (Phase 2)

Global Optimization (Phase 1)

Global Optimization (Phase 2)

Global Optimization (Phase 3)

Global Optimization (Phase 4)

Global Optimization (Phase 5)

Global Optimization (Phase 6)

Global Optimization (Phase 7)

Global Optimization (Phase 8)

Global Optimization (Phase 9)

Global Optimization (Phase 10)

Global Optimization (Phase 11)

Global Optimization (Phase 12)

Global Optimization (Phase 13)

Global Optimization (Phase 14)

Global Optimization (Phase 15)

Global Optimization (Phase 16)

Global Optimization (Phase 17)

Global Optimization (Phase 18)

Global Optimization (Phase 19)

Global Optimization (Phase 20)

Global Optimization (Phase 21)

Global Optimization (Phase 22)

Global Optimization (Phase 23)

Global Optimization (Phase 24)

Global Optimization (Phase 25)

Global Optimization (Phase 26)

Global Optimization (Phase 27)

Global Optimization (Phase 28)

Global Optimization (Phase 29)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Delay Optimization Phase

----------------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:01 656.0 0.00 0.0 0.0 0.00

0:00:01 656.0 0.00 0.0 0.0 0.00

0:00:01 656.0 0.00 0.0 0.0 0.00

0:00:01 656.0 0.00 0.0 0.0 0.00

0:00:01 656.0 0.00 0.0 0.0 0.00

0:00:01 656.0 0.00 0.0 0.0 0.00

0:00:01 656.0 0.00 0.0 0.0 0.00

0:00:01 656.0 0.00 0.0 0.0 0.00

0:00:01 656.0 0.00 0.0 0.0 0.00

0:00:01 656.0 0.00 0.0 0.0 0.00

0:00:01 656.0 0.00 0.0 0.0 0.00

Beginning Delay Optimization

----------------------------

0:00:01 656.0 0.00 0.0 0.0 0.00

0:00:01 656.0 0.00 0.0 0.0 0.00

0:00:01 656.0 0.00 0.0 0.0 0.00

0:00:01 656.0 0.00 0.0 0.0 0.00

0:00:01 656.0 0.00 0.0 0.0 0.00

0:00:01 656.0 0.00 0.0 0.0 0.00

0:00:01 656.0 0.00 0.0 0.0 0.00

0:00:01 656.0 0.00 0.0 0.0 0.00

0:00:01 656.0 0.00 0.0 0.0 0.00

0:00:01 655.5 0.00 0.0 0.0 0.00

0:00:01 655.5 0.00 0.0 0.0 0.00

Loaded alib file './alib-52/tc240c.db\_NOMIN25.alib'

0:00:02 655.5 0.00 0.0 0.0 0.00

0:00:02 655.5 0.00 0.0 0.0 0.00

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:02 655.5 0.00 0.0 0.0 0.00

0:00:02 655.5 0.00 0.0 0.0 0.00

Beginning Area-Recovery Phase (max\_area 0)

-----------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:02 655.5 0.00 0.0 0.0 0.00

Global Optimization (Phase 30)

Global Optimization (Phase 31)

Global Optimization (Phase 32)

Global Optimization (Phase 33)

Global Optimization (Phase 34)

Global Optimization (Phase 35)

Global Optimization (Phase 36)

Global Optimization (Phase 37)

Global Optimization (Phase 38)

Global Optimization (Phase 39)

Global Optimization (Phase 40)

Global Optimization (Phase 41)

Global Optimization (Phase 42)

Global Optimization (Phase 43)

Global Optimization (Phase 44)

Global Optimization (Phase 45)

Global Optimization (Phase 46)

Global Optimization (Phase 47)

0:00:02 650.0 0.00 0.0 0.0 0.00

0:00:02 650.0 0.00 0.0 0.0 0.00

0:00:02 650.0 0.00 0.0 0.0 0.00

0:00:02 650.0 0.00 0.0 0.0 0.00

0:00:02 650.0 0.00 0.0 0.0 0.00

0:00:02 650.0 0.00 0.0 0.0 0.00

0:00:02 650.0 0.00 0.0 0.0 0.00

0:00:02 650.0 0.00 0.0 0.0 0.00

0:00:02 650.0 0.00 0.0 0.0 0.00

0:00:02 650.0 0.00 0.0 0.0 0.00

0:00:02 650.0 0.00 0.0 0.0 0.00

0:00:02 650.0 0.00 0.0 0.0 0.00

0:00:02 650.0 0.00 0.0 0.0 0.00

0:00:02 650.0 0.00 0.0 0.0 0.00

0:00:02 650.0 0.00 0.0 0.0 0.00

0:00:02 650.0 0.00 0.0 0.0 0.00

0:00:02 650.0 0.00 0.0 0.0 0.00

0:00:02 650.0 0.00 0.0 0.0 0.00

0:00:02 650.0 0.00 0.0 0.0 0.00

0:00:02 650.0 0.00 0.0 0.0 0.00

Loading db file '/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_NOMIN25'

Optimization Complete

---------------------

1

create\_clock clk -name clk -period 4.0

1

update\_timing

Information: Updating design information... (UID-85)

1

report\_timing -max\_paths 3

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 3

Design : scramblerLFSR

Version: I-2013.12-SP5

Date : Tue Dec 1 21:29:39 2015

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: NOMIN25 Library: tc240c

Wire Load Model Mode: top

Startpoint: s\_reg[30] (rising edge-triggered flip-flop clocked by clk)

Endpoint: rnd1[7] (output port clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

scramblerLFSR T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

s\_reg[30]/CP (CFD2QXL) 0.00 0.00 r

s\_reg[30]/Q (CFD2QXL) 0.83 0.83 r

U267/Z (CENX1) 0.46 1.29 r

U268/Z (CEOX1) 0.38 1.67 r

U340/Z (CENX1) 0.22 1.89 r

U341/Z (CENX1) 0.19 2.08 r

U342/Z (CENX1) 0.20 2.28 r

U343/Z (CENX1) 0.17 2.44 r

rnd1[7] (out) 0.00 2.44 r

data arrival time 2.44

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

output external delay -0.30 3.45

data required time 3.45

-----------------------------------------------------------

data required time 3.45

data arrival time -2.44

-----------------------------------------------------------

slack (MET) 1.01

Startpoint: s\_reg[29] (rising edge-triggered flip-flop clocked by clk)

Endpoint: rnd1[17] (output port clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

scramblerLFSR T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

s\_reg[29]/CP (CFD2QXL) 0.00 0.00 r

s\_reg[29]/Q (CFD2QXL) 0.88 0.88 r

U335/Z (CEOX1) 0.49 1.37 r

U336/Z (CENX1) 0.29 1.67 r

U372/Z (CENX1) 0.21 1.88 r

U373/Z (CENX1) 0.19 2.07 r

U374/Z (CENX1) 0.20 2.27 r

U375/Z (CENX1) 0.17 2.44 r

rnd1[17] (out) 0.00 2.44 r

data arrival time 2.44

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

output external delay -0.30 3.45

data required time 3.45

-----------------------------------------------------------

data required time 3.45

data arrival time -2.44

-----------------------------------------------------------

slack (MET) 1.01

Startpoint: s\_reg[19] (rising edge-triggered flip-flop clocked by clk)

Endpoint: rnd1[29] (output port clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

scramblerLFSR T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

s\_reg[19]/CP (CFD2QX1) 0.00 0.00 r

s\_reg[19]/Q (CFD2QX1) 0.47 0.47 r

U311/Z (CEOX1) 0.46 0.93 r

U312/Z (CENX1) 0.32 1.25 r

U313/Z (CENX1) 0.28 1.53 r

U314/Z (CENX1) 0.27 1.80 r

U315/Z (CENX1) 0.22 2.02 r

U316/Z (CENX1) 0.18 2.20 r

U317/Z (CEOXL) 0.23 2.43 r

rnd1[29] (out) 0.00 2.43 r

data arrival time 2.43

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

output external delay -0.30 3.45

data required time 3.45

-----------------------------------------------------------

data required time 3.45

data arrival time -2.43

-----------------------------------------------------------

slack (MET) 1.02

1

analyze -format verilog se14.v

Running PRESTO HDLC

Searching for ./se14.v

Compiling source file ./se14.v

Warning: ./se14.v:370: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:371: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:377: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:381: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:385: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:389: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:393: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:397: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:400: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:404: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:408: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:412: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:416: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:420: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:424: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:428: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:432: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:436: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:440: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:444: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:448: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:452: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:456: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:460: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:464: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:468: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:472: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:476: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:480: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:484: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:488: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:492: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:496: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:500: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:504: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:508: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:511: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:514: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:517: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:520: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:523: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:526: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:529: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:532: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:535: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:538: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:541: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:544: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:547: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:550: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:553: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:556: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:559: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:562: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:565: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:568: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:571: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:574: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:577: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:580: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:583: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:586: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:589: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:592: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:595: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:598: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:601: Intraassignment delays for blocking assignments are ignored. (VER-129)

Warning: ./se14.v:604: Intraassignment delays for blocking assignments are ignored. (VER-129)

Presto compilation completed successfully.

1

elaborate se14

Running PRESTO HDLC

Statistics for case statements in always block at line 368 in file

'./se14.v'

===============================================

| Line | full/ parallel |

===============================================

| 376 | auto/auto |

| 507 | auto/auto |

===============================================

Inferred memory devices in process

in routine se14 line 164 in file

'./se14.v'.

==================================================================================

| Register Name | Type | Width | Bus | MB | AR | AS | SR | SS | ST |

==================================================================================

| write\_d1\_reg | Flip-flop | 1 | N | N | Y | N | N | N | N |

| P15\_d1\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| P14\_d1\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| P13\_d1\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| P12\_d1\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| P11\_d1\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| P10\_d1\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| P9\_d1\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| P8\_d1\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| P7\_d1\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| P6\_d1\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| P5\_d1\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| P4\_d1\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| P3\_d1\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| P2\_d1\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| P1\_d1\_reg | Flip-flop | 39 | Y | N | Y | N | N | N | N |

| P0\_d1\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| entrophy\_d1\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| datain\_d1\_reg | Flip-flop | 8 | Y | N | Y | N | N | N | N |

| pushin\_d3\_reg | Flip-flop | 1 | N | N | Y | N | N | N | N |

| pushin\_d2\_reg | Flip-flop | 1 | N | N | Y | N | N | N | N |

| pushin\_d1\_reg | Flip-flop | 1 | N | N | Y | N | N | N | N |

| pushout\_d3\_reg | Flip-flop | 1 | N | N | Y | N | N | N | N |

| pushout\_d2\_reg | Flip-flop | 1 | N | N | Y | N | N | N | N |

| pushout\_d1\_reg | Flip-flop | 1 | N | N | Y | N | N | N | N |

| initialScramble\_d1\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| dataScramble\_d1\_reg | Flip-flop | 16 | Y | N | Y | N | N | N | N |

| pushout\_d4\_reg | Flip-flop | 1 | N | N | Y | N | N | N | N |

| datain\_d2\_reg | Flip-flop | 8 | Y | N | Y | N | N | N | N |

| entrophy\_d2\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| sel1\_d1\_reg | Flip-flop | 5 | Y | N | Y | N | N | N | N |

| sel2\_d1\_reg | Flip-flop | 5 | Y | N | Y | N | N | N | N |

| P0\_d2\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| P1\_d2\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| P2\_d2\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| P3\_d2\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| P4\_d2\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| P5\_d2\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| P6\_d2\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| P7\_d2\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| P8\_d2\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| P9\_d2\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| P10\_d2\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| P11\_d2\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| P12\_d2\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| P13\_d2\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| P14\_d2\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

| P15\_d2\_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |

==================================================================================

Presto compilation completed successfully.

Elaborated 1 design.

Current design is now 'se14'.

1

create\_clock clk -name clk -period 3.0

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_clock\_uncertainty 0.25 clk

1

set\_propagated\_clock clk

Information: set\_input\_delay values are added to the propagated clock skew. (TIM-113)

1

set\_output\_delay 0.5 -clock clk [all\_outputs]

1

set all\_inputs\_wo\_rst\_clk [remove\_from\_collection [remove\_from\_collection [all\_inputs] [get\_port clk]] [get\_port rst]]

{write addr[11] addr[10] addr[9] addr[8] addr[7] addr[6] addr[5] addr[4] addr[3] addr[2] addr[1] addr[0] wdata[31] wdata[30] wdata[29] wdata[28] wdata[27] wdata[26] wdata[25] wdata[24] wdata[23] wdata[22] wdata[21] wdata[20] wdata[19] wdata[18] wdata[17] wdata[16] wdata[15] wdata[14] wdata[13] wdata[12] wdata[11] wdata[10] wdata[9] wdata[8] wdata[7] wdata[6] wdata[5] wdata[4] wdata[3] wdata[2] wdata[1] wdata[0] pushin datain[7] datain[6] datain[5] datain[4] datain[3] datain[2] datain[1] datain[0] entrophy[31] entrophy[30] entrophy[29] entrophy[28] entrophy[27] entrophy[26] entrophy[25] entrophy[24] entrophy[23] entrophy[22] entrophy[21] entrophy[20] entrophy[19] entrophy[18] entrophy[17] entrophy[16] entrophy[15] entrophy[14] entrophy[13] entrophy[12] entrophy[11] entrophy[10] entrophy[9] entrophy[8] entrophy[7] entrophy[6] entrophy[5] entrophy[4] entrophy[3] entrophy[2] entrophy[1] entrophy[0]}

set\_driving\_cell -lib\_cell CND2X1 $all\_inputs\_wo\_rst\_clk

Warning: Design rule attributes from the driving cell will be

set on the port. (UID-401)

Warning: Design rule attributes from the driving cell will be

set on the port. (UID-401)

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set\_input\_delay 0.6 -clock clk $all\_inputs\_wo\_rst\_clk

1

set\_output\_delay 0.6 -clock clk [all\_outputs]

1

set\_fix\_hold [ get\_clocks clk ]

1

set\_output\_delay 0.3 -clock clk [all\_outputs]

1

set\_wire\_load\_model -name T8G00TW8

1

compile\_ultra

Alib files are up-to-date.

Information: Sequential output inversion is enabled. SVF file must be used for formal verification. (OPT-1208)

Information: There are 2238 potential problems in your design. Please run 'check\_design' for more information. (LINT-99)

Information: Ungrouping hierarchy L0 before Pass 1 (OPT-776)

Information: Ungrouping hierarchy L1 before Pass 1 (OPT-776)

Information: Ungrouping hierarchy L2 before Pass 1 (OPT-776)

Information: Ungrouping hierarchy L3 before Pass 1 (OPT-776)

Information: Ungrouping hierarchy L4 before Pass 1 (OPT-776)

Information: Ungrouping hierarchy L5 before Pass 1 (OPT-776)

Information: Ungrouping hierarchy L6 before Pass 1 (OPT-776)

Information: Ungrouping hierarchy L7 before Pass 1 (OPT-776)

Information: Ungrouping hierarchy L8 before Pass 1 (OPT-776)

Information: Ungrouping hierarchy L9 before Pass 1 (OPT-776)

Information: Ungrouping hierarchy L10 before Pass 1 (OPT-776)

Information: Ungrouping hierarchy L11 before Pass 1 (OPT-776)

Information: Ungrouping hierarchy L12 before Pass 1 (OPT-776)

Information: Ungrouping hierarchy L13 before Pass 1 (OPT-776)

Information: Ungrouping hierarchy L14 before Pass 1 (OPT-776)

Information: Ungrouping hierarchy L15 before Pass 1 (OPT-776)

Information: Ungrouping hierarchy data\_select before Pass 1 (OPT-776)

Information: Ungrouping hierarchy sl before Pass 1 (OPT-776)

Information: Ungrouping 18 of 20 hierarchies before Pass 1 (OPT-775)

Beginning Pass 1 Mapping

------------------------

Processing 'se14'

Information: In design 'se14', the register 'pushin\_d1\_reg' is removed because it is merged to 'pushout\_d1\_reg'. (OPT-1215)

Information: In design 'se14', the register 'pushin\_d2\_reg' is removed because it is merged to 'pushout\_d2\_reg'. (OPT-1215)

Information: In design 'se14', the register 'pushin\_d3\_reg' is removed because it is merged to 'pushout\_d3\_reg'. (OPT-1215)

Implement Synthetic for 'se14'.

Processing 'initialize\_scrambler'

Updating timing information

Information: Updating design information... (UID-85)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Complementing port 'reset' in design 'initialize\_scrambler'.

The new name of the port is 'reset\_BAR'. (OPT-319)

Information: Complementing port 'reset\_BAR' in design 'initialize\_scrambler'.

The new name of the port is 'reset'. (OPT-319)

Beginning Mapping Optimizations (Ultra High effort)

-------------------------------

Mapping Optimization (Phase 1)

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:37 86780.5 0.25 31.6 0.0 0.00

0:00:37 86780.5 0.25 31.6 0.0 0.00

0:00:37 86780.5 0.25 31.6 0.0 0.00

0:00:37 86774.5 0.25 31.6 0.0 0.00

Re-synthesis Optimization (Phase 1)

Re-synthesis Optimization (Phase 2)

Global Optimization (Phase 1)

Global Optimization (Phase 2)

Global Optimization (Phase 3)

Global Optimization (Phase 4)

Global Optimization (Phase 5)

Global Optimization (Phase 6)

Global Optimization (Phase 7)

Global Optimization (Phase 8)

Global Optimization (Phase 9)

Global Optimization (Phase 10)

Global Optimization (Phase 11)

Global Optimization (Phase 12)

Global Optimization (Phase 13)

Global Optimization (Phase 14)

Global Optimization (Phase 15)

Global Optimization (Phase 16)

Global Optimization (Phase 17)

Global Optimization (Phase 18)

Global Optimization (Phase 19)

Global Optimization (Phase 20)

Global Optimization (Phase 21)

Global Optimization (Phase 22)

Global Optimization (Phase 23)

Global Optimization (Phase 24)

Global Optimization (Phase 25)

Global Optimization (Phase 26)

Global Optimization (Phase 27)

Global Optimization (Phase 28)

Global Optimization (Phase 29)

Global Optimization (Phase 30)

Global Optimization (Phase 31)

Global Optimization (Phase 32)

Global Optimization (Phase 33)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('fall') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Information: Input delay ('rise') on clock port 'clk' will be added to the clock's propagated skew. (TIM-112)

Beginning Delay Optimization Phase

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TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:48 66828.5 0.00 0.0 27250.3 0.00

0:00:48 66828.5 0.00 0.0 27250.3 0.00

0:00:48 66828.5 0.00 0.0 27250.3 0.00

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Beginning Delay Optimization

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0:00:48 66828.5 0.00 0.0 27250.3 0.00

0:00:48 66828.5 0.00 0.0 27250.3 0.00

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0:00:48 66828.5 0.00 0.0 27250.3 0.00

Beginning Design Rule Fixing (min\_path) (max\_capacitance)

----------------------------

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:00:48 66828.5 0.00 0.0 27250.3 -155.11

Global Optimization (Phase 34)

Global Optimization (Phase 35)

Global Optimization (Phase 36)

0:00:50 64896.5 0.00 0.0 0.0 datain\_d2\_reg[5]/D -99.49

0:00:51 65564.5 0.00 0.0 0.0 P9\_d2\_reg[41]/D -37.77

0:00:52 65972.5 0.00 0.0 0.0 0.00

0:01:01 59667.5 0.00 0.0 0.0 -43.72

0:01:01 59667.5 0.00 0.0 0.0 -43.72

Loaded alib file './alib-52/tc240c.db\_NOMIN25.alib'

0:01:02 59667.5 0.00 0.0 0.0 -43.72

0:01:02 59667.5 0.00 0.0 0.0 -43.72

0:01:03 60113.5 0.00 0.0 0.0 P7\_d2\_reg[32]/D -17.13

0:01:03 60373.5 0.00 0.0 0.0 0.00

TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:01:03 60373.5 0.00 0.0 0.0 0.00

0:01:07 59525.0 0.07 0.1 0.0 -0.19

0:01:09 59523.0 0.00 0.0 0.0 -0.19

Beginning Area-Recovery Phase (max\_area 0)

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TOTAL

ELAPSED WORST NEG SETUP DESIGN MIN DELAY

TIME AREA SLACK COST RULE COST ENDPOINT COST

--------- --------- --------- --------- --------- ------------------------- ---------

0:01:09 59523.0 0.00 0.0 0.0 -0.19

Global Optimization (Phase 37)

Global Optimization (Phase 38)

Global Optimization (Phase 39)

Global Optimization (Phase 40)

Global Optimization (Phase 41)

Global Optimization (Phase 42)

Global Optimization (Phase 43)

Information: Complementing port 'reset' in design 'initialize\_scrambler'.

The new name of the port is 'reset\_BAR'. (OPT-319)

Global Optimization (Phase 44)

Global Optimization (Phase 45)

Global Optimization (Phase 46)

Global Optimization (Phase 47)

Global Optimization (Phase 48)

Global Optimization (Phase 49)

Global Optimization (Phase 50)

Global Optimization (Phase 51)

Global Optimization (Phase 52)

Global Optimization (Phase 53)

Global Optimization (Phase 54)

Global Optimization (Phase 55)

Global Optimization (Phase 56)

Global Optimization (Phase 57)

Global Optimization (Phase 58)

0:01:21 56912.5 0.00 0.0 0.0 -143.84

0:01:21 56912.5 0.00 0.0 0.0 -143.84

0:01:22 57708.5 0.00 0.0 0.0 P1\_d2\_reg[28]/D -84.79

0:01:23 58376.5 0.00 0.0 0.0 P12\_d2\_reg[132]/D -22.96

0:01:24 58624.5 0.00 0.0 0.0 0.00

0:01:24 58624.5 0.00 0.0 0.0 0.00

0:01:24 58624.5 0.00 0.0 0.0 0.00

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0:01:24 58624.5 0.00 0.0 0.0 0.00

Loading db file '/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_NOMIN25'

Optimization Complete

---------------------

Warning: Design 'se14' contains 2 high-fanout nets. A fanout number of 1000 will be used for delay calculations involving these nets. (TIM-134)

Net 'clk': 6756 load(s), 1 driver(s)

Net 'net82346': 4200 load(s), 1 driver(s)

1

create\_clock clk -name clk -period 4.0

1

update\_timing

Information: Updating design information... (UID-85)

Warning: Design 'se14' contains 2 high-fanout nets. A fanout number of 1000 will be used for delay calculations involving these nets. (TIM-134)

1

report\_timing -max\_paths 3

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 3

Design : se14

Version: I-2013.12-SP5

Date : Tue Dec 1 21:31:07 2015

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

# A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: NOMIN25 Library: tc240c

Wire Load Model Mode: top

Startpoint: sl/s\_reg[20]

(rising edge-triggered flip-flop clocked by clk)

Endpoint: dataout[29]

(output port clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

se14 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

sl/s\_reg[20]/CP (CFD2QXL) 0.00 # 0.00 r

sl/s\_reg[20]/Q (CFD2QXL) 0.76 0.76 r

U12413/Z (CENX1) 0.36 1.12 r

U12414/Z (CENX1) 0.28 1.40 r

U12415/Z (CEOX1) 0.40 1.81 r

U20652/Z (CENX1) 0.24 2.04 r

U20653/Z (CENX1) 0.18 2.22 r

U20654/Z (CEOXL) 0.23 2.45 r

dataout[29] (out) 0.00 2.45 r

data arrival time 2.45

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

output external delay -0.30 3.45

data required time 3.45

-----------------------------------------------------------

data required time 3.45

data arrival time -2.45

-----------------------------------------------------------

slack (MET) 1.00

Startpoint: pushin (input port clocked by clk)

Endpoint: L0/lfsr0\_reg[70]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

se14 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 r

pushin (in) 0.30 0.90 r

U12068/Z (CND2X1) 0.49 1.39 f

U12047/Z1 (CIVDX2) 0.21 1.60 f

U11508/Z (CNIVX2) 0.40 2.00 f

U11438/Z (CNR2X1) 0.30 2.29 r

U14689/Z (CND2X1) 0.15 2.44 f

U14691/Z (COND3X1) 0.08 2.53 r

L0/lfsr0\_reg[70]/D (CFD2QXL) 0.00 2.53 r

data arrival time 2.53

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

L0/lfsr0\_reg[70]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

-----------------------------------------------------------

data required time 3.53

data arrival time -2.53

-----------------------------------------------------------

slack (MET) 1.00

Startpoint: pushin (input port clocked by clk)

Endpoint: L0/lfsr0\_reg[50]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

se14 T8G00TW8 tc240c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.60 0.60 r

pushin (in) 0.30 0.90 r

U12068/Z (CND2X1) 0.49 1.39 f

U12047/Z1 (CIVDX2) 0.21 1.60 f

U11508/Z (CNIVX2) 0.40 2.00 f

U11438/Z (CNR2X1) 0.30 2.29 r

U20189/Z (CND2X1) 0.15 2.44 f

U20191/Z (COND3X1) 0.08 2.53 r

L0/lfsr0\_reg[50]/D (CFD2QXL) 0.00 2.53 r

data arrival time 2.53

clock clk (rise edge) 4.00 4.00

clock network delay (ideal) 0.00 4.00

clock uncertainty -0.25 3.75

L0/lfsr0\_reg[50]/CP (CFD2QXL) 0.00 3.75 r

library setup time -0.22 3.53

data required time 3.53

-----------------------------------------------------------

data required time 3.53

data arrival time -2.53

-----------------------------------------------------------

slack (MET) 1.00

1

write -hierarchy -format verilog -output se14\_gates.v

Writing verilog file '/home/po/pooj8719/SCRAMBLER/se14\_gates.v'.

Warning: Verilog 'assign' or 'tran' statements are written out. (VO-4)

1

quit

Thank you...