Assignment – 2
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2020MT10784

1. Synchronous 4-bit Gray-Code Counter

State table is given by:-

Q3	Q2	Q1	Q0	Q3’	Q2’	Q1’	Q0’	S0	R0	S1	R1	S2	R2	S3	R3
0	0	0	0	0	0	0	1	1	0	0	X	0	X	0	X
0	0	0	1	0	0	1	1	X	0	1	0	0	X	0	X
0	0	1	1	0	0	1	0	0	1	X	0	0	X	0	X
0	0	1	0	0	1	1	0	0	X	X	0	1	0	0	X
0	1	1	0	0	1	1	1	1	0	X	0	X	0	0	X
0	1	1	1	0	1	0	1	X	0	0	1	X	0	0	X
0	1	0	1	0	1	0	0	0	1	0	X	X	0	0	X
0	1	0	0	1	1	0	0	0	X	0	X	X	0	1	0
1	1	0	0	1	1	0	1	1	0	0	X	X	0	X	0
1	1	0	1	1	1	1	1	X	0	1	0	X	0	X	0
1	1	1	1	1	1	1	0	0	1	X	0	X	0	X	0
1	1	1	0	1	0	1	0	0	X	X	0	0	1	X	0
1	0	1	0	1	0	1	1	1	0	X	0	0	X	X	0
1	0	1	1	1	0	0	1	X	0	0	1	0	X	X	0
1	0	0	1	1	0	0	0	0	1	0	X	0	X	X	0
1	0	0	0	0	0	0	0	0	X	0	X	0	X	0	1

In the above table, Q3, Q2, Q1, and Q0 are the outputs of the previous states, whereas Q3’, Q2’, Q1’ and Q0’ are the outputs of the next states.

Si, Ri (0 ≤ i ≤ 3) are corresponding values for each of the flip-flops, according to their respective transitions of states (x denotes the don’t care conditions).

No. of SR flip-flops required = 4.

After drawing all the K-maps,

S0 = $\overline{Q3\,.\,Q2\,.\,Q1} + \overline{Q3}.\,Q2.\,Q1 + Q3.\,\overline{Q2}.\,Q1 + Q3.\,Q2.\,\overline{Q1}$

K map for S0 ,

Q3 Q2\Q1 Q0	00	01	11	10
00	1	x	0	0
01	0	0	x	1
11	1	x	0	0
10	0	0	x	1

R0 = $\overline{Q3.Q2}.Q1 + \overline{Q3}.Q2.\overline{Q1} + Q3.\overline{Q2.Q1} + Q3.Q2.Q1$

K map for R0

Q3 Q2\Q1 Q0	00	01	11	10
00	0	0	1	x
01	x	1	0	0
11	0	0	1	x
10	x	1	0	0

S1 = $\overline{Q3}.Q2.Q0 + Q3.Q2.Q0$

K map for S1,

Q3 Q2\Q1 Q0	00	01	11	10
00	0	1	x	x
01	0	0	0	x
11	0	1	x	x
10	0	0	0	x

R1 = $\overline{Q3}.Q2.Q0 + Q3.\overline{Q2}.Q0$K map for R1 ,

Q3 Q2\Q1 Q0	00	01	11	10
00	x	0	0	0
01	x	x	0	0
11	x	0	0	0
10	x	x	1	0

S2 = $\overline{Q3}.Q1.\overline{Q0}$

K map for S2 ,

Q3 Q2\Q1 Q0	00	01	11	10
00	0	0	0	1
01	x	x	x	x
11	x	x	x	0
10	0	0	0	0

R2 = $Q3.Q1.\overline{Q0}$

K map for R2 ,

Q3 Q2\Q1 Q0	00	01	11	10
00	x	x	x	0
01	0	0	0	0
11	0	0	0	1
10	x	x	x	x

S3 = $Q2.\overline{Q1.Q0}$

K map for S3,

Q3 Q2\Q1 Q0	00	01	11	10
00	0	0	0	0
01	1	0	0	0
11	x	x	x	x
10	0	x	x	x

R3 = $\overline{Q2.Q1.Q0}$

K map for R3 ,

Q3 Q2\Q1 Q0	00	01	11	10
00	x	x	x	x
01	0	x	x	x
11	0	0	0	0
10	1	0	0	0

Verilog Code-

2. Synchronous Ring Counter

No. of flip-flops required = 4.

My Entry No. is 2020MT10784. So, the counter starts from the state 0100.

State table is given by :-

Q3	Q2	Q1	Q0	D3	D2	D1	D0
0	1	0	0	0	0	1	0
0	0	1	0	1	0	0	1
1	0	0	1	1	1	0	0
1	1	0	0	0	1	1	0
0	1	1	0	1	0	1	1
1	0	1	1	0	1	0	1
0	1	0	1	1	0	1	0
1	0	1	0	1	1	0	1
1	1	0	1	1	1	1	0
1	1	1	0	1	1	1	1
1	1	1	1	0	1	1	1
0	1	1	1	0	0	1	1
0	0	1	1	0	0	0	1

0	0	0	1	1	0	0	0
1	0	0	0				
1	0	0	0	0	1	0	0

As observed, the counter does not cover all 16 possible states. This is because the state 0000 (Q3 Q2 Q1 Q0) is absent, when all the outputs Q3, Q2, Q1, and Q0 are zeroes, it proceeds to an infinite loop, because all the inputs will also be zero always. Moreover, the counter shows the nature of right-shift after each clock cycle.

The K- maps are given as:

:

For D3

Q3 Q2 \Q1 Q0	00	01	11	10
00	x	1	0	1
01	0	1	0	1
11	0	1	0	1
10	0	1	0	1

$$D3 = \overline{Q1}.Q0 + \ Q1.\overline{Q0}$$

For D2

Q3 Q2 \Q1 Q0	00	01	11	10
00	x	0	0	0
01	0	0	0	0
11	1	1	1	1
10	1	1	1	1

$$D2 = Q3$$

For D1:

Q3 Q2 \Q1 Q0	00	01	11	10
00	x	0	0	0
01	1	1	1	1
11	1	1	1	1

10	0	0	0	0

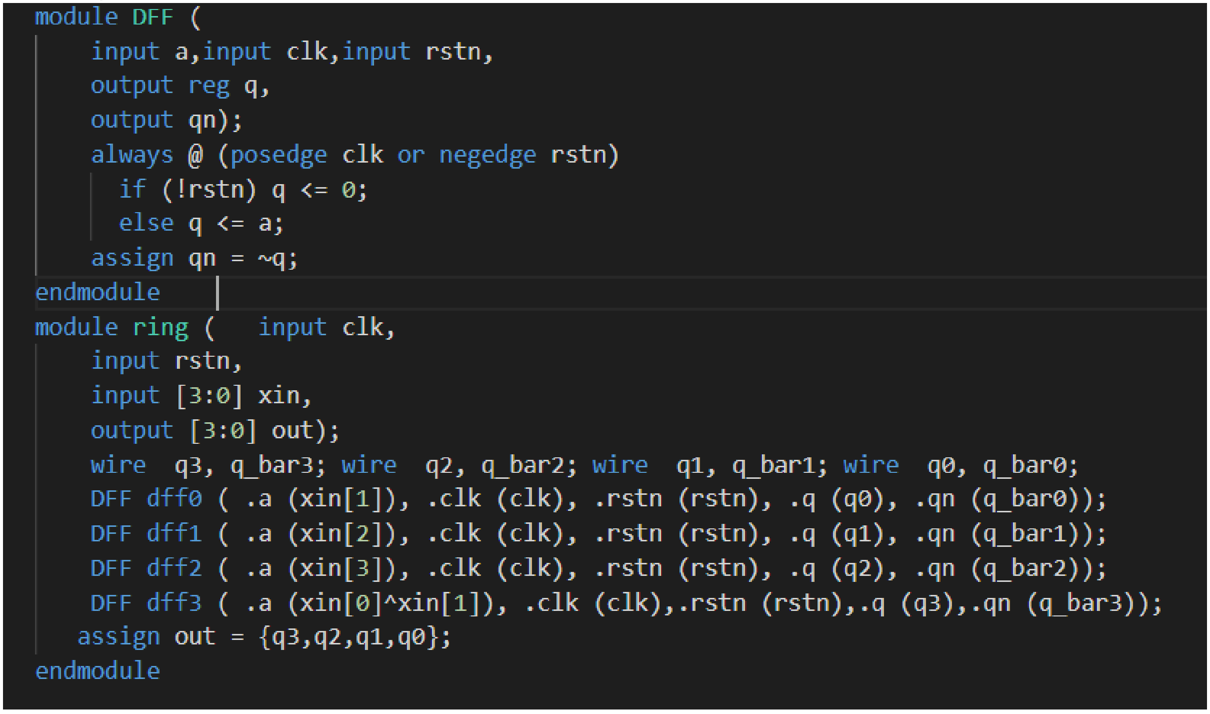
$D1 = Q2$

For D0:

Q3 Q2 \Q1 Q0	00	01	11	10
00	x	0	1	1
01	0	0	1	1
11	0	0	1	1
10	0	0	1	1

$$D0 = Q1$$

Verilog Code:-



```
module DFF (
    input a,input clk,input rstn,
    output reg q,
    output qn);
    always @ (posedge clk or negedge rstn)
      if (!rstn) q <= 0;
      else q <= a;
    assign qn = ~q;
endmodule
module ring (   input clk,
    input rstn,
    input [3:0] xin,
    output [3:0] out);
    wire  q3, q_bar3; wire  q2, q_bar2; wire  q1, q_bar1; wire  q0, q_bar0;
    DFF dff0 ( .a (xin[1]), .clk (clk), .rstn (rstn), .q (q0), .qn (q_bar0));
    DFF dff1 ( .a (xin[2]), .clk (clk), .rstn (rstn), .q (q1), .qn (q_bar1));
    DFF dff2 ( .a (xin[3]), .clk (clk), .rstn (rstn), .q (q2), .qn (q_bar2));
    DFF dff3 ( .a (xin[0]^xin[1]), .clk (clk),.rstn (rstn),.q (q3),.qn (q_bar3));
   assign out = {q3,q2,q1,q0};
endmodule
```