Efficient circuit design for Content-addressable Memory in Quantum-dot Cellular Automata Technology

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Abstract — Building computational circuits uses a type of nanotechnology known as quantum-dot cellular automata (QCA). Due to low delay and area, CMOS has a drawback at the nano-scale level. With the help of Content-Addressable Memory (CAM), we can perform quick searches and that's why CAM is now mostly used in network routing and processors. The study done has shown a loss in area, cost, cell, and, latency in the proposed QCA design. We are using QCA Designer tool version 2.0.3 for demonstrating the results. The developed structure for CAM has 0.75 clock cycles, 0.03 μm2 area, and 32 cells in total. An effective CAM circuit structure is created using the designed memory unit. The results demonstrate that the designed structure for CAM circuit has 32 cells, 0.03 m2 area, 0.75 clock cycles, and a decrease of 20% in cost and 40% in latency compared to existing works.

Keywords: Content-Addressable Memory, Quantum-dot Cellular Automata, Memory Unit, Latency

Article Highlights:

- Designing the CAM circuit with the help of QCA Memory unit.
- Reduced area, cell count, cost, and latency in the proposed QCA memory unit and CAM Circuit.
- Use of QCA Designer tool version 2.0.3.

I. INTRODUCTION

CMOS technology plays a very important role in digital circuits designs. But, at the nano-scale level, it starts to show several drawbacks. At the nano-scale level, QCA (Quantum-dot Cellular Automata) technology is used for the implementation of digital circuits. This technology has low delay and area compared to CMOS technology. Cell is the fundamental element in the QCA technology and it consists of two electrons and four dots. Each cell's electrons have the ability to migrate across the dots. As a result, each cell has two stable states based on coulombic repulsion. In digital circuits, these stable states correspond to logic "0" and "1". The CAM circuit is used to improve the speed as it is accessed in parallel and simultaneously based on content of the data rather than the specific location or address simultaneously based on content of the data rather than the specific location or address.

II. BACKGROUND

A. QCA cells :

Each cell has four dots that are located on the four corners of square and each cell has two electrons that can move freely between dots

The simplest cell arrangement is by placing QCA cells in Series to the side of each other. If the Polarization of any of the cells in the arrangement is changed, then the rest of the cells polarization would synchronize with the new polarization due to the coulombic interactions between them

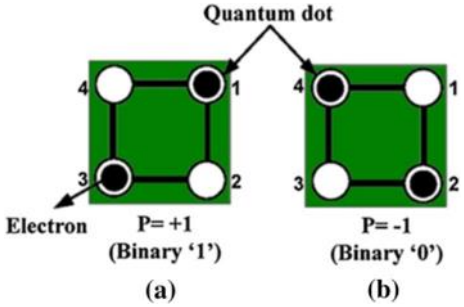


Fig.1 Polarization of the QCA cell (a) P = +1 and (b) P = -1

B. QCA gates :

Majority gate and Inverter gate are the two important QCA gates. If the majority gate inputs are shown by X, Y and Z, the output is shown as:

$$F=MG(X, Y, Z) = ZY+ZX+YX$$

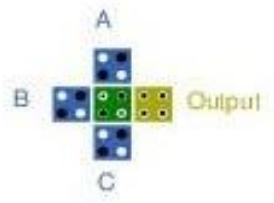


Fig.2 Three-input majority gate

For the inverter gate, the output will be the inverse of its input. There will be no noise in the output for the complex inverter circuit and for the simple inverter gate, it can be designed with the help of only two QCA cells.

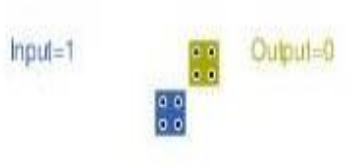


Fig.3(a) QCA Simple Inverter gate

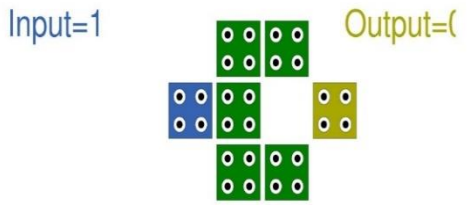


Fig.3(b) QCA Complex Inverter gate

C. CAM Circuits :

The CAM circuits can perform any search operation in very short time

- This circuit is 1-bit RAM circuit which is having a MUX gate that has set and reset ability. In this circuit, clock is present to read/write the signals to synchronize the input signals. The circuit given has 109 cells, 0.13 µm2 area, and 1.75 clock cycles. After observing the output of the circuit, whenever the read/write = 0 it is observed that the value of D Flip Flop is not changed and whenever the read/write = 1 the new input value or Set/Reset can be sent to output but whenever Select = 0
  Set/Reset signal is sent as the output whereas by using Select=1 the new input is transmitted to output.

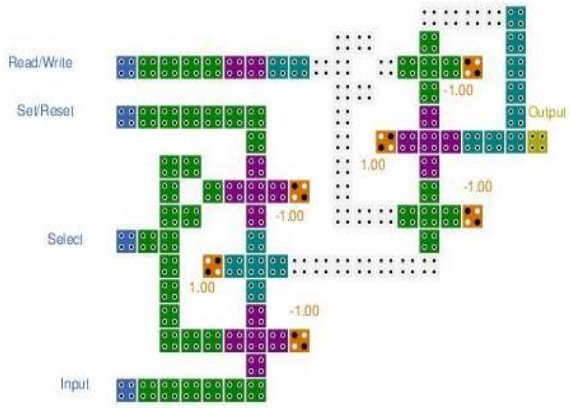


Fig.4 Developed 1-bit QCA RAM circuit

- This circuit is 1-bit RAM circuit which is having a 5-input MG and 3-input MG that is shown in the below figure. The circuit contains 3 AND gates and 1 5-input PMG. In this circuit we have 2 control pins Set and Reset, for reading and write operation we set 'Set' pin to logic-0 and 'Reset' pin to logic-1 whereas for write operation select as well as Read/Write pin is of logic-1 so that the input bit is transmitted at the output. The output of the circuit is controlled with the help of set and reset ability of the memory circuit. The circuit given has 88 cells, 0.08 µm2 area, and 1.5 clock cycles.

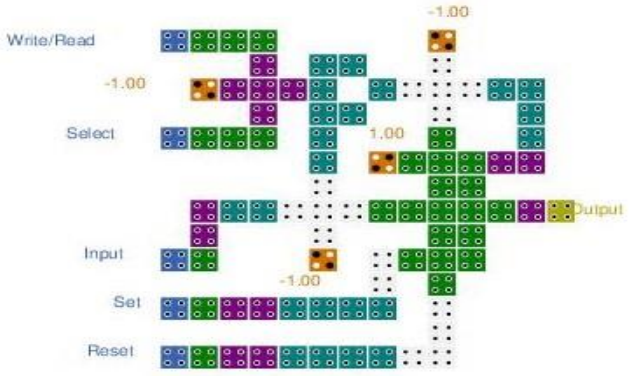


Fig.5 Developed 1-bit RAM circuit

- This circuit is 1-bit RAM circuit which is having Select ability and it has Inverter gate, 5 3-input MG and a MUX gate. This designed RAM circuit is composed of 87 cells, 0.13 µm^2 area and 1.5 clock cycles and the cost that is (Cost = Area*Latency) we get for this circuit is 0.195

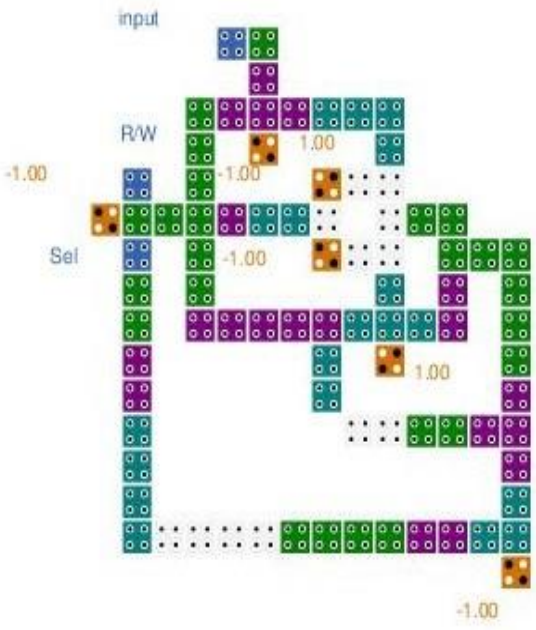


Fig.6 Developed 1-bit RAM circuit

- This circuit is 1-bit RAM circuit and it is developed using 2-1 multiplexers and D-latch circuits. Half-cell misplacement is used for implementation of Inverse Operation in this Multiplexer circuit This circuit has a 3-input MG which is advantage. This circuit consists of 26 cells, 1 clock cycle and an area of 0.026 µm^2 and a latency of 0.026

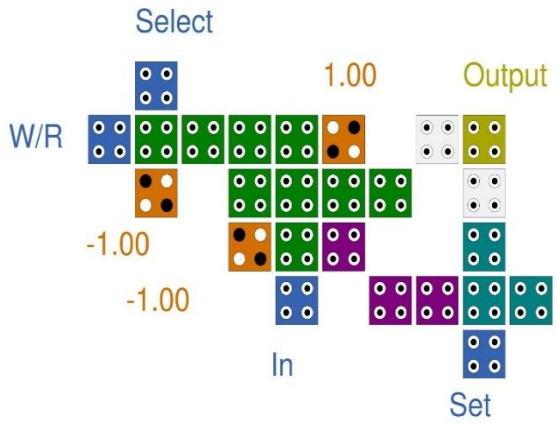


Fig.7 Developed 1-bit RAM circuit

- This circuit is 1-bit CAM circuit which is having a MUX gate, an inverter gate, and five 3-input MG that is shown in the below figure. The output of the circuit is controlled with the help of set and reset ability of the memory circuit. The circuit given has 100 cells, 0.14 µm2 area, and 2 clock cycles

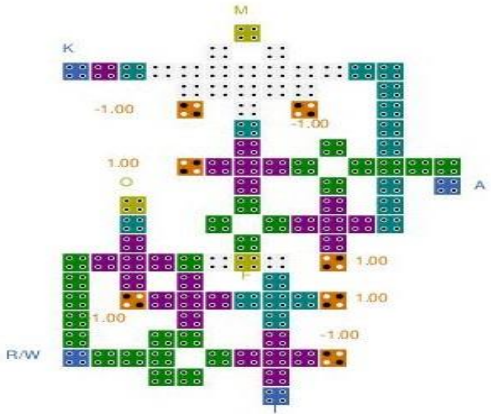


Fig.8 Developed 1-bit CAM circuit

- This circuit is 1-bit CAM circuit which has been made with 3-layers. This circuit is the modified version of the previous circuit. The circuit given has 89 cells, 0.09 µm2 area, and 2 clock cycles.

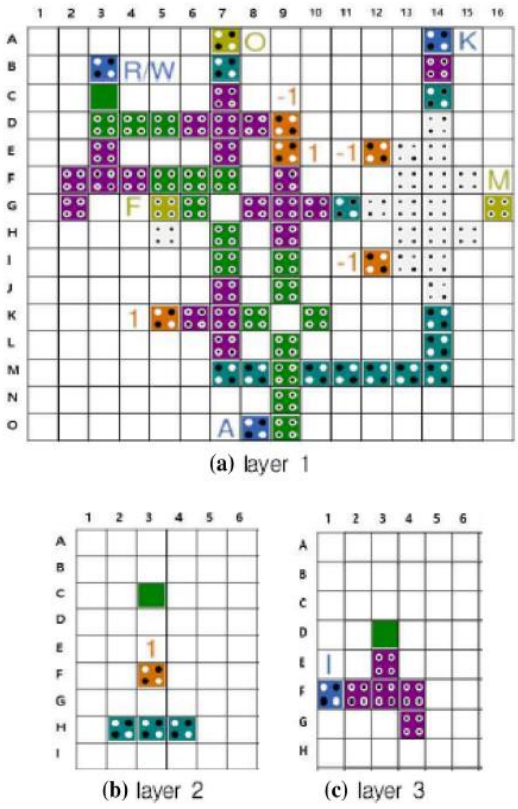


Fig.9 Designed 1-bit CAM circuit

- This circuit is 1-bit CAM circuit which is having a 5-input MG that is shown in the below figure. With the help of 5-input MG, the performance of the circuit is increased. The circuit given has 87 cells, 0.11 µm2 area, and 2 clock cycles.

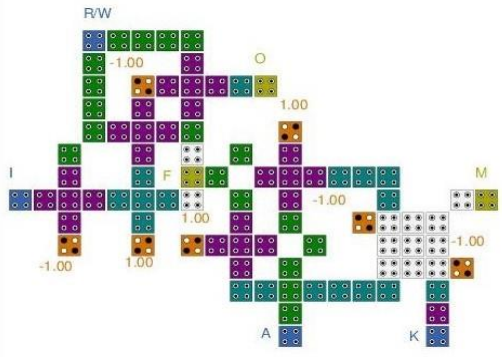


Fig.10 Designed 1-bit CAM circuit

- This circuit is 1-bit CAM circuit which is designed by a unique gate structure using XOR gate and a 3-input MG which is shown in the below figure. The circuit given has 46 cells, 0.04 μm2 area, and 1.25 clock cycles.

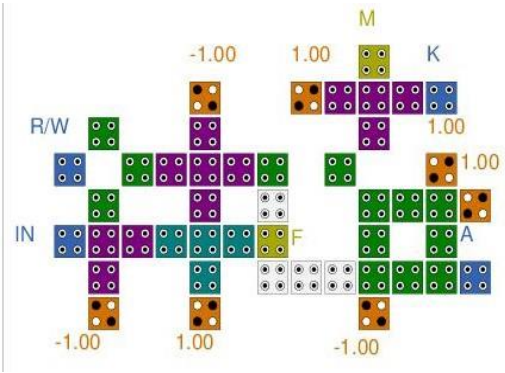


Fig.11 Designed 1-bit CAM circuit

- This circuit is 1-bit CAM circuit which is designed using an optimal unique block using 3-input MG and 2-input XOR gate which is shown in the below figure. A novel CAM circuit is developed using these unique optimal blocks. The circuit given has 40 cells, 0.04 μm2 area, and 1.25 clock cycles.

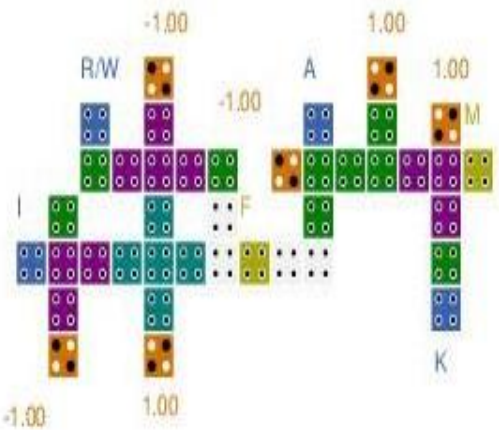


Fig.12 Designed 1-bit CAM circuit

III. PROPOSED CIRCUITS

The proposed structure for the CAM Circuit is composed of two components that is the developed memory unit block and the identity gate. The control signal controls the read and write operation in the memory unit. The output of this unit is the input of the identity gate. It is the task of the identity gate to match the memory unit's output to the desired data.

A. Proposed Memory Unit

The proposed memory unit works on the given equation.

- Assuming (R/W) as X, the equation

$$\mathbf{M = \bar{A}\ IN + \bar{A}\ M}$$

Here, if the R/W which is represented as A in the equation is 0, the input signal IN will be displayed in the output M. In the case of R/W as 1, the previous value will be hold in the output regardless of any input. The proposed memory unit consists of 2-1 multiplexer and negative feedback. The circuit given has 16 cells, 0.01 μm2 area, and 0.25 clock cycles.

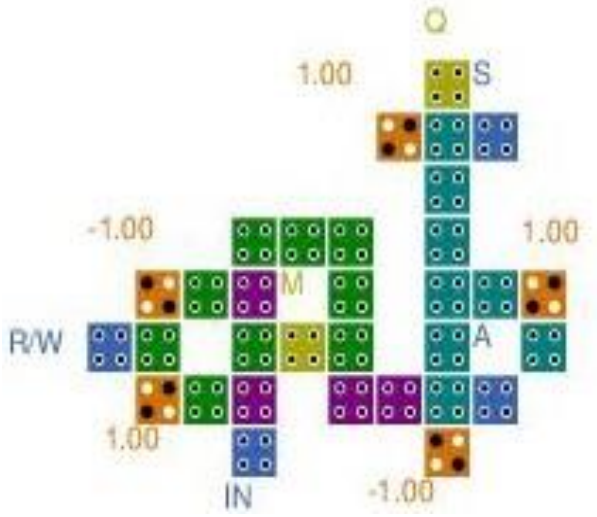
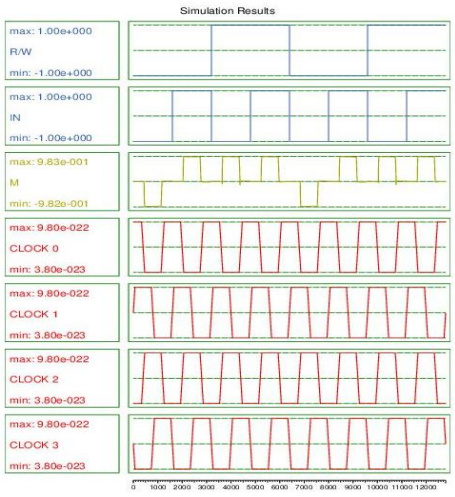


Fig.13 Proposed Memory Unit

- Simulated Result : Proposed Memory Unit Output



- Truth table for Developed Memory Unit

R/W	IN	M
0	0	0
0	1	1
1	0	1
1	1	1

Table 1

B. Proposed CAM Circuit :

The proposed structure for the developed CAM circuit works on the given equation.

- **Q = (A XNOR M) + S**

- The developed circuit given has 32 cells, 0.03 µm2 area, and 0.75 clock cycles.
- In this circuit, one of the inputs to the identity gate is the output coming from memory unit block. A and S are the other two inputs of the identity gate. The output of the identity gate is the output of the developed CAM circuit.
- The table given below will show the results of the developed CAM circuit based on the equation given above. According to the equation, if R/W of the memory unit of the proposed CAM circuit is 0, the output of the memory unit will be input IN. On the other hand, if R/W of the memory unit of the proposed CAM circuit is 1, the output of the memory unit will be the previous value. When the S value is 1, the output Q will be 1, and when the value of S is 0, the output Q is determined based on the inputs of A and M. 1

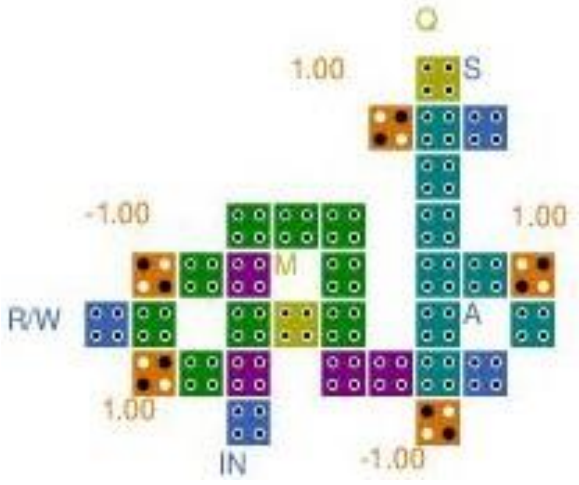


Fig.14 Proposed CAM circuit

- Simulated Output: Proposed CAM Output

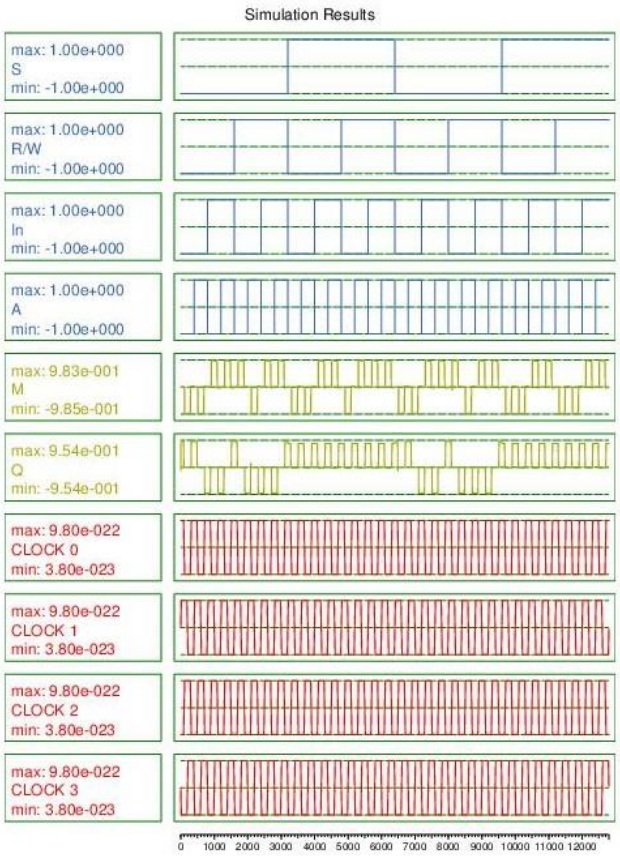


Fig.16 Results of the designed content-addressable memory circuit

- Truth Table for Proposed CAM circuit

S	R/W	IN	A	M=(IN+R/W)	Q=(A XNOR M)+ S
0	0	0	0	0	1
0	0	0	1	0	0
0	0	1	0	1	0
0	0	1	1	1	1
0	1	0	0	1	0
0	1	0	1	1	1
0	1	1	0	1	0
0	1	1	1	1	1
1	0	0	0	0	1
1	0	0	1	0	1
1	0	1	0	1	1
1	0	1	1	1	1

1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

Table 2 Comparative table for CAM circuits

IV. RESULTS AND COMPARISONS

This section describes the simulation results and comparison of the obtained results of the developed circuits with other published circuits. The developed CAM and the developed memory unit are compared with the simulation results that are published in other works. Version 2.0.3 of the QCA designer application is used to simulate the given developed circuits.

A. Proposed MEMORY Unit

The simulation of result of the memory unit is shown in the Figure 15. For this implementation, Bistable approximation is used. The functionality of the designed memory unit is verified by the given simulation results. The given table 3 shows the better performance of proposed memory unit with regards to area, cell count, latency and cost.

Fig	Reference	Cell Count	Area (μm^2)	Latency (clock cycle)	Cost
12	1-bit CAM circuit	24	0.02	0.5	0.01
13	Proposed Memory Unit	16	0.01	0.25	0.0025

Table 3 Comparitive table for memory units

Proposed Content Addressable Memory(CAM)

The results of the proposed content addressable memory have been shown in the figure 16. The functionality of the designed content addressable memory has been verified by the simulation results. Our circuit is having 0.75 clock cycles delay. Table 4 is given which shows the comparison of the proposed content addressable memory with other developed circuits. Based on the results given in the table 4, we can clearly observe that our proposed CAM circuit is better than other given circuits in terms of cell counts, area, latency and cost.

Fig.	Reference	Cell Count	Area	Latency	Cost
4	1-bit QCA RAM circuit	109	0.13	1.75	0.227
5	1-bit RAM circuit	88	0.08	1.5	0.12
6	1-bit RAM circuit	87	0.13	1.5	0.195
7	1-bit RAM circuit	26	0.026	1	0.026
8	1-bit CAM circuit	100	0.14	2	0.28
9	1-bit CAM circuit	89	0.09	2	0.37
10	1-bit CAM circuit	87	0.11	2	0.22
11	1-bit CAM circuit	46	0.04	1.25	0.05
12	1-bit CAM circuit	40	0.04	1.25	0.05
	Memory Unit	24	0.02	0.5	0.01
13	Proposed Memory Unit	16	0.03	0.25	0.0025
14	Proposed CAM circuit	32	0.03	0.75	0.02

Table 4 Comparative table for the CAM circuits

CONCLUSION

The QCA technology is one of the cutting-edge nanotechnologies that, by utilising its superior properties like speed and area, has been able to replace the CMOS. A memory circuit type that is mostly used in high-speed systems is the CAM circuit. In this paper, a new memory unit circuit was developed. This new memory unit was then used to create a CAM circuit for the QCA technology. With the help of QCA Designer tool version 2.0.3, all the outcomes are attained. The suggested CAM circuit requires 32 cells, 0.75 clock cycles of delay, and 0.03 μm2 of space. The simulation results show that the developed circuit performs better than other circuits. In terms of area, cell count, latency, and cost, the suggested CAM circuit has been improved by around 25%, 20%, 40%, and 60%, respectively, over the recently designed CAM circuit.