

top: project/pd*/verif/tests/test_*.v

design_wrapper dut: project/pd*/design/design_wrapper.v

clockgen clkg:
project/pd*/verif/tests/clockgen.v

clock

reset

`TOP_MODULE core: project/pd*/design/code/*.v

YOUR DESIGN FILES AND
OTHER SUBMODULES HERE

a.v
b.v
...
...

probes defined in
project/pd*/design/signals.v

`define PROBE_NAME \
 probe.path.to.signal

`TOP_MODULE defined in
project/pd*/design/signals.h

`define TOP_MODULE riscv

project/pds/verif/scripts/design.f

FILE LIST OF YOUR DESIGN:
a.v
b.v
...