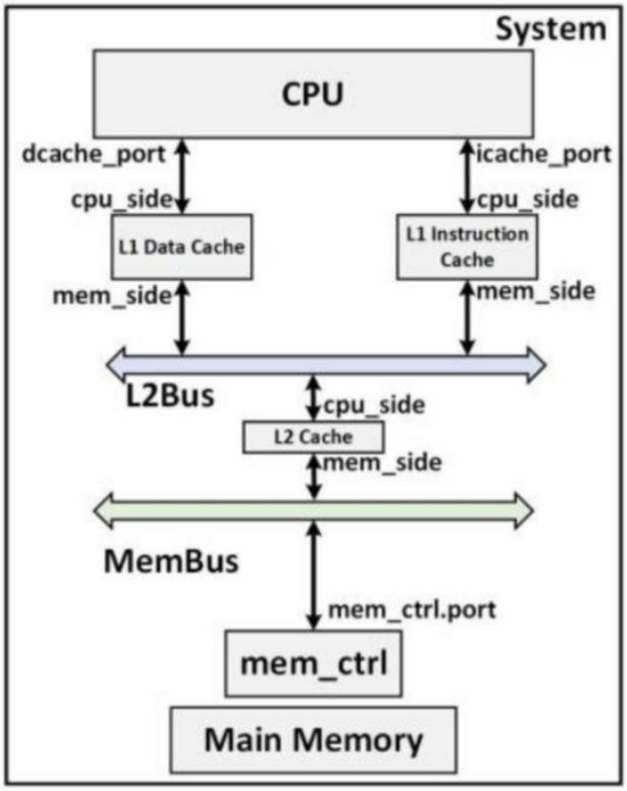
Computer Architecture (CSE511/ ECE 511)

Simulation Assignment - 1

-Aditya Saini, 2018125, B.Tech ECE

Introduction

The objective of the assignment was to simulate the following microarchitecture in the X86



ISA by changing the properties of L2 cache (like memory size and associations) and finally report/plot the obtained L2 cache miss rate by running the Susan benchmark from the MiSuite.

Contents of the directory

The contents of the folder are as follows:

- **Report.pdf (opened document)** - Report containing the finalized plot values, results, and thorough reasoning behind them
- **Q1.py** - The config file for the given microarchitecture.
    - Reference: http://learning.gem5.org/
- **Q2_table_helper.py, Q2_plot_helper.py, Plotter.py** - Basic helper functions which help in obtaining the output values

Miss rate values

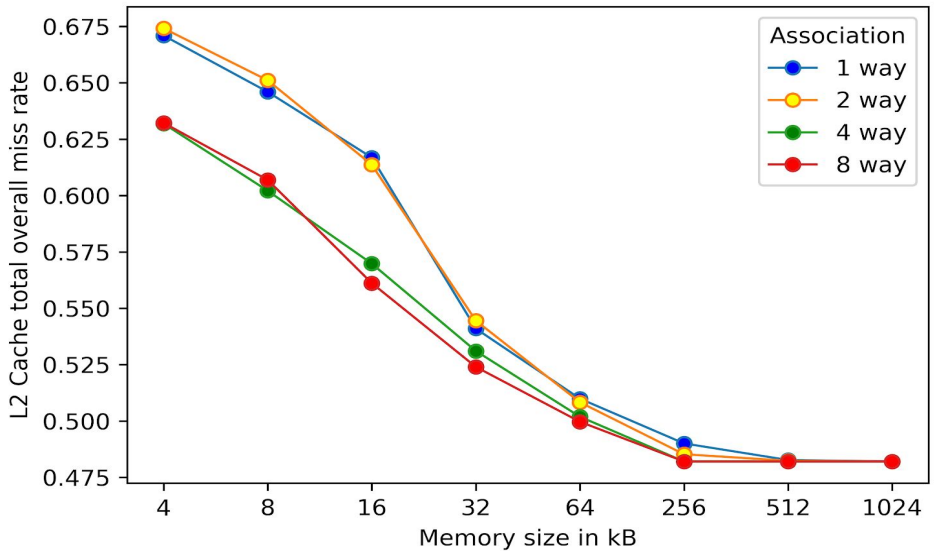
The values were obtained by running the config file on the Susan benchmark from the MiSuite and varying L2 cache properties. These values are:

```
assocs_1_total=['0.670935', '0.645967', '0.616837', '0.540973', '0.509923', '0.490077', '0.482714', '0.482074']
assocs_1_inst=['1', '1', '0.995536', '0.985119', '0.958333', '0.901786', '0.875000', '0.872024']
assocs_1_data=['0.580750', '0.548940', '0.513051', '0.419250', '0.387031', '0.377243', '0.375204', '0.375204']
assocs_1_demand_total=['0.670935', '0.645967', '0.616837', '0.540973', '0.509923', '0.490077', '0.482714', '0.482074']
assocs_2_total=['0.674136', '0.651088', '0.613636', '0.544494', '0.508323', '0.485275', '0.482394', '0.482074']
assocs_2_inst=['1', '1', '0.992560', '0.980655', '0.952381', '0.883929', '0.873512', '0.872024']
assocs_2_data=['0.584829', '0.555465', '0.509788', '0.424959', '0.386623', '0.376020', '0.375204', '0.375204']
assocs_2_demand_total=['0.674136', '0.651088', '0.613636', '0.544494', '0.508323', '0.485275', '0.482394', '0.482074']
assocs_4_total=['0.631882', '0.602113', '0.569782', '0.531050', '0.501921', '0.482074', '0.482074', '0.482074']
assocs_4_inst=['1', '1', '0.994048', '0.982143', '0.933036', '0.872024', '0.872024', '0.872024']
assocs_4_data=['0.530995', '0.493067', '0.453507', '0.407423', '0.383768', '0.375204', '0.375204', '0.375204']
assocs_4_demand_total=['0.631882', '0.602113', '0.569782', '0.531050', '0.501921', '0.482074', '0.482074', '0.482074']
assocs_8_total=['0.632202', '0.606914', '0.561140', '0.524008', '0.499680', '0.482074', '0.482074', '0.482074']
assocs_8_inst=['1', '1', '0.986607', '0.979167', '0.938988', '0.872024', '0.872024', '0.872024']
assocs_8_data=['0.531403', '0.499184', '0.444535', '0.399266', '0.379282', '0.375204', '0.375204', '0.375204']
assocs_8_demand_total=['0.632202', '0.606914', '0.561140', '0.524008', '0.499680', '0.482074', '0.482074', '0.482074']
```

2.b: Plots of miss rate values

L2 cache total overall miss rate vs. L2 cache size

The plot has been generated for four association levels = {1,2,4,8}

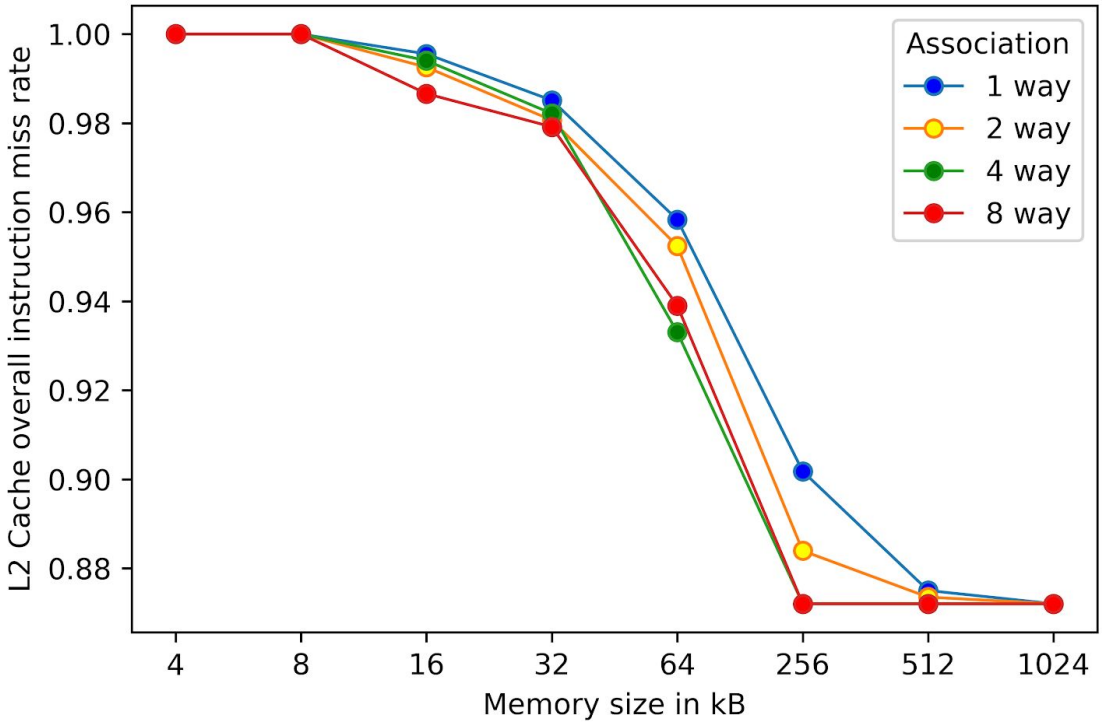


Configurations

Cache Memory in kB	Association Level = 1	Association Level = 2	Association Level = 4	Association Level = 8
4	0.670935	0.674136	0.631882	0.632202
8	0.645967	0.651088	0.602113	0.606914
16	0.616837	0.613636	0.569782	0.56114
32	0.540973	0.544494	0.53105	0.524008
64	0.509923	0.508323	0.501921	0.49968
256	0.490077	0.485275	0.482074	0.482074
512	0.482714	0.482394	0.482074	0.482074
1024	0.482074	0.482074	0.482074	0.482074

L2 cache overall instruction miss rate vs. L2 cache size

The plot has been generated for four association levels = {1,2,4,8}

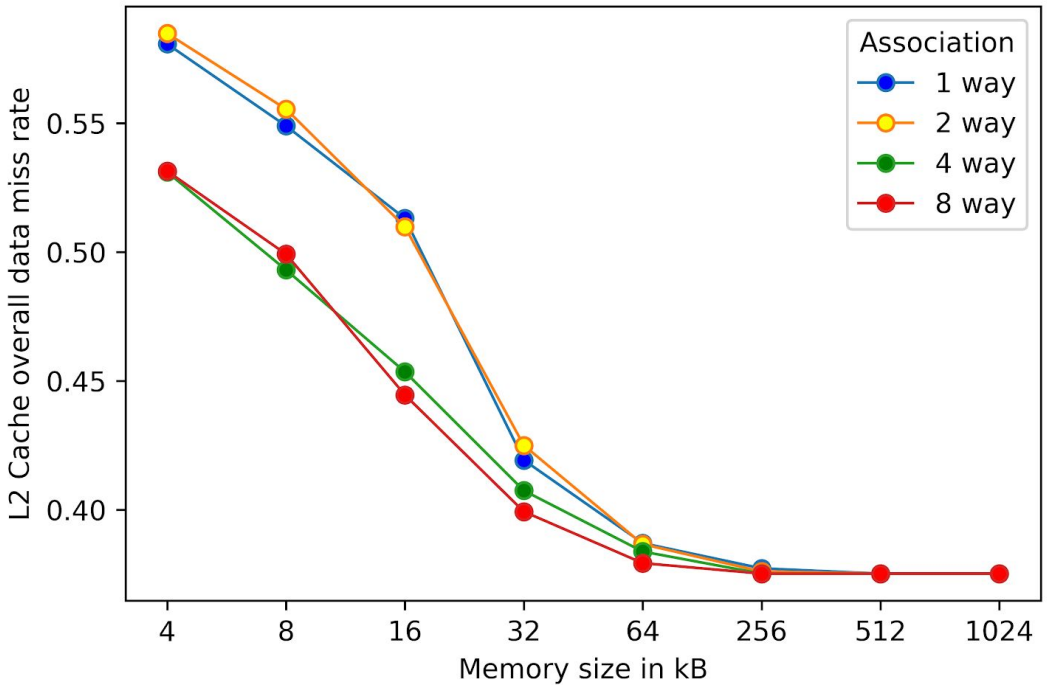


Configurations

Cache Memory in kB	Association Level = 1	Association Level = 2	Association Level = 4	Association Level = 8
4	1.0	1.0	1.0	1.0
8	1.0	1.0	1.0	1.0
16	0.995536	0.99256	0.994048	0.986607
32	0.985119	0.980655	0.982143	0.979167
64	0.958333	0.952381	0.933036	0.938988
256	0.901786	0.883929	0.872024	0.872024
512	0.875	0.873512	0.872024	0.872024
1024	0.872024	0.872024	0.872024	0.872024

L2 cache overall data miss rate vs. L2 cache size

The plot has been generated for four association levels = {1,2,4,8}



Configurations

Cache Memory in kB	Association Level = 1	Association Level = 2	Association Level = 4	Association Level = 8
4	0.58075	0.584829	0.530995	0.531403
8	0.54894	0.555465	0.493067	0.499184
16	0.513051	0.509788	0.453507	0.444535
32	0.41925	0.424959	0.407423	0.399266
64	0.387031	0.386623	0.383768	0.379282
256	0.377243	0.37602	0.375204	0.375204
512	0.375204	0.375204	0.375204	0.375204
1024	0.375204	0.375204	0.375204	0.375204

2.c: Observations & Reasoning

Observations

From the above graphs, the following observations can be made:

1. **Irrespective of the number of the set-associations, *the miss rate value decreases as we increase the size of our L2 cache*.**
2. **Irrespective of the memory size, t*he miss rate value decreases as we increase the number of set-association levels.***
    - This effect saturates as we reach larger memory sizes.

Reasoning

1st observation: Suppose a scenario where we have a really low cache size, and the processor wants to use more blocks than the cache's capacity. In this case, a lot of cache misses will happen as there isn't enough size on the cache to accommodate all the blocks. These types of misses are called *capacity misses*.

So, if we have a larger cache size, **we'd be able to accommodate more overhead from the processors as there will be more space for every block**. Thus, increasing the cache size will undoubtedly reduce the cache miss rate.

2nd observation: As we increase the number of set-association levels, we give more *choices* to a block for its placement in the cache. What happens is that in small levels of association, a block gets really limited space. So *it becomes possible that many same blocks get mapped to the same location in the cache due to inefficient placement strategies (maybe because of an inadequate hash function)*. Therefore, some particular blocks aren't able to coexist in the cache. These types of misses are called *conflict misses.*

So if we have a large number of set-association levels, **we increase the choices or safety of a given block**, thus significantly reducing the cache miss rate.