1. How many cycles should the `SUB` instruction be stalled so that it executes correctly?

   Answer: 3

2. Which instruction will require in its `MEM` stage, data produced by a previous instruction?

   (a) reg-reg
   (b) `lw`
   (c) `sw`
   (d) `beq`
   (e) None of the above

   Answer: (c)

3. Without data forwarding, how many cycles of stall are required for `sw`, when register file isn't arranged so that write happens before read ?

   Answer: 3

4. Without data forwarding, how many cycles of stall are required for `sw`, when register file is arranged so that write happens before read ?

   Answer: 2

5. In the case, without any data forwarding, and assuming register file does not do read after write, how many cycles of stall are required for the `sw` instruction?

   Answer: 2

6. In the case, without any data forwarding, and assuming register file does read after write, how many cycles of stall are required for the `sw` instruction?

   Answer: 1

7. How can we avoid stalls for the `sw` instruction in this example?

   (a) Forward from the register file
   (b) Forward from the `EX/MEM` latch
   (c) Forward from the `MEM/WB` latch

(d) There's no latch shown from which we can forward the needed data

Answer: (d)

8. Is a data hazard possible in a memory location?

   (a) Yes, in all architectures

   (b) Yes, but not in MIPS

   (c) Not possible in any architecture

   Answer: (b)

9. Which of the following is an example of structural hazard due to different number of cycles for different instructions? Select all that apply.

   (a) Any non-dependent instruction between `LW` and `ADD` will cause a structural hazard between `LW` and `ADD`

   (b) Any `ADD` instruction following the given `ADD` will cause a structural hazard with the original `ADD`

   (c) Any `ADD` instruction following the given `ADD` will cause a structural hazard with the original `LW`

   (d) A `LW` instruction following the given `ADD` will cause a structural hazard with the original `LW`

   Answer: (b), (d)

10. What is the minimum number of cycles of stall required for the `add` instruction, assuming that we arrange for the necessary data forwarding?

    Answer: 1

11. Which of the following data forwarding will come into play for the dependent add, following the `lw` ?

    (a) Forward from `MEM/WB` to `EX` stage

    (b) Forward from Post-`WB` to `EX` stage

    (c) Forward from `EX/MEM`to `EX` stage

    (d) Forward from `MEM/WB` to `MEM` stage

    Answer: (a)