1. What are the two inputs to this 2-to-1 mux going to be, to determine the memory address?

   (a) PC and MemOut
   (b) PC+4 and ALUOut
   (c) PC and ALUOut
   (d) PC+4 and Reg2Val

   Answer: (c)

2. What will be the changes from the single cycle implementation on the output side of ALU ?

   (a) ALU will now have two 32 bit output results
   (b) ALU will now have four 32 bit output results
   (c) There will now be a latch to store the ALUOut
   (d) There will be no change

   Answer: (c)

3. Why are we computing the branch target even if it is not a branch instruction, and even before knowing the branch condition?

   (a) We're doing it because we can be ready with the branch target if and when needed
   (b) This is inefficient and should not be done; it is mentioned so here just for ease of instruction

   Answer: (a)

4. Is the lw instruction complete after 5 stages?

   (a) Yes
   (b) No

   Answer: (a)