CS230 In-Video Quiz **Lecture 11**

1. What would be the cycle length in a single cycle implementation of MIPS?

   (a) 1 ns
   (b) 1 μs
   (c) $\sqrt{e}$ μs
   (d) The question does not have enough information to determine the answer

   Answer: (d)

2. What would be the average CPI in a single cycle implementation of MIPS?

   (a) 1
   (b) 2
   (c) This depends on the instruction mix of the program
   (d) This depends on the number of floating point instructions in the program

   Answer: (a)

3. What kind of arguments does `add` take in MIPS? Select all that apply.

   (a) Two registers to be added and the result stored onto a third register
   (b) Three registers to be added and the result stored onto a fourth register
   (c) A register and a memory location to be added and the result stored onto another register
   (d) Two registers to be added and the result stored onto a memory location

   Answer: (a)

4. How many registers need to be specified in the `lw` instruction?

   (a) 1
   (b) 2
   (c) 3
   (d) 4

   Answer: (b)

5. How many registers need to be specified in the `sw` instruction?

(a) 1

(b) 2

(c) 3

(d) 4

Answer: (b)

6. What is the least (numeric) integer value of the offset in `lw`?

   Answer: -32768 = -2^{15}

7. What is the largest (numeric) integer value of the offset in `sw`?

   Answer: $32767 = 2^{15} - 1$

8. Which instruction format is used by `beq`?

   (a) R

   (b) I

   (c) J

   (d) Some other format

   Answer: (b)

9. What is the role of the `immediate` operand in `beq`?

   (a) It is added to one of the given registers to compute the branch target

   (b) It is added to both of the given registers to compute the branch target

   (c) It is added to PC to compute the branch target

   (d) It is added to PC+4 compute the branch target

   Answer: (d)

10. Which of the 3 instruction formats is not relevant for MIPS ISA subset consisting of: `add, sub, and, or, slt, lw, sw, beq`?

    (a) R

    (b) I

    (c) J

    (d) All 3 formats are relevant

Answer: (c)

11. What are the two steps involved in program execution?

    (a) compiling and linking
    (b) linking and loading
    (c) instruction fetching and instruction execution
    (d) instruction fetching and data fetching

    Answer: (c)

12. Among the instructions `add, sub, and, or, slt, lw, sw, beq`, is there any common substep in instruction execution, after instruction fetch?

    (a) Yes, the step of reading registers is common
    (b) Yes, the step of reading memory is common
    (c) Yes, the step of writing a register is common
    (d) No, there is no common substep in instruction execution

    Answer: (a)

13. Is there another common substep in instruction execution, among `add, sub, and, or, slt, lw, sw, beq`?

    (a) Yes, the substep of writing a register
    (b) Yes, the substep of computing PC+4
    (c) No, there are no further common substeps in execution

    Answer: (b)

14. Is the instruction memory a sequential component or a combinatorial component?

    (a) Sequential
    (b) Combinatorial

    Answer: (a)

15. Where does the instruction address come from?

    (a) The OS provides it

(b) The loader provides it

(c) The special register PC (Program Counter)

(d) One of the registers in the register file with the 32 registers

Answer: (c)

16. Is the PC a sequential component or a combinatorial component?

    (a) Sequential

    (b) Combinatorial

    Answer: (a)

17. For which instruction among `add, sub, and, or, slt, lw, sw, beq`, is reading only one register sufficient? (Answer in lowercase).

    Answer: `lw`

18. How many bits does it take to specify each of Reg1 (first register to be read), Reg2 (second register to be read), and WrReg (register to be written)?

    Answer: 5

19. How many lines (bits) does Reg1Val involve?

    Answer: 32

20. Is the register file a sequential component or a combinatorial component ?

    (a) Sequential

    (b) Combinatorial

    Answer: (a)

21. Which of the following instructions DO NOT involve a register write? Select all that apply

    (a) `add`

    (b) `slt`

    (c) `lw`

    (d) `sw`

    (e) `beq`

    Answer: (c), (d), (e)

22. For which instruction in our subset is the output from ALU zero? Useful?

    Answer: `beq`

23. Is the ALU a sequential component or a combinatorial component?

    (a) Sequential
    (b) Combinatorial

    Answer: (b)

24. Is the data memory sequential or combinatorial?

    (a) Sequential
    (b) Combinatorial

    Answer: (a)

25. Is the adder component sequential or combinatorial?

    (a) Sequential
    (b) Combinatorial

    Answer: (b)

26. Can the earlier (main) ALU be used for computing PC+4?

    (a) Yes, the adder shown here is the main ALU itself, with the control lines set for `add`
    (b) Yes, but we need additional muxes for the ALU input
    (c) Yes, but we need additional muxes for the ALU input as well as ALU output
    (d) No, this is not possible since the same unit cannot perform two functionalities in a cycle

    Answer: (d)

27. What is the first input to the adder which computes the branch target?

    (a) The first register value read
    (b) The second register value read
    (c) PC

(d) PC+4

(e) The instruction which is read

Answer: (d)

28. What is the second input to the adder computing the branch target?

(a) The third register value

(b) PC+4

(c) Immediate offset

(d) Sign extended immediate offset

(e) Sign extended immediate offset shifted by 2

Answer: (e)