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CS23	230 DLDCA End-Sem <u>LITE</u> , Tue 12 Nov 2024, 13.	30-16.30, Max. Marks: 40
Gener •	eral instructions Write only in the space provided. Answer briefly but crisply (no	ot lengthily or loosely).
•	You are allowed to refer to your own hand-written notes only. Write neatly and clearly. Up to +2 HP for neat handwriting, neatly have to be (briefly) explained. State any necessity of the second	•
[Q1]] Short answer questions: [1x13+2=15 marks]	
1.	. What real instruction(s) does the pseudo-instruction 'la' (load add	dress) translate to?
2.	. MIPS has a convention as to which registers are caller saved ver the need for such a convention?	sus which are callee saved. What is
3.	. Are RAW hazards in memory locations possible in the 5-stage M	IIPS pipeline? Explain.
4.	. Give an example of spatial locality in instruction memory access	5.

5. When we say that a machine is a 32-bit architecture, what does this 32-bit refer to?

6. State one use of virtual memory as a level of indirection.

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7.	What is the typical hit-time of TLB, in terms of number of cycles?	
8.	State one advantage of having a long pipeline, i.e. a large number	of stages
9.	State one disadvantage of having a long pipeline, i.e. a large numb	per of stages
10.	What are the three kinds of bus lines?	
11.	In MIPS, not R1 , R2 is a pseudo-instruction where R1 gets ass the bit-wise toggling of R2. Implement this pseudo-instruction us	
12.	In the instructions srl & sll , which of the registers {Rs, Rt neither read and used, nor written)?	Rd }, if any, are ignored (i.e.
13.	What does the instruction jalr do?	
14.	[2 marks] Complete the following MIPS assembly code such that L3, \$s0 has the value of PC.	when executing the instruction at
	L1:	
	L2:	
	L3: # here, \$s0 must be PC (i.e address con	responding to L3)

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[Q2]	MIPS ISA [5 marks]		
		nction MOVZ which copies a sou b. For example, the instruction	arce register to a destination
MOVZ	2 \$8, \$11, \$4		
copies nothin		o register 8, only-if register 4 is a	zero (otherwise it does
1.		egular MIPS machine whose asse how MOVZ \$a, \$b, \$c can be in	<u> </u>
2.	_	would have used a branch instruine code of this branch instruction	
3.	instruction. A program P wh	nds the MIPS ISA by implement ile executing on M2, has 5% of e I1 and M2 have the same clock o aster and by what factor?	executed instructions as
4.	[1 mark] M2's clock speed is	s 2.1GHz. What is M1's clock sp	peed?

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[Q3]]	Pipelining [8 marks]		
indepe		on as above (except for the definition n). Machine M2 implements MOVZ on.	
1.	[2 marks] Suggest an appropriate drawing with justification.	oriate instruction format for MOVZ	\$a, \$b. \$c. Provide a
2.	[1 mark] In which stage of e line? Explain briefly.	execution does MOVZ need the Reg	Wr (Register Write) control
3.	[1 marks] At the end of which determined?	ch stage of MOVZ's execution can the	he RegWr line be
4.	the 'move' has an RAW deper	warding for the MOVZ instruction valuence on a previous instruction (con appropriate pipeline timing diagra	onsider <i>only</i> these instances

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[Q4] MIPS Assembly Language [7 marks]

Fill-in-the-blanks to complete the MIPS32 assembly translation of the given C code.

```
struct Complex {
                          # Code begins here; see assumptions given
 int re, im;
                            addi $s0, $s1, 0
struct Complex C1[], C2[];
int i, N, k;
// Some C code here
                          LOOP:
// which need not
                                   _____ # if i is out of C2's range
// be translated
                                # jump to OutOfBounds
for(i = k; i < N; i++) {
 C1[i] = C2[i];
                                _____ # if i is out of C1's range
                                     _____ # jump to OutOfBounds
# Assume:
# i in $s0, k in $s1
                            sll $t0, $s0, 3
# N in $s2
                                 $t2, $t0, $s4 # t2 is now &C2[i]
                            add
# C1 in $s3
                            add $t1, $t0, $s3 # t1 is now &C1[i]
# C1's length in $t3
                            # Next four lines achieve C1[i]=C2[i]
# C2 in $s4
                            # 1 mark each for next 4 lines
# C2's length in $t4
# Use other temporary
# regs as needed
# Assume int and
# pointers size = 1 word
                            addi $s0, $s0, 1 # i++
                          COMPARE:
                            slt $t0, $s0, $s2
                                     _____ # loop back as necessary
```

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[Q5] Majority Gate [1+1+1+2=5 marks]

Consider the following function: M(x, y, z) = xy + yz + xz. This is called a majority function/gate. This is because the function evaluates to 1(0) only if at least two of the 3 variables are 1(0). In this question, we shall be exploring the majority gates. Turns out that such majority functions have very interesting applications in nanotechnology-based circuits. Implement the following functions using only majority gates. You may use 0 or 1 as input where appropriate. You may also assume that where needed, the complemented input x of an input variable x is also available, in addition to x itself.

- 1. F(x) = x; use exactly one majority gate
- 2. F(x,y) = x+y; use exactly one majority gate
- 3. F(x,y) = xy; use exactly one majority gate
- 4. F(x,y,z) = xy' + y'z; use exactly two majority gates

[Q6] Dharavi and the "once-in-a-century" "pandemic" [optional, 10HP]

The official claim regarding Covid is that it was a highly transmissible, deadly, "once-in-a-century" "pandemic", overwhelming hospitals everywhere. The Dharavi slum is one of the densest and poorest places on earth, with poor access to healthcare. What percentage of people in Dharavi died of Covid? (The next time you meet someone from the working class, ask them whether they found the "pandemic" deadly as claimed).