CS230 DLDCA End-Sem, Tue 12 Nov 2024, 13.30-16.30, Max. Marks: 40

General instructions

- Write only in the space provided. Answer briefly but crisply (not lengthily or loosely).
- You are allowed to refer to your own hand-written notes only.
- Write neatly and clearly. Up to **+2 HP** for neat handwriting, neat/crisp answers.
- Answers generally have to be (briefly) explained. State any necessary assumptions.

[Q1] Short answer questions: [1x10=10 marks]

1. What real instruction(s) does the pseudo-instruction 'la' (load address) translate to?

2. MIPS has a convention as to which registers are caller saved versus which are callee saved. What is the need for such a convention?

3. Are RAW hazards in memory locations possible in the 5-stage MIPS pipeline? Explain.

4. State two reasons why cache memory is faster than main memory.

5. A 32-bit machine has 1GB of physical memory and a 4KB page size. What is the maximum index of an integer array a program can use in this machine? Assume sizeof(int) is 1 word.

6. State one use of virtual memory as a level of indirection.

7. Some machines have a TLB with a PID (process-ID) field. What is the purpose behind this?

8. State one advantage of having a long pipeline, i.e. a large number of stages

9. State one disadvantage of having a long pipeline, i.e. a large number of stages

10. What are the three kinds of bus lines?

[Q2] Majority Gate [1+1+1+2=5 marks]

Consider the following function: M (x, y, z) = xy + yz + xz. This is called a *majority* function/gate. This is because the function evaluates to 1(0) only if at least two of the 3 variables are 1(0). In this question, we shall be exploring the majority gates. Turns out that such majority functions have very interesting applications in nanotechnology-based circuits. Implement the following functions using only majority gates. You may use 0 or 1 as input where appropriate. You may also assume that where needed, the complemented input x' of an input variable x is also available, in addition to x itself.

1. F(x) = x ; use exactly one majority gate

2. F(x,y) = x+y ; use exactly one majority gate

3. F(x,y) = xy ; use exactly one majority gate

4. F(x,y,z) = xy' + y'z ; use exactly two majority gates

[Q3] MIPS ISA [5 marks]

Consider the conditional move instruction MOVZ which copies a source register to a destination register only if a third register is zero. For example, the instruction

MOVZ $8, $11, $4

copies the contents of register 11 into register 8, only-if register 4 is zero (otherwise it does nothing).

1. **[1 mark]** Machine M1 is a regular MIPS machine whose assembler implements MOVZ as a pseudo-instruction. Indicate how MOVZ $a, $b, $c can be implemented using real MIPS instruction(s).

2. **[1 mark]** Your answer above would have used a branch instruction. Give the 16-bit immediate value in the machine code of this branch instruction.

3. **[2 marks]** Machine M2 extends the MIPS ISA by implementing MOVZ as a real instruction. A program P while executing on M2, has 5% of executed instructions as MOVZ. For this program, M1 and M2 have the same MIPS (Millions of Instructions Per Second) rating and the same CPI. Which machine executes P faster and by what factor?

4. **[1 mark]** M2's clock speed is 2.1GHz. What is M1's clock speed?

[Q4] Pipelining [11 marks]

Consider the same MOVZ instruction as above (except for the definition of MOVZ, this question is independent of the previous question). Machine M2 implements MOVZ by minimally modifying the original 5-stage MIPS pipeline implementation.

1. **[2 marks]** Suggest an appropriate instruction format for MOVZ $a, $b. $c. Provide a drawing with justification.

2. **[1 mark]** In which stage of execution does MOVZ need the RegWr (Register Write) control line? Explain briefly.

3. **[1 marks]** At the end of which stage of MOVZ's execution can the RegWr line be determined?

4. **[3 marks]** Consider data forwarding for the MOVZ instruction when the source register of the 'move' has an RAW dependence on a previous instruction (consider *only* these instances of data forwarding). Draw an appropriate pipeline timing diagram to illustrate the possible scenarios of data forwarding. Draw also the datapath modifications necessary to support these scenarios of data forwarding.

5. **[3 marks]** Write the pseudo-micro-code logic to generate the control line(s) required for the above data forwarding. The logic should be written to execute in the dependent MOVZ's ID stage. You need to consider *only* register-register instructions as possible data producing instructions.

[Q5] Delay slot scheduling [4 marks]

Consider the same MOVZ instruction as above (except for the definition of MOVZ, this question is independent of the previous questions). Machine M2 implements MOVZ by extending the original 5-stage MIPS pipeline implementation. It has a 2-stage branch completion scheme. It also has a branch delay slot. Construct an example assembly language code snippet (a simple one) where MOVZ helps fill a branch delay slot which cannot be filled had there been no MOVZ in the instruction set.

[Q6] Paged page tables: 1+1+3=5 marks

A computer has a 32-bit VA space, and 64GB of main memory. Page table entries are of size 1 word, and the page size is 64KB. It uses a paged (or virtualized) page-table scheme. Answer the following questions.

1. What is the per-process page-table size (in VM) in this scheme ?

2. The OS stores page tables in a special process's VM, starting from virtual address 0x1000 0000. The page-table of process with PID *p* is in virtual address 0x1000 0000 + *p* * (PT size). Now, a process with PID 256 is running. What is the value of the page-table register (in hex format) ?

3. The page-table of the special OS process is pinned, starting from PA 0x 0 8000 0000. The process with PID 256 accesses VA 0x 0002 A804, which results in a TLB miss. What is the first physical address (express in hex format) accessed while handling this TLB miss? Assume all caches/TLB to be cold to begin with.

[Q7] Dharavi and the "once-in-a-century" "pandemic" [optional, 10HP]

The official claim regarding Covid is that it was a highly transmissible, deadly, "once-in-a-century" "pandemic", overwhelming hospitals everywhere. The Dharavi slum is one of the densest and poorest places on earth, with poor access to healthcare. What percentage of people in Dharavi died of Covid? (The next time you meet someone from the working class, ask them whether they found the "pandemic" deadly as claimed).