1. What will be the value of PCWr in stage3 of the beq instruction?

   (a) 0
   (b) 1
   (c) Don't care
   (d) zero?
   (e) (NOT zero?)

   Answer: (d)

2. Is the MDRWr control line needed? Why or why not?

   (a) MDRWr is needed: it should be enabled only in stg4 of lw
   (b) MDRWr is needed: it should be enabled only in stg4 of sw
   (c) MDRWr is implicit: it can be enabled in all stages for all instructions
   (d) MDRWr is implicit: it can be disabled in all stages for all instructions

   Answer: (c)

3. What had the earlier tables with the set of control lines in each stage of the execution plan specified?

   (a) The mapping from current state number to the next state number
   (b) The mapping from current state number to the control lines
   (c) The mapping from don't cares to control lines
   (d) The mapping from your palm lines to your destiny

   Answer: (b)

4. What can we give as input to implement our control logic as a state machine?

   (a) The program
   (b) The compiler
   (c) The opcode of the instruction
   (d) The immediate value in the instruction

   Answer: (c)

5. If we use a state machine to implement the control logic for the multi-cycle implementation, what will the output be?

   (a) The opcode
   (b) The next state
   (c) The next instruction
   (d) The control lines for the current stage of the current instruction

   Answer: (d)

6. Will the state machine to implement the control logic for the multi-cycle MIPS implementation, be a Moore machine or a Mealy machine?

   (a) Moore machine
   (b) Mealy machine
   (c) Both
   (d) Neither

   Answer: (b)