CS230 In-Video Quiz **Lecture 13**

1. Should the single cycle implementation be edge triggered or level triggered?

   (a) Edge triggered
   (b) Level triggered

   Answer: (b)

2. Can the data memory be written in the first half the cycle? Will this approach affect correctness? Will this approach affect efficiency?

   (a) It will affect neither efficiency nor correctness
   (b) It will affect efficiency but not correctness
   (c) It will affect correctness but not efficiency
   (d) It will affect both correctness and efficiency

   Answer: (b)

3. Which of j and lw necessarily requires a longer clock cycle?

   (a) j incurs a significantly longer delay than lw
   (b) lw incurs a significantly longer delay than j
   (c) Both instructions incur about the same delay

   Answer: (b)

4. What additional piece of information do you need to compare the performance of the single cycle implementation with the hypothetical variable-clock-cycle scenario?

   (a) The compiler used to produce the program
   (b) The assembler used to produce the program
   (c) The instruction mix of the program
   (d) The phase of the moon when the program was run

   Answer: (c)