1. What is the ideal CPI of a pipelined MIPS implementation?

   Answer: 1

2. A multi-cycle implementation has 9 ns cycle time. A pipelined implementation has 10 ns cycle time (due to extra datapath overheads). The instructions are a mix of 65% reg-reg, 15% `beq`, 15% `lw` and 5% `sw`.

   (a) What is the ideal speed-up?
   Answer: 3.6 ns

   (b) What is the speed-up with structural hazard in memory?
   Answer: 3 ns