

ARM Processor

Cortex[®]-A72 MPCore

Product Revision r0

Software Developers Errata Notice

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Software Developers Errata Notice

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- the document title
- the document number, ARM-EPM-012079
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Release Information

Errata are listed in this section if they are new to the document, or marked as “updated” if there has been any change to the erratum text in Chapter 2. Fixed errata are not shown as updated unless the erratum text has changed. The summary table in section 2.2 identifies errata that have been fixed in each product revision.

06 May 2016: Changes in Document v6

| Page | Status | ID | Cat | Rare | Summary of Erratum- |
|------|--------|--------|------|------|---|
| 21 | New | 856026 | CatC | | Trace on packets from ETM are not generated in specific conditions around System Error exceptions |

13 Jan 2016: Changes in Document v5

| Page | Status | ID | Cat | Rare | Summary of Erratum- |
|------|--------|--------|------|------|---|
| 8 | New | 853709 | CatB | | Writes to DACR32_EL2 in AArch64 state might not have desired effect on domain settings |
| 9 | New | 854173 | CatB | | Distributed Virtual Memory operations during hardware flush might cause deadlock |
| 19 | New | 852124 | CatC | | Trace On packets from ETM are not generated in specific conditions around Debug Halt exceptions |
| 20 | New | 854172 | CatC | | An external data snoop might cause data corruption when an Evict transaction is pending |

01 Sep 2015: Changes in Document v4

| Page | Status | ID | Cat | Rare | Summary of Erratum |
|------|--------|--------|------|------|--|
| 16 | New | 851022 | CatC | | Persistent evictions combined with interconnect backpressure might stall Write-Back No-Allocate stores |
| 17 | New | 852122 | CatC | | Direct branch instructions executed before a trace flush might be output in an atom packet after flush acknowledgement |
| 18 | New | 852123 | CatC | | Trace Context packet might not be output on a Reset or System Error exception |

05 Jun 2015: Changes in Document v3

| Page | Status | ID | Cat | Rare | Summary of Erratum |
|------|--------|--------|------|------|--|
| 13 | New | 848970 | CatC | | Data Synchronization Barrier might be stalled by a continuous stream of snoop transactions |
| 14 | New | 850321 | CatC | | ATB stall from trace subsystem might deadlock the processor |
| 15 | New | 850419 | CatC | | Cortex-A72 incorrectly allows access to GICv3 common registers in a specific configuration |

19 Feb 2015: Changes in Document v2

| Page | Status | ID | Cat | Rare | Summary of Erratum |
|------|---------|--------|------|------|--|
| 7 | Updated | 838569 | CatA | | DSB might be stalled by a steady stream of prefetch requests |
| 11 | New | 842569 | CatC | | Accesses to RAMINDEX system control register might return incorrect data |
| 12 | New | 843820 | CatC | | Syndrome value incorrect for software-induced Virtual Abort exception |

03 Dec 2014: Changes in Document v1

| Page | Status | ID | Cat | Rare | Summary of Erratum |
|------|--------|--------|------|------|--|
| 7 | New | 838569 | CatA | | DSB might be stalled by a steady stream of prefetch requests |

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Chapter 1.

Introduction

This chapter introduces the errata notice for the ARM Cortex-A72 processors.

1.1. Scope of this document

This document describes errata categorized by level of severity. Each description includes:

- the current status of the defect
- where the implementation deviates from the specification and the conditions under which erroneous behavior occurs
- the implications of the erratum with respect to typical applications
- the application and limitations of a ‘work-around’ where possible

This document describes errata that may impact anyone who is developing software that will run on implementations of this ARM product.

1.2. Categorization of errata

Errata recorded in this document are split into the following levels of severity:

Table 1 **Categorization of errata**

| Errata Type | Definition |
|------------------|--|
| Category A | A critical error. No workaround is available or workarounds are impactful. The error is likely to be common for many systems and applications. |
| Category A(rare) | A critical error. No workaround is available or workarounds are impactful. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage. |
| Category B | A significant error or a critical error with an acceptable workaround. The error is likely to be common for many systems and applications. |
| Category B(rare) | A significant error or a critical error with an acceptable workaround. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage. |
| Category C | A minor error. |

Chapter 2.

Errata Descriptions

2.1. Product Revision Status

The *mpn* identifier indicates the revision status of the product described in this book, where:

- mn*** Identifies the major revision of the product.
- pn*** Identifies the minor revision or modification status of the product.

2.2. Revisions Affected

Table 2 below lists the product revisions affected by each erratum. A cell marked with **X** indicates that the erratum affects the revision shown at the top of that column.

This document includes errata that affect revision r0 only.

Refer to the reference material supplied with your product to identify the revision of the IP.

Table 2

Revisions Affected

| ID | Cat | Rare | Summary of Erratum | r0p0 | r0p1 | r0p2 | r0m3 |
|--------|------|------|--|------|------|------|------|
| 838569 | CatA | | DSB might be stalled by a steady stream of prefetch requests | X | | | |
| 854173 | CatB | | Distributed Virtual Memory operations during hardware flush might cause deadlock | X | X | X | |
| 853709 | CatB | | Writes to DACR32_EL2 in AArch64 state might not have desired effect on domain settings | X | X | X | |
| 856026 | CatC | | Trace on packets from ETM are not generated in specific conditions around System Error exceptions | X | X | X | X |
| 854172 | CatC | | An external data snoop might cause data corruption when an Evict transaction is pending | X | X | X | X |
| 852124 | CatC | | Trace On packets from ETM are not generated in specific conditions around Debug Halt exceptions | X | X | X | |
| 852123 | CatC | | Trace Context packet might not be output on a Reset or System Error exception | X | X | X | |
| 852122 | CatC | | Direct branch instructions executed before a trace flush might be output in an atom packet after flush acknowledgement | X | X | X | |
| 851022 | CatC | | Persistent evictions combined with interconnect backpressure might stall Write-Back No-Allocate stores | X | X | X | X |
| 850419 | CatC | | Cortex-A72 incorrectly allows access to GICv3 common registers in a specific configuration | X | X | | |
| 850321 | CatC | | ATB stall from trace subsystem might deadlock the processor | X | X | X | X |
| 848970 | CatC | | Data Synchronization Barrier might be stalled by a continuous stream of snoop transactions | X | X | | |
| 843820 | CatC | | Syndrome value incorrect for software-induced Virtual Abort exception | X | | | |
| 842569 | CatC | | Accesses to RAMINDEX system control register might return incorrect data | X | | | |

2.3. Category A

838569: DSB might be stalled by a steady stream of prefetch requests

Category A

Products Affected: Cortex-A72 MPCORE.

Present in: r0p0

Description

A DSB following a TLB maintenance instruction executed on processor (PROC1) might be stalled by one or more other processors (PROCn) if the software executing on PROCn repeatedly activates the L1 hardware prefetcher. The L1 hardware prefetch requests must be presented to the L2 cache with specific timing and must win arbitration in a cluster of Cortex-A72 processors waiting to respond to the DSB completion request. If these prefetch requests occur repeatedly, with the correct timing, it is possible for the DSB completion to be stalled indefinitely.

Note: This erratum corresponds to issue #283 in the ARM internal tracking system.

Configurations affected

Systems with multiple processors.

Conditions

- 1) An ARM processor (PROC1) executes a TLB maintenance instruction followed by a DSB instruction.
- 2) One or more Cortex-A72 processors (PROCn) are running software that generates L1 hardware prefetches in a Cortex-A72 cluster that is trying to respond to the DSB completion request. Note that PROC1 and PROCn do not have to be in the same cluster.
- 3) The PROCn processors continuously execute instruction sequences that generate L1 hardware prefetch requests.
- 4) These prefetch requests arrive and win arbitration in the L2 cache before all existing outstanding prefetch operations have time to complete.

Implications

If the above conditions are met, the DSB instruction executing on PROC1 will be stalled until the continuous stream of prefetch requests stops.

Workaround

There is no workaround.

2.4. Category A (Rare)

There are no errata in this category.

2.5. Category B

853709: Writes to DACR32_EL2 in AArch64 state might not have desired effect on domain settings

Category B

Products Affected: Cortex-A72 MPCORE.

Present in: r0p0, r0p1, r0p2

Description

AArch32 memory domain access permissions are controlled by the DACR register. This register is accessible in AArch64 state by reading or writing the DACR32_EL2 register. If a Cortex-A72 processor attempts to write the DACR in AArch64 state using the DACR32_EL2 register, the updated register settings might not be seen by the processor.

Note: This erratum corresponds to issue #345 in the ARM internal tracking system.

Configurations affected

Systems running a hypervisor in EL2 in AArch64 state with AArch32 guests that use short-descriptor translation table format and domains to control access to pages.

Conditions

- 1) The hypervisor writes the DACR by writing to DACR32_EL2 before returning to an AArch32 guest.
- 2) The hypervisor does not write any other SPRs related to memory management, including SCTLR_EL1, TCR_EL1, TTBR0_EL1, TTBR1_EL1, or CONTEXTIDR_EL1 within the same bounds of context synchronizing events (such as an ISB).

Implications

If the above conditions are met, the Cortex-A72 processor might not properly use the updated DACR written by the hypervisor. This might result in spurious domain faults in the guest O/S, or possibly allow EL0 processes in the guest O/S access to the operating system privileged data or code.

Workaround

The hypervisor code in EL2 should write one or more of SCTLR_EL1, TCR_EL1, TTBR0_EL1, TTBR1_EL1, or CONTEXTIDR_EL1 after the write of DACR32_EL2.

854173: Distributed Virtual Memory operations during hardware flush might cause deadlock or data corruption**Category B****Products Affected: Cortex-A72 MPCORE.****Present in: r0p0, r0p1, r0p2****Description**

During execution of L2 hardware cache flush, as part of the powerdown sequence, Distributed Virtual Memory (DVM) operations received by the Cortex-A72 processor might be dropped leading to a deadlock or data corruption.

Note: This erratum corresponds to issue #358 in the ARM internal tracking system.

Configurations affected

All configurations are affected.

Conditions

- 1) L2 hardware cache flush is initiated following the powerdown sequence in the Cortex-A72 Technical Reference Manual by asserting L2FLUSHREQ.
- 2) During the L2 hardware cache flush sequence, the Cortex-A72 processor receives external DVM operations.
- 3) The L2 Fill Evict Queue (FEQ) becomes completely full with L2 hardware cache flush transactions or external DVM operations.
- 4) Very specific timing, so an L2 hardware cache flush transaction is allocated to a particular FEQ entry in the same cycle that another FEQ entry is deallocated.
- 5) DVM operation is later allocated to the last entry in the FEQ, causing the FEQ to be completely full.

Implications

If the above conditions are met, the Cortex-A72 processor drops the external DVM operation in step 5). This might cause data corruption for subsequent snoops and prevents the powerdown sequence from completing, because the Cortex-A72 processor does not respond to all the external DVM operations, and the system will deadlock.

Workaround

The workaround for this erratum applies only to the power management software, which in some cases is running on a system control processor (SCP), for the powering down of the Cluster and the L2 caches.

- 1) The preferred workaround involves the modification of the power management software running on the SCP using the L2 hardware cache flush mechanism as described in the ARM Cortex-A72 MPCore Processor Technical Reference Manual (rev0.2) section "Processor powerdown with system driven L2 flush". This mechanism involves using an implementation defined mechanism within the SoC to drive the signals L2FLUSHREQ and either ACINACTM or SINACT. In order to work around this erratum, while still using this mechanism, the power management software must be able to disable DVM operations before the SoC assertion of L2FLUSHREQ (step 6 of documented sequence) separately from disabling snoop requests (which is typically done by the management software between steps 8 and 9 of the documented sequence by writing to a register within the SoC level interconnect). For the ARM implemented interconnects, the following approaches are used:
 - a. For CCI-400/500/550 based ACE interconnect systems, the power management software must program the Snoop Control Register (snoop_ctrl) to disable DVM operations to the Cortex-A72 processor and poll the Status Register to confirm changes to the Snoop Control Register have taken effect, just before step 6, where the SoC asserts L2FLUSHREQ. After step 8, where L2FLUSHDONE is asserted by the Cortex-A72, program the Snoop Control Register to disable snoop requests and poll the Status Register to confirm changes have taken effect before asserting ACINACTM (this operation is required even without the errata workaround, but would also have including the disabling of DVM operations at this point).. Please refer to the appropriate CCI documentation for disabling snoops and DVM operations

- b. For CCN-based AMBA 5 CHI interconnect systems, the power management software must write to the DVM Domain Control Clear Register (DDCR_Clear) to disable DVM operations to the Cortex-A72 processor and poll the DVM Domain Control Register (DDCR) to confirm changes to the DDCR have taken effect, just before step 6 where the SoC asserts L2FLUSHREQ. After step 8, where L2FLUSHDONE is asserted by the Cortex-A72, program the Snoop Domain Control Clear Register (SDCR_clear) to disable snoops and poll the Snoop Domain Control Register (SDCR) to confirm changes to the SDCR have taken effect (this operation is required even without the errata workaround but would also have including the disabling of DVMs at this point). Please refer to the appropriate CCN documentation for disabling snoops and DVM operations.

The steps required for power management operations are described in more detail in the ARM Power Control System Architecture v1.0 (ARM DEN 0050B).

- 2) If the SoC is such that DVM operations cannot be disabled independently from disabling snoops by power management software, then the caches must be cleaned and invalidated by software running the Cortex-A72 core as part of the power management software, following the steps in the Cortex-A72 MPCore Technical Reference Manual section “Processor powerdown without system driven L2 flush” using data or unified cache line clean and invalidate by set/way instructions (DCCISW) to clean and invalidate all data from the L2 data cache.

2.6. Category B (Rare)

There are no errata in this category.

2.7. Category C

842569: Accesses to RAMINDEX system control register might return incorrect data

Category C

Products Affected: Cortex-A72 MPCORE.

Present in: r0p0

Description

When reading the L1 instruction data array using the RAMINDEX register, the returned data should always be either 0x0, or the contents of a single RAM entry. However, if Debug state is entered while a table walk is occurring, and the L1 instruction data array is read before the table walk completes, the data returned might be incorrect.

Note: This erratum corresponds to issue #293 in the ARM internal tracking system.

Configurations affected

All configurations are affected.

Conditions

- 1) MMU is enabled.
- 2) An L1-I TLB miss occurs, causing a table walk.
- 3) Debug state is entered after the L1-I TLB miss but before the associated table walk completes.
- 4) A RAMINDEX operation is performed targeting the L1 instruction data array.

Implications

If the above conditions are met, the data read from the RAMINDEX operation might be incorrect.

Workaround

In Debug state, before writing the RAMINDEX register, disable the MMU by writing SCTL_R_ELx.M = 0 where ELx is the exception level the RAMINDEX operation is performed at.

843820: Syndrome value incorrect for software-induced Virtual Abort exception**Category C****Products Affected: Cortex-A72 MPCORE.****Present in: r0p0****Description**

If a 32-bit hypervisor injects a virtual abort into a guest operating system by writing HCR.VA=1'b1, the DFSR syndrome value will be incorrect. The abort is correctly taken, but the DFSR will not provide correct information on what caused the asynchronous abort.

Note: This erratum corresponds to issue #297 in the ARM internal tracking system.

Configurations affected

Cortex-A72 systems with EL2 implemented and using AArch32.

Conditions

- 1) HCR.AMO is programmed to 1'b1, enabling virtual exceptions.
- 2) HCR.VA is programmed to 1'b1 to generate a virtual asynchronous abort.
- 3) An exception return is performed to Non-secure EL1.

Implications

If the above conditions occur, a virtual asynchronous abort will be correctly taken, but the DFSR syndrome value will be all zeroes, which is incorrect. This erratum is not expected to impact any existing systems. It requires a 32-bit hypervisor using virtual asynchronous aborts to generate exceptions in guest operating systems. There is no known hypervisor for Cortex-A72 that meets these conditions. Also, even if utilized, a virtual asynchronous abort of this type would be a fatal error, making the syndrome not helpful in system recovery.

Workaround

No workaround is required.

848970: Data Synchronization Barrier might be stalled by a continuous stream of snoop transactions**Category C****Products Affected: Cortex-A72 MPCORE.****Present in: r0p0, r0p1****Description**

A core in a Cortex-A72 cluster executing a Data Synchronization Barrier (DSB) operation might be stalled by a continuous stream of snoop transactions to any core in the cluster. The Cortex-A72 waits for all outstanding snoop transactions in the cluster to finish before completing a DSB operation. If a pattern forms where new snoop transactions are continuously issued before existing snoop transactions complete, DSB completion will stall until there is a break in snoop activity.

Note: This erratum corresponds to issue #312 in the ARM internal tracking system.

Configurations affected

All configurations are affected.

Conditions

- 1) A core (CORE1) in a Cortex-A72 cluster executes a Data Synchronization Barrier (DSB) operation. An operation occurred since the last DSB that requires synchronization (that is, a TLB maintenance, IC invalidate, or brand predictor invalidate operation). If none occurred, the hardware optimizes the DSB and does not actually perform a synchronization.
- 2) A continuous stream of snoop transactions is processed by the shared L2 memory subsystem. These snoop requests can come from other cores in the cluster, or from outside the cluster on the external snoop request interface (AC Channel in AMBA 4 ACE configurations or RXSNP channel in AMBA 5 CHI configurations).
- 3) Specific latency and timing of snoop transactions such that there is always a new snoop transaction issued before existing snoop transactions complete.

Implications

If the above conditions are met, the DSB executing on CORE1 will stall until a period when all outstanding snoop transactions are complete and no new snoop transactions are pending. This erratum is not expected to impact typical systems, but malicious code could be written to exploit this in a denial of service attempt.

Workaround

A denial of service can be avoided if a timer-based interrupt source is used to interrupt all snoop generating masters periodically.

850321: ATB stall from trace subsystem might deadlock the processor**Category C****Products Affected: Cortex-A72 MPCORE.****Present in: r0p0, r0p1, r0p2, r0p3****Description**

A processor can use the Wait for Event (WFE) or Wait for Interrupt (WFI) mechanism to enter low-power state. A processor can enter low-power state only after the Embedded Trace Macrocell (ETM) drains all trace bytes on the AMBA ATB interface. Under certain conditions an AMBA ATB stall can cause the processor to hang until the AMBA ATB stall condition is cleared. Some trace subsystems might require instructions to be executed on the processor to clear the AMBA ATB stall condition. An example of such trace subsystems involves draining the trace to the memory subsystem via an SMMU. A processor deadlock might occur when such trace subsystems are used.

Note: This erratum corresponds to issue #318 in the ARM internal tracking system.

Configurations affected

All configurations are affected.

Conditions

- 1) Trace subsystem requires instructions to be executed on the processor to clear an AMBA ATB stall condition.
- 2) The ETM is enabled.
- 3) The processor is executing a WFI or WFE instruction.
- 4) The ETM is unable to drain trace data as a trace stall is continuously asserted.

Implications

An interrupt might be raised in order to execute instructions on the processor to relieve the trace stall condition. This erratum means that the interrupt will not be taken and therefore a processor deadlock will occur.

Workaround

Ensure that the trace subsystem does not have interlock with software for draining the trace bytes.

850419: Cortex-A72 incorrectly allows access to GICv3 common registers in a specific configuration**Category C****Products Affected: Cortex-A72 MPCORE.****Present in: r0p0, r0p1****Description**

If the Cortex-A72 internal GIC CPU interface is enabled and configured in system register mode, a specific access to one of the GICv3 common registers with ICH_HCR_EL2.TC=1 might incorrectly allow an access when an UNDEFINED exception or Monitor Trap should have been taken. ICH_HCR_EL2.TC=1 should not have any effect on GICv3 common register accesses in EL1S or EL2.

Note: This erratum corresponds to issue #319 in the ARM internal tracking system.

Configurations Affected

Systems implementing EL1, EL2 and EL3, and the external pin GICCDISABLE=0 (that is, Internal GIC CPU interface is enabled).

Conditions

- 1) Operating in System Register enabled mode, which has the system registers enabled for the current exception level.
- 2) Operating in exception level EL1S or EL2.
- 3) ICH_HCR_EL2.TC=1.
- 4) SCR_EL3.FIQ=1.
- 5) SCR_EL3.IRQ=1.
- 6) Read or write to one of the GICv3 common registers occurs. GICv3 common registers include: ICC_SGI0R_EL1, ICC_SGI1R_EL1, ICC_ASGI1R_EL1, ICC_CTLR_EL1, ICC_DIR_EL1, ICC_PMR_EL1, and ICC_RPR_EL1.

Implications

If EL3 is using AArch64, and the above conditions occur, a Monitor Trap exception should be taken because SCR_EL3.FIQ=1 and SCR_EL3.IRQ=1. If EL3 is using AArch32, an UNDEFINED exception should be taken. However, because of this erratum, the access is allowed.

Workaround

There is no workaround.

851022: Persistent evictions combined with interconnect backpressure might stall Write-Back No-Allocate stores**Category C****Products Affected: Cortex-A72 MPCORE.****Present in: r0p0, rop1, r0p2, r0p3****Description**

In a coherent ACE system, a Write-Back No-Allocate (WBNA) store might be stalled if WriteUnique/WriteLineUnique (WU/WLU) transactions are enabled and the store is attempted when one or more cache evictions are pending. ACE requires that WU/WLU transactions do not bypass any outstanding evict type transactions (WriteBack/WriteEvict/WriteClean). To satisfy this requirement, a microarchitectural hazard is used to force a replay if a WU/WLU transaction is attempted when an eviction is pending. In rare scenarios with a persistent stream of L2 cache linefills and associated evictions, combined with significant backpressure in the interconnect, and with specific timing, it is possible for a WBNA store to be stalled indefinitely.

Note: This erratum corresponds to issue #327 in the ARM internal tracking system.

Configurations affected

Coherent ACE systems that enable WriteUnique/WriteLineUnique transactions.

Conditions

- 1) WriteUnique/WriteLineUnique transactions are enabled by changing the default value of L2ACTLR[4] and setting it to 1'b0.
- 2) A Cortex-A72 processor issues a Write-Back No-Allocate store (OP1). This can be a streaming store that was downgraded to Write-Back No-Allocate by the processor.
- 3) There is a pending eviction, forcing (OP1) to stall because of ACE requirements that require outstanding evictions to complete before WriteUnique/WriteLineUnique stores are performed.
- 4) A continuous stream of L2 cache linefills occurs, from other cores and/or prefetch, which triggers new evictions.
- 5) There is significant sustained backpressure in the interconnect, which keeps the system backed up and the ACE write channel queue near full.
- 6) Specific arbitration and timing conditions exist which, when combined with condition 5), trigger a microarchitectural hazard that causes condition 3) to repeat.

Implications

If the above conditions are met, (OP1) will stall until the specific timing conditions and backpressure in the L2 subsystem are relieved. Interrupts and barriers after the Write-Back No-Allocate store are also delayed until the store completes. The conditions for this erratum are rare and not expected to significantly impact real system performance. Additionally, most systems perform better when the reset value for L2ACTLR[4] is used and WriteUnique/WriteLineUnique transactions are disabled.

Workaround

If WriteUnique/WriteLineUnique transactions are not required, disable them by setting L2ACTLR[4] = 1'b1. This is the reset value. Otherwise, set L2ACTLR[7] = 1'b1 to enable L2 hazard detection timeout. This will force the L2 cache to periodically re-evaluate hazards, at which point the stall will be released.

852122: Direct branch instructions executed before a trace flush might be output in an atom packet after flush acknowledgement**Category C****Products Affected: Cortex-A72 MPCORE.****Present in: r0p0, r0p1, r0p2****Description**

The Embedded Trace Macrocell (ETMv4) architecture requires that when a trace flush is requested on the AMBA Trace Bus (ATB), a processor must complete any packets that are in the process of being encoded and output them prior to acknowledging the flush request. When trace is enabled, the Cortex-A72 processor attempts to combine multiple direct branch instructions into a single Atom packet. If a direct branch instruction is executed, and an Atom packet is in the process of being generated, Cortex-A72 does not force completion of the packet prior to acknowledging the flush request. This is a violation of the ETMv4 architecture.

Note: This erratum corresponds to issue #330 in the ARM internal tracking system.

Configurations affected

All configurations are affected.

Conditions

- 1) ETM is enabled.
- 2) Instruction tracing is active.
- 3) One or more direct branch instructions are executed.
- 4) An Atom packet is being encoded but is not complete.
- 5) A trace flush is requested on the AMBA ATB.

Implications

When the above conditions occur, the Atom packet being encoded should complete and be output prior to the trace flush request being acknowledged. Because of this erratum, the Atom packet is output after the flush is acknowledged. Therefore, it will appear to software monitoring the trace that the direct branch was executed after that requested flush.

Workaround

Enabling the timestamp by setting TRCCONFIGR.TS will solve the issue as it will complete the atom packets through the timestamp behavior.

852123: Trace Context packet might not be output on a Reset or System Error exception**Category C****Products Affected: Cortex-A72 MPCORE.****Present in: r0p0, r0p1, r0p2****Description**

In some scenarios, Cortex-A72 might not output a Context packet for the handler of the exception over the AMBA Trace Bus (ATB) when a reset exception or System Error exception causes an Exception level change. In all scenarios, the required Trace on, Exception, and Address trace packets are properly encoded and output.

Note: This erratum corresponds to issue #331 in the ARM internal tracking system.

Configurations Affected

All configurations are affected.

Conditions

The ETM is enabled but not currently active.

- 1) CID and VMID tracing is off (TRCCIDCCTLR0 is 0x0).
- 2) Reset exceptions are always traced (TRCVICTRL.TRCRESET = 1 or TRCVICTRL.TRCERROR = 1).
- 3) Exception level changes on a reset or System Error.
- 4) Tracing continues at handler.

Implications

If the above conditions occur, a Context packet is not output on AMBA ATB, as required by the architecture. For the reset exception, software can assume that the Exception level will always change to EL3 coming out of reset. A System Error might be routed to different Exception levels, so it would require software to query processor configuration registers bits to determine the Exception level for the context change.

Workaround

Enable CID and VMID tracing.

852124: Trace On packets from ETM are not generated in specific conditions around Debug Halt exceptions**Category C****Products Affected: Cortex-A72 MPCORE.****Present in: r0p0, r0p1, r0p2****Description**

The processor might not output a Trace On packet in certain conditions surrounding Debug state. Specifically, a Trace On packet is not output when the processor generates a Debug Halt exception element that is traced followed by another exception element. The processor does generate the exception, address, and Context packets for this case.

Also, a Trace On packet is not output when the processor activates trace directly before a Debug Halt exception element wherein that debug entry is a P0 element that should be traced. The processor does generate the exception, address, and Context packets for this case.

Note: This erratum corresponds to issue #333 in the ARM internal tracking system.

Configurations affected

All configurations are affected.

Conditions

Condition Set A

- 1) ETM is enabled.
- 2) The core halts and a Debug Halt exception is traced.
- 3) a) An exception occurs on the first instruction after leaving Debug state.
- 4) b) A processor warm reset occurs while in Debug state.

Or

Condition Set B

- 1) ETM is enabled.
- 2) The core halts but the Debug Halt exception is not traced because tracing is inactive.
- 3) On exit from Debug state, one or more instructions are executed and are traced.
- 4) The core halts again, resulting in a Debug Halt exception being traced

Implications

If Condition Set A occurs, then a Trace On packet is not output after the Debug state exit, before the new exception is traced. The target address and context of the Debug state exit is traced correctly, as is the exception from step 3a or 3b. The missing Trace On element means that a trace analyzer might not highlight a gap in the trace, however this can be inferred by the trace analyzer because the Debug Halt exception is traced.

Or

If Condition Set B occurs, then a Trace On packet is not output before the first traced instruction out of Debug state at step 3. The target address and context are output correctly for the first instruction that is traced. The missing Trace On element means that a trace analyzer will not highlight the gap in the trace for the execution that was not traced before entering Debug state.

Workaround

For Condition Set A, a trace analyzer might be able to infer the Trace On packet because the Debug Halt exception is traced.

For both sets of conditions, a workaround is to disable and re-enable the ETM while the core is in Debug state.

854172: An external data snoop might cause data corruption when an Evict transaction is pending**Category C****Products Affected: Cortex-A72 MPCORE.****Present in: r0p0, r0p1, r0p2, r0p3****Description**

If the Cortex-A72 is configured to send Evict transactions for a cache line in UniqueClean (UC) state, then the Cortex-A72 might return stale data on a snoop response.

Note: This erratum corresponds to issue #357 in the ARM internal tracking system.

Configurations affected

Systems using a non-ARM CHI-based interconnect that implement a snoop filter that can track cache lines with SharedClean (SC) state to the precise CPU cluster. CCN-5xx ARM implementations are not affected by this erratum.

Conditions

- 1) The Cortex-A72 is configured not to send data for UC evictions. This is accomplished by setting the value of L2ACTLR[14] to 1'b0. The default value of this bit is 1'b1.
- 2) The Cortex-A72 is configured to push dataless Evict transactions to the external world. This is accomplished by setting the value of L2ACTLR[3] to 1'b0. The default value of this bit is 1'b1.
- 3) The Cortex-A72 issues a dataless Evict transaction (one of SnpClean, SnpShared, and SnpUnique transactions) for a cache line in UC state.
- 4) The Cortex-A72 issues an Evict transaction and is waiting for a completion response (COMP) from the interconnect.
- 5) The interconnect issues a COMP followed by a snoop request to the same cache line address.
- 6) The Cortex-A72 receives the snoop request before the COMP because of a race condition in the interconnect.

Implications

If the above conditions are met, there is a possibility of data corruption.

Workaround

There are multiple workarounds:

- 1) Configure the Cortex-A72 to send data for UC evictions. This can be accomplished by setting L2ACTLR[14] to 1'b1.
- Or
- 2) Configure the Cortex-A72 to not push Clean/Evict transactions to the external world. This can be accomplished by setting L2ACTLR[3] to 1'b1.

856026: Trace on packets from ETM are not generated in specific conditions around System Error exceptions**Category C****Products Affected: Cortex-A72 MPCORE.****Present in: r0p0, r0p1, r0p2, r0p3****Description**

The processor might not output a Trace On packet in certain conditions surrounding System Error exception. Specifically, a Trace On packet is not output when the processor generates an asynchronous System Error exception element that is traced on a specific corner case while the trace is becoming active. The processor does generate the exception packet for this case.

Note: This erratum corresponds to issue #367 in the ARM internal tracking system.

Configurations affected

All configurations are affected.

Conditions

- 1) The ETM is enabled.
- 2) Trace becomes active through trace_force_active_excep_t2.
- 3) System Error exception packet asserted between the T3 and T4 stages in trace RTL.

Implications

A Trace On packet is not output for the exception packet. The exception packet is output correctly. The missing Trace On element means that a trace analyzer might not highlight the gap in the trace for the execution. Thus, a trace decompressor might incorrectly attribute a longer continuous stream. This should be a rare usage model, and there should be no serious effect if this erratum is encountered.

Workaround

Only trace exceptions. Such a workaround would require other features to be turned off in order to capture this issue.