Project Report : Write Configuration Logic

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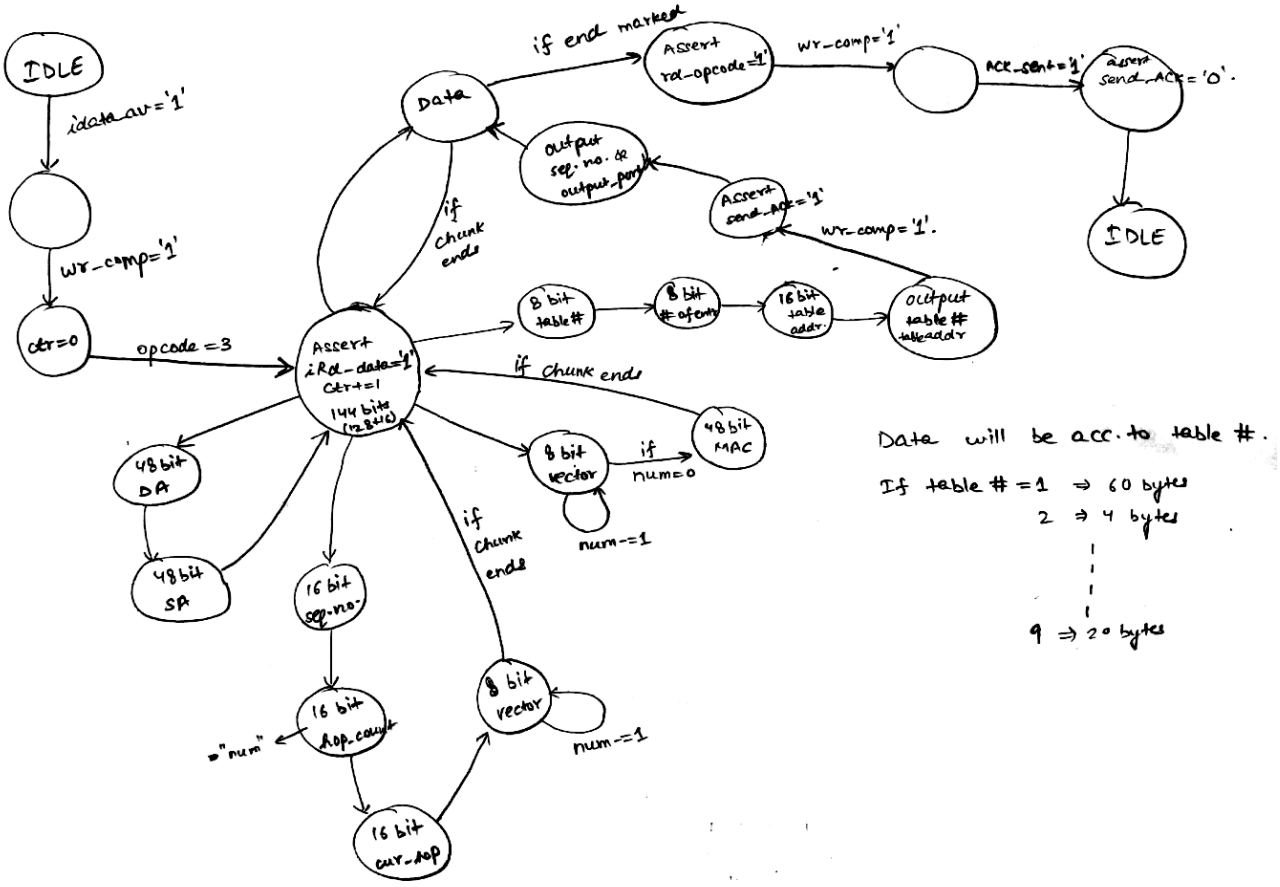
State Diagram



State Description and Transitions

- IDLE State : This is the initial state of the state machine. On reading iData_av = '1' the state changes to WAITING_FOR_OPCODE state.
- WAITING_FOR_OPCODE : In this state, it waits till Wr_complete = '1'. This means that the remote machine has completed writing to the registers.
- READY : This is the state where the packet reading is started and the required data is extracted from the packet . On Opcode = "011", it changes to next state. The packet reading happens in multiple states starting with Reading_H1.
- READING_H1 state : It extracts DA(48 bits), SA(48), Ether Type(16) and Ether value(16) from data.
- READING_H2 state : It extracts Sequence no.(32 bits), hop count(16 bits), current hop(16 bits) and then path_info which is equal to the number represented by hop count bytes.
- INCOMP_PATH_INFO : This state represents that previous 144 bit chunk did not contain complete path info and this chunk contains some of the remaining path info. Extracts path info from the packet.
  If path info is completed in the current chunk, it proceeds to read MAC and other fields that the packet contains.
  If the path info is distributed in multiple 144 bit chunks, then it stays in this state until the whole of the path info is read then moves to read MAC.
- INCOMP_MAC : This state represents that previous 144 bit chunk did not contain complete MAC and this chunk contains some of the remaining MAC address. This state reads the MAC data and other fields from the incoming packet and moves to next state accordingly.

- TAB_NUM : This state represents that first part of the 144 bit chunk is Table number. It reads the table number and other fields from the packet, sends this data to the output port and moves to next state accordingly.
- INCOMP_TAB_ADDR : This states assigns the rest of table_addr which is of 2 bytes.
- PURE_DATA : This state reads data and assigns appropriate value to write_data until it is read completely.
- WR_COMP : In this state, it waits until Wr-complete is '1' and then wr_ack is sent at the output port and moves to WR_ACK state.
- WR_ACK : In this state, the router waits of ACK and if Ack_sent is assigned, then wr_ack is set to 0 and state becomes IDLE.

Synthesise Report

Summary:
inferred 4 RAM(s).
inferred 28 Adder/Subtractor(s).
inferred 4 D-type flip-flop(s).
inferred 1112 Latch(s).
inferred 10 Comparator(s).
inferred 54497 Multiplexer(s).
Maximum combinational path delay: **4.912 ns**

Timing Diagram