CS 231 - DLDCA Lab

Lab Assignment 4

Part 2

Report

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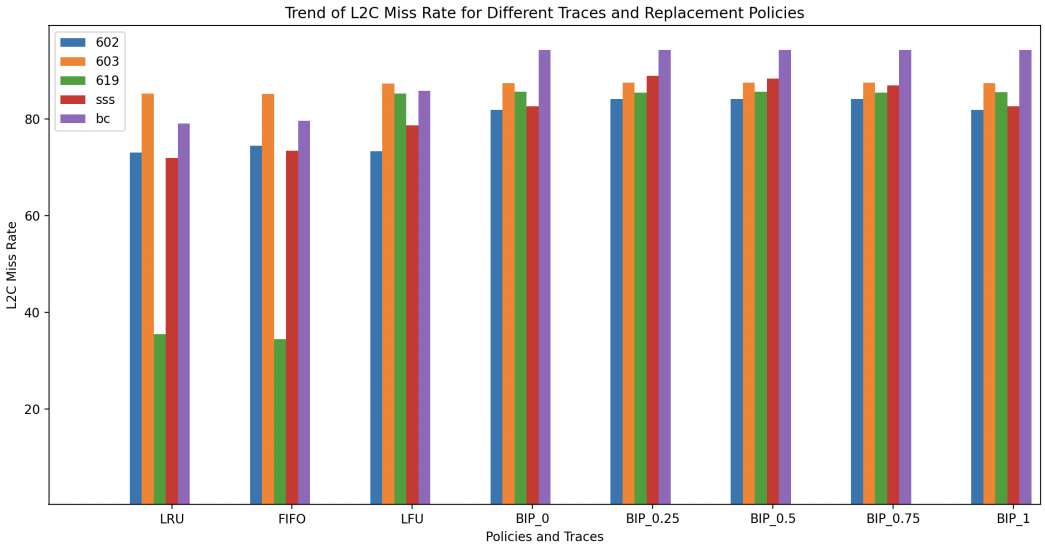
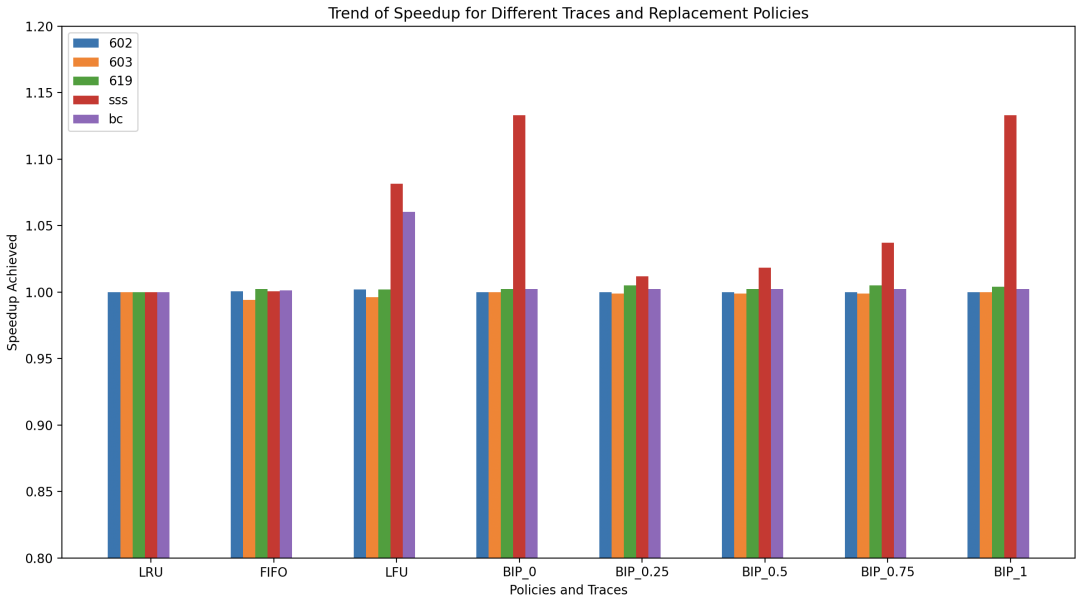
Lab 4.2.1: Replacement Policies

In this lab we implemented various cache replacement policies and tested them using the simulator **Champsim**.
The following graphs show the performance of the different policies viz. **FIFO, LFU** and **BIP** with respect to the **LRU** replacement policy. We compare their **Speedup** and **L2C Cache Miss Rate**.





Explanation:

L2C Miss Rate:

There is more variation in the L2C miss rate unlike the speedup as seen in the graph. This can be attributed to the trace files. The trace files have different **memory access patterns** and **data locality** which give different miss rates. Traces having **predictable access patterns** and more **temporal or spatial locality** tend to have **lower miss rates**. Workloads involving **higher data dependencies**, i.e. in which the future computation depends on the previous values tend to have **more misses**.
It also depends on the **replacement policy**. As we can see LRU generally has lower miss rate than the other policies whereas BIP tends to have miss rates on the higher side.

Speedup:

There is not much variation in the speedup except a few outliers which are observed in the sssp-3.trace.gz file. This may happen because the **bottleneck** is something other than cache. The **CPU** or the **memory** could be the limiting factor, in which case the cache replacement policy doesn't affect much because the cache is not a major factor in the latency of the system.