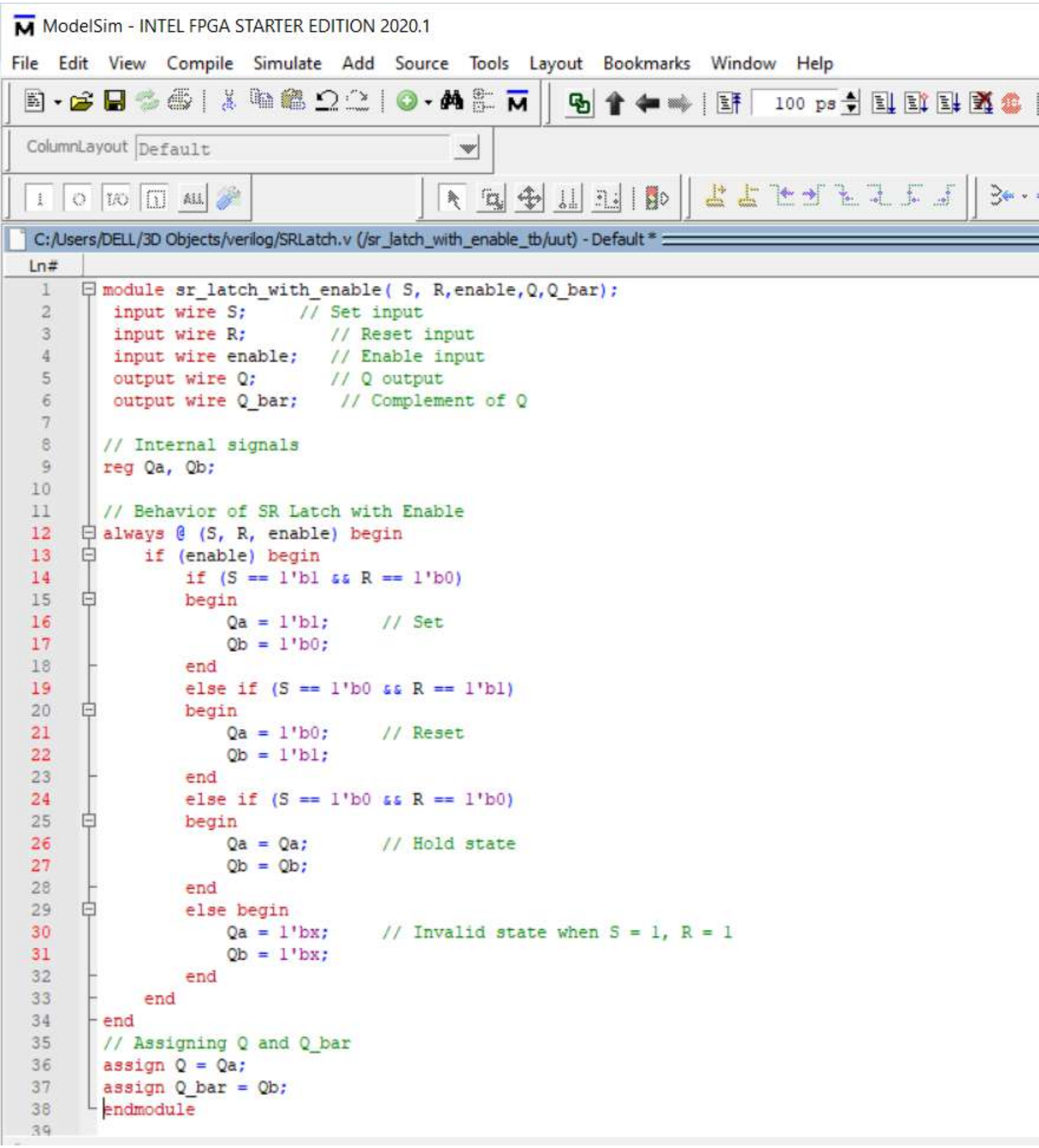
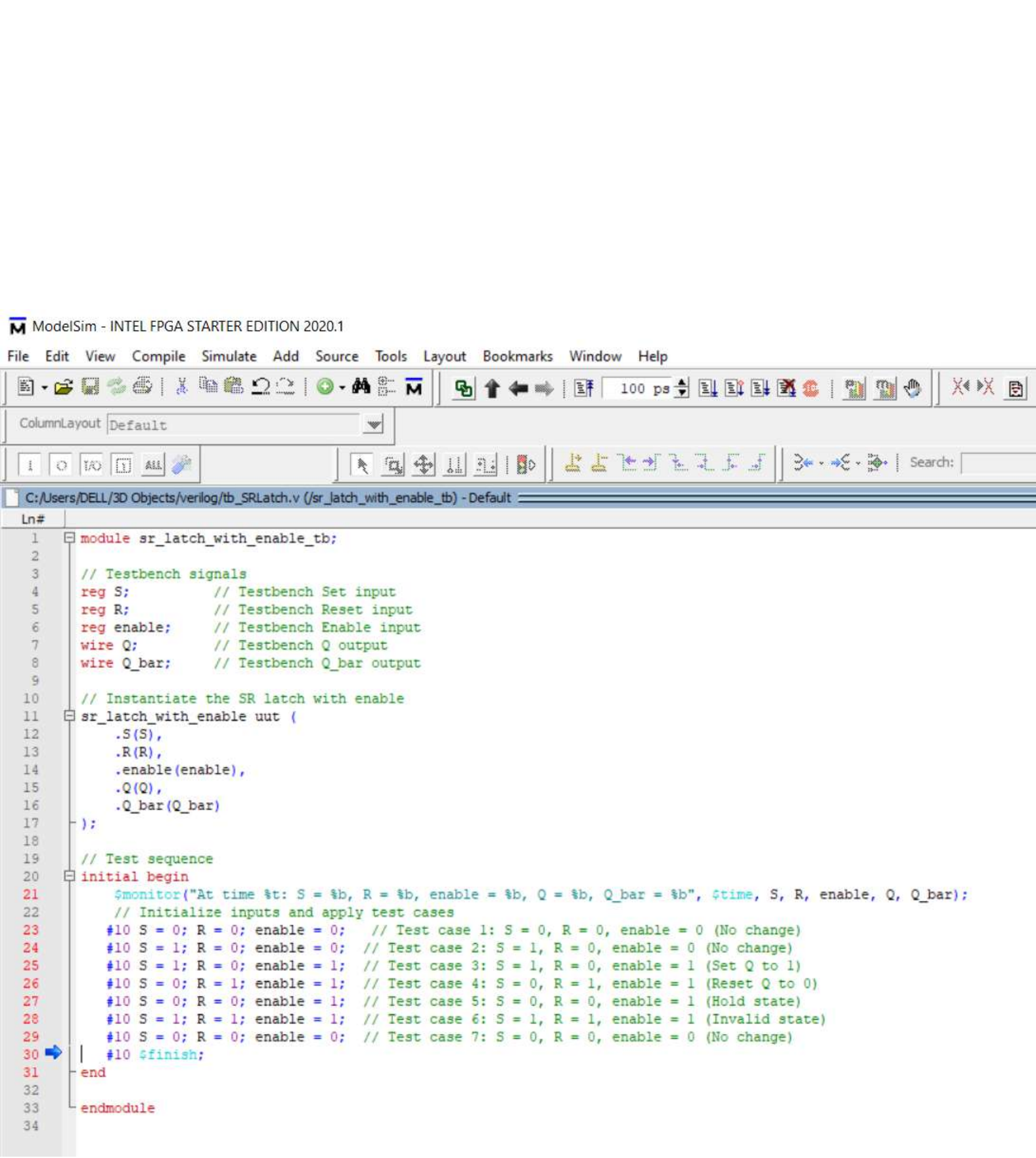
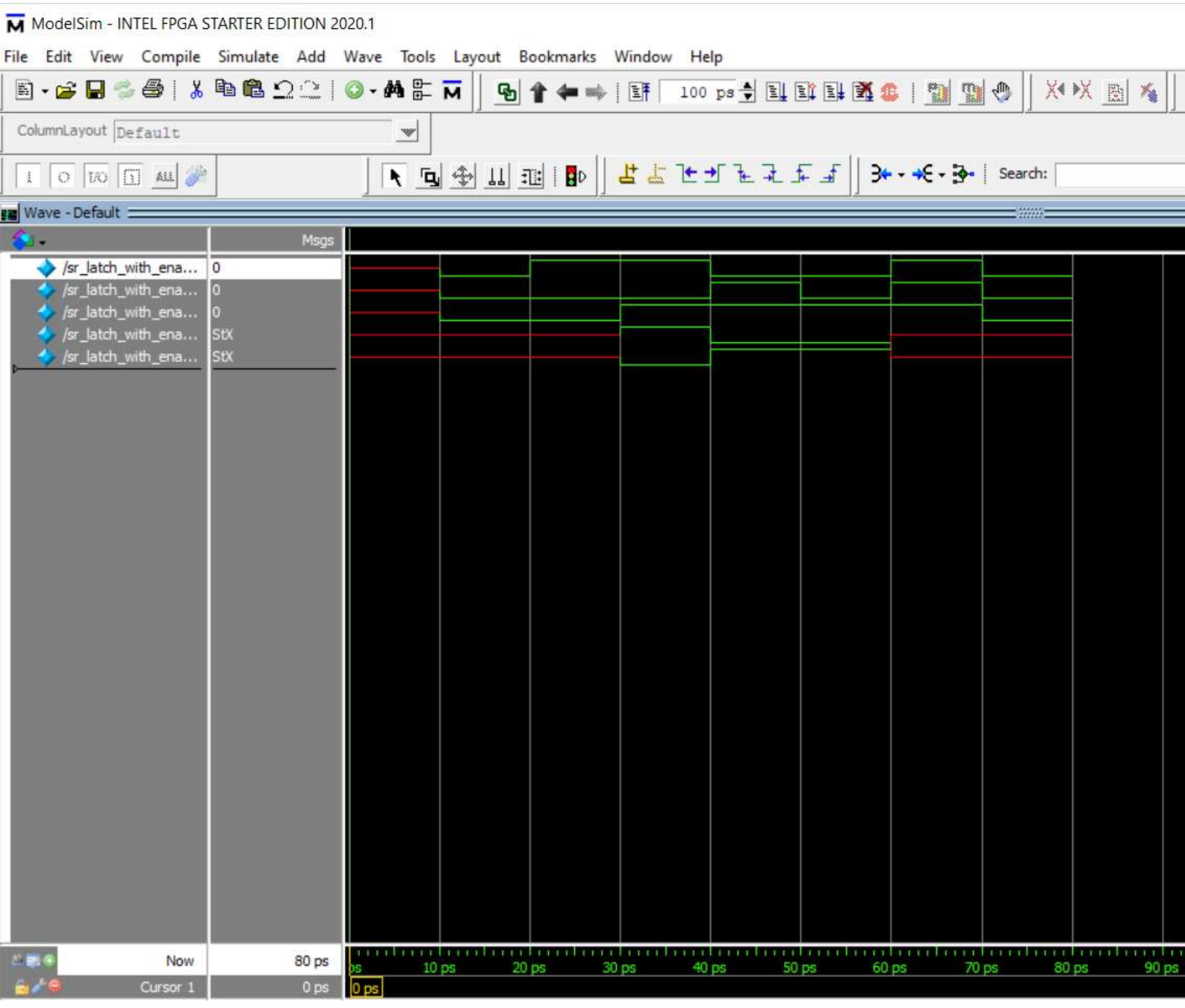

ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
100 ps
ColumnLayout Default
C:/Users/DELL/3D Objects/verilog/SRLatch.v (/sr_latch_with_enable_tb/uut) - Default *
Ln#
1 module sr_latch_with_enable(S, R,enable,Q,Q_bar);
2 input wire S; // Set input
3 input wire R; // Reset input
4 input wire enable; // Enable input
5 output wire Q; // Q output
6 output wire Q_bar; // Complement of Q
7
8 // Internal signals
9 reg Qa, Qb;
10
11 // Behavior of SR Latch with Enable
12 always @ (S, R, enable) begin
13 if (enable) begin
14 if (S == 1'b1 && R == 1'b0)
15 begin
16 Qa = 1'b1; // Set
17 Qb = 1'b0;
18 end
19 else if (S == 1'b0 && R == 1'b1)
20 begin
21 Qa = 1'b0; // Reset
22 Qb = 1'b1;
23 end
24 else if (S == 1'b0 && R == 1'b0)
25 begin
26 Qa = Qa; // Hold state
27 Qb = Qb;
28 end
29 else begin
30 Qa = 1'bx; // Invalid state when S = 1, R = 1
31 Qb = 1'bx;
32 end
33 end
34 end
35 // Assigning Q and Q_bar
36 assign Q = Qa;
37 assign Q_bar = Qb;
38 endmodule


ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
100 ps
ColumnLayout Default
Search:
C:/Users/DELL/3D Objects/verilog/tb_SRLatch.v (/sr_latch_with_enable_tb) - Default
Ln#
1 module sr_latch_with_enable_tb;
2
3 // Testbench signals
4 reg S; // Testbench Set input
5 reg R; // Testbench Reset input
6 reg enable; // Testbench Enable input
7 wire Q; // Testbench Q output
8 wire Q_bar; // Testbench Q_bar output
9
10 // Instantiate the SR latch with enable
11 sr_latch_with_enable uut (
12 .S(S),
13 .R(R),
14 .enable(enable),
15 .Q(Q),
16 .Q_bar(Q_bar)
17);
18
19 // Test sequence
20 initial begin
21 $monitor("At time %t: S = %b, R = %b, enable = %b, Q = %b, Q_bar = %b", $time, S, R, enable, Q, Q_bar);
22 // Initialize inputs and apply test cases
23 #10 S = 0; R = 0; enable = 0; // Test case 1: S = 0, R = 0, enable = 0 (No change)
24 #10 S = 1; R = 0; enable = 0; // Test case 2: S = 1, R = 0, enable = 0 (No change)
25 #10 S = 1; R = 0; enable = 1; // Test case 3: S = 1, R = 0, enable = 1 (Set Q to 1)
26 #10 S = 0; R = 1; enable = 1; // Test case 4: S = 0, R = 1, enable = 1 (Reset Q to 0)
27 #10 S = 0; R = 0; enable = 1; // Test case 5: S = 0, R = 0, enable = 1 (Hold state)
28 #10 S = 1; R = 1; enable = 1; // Test case 6: S = 1, R = 1, enable = 1 (Invalid state)
29 #10 S = 0; R = 0; enable = 0; // Test case 7: S = 0, R = 0, enable = 0 (No change)
30 #10 $finish;
31 end
32
33 endmodule
34


ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
100 ps
ColumnLayout Default
Search:
Wave - Default
Msgs
/sr_latch_with_ena... 0
/sr_latch_with_ena... 0
/sr_latch_with_ena... 0
/sr_latch_with_ena... StX
/sr_latch_with_ena... StX
Now 80 ps
Cursor 1 0 ps
10 ps 20 ps 30 ps 40 ps 50 ps 60 ps 70 ps 80 ps 90 ps
0 ps