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ModelSim - INTEL FPGA STARTER EDITION 2020.1
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 ColumnLayout Default
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 C:/Users/DELL/3D Objects/verilog/tb_JK_FF.v (/jk_flip_flop_tb) - Default =
 Ln#
  1
      module jk_flip_flop_tb;
  3
        // Testbench signals
  4
        req J;
                      // J input for testbench
  5
        reg K;
                      // K input for testbench
                      // Clock input for testbench
  6
        reg clk;
        wire Q;
                      // Q output for testbench
  8
        wire Q bar;
                      // Q bar output for testbench
  9
       // Instantiate the JK Flip-Flop without reset
 10
 11
      □ jk flip flop uut (
 12
           .J(J),
 13
            .K(K),
 14
            .clk(clk),
 15
           .Q(Q),
 16
            .Q bar (Q bar)
 17
      -);
 18
 19
       // Clock generation
 20
      initial begin
 21
           clk = 0:
           forever #5 clk = ~clk; // Clock period = 10 time units
 22
 23
      - end
 24
 25
       // Test sequence
      initial begin
 26
 27
           $monitor("At time %t: J = %b, K = %b, clk = %b, Q = %b, Q bar = %b", $time, J, K, clk, Q, Q bar);
 28
           // Initialize inputs
           $10 J = 0; K = 0; // Test case 1: J = 0, K = 0 (No change)
 29
           $10 J = 0; K = 1; // Test case 2: J = 0, K = 1 (Reset Q)
 30
 31
           #10 J = 1; K = 0;
                             // Test case 3: J = 1, K = 0 (Set Q)
 32
           #10 J = 1; K = 1; // Test case 4: J = 1, K = 1 (Toggle Q)
 33
           #10 $finish;
 34
       end
 35
 36
      endmodule
 37
```

