



ColumnLayout Default



C:/Users/DELL/3D Objects/verilog/tb_ring_counter.v (/tb_self_starting_ring_counter) - Default

Ln#

```
1 module tb_self_starting_ring_counter;
2
3     reg clk;
4     wire [3:0] count;
5
6     // Instantiate the self-starting ring counter
7     self_starting_ring_counter uut (
8         .clk(clk),
9         .count(count)
10    );
11
12    // Generate clock signal
13    initial begin
14        clk = 0;
15        forever #5 clk = ~clk; // 10 time units clock period
16    end
17
18    // Test sequence
19    initial begin
20        // Let the counter run for some time
21        #100; // Run for 100 time units
22
23        // End the simulation
24        #10 $finish;
25    end
26
27    // Monitor count value
28    initial begin
29        $monitor("Time: %0d, Count: %b", $time, count);
30    end
31
32 endmodule
```

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C:/Users/DELL/3D Objects/verilog/ring_counter.v (/tb_self_starting_ring_counter/uut) - Default

Ln#	
1	module self_starting_ring_counter (
2	input clk, // Clock input
3	output reg [3:0] count // 4-bit output count
4);
5	initial begin
6	count = 4'b0000; // Start with '0000'
7	end
8	
9	always @(posedge clk) begin
10	// NOR gate logic to prevent the state '0000'
11	if (~count[0] & ~count[1] & ~count[2]) begin
12	count <= 4'b0001; // Reset to '0001' if all FFs are '0'
13	end else begin
14	// Shift the '1' through the count
15	count <= {count[2:0], count[3]}; // Rotate the bits (left shift)
16	end
17	end
18	
19	endmodule

100 ps

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