OPTIMUM DxExp Library Reference Guide

Symbols

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SYMBOLS

The Symbols Library's Structure

Short descriptions of Symbol Libraries

BUILTIN – All non-PCB mount part type symbols, such as sheet borders and other documentation-related symbols (e.g., bus rippers, on-/off-sheet connectors, and power supply symbols)

CONNECTOR – Plug and socket symbols for all part types of connectors

DIODE_LED – Symbols for all diodes, LEDs, transzorbs, and bridge rectifiers

DISCRETE – Symbols for all capacitors, inductors, resistors, fuses, varistors, etc.; also includes symbols for non-device PCB mount entities, such as links, mounting holes, and test points

IC– Integrated circuit symbols

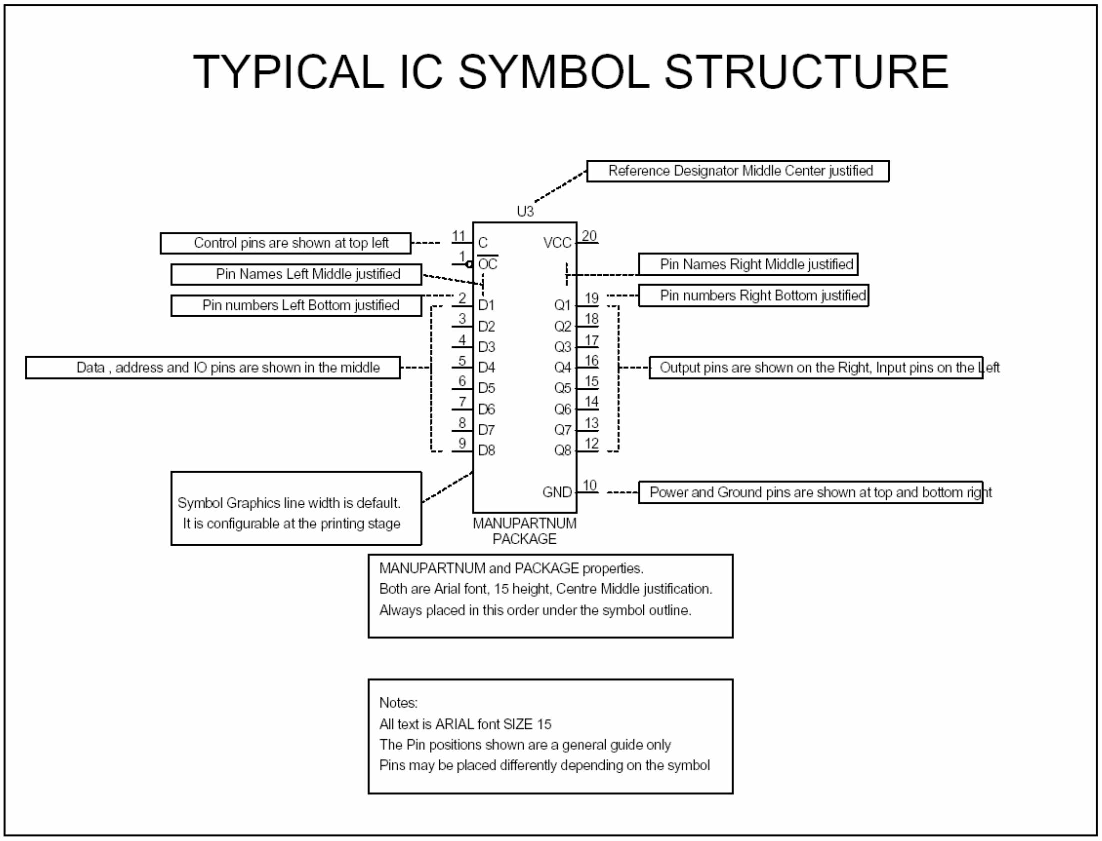
IC_EPLD – Integrated circuit symbols specific to programmable logic devices such as PALs, GALs, FPGAs, EPLDs, and support devices

SWITCH_RELAY – Symbols for switches and relays

TEMPLATES – Contains symbols of various part types that contain pre-positioned text properties and graphics, as well as pin number placeholders

TRANSISTOR – Symbols for transistors and MOSFETs

XTAL_OSC – Symbols for crystals and oscillators



Reference Designator Middle Center justified

Control pins are shown at top left

Pin Names Left Middle justified

Pin numbers Left Bottom justified

Data , address and IO pins are shown in the middle

Pin Names Right Middle justified

Pin numbers Right Bottom justified

Output pins are shown on the Right, Input pins on the Left

Power and Ground pins are shown at top and bottom right

Symbol Graphics line width is default.
It is configurable at the printing stage

MANUPARTNUM and PACKAGE properties.
Both are Arial font, 15 height, Centre Middle justification.
Always placed in this order under the symbol outline.

Notes:
All text is ARIAL font SIZE 15
The Pin positions shown are a general guide only
Pins may be placed differently depending on the symbol

Reproduced from "*Symbol Samples*"

Symbol naming conventions

GENERAL INFORMATION

Symbol Name Prefixes

All symbol names, with the exception of IC_ECL and IC_74LOGIC, have a prefix that is either:
a "part type" qualifier prefix, followed by as many qualifiers as necessary to adequately identify the symbol, or
a manufacturer abbreviation qualifier prefix in the case of "1:1 symbol:device" symbols.

The symbol prefixes are self-explanatory as to what part type the component symbol represents, and most are in the form of widely used, industry-standard abbreviations. For example, PLG = PLUG, CAP = capacitor, MOT = MOTOROLA.

For a list of part type qualifiers, see the document, "*ODA DxDesigner Library Reference Guide: Symbol Abbreviations List*." For a list of manufacturer abbreviations qualifiers, see the document, "*ODA Manufacturers Abbreviations*."

Symbol Name Qualifiers

Manufacturer part number qualifiers

Many symbols simply use the full manufacturer part number as the symbol name qualifier. This convention is mainly used for ICs, but may be used for other symbols where deemed appropriate. For example, Maxim part number MAX-MAX211CAI.

Multiple symbol qualifiers

There are two naming conventions used in the library for situations where multiple symbols are required for one device:
pin group qualifiers (suffix), used to separate the pins of the device into symbols according to the various pin groups; for example, GND, CNFG, BNK7
n of symbols qualifiers (suffix), simply uses the format of SYM1, SYM2, SYM3,…

Part type qualifiers

As well as using the part type prefixes, many symbols also use other descriptive part type qualifiers in their naming conventions. Most of these qualifiers are readily identifiable as industry standard abbreviations. For example, VAR = VARIABLE, DIL = DUAL IN LINE, POL = POLARIZED. For a list of part type qualifiers, see the document, "*ODA DxDesigner Library Reference Guide: Symbol Abbreviations List*."

Package type qualifiers

IC symbols *may* contain a package type suffix where devices are available in different package pinouts. This applies to IC_74LOGIC and IC_ECL symbols. If no suffix is used in the symbol name, the symbol is the standard SOIC/DIP style pinout version of the device. Since "no suffix" = SOIC/DIP, generally, the only suffixes used will be –LCC or –BGA.

Pin number qualifiers in symbol names

Many symbols have pin number information included in the symbol name. This is our preferred method of making symbols as generic as possible without the need for additional "side" files or attributes to manipulate pin orders and numbers.

For example, the symbol ***"reg-i1o2g3.1"*** can be used for any regulator that has the pinout of input=pin1, output=pin2, ground=pin3. Note that the naming convention uses actual pin numbers, NOT numbers of pins (i.e., g3 means that pin number 3 is the GND pin. It does NOT mean that there are three GND pins.)

This method enables the use of one symbol for many different devices. This naming convention may be used for any part type having a maximum of 8 pins.

A list of the letters used and their meanings can be found in the document, "*ODA DxDesigner Library Reference Guide: Symbol Abbreviations List*."

File extensions in symbol names

Each symbol is stored in the form of a text file, with the file extension of .1, .2, .3, and so on. Different symbol file extensions are used to depict different views of the device. This enables the user to:

- Place different symbol views that have all of their text in the correct orientation
  All of the widely used 2-pin symbols, such as RES and CAP,
  have a symbol with both a .1 and a .2 extension.
  .1 = horizontal view
  .2 = vertical view

- Have symbols that allow for closer placement of symbols without overlapping text/graphics
  These are generally used for pull up or pull down resistor groups.
  .3 = horizontal slimline
  .4 = vertical slimline

- Place different views according to "gate level" or "all pins" symbols
  These symbols are usually resistor, capacitor or diode packs. Any device that can be shown as all pins in one symbol or as individual gates can use this method.
  .1 = all pins on one symbol - ***res-pack-4res.1***
  .2 = multiple gates of the same symbol - ***res-pack-4res.2***

  Note: The "normal" resistor symbol cannot be used for multiple gates in a resistor pack due to the PARTS= attribute. Since this attribute tells the system that there is only one gate (PARTS=1) for a normal single resistor, it cannot also be used to tell the system that PARTS=4 for an 8-pin, 4-resistor pack. Therefore, a single resistor with PARTS=4 is required (***res-pack-4res.2***).

Having the different views reduces the need to continually rotate text to match the view of the symbol.

By not including the file extension in the DxDatabook entry, all symbols with the matching symbol name are available in the DxDatabook symbol selection window.

LIBRARY-SPECIFIC INFORMATION

Builtin

The Builtin library contains all of the schematic page utility symbols, such as sheet borders, power and ground symbols, bus rippers, and on- and off-page connectors. The symbol names are self-explanatory.

Connectors

- Symbol names for connectors are in the form of:

Plug prefix is PLG-*x*-QUALIFIER/S
Socket prefix is SKT-*x*-QUALIFIER/S

Where ***x*** represents the number of connector pins, excluding mounting holes

- The QUALIFIERS may contain additional information as to what the symbol represents, and are always in a descriptive form. E.g., "PLG-10-ODD-EVEN" is a 10-pin plug with the alternative pinout of having 2 rows of 5 pins with odd number pins on one side and even number pins on the other. "PLG-20-PAIRS" is a 20-pin plug with the alternative pinout of having pin 1 then pin 11, etc., which is suitable for schematic entry of differential pair signals. And "PLG-10-JTAG" is a 10-pin plug with JTAG pin names.

The MANUFACTURER ABBREVIATION–FULL MANUFACTURER PART NUMBER symbol naming convention may also be used for connectors, where deemed appropriate.

Diode_led

- Symbol names for diodes and LEDs are derived from the part type (PART TYPE PREFIX – PART TYPE/PIN QUALIFIER/S). For example:

DIO	Diode
DIO–SCH	Schottky Diode
DIO–ZEN	Zener Diode
DIO-SCH-C1A3NC2	Diode Schottky, cathode=pin1, anode=pin3, no connect=pin2

Default pin numbers on the simplest form of each diode or LED are: cathode = 1 and anode = 2. Diode and LED symbols may also include pin number qualifiers in the symbol name when devices have more than two pins, or when the pinout IS NOT numbered according to the default (i.e., cathode ≠ 1 and anode ≠ 2).
The MANUFACTURER ABBREVIATION–FULL MANUFACTURER PART NUMBER symbol naming convention may also be used for diodes or LEDs where deemed appropriate.

See the general information section for an explanation of ***part type qualifiers*** and ***pin number qualifiers***.

Discretes

- Symbol names for discretes are derived from the part type (PART TYPE PREFIX – PART TYPE/PIN QUALIFIER/S. For example:

CAP-POL	Polarized Capacitor
IND-VAR	Variable Inductor
RES-VAR-MAX3MIN1ADJ2	Variable Resistor, maximum=pin3, minimum=pin1, adjust=pin2

Default pin numbers on all non-polarized devices are 1 and 2.
Default pin numbers on polarized capacitors are: positive = 1, negative = 2.
Discrete symbols may also include pin number qualifiers in the symbol name when devices have more than 2 pins.
A symbol without a qualifier represents the simplest form of the device. For example:
CAP – non-polarized fixed capacitor
RES – simple fixed resistor

See the general information section for an explanation of ***part type qualifiers*** and ***pin number qualifiers.***

IC

As these symbols are all “1:1 symbol:device” symbols (i.e., not used in multiple PDBs), they are identified with a form of the manufacturer’s part number: MANUFACTURER ABBREVIATION–FULL MANUFACTURER PART NUMBER-MULTIPLE SYMBOL QUALIFIER. For example:

MAX-MAX211CAI
AD-AD7814ARM

IC (generically named)

Symbol names for generic IC’s are derived from the part type: PART TYPE PREFIX – PART TYPE/PIN QUALIFIER/S. For example:

REG-I1O2ADJ3.1	Regulator, input=pin1, output=pin2, adjust=pin3
AMPFR-I1O3G24.1	Amplifier, input=pin1, output=pin3, ground=pins2 and 4
VLTMON-O1G4V2NC35678.1	Voltage Monitor, output=pin1, ground=pin4, VCC=pin2, no connect=pins3,5,6,7 and 8

These IC symbols can be used for many different devices.
Generic IC symbols include pin number qualifiers in the symbol name.
The following three rules apply to generic IC symbols:

1. Generic IC symbols may only be used for devices with eight pins or less.
2. Numbers after letters in symbol names represent actual pin numbers, not the number of pins.
3. Multiple numbers of the same pin types are not separated.

Example 1: Reg-i3o1g2

- Regulator
- Input = 3
- Output = 1
- Ground = 2

Example 2: Reg-i3o1g24

- Regulator
- Input = 3
- Output = 1
- Ground = 2
- Ground = 4
- Ground= pins 2 and 4 (not pin 24)

See the general information section for an explanation of ***part type qualifiers*** and ***pin number qualifiers***.

IC (ECL)

These symbols are named by using the industry-standard function/part number and an optional package qualifier:

IC_NUMBER-PACKAGE QUALIFIER

IC_NUMBER represents significant digits in the part number.
IC_NUMBER does **not** include a prefix denoting the manufacturer.
A suffix may be used to denote the package/pinout part type. If no suffix is used, the package pinout part type = standard SOIC/DIP.
A **letter** may be used as a significant “digit,” when required. For example:

100EL90
100E101-LCC

IC (74logic)

These symbols are named by IC_NUMBER = “74XXyyy,” where “yyy” represents an industry-standard function number. For example:

74XX161
74XX373

IC_NUMBER does **not** include a prefix denoting the manufacturer.
A suffix may be used to denote the package/pinout part type. If no suffix is used, the package pinout part type = standard SOIC/DIP.
IC_74logic’s symbols may be either multiple gate part type symbols or as all pins shown on one symbol.
Templates for logic gate part type symbols can be found in the templates library.

IC_EPLD

As these symbols are all “1:1 symbol:device” symbols (i.e., not used in multiple PDBs), they are identified with a form of the manufacturer’s part number:
MANUFACTURER ABBREVIATION–FULL MANUFACTURER PART NUMBER-QUALIFIER
The OPTIMUM default method for organizing the multiple symbols for EPLDs is to create one symbol for each bank. Symbols are also created for power, ground and configuration pins, with the organization of these symbols being dependent on the number of pins in the device.
Any number of qualifiers may be used, and in all cases the qualifier is obvious in describing the pins contained in the symbol.
Any numbers or letters that refer to **speed grades** or **temperature ranges** in the manufacturer’s part number are not included in the naming convention.
Examples:

XIL-XC2V1000-FG256-BNK7
XIL-XC2V1000-FG256-PWR
XIL-XC2V1000-FG256-CFG

The pin group qualifier is used when multiple symbols are required to represent a device. The qualifier will vary according to the part types of pins on the symbols:

-BNK7 is all of the pins in BANK 7 of the device
-PWR-GND is all power and ground pins shown on one symbol
-PWR1 is the first power pin symbol of a device having a large number of power pins
-PWR2 is the second power pin symbol of a device having a large number of power pins
-CNFG is all of the configuration pins of a device
-RIO is all of the Rocket I/O pins of a device

Switch_Relay

- Symbol names for switches and relays are derived from the part type: PART TYPE PREFIX – PART TYPE/PIN QUALIFIER/S. For example:

RELAY-CL15CM2NC4NO3	Relay, coil=pins1 and 5, common =pin2, normally closed =pin4, normally open=pin3

SSR-CP3-CN4-LD12	Solid State Relay control pos = pin3, control neg = pin3, load = pins 1 and 2
SWITCH-DIL-02	Switch, dual-in-line, 2 way

- The MANUFACTURER ABBREVIATION–FULL MANUFACTURER PART NUMBER symbol naming convention may also be used for switches or relays, where deemed appropriate.

Templates

- Symbol templates are provided for a variety of devices. These templates are provided with all of the necessary attributes, as well as pin number placeholders. Just add the correct pin numbers instead of the placeholders and the symbol is ready to add to the appropriate library.

Transistor

- Symbol names for transistors are derived from the part type: PART TYPE PREFIX – PART TYPE/PIN QUALIFIER/S. For example:

MOSFET-N-GT1D3S2	MOSFET, N channel, gate=pin1, drain=pin3, source=pin2
XISTOR-NPN-E1B2C3	Transistor, NPN, emitter=pin1, base-pin2, collector=pin3

- The MANUFACTURER ABBREVIATION–FULL MANUFACTURER PART NUMBER symbol naming convention may also be used for transistors, where deemed appropriate.

Xtal_Osc

- Symbol names for switches and relays are derived from the part type: PART TYPE PREFIX – PART TYPE/PIN QUALIFIER/S. For example:

CRYSTAL-I1O3NC24	Crystal, input=pin1, output =pin3, no connect=pins2 and 4
OSC-ENH1O3G2V4	Oscillator, enable high=pin1, output=pin3, ground=pin2 VCC=pin4

- The MANUFACTURER ABBREVIATION–FULL MANUFACTURER PART NUMBER symbol naming convention may also be used for switches or relays, where deemed appropriate.

What is in a symbol?

Symbols are made up of three items: GRAPHICS, TEXT, and PINS.

Graphics

Graphics consist of a symbol body outline, and also as shapes that symbolize the electronic functionality of the symbol or of individual pins. Line width is default. The line width may be defined during the printing process.

Text

Text consists of text that is attached to the ***SYMBOL***, and text that is attached to ***PINS***. All visible text is ARIAL font, size 15.

SYMBOL TEXT

The following attributes are placed as visible text attached to the symbols. Attributes are either (OPTIMUM added) or (DX default).

MANUPARTNUMBER (OPTIMUM added) – Manufacturer part number

This attribute gets its value from DxDatabook. It is the same as the DEVICE attribute except that it does not have the OPTIMUM manufacturer prefix. It can be used in a BOM for ordering parts.

VALUE (OPTIMUM added) - shown on Res, Cap, Ind, Xtal, Osc (10k, 150nF, 10nH, 20.000Mhz, etc.)

This is used for the actual value in Ohms, Farads, Henrys, or Hertz in discrete devices. Discrete devices do not show MANUPARTNUMBER as a visible attribute.

PACKAGE (OPTIMUM added) – industry standard package name, SO8, 0805, BGA256, etc.

If no industry standard exists, then either THP (thru hole plated) or SMD (surface mount device) is used to specify the basic mounting type of the package.

CHIPNAME (OPTIMUM added) – used on programmable ICs

This attribute accommodates a user-defined chip name.

REFDES (DX default) – reference designator

NC (DX default) – no-connect pins (if used)

SIGNAL (DX default) – implicit signal pins (if used)

The following attributes are placed as invisible text on the symbols. Attributes are either (OPTIMUM added) or (DX default)

LEVEL (DX default) – used for determining hierarchy (see DxDesigner help system)

DEVICE (DX default) – used as the PARTNUMBER (PDB name) when exported to Expedition

PKG_TYPE (DX default) – used as the CELLNAME when exported to expedition

PARTS (DX default) – used to determine the number of gates within a device (see DxDesigner help system)

PINSWAP (DX default) – used to determine pin swapability (see DxDesigner help system)

HETERO (DX default) – used in various forms to determine multiple symbol devices (see DxDesigner help system)

The following table can be printed out as a quick reference guide to symbol attributes:

ATTRIBUTE TABLE

ATTRIBUTE	**DEFAULT VALUE**	**DEFAULT VALUE REPLACED WTH DX DATABOOK VALUE**	**VISIBILITY**	**USAGE**
MANUPARTNUMBER	MANUPART	YES	VISIBLE (invisible on discretes)	MAUFACTURER PART NUMBER
VALUE (discretes only)	VAL	YES	VISIBLE	VALUE FOR DISCRETES, 10k 150pF 120nH etc
PACKAGE	PACK	YES	VISIBLE	INDUSTRY STANDARD PACKAGE TYPE
CHIPNAME	CHIPNAME	NO , VALUE GIVEN AT SCHEMATIC LEVEL	VISIBLE	USER'S OWN CHIPNAMES FOR PROGRAMMABLE IC's
REFDES	REFDES PREFIX?	NO, VALUE GIVEN WHEN "CREATE REFDES" COMMAND IS EXECUTED	VISIBLE	REFERENCE DESIGNATOR
NC	NONE	NO, THE ACTUAL VALUE IS DEFINED DURING SYMBOL CREATION	VISIBLE	DEFINITION OF NO CONNECT PINS
SIGNAL	NONE	NO, THE ACTUAL VALUE IS DEFINED DURING SYMBOL CREATION	VISIBLE	DEFINITION OF POWER AND GROUND PINS
LEVEL	STD	NO, THE ACTUAL VALUE IS DEFINED DURING SYMBOL CREATION	INVISIBLE	USED FOR HEIRACHY
DEVICE	DEV	YES	INVISIBLE	LINKS TO PARTNUMBER IN EXPEDITION
PKG_TYPE	PKG	YES	INVISIBLE	LINKS TO CELLNAME IN EXPEDITION
PARTS	NONE	NO, THE ACTUAL VALUE IS DEFINED DURING SYMBOL CREATION	INVISIBLE	DEFINITION OF GATES IN DEVICE. ENABLES GATE SWAPPABILITY IN EXPEDITION
PINSWAP	NONE	NO, THE ACTUAL VALUE IS DEFINED DURING SYMBOL CREATION	INVISIBLE	DEFINITION OF PIN SWAPS IN DEVICE. ENABLES PIN SWAPPABILITY IN EXPEDITION
HETERO	NONE	NO, THE ACTUAL VALUE IS DEFINED DURING SYMBOL CREATION	INVISIBLE	DEFINITION OF HETEROGENOUS SYMBOLS IN DEVICE

PIN TEXT

Each pin name must be unique. Duplicate names are not allowed, because pins cannot be mapped in an Expedition PDB if there are two pins with the same name.

If more than one pin performs the same function (e.g., a ground connection), then the pin names must still be different. These pins are typically differentiated with the addition of a number at the end of the pin name. For example, GND1, GND2, etc.

PIN NAMES may or may not be visible, depending on the symbol. As a general guide, pin names are not shown on discrete, connector, or logic gate symbols, whereas they are shown on IC symbols.

PIN NUMBERS are always visible. This includes discretes. They are easily turned on and off with the “lightbulbs” on the TRANSFORM TOOLBAR in DxDesigner.

PIN TYPES are always invisible. Pin types used are IN, OUT, BI, TRI, and ANALOG. Note that some pin type text may not be Arial size 15 font, but as it is always invisible, this should not pose any problems.

Uniformity of the text used for pin names and number is highly desirable. This uniformity is best achieved with the use of the “save copy as” method of creating symbols, rather than creating everything from scratch.

Pins

Pin connection points

The connection point of a pin is determined by where the pin meets the symbol BLOCK border. This border appears as a white box around the symbol during symbol editing, and its size is determined by the width and height specified in the symbol properties dialog box.
Pins can be moved around and rotated inside the block border, and can be of any length within that border, but the connection point remains where the pin meets the block border.

Pin shapes

There are four pin shapes on the symbols. Normal and inverted pins consist of the pin only (no drawn graphics are used), whereas the clock pin is a normal pin plus a clock graphic. The dot pins are created with the use of the “invert pin option.”

Normal – active high input or output
Dot – active low input or output
Clock – active high clock input or output
Dot Clock – active low clock input or output

Negative logic pins

Negative logic pins are signified with the use of overbars in the pin name. The overbar is created automatically by checking the “inverted” checkbox in the pin properties dialog. Selecting “invert pin” from the same dialog will give the pin a “dot”/“bubble” pin.

Power, ground, and no-connect pins

- Power and ground connections may be made using the following methods:

    1. With the use of the visible SIGNAL attribute in the form of:

SIGNAL=NETNAME;PIN NUMBER/S

For example, SIGNAL=GND7, SIGNAL=VCC14. This method is mostly used on gate level devices (see “GATED DEVICES”).

2. Showing power and ground pins on the symbol (on one-symbol-per-device symbols). This is the default method for most ICs.

3. On high-pin-count devices, using a combination of multiple “signal pins” symbols and a specifically named “supply pins” symbol. E.g., XC2V1000-#FG256#-PWR-GND.

- No-connects are signified by either:

    1. Using the visible NC attribute on the symbol in the form of:

        NC=PIN NUMBER,PIN NUMBER

        If this method is used, the pins do not show up as either unconnected pins or as single-pin nets in the design rules checking procedure.

    2. Showing the no-connect explicitly on the symbol as a pin named NC (or as NC1, NC2,…), then these pins can be given an instance-specific, no-connect attribute at the schematic entry level, so that they do not show up as either unconnected pins or as single-pin nets in the design rules checking procedure.

Other symbol issues

Gated devices

Devices that use multiple gates have a PARTS= attribute. This attribute value determines the number of gates in the device. Where gated devices have been created for ICs, the power and ground pins are defined with the use of the SIGNAL= attribute. This does away with the need to have a “power pin gate.”

Gates (through definition of the PARTS= attribute) will be swappable in Expedition PCB.

Heterogeneous devices

There are various forms of heterogeneous symbols in DxDesigner. This allows the system to recognize that all of the symbols with the same hetero attribute value are all part of the one device, and are all given the same reference designator when “create refdes” is run.

Schematic page layout Symbols

Symbols are designed for use with a D (A1) size screen schematic page.
The schematics can be printed to any size sheet and are readable right down to A-size “Letter” (A4).

Pin and Gate Swaps

Pin and gate swaps are built into the DxDesigner symbols, rather than being mapped at only the PDB level. This gives greater flexibility by allowing the symbols to be used with other layout tools. It also saves time during PDB creation/editing because both pin swaps and gates swaps are automatically embedded in the PDBs that are created by the netlist forward-annotation process. Pin swaps are determined by the PINSWAP attribute on the symbols (see DxDesigner help system). Gates, by definition of the PARTS= attribute, may be swapped in the PDBs that are created by the netlist forward-annotation process.

SYMBOL CREATING AND EDITING TIPS

Creating (Copying) a new symbol from a template

Symbols are most easily created using the "FILE/SAVE COPY AS" menu selections. By copying an existing similar symbol, you will already have all of the necessary attributes existing in the symbol. These attributes can then be altered to suit.

This procedure is especially relevant to DxDesigner, as it does not have drop-down boxes from which to make selections of attributes. All new attributes must have both their name and value typed in every time you make a new symbol. This is both time consuming and prone to typographical errors.

The Template library has a selection of symbols that can be used for this purpose. Simply select a symbol and perform a "save copy as" to create your new symbol. Then it is just a matter of replacing the # pin number placeholders with actual pin numbers, and updating any attributes.

Placing Pin Graphics and Pin Text

Pins are usually *copied* along with their text and graphics, and are *pasted* as one combination to produce a new pin. This keeps all text and graphics consistent in size, justification, and placement in relation to the relevant pin, and is much faster and more accurate than drawing it all from scratch.

Once the pin combination has been copied to a new location, the pin is then given a unique name, number and type.

Symbols are text files

The DxDesigner symbol files can be edited in any text editor. Changes can be made to all of the symbols at once very easily. The global addition or deletion of an attribute or change to an attribute's visibility can be done very simply with the search and replace function.

Of course, endless possibilities exist for editing with the writing of more advanced programs and scripts to manipulate the symbol files.

Additional documentation

More information may be found in the following documents:

Symbol Samples

- ○ *ODA DxDesigner Symbol Samples: A3*
- ○ *ODA DxDesigner Symbol Samples: A4*

Abbreviations

- ○ *ODA DxDesigner Library Reference Guide: Symbol Abbreviations List*
- ○ *ODA Manufacturers Abbreviations*