SOFTWARE ASSIGNMENT-1

The main.cpp files calculate the delay for the PRIMARY_OUTPUTS , by reading the circuit.txt file. First all the primary inputs are pushed into a vector, followed by internal signals and finally the primary outputs. Then these are mapped to their initial delays. All the primary inputs are mapped to 0 at the beginning.

The input gates must be given in order for the code to work correctly. Otherwise there will be error in the final outputs. After primary inputs,outputs and internal signals have been mapped , gates are now fed to the while loop until there is nothing to read. All the computation happens in this while loop. The

```
if(type=="INV"){
    iss >>element;
    string t = element;
    iss >> element;
    delays[element]=delays[t]+2;
}
if(type=="AND2"){
    iss >>element;
    string t = element;
    iss >> element;
    string t2 =element;
    iss>>element;
    delays[element]=max(delays[t],delays[t2]) +4;
}
if(type=="NAND2"){
    iss >>element;
    string t = element;
    iss >> element;
    string t2 =element;
    iss>>element;
    delays[element]=max(delays[t],delays[t2]) +3;
}
if(type=="OR2"){
    iss >>element;
    string t = element;
    iss >> element;
    string t2 =element;
    iss>>element;
    delays[element]=max(delays[t],delays[t2]) +4.5;
}
if(type=="NOR2"){
    iss >>element;
    string t = element;
    iss >> element;
    string t2 =element;
    iss>>element;
    delays[element]=max(delays[t],delays[t2]) +3.5;
}
```

conditionals take care of the different types of gates. As can be seen from the above image , as each of the gate types are encountered the , inputs are looked up in the map and then the max delay time of the inputs to the gates is incremented by the respective gate delay and is mapped to the output.This happens only in case of AND,OR,NOR,NAND gates as the NOT gate has only single input.

Time Complexity Analysis:
Consider a circuit with p_1 primary inputs including repetition, p_2 internal signals a including repetition and p_3 primary outputs.Assuming worst case scenario, suppose there are only gate types that require most searches for input and output signals in the map.Since each gate would require atmost 3 searches for elements in the signal map , it would take 3*log(n) order of time for each gate , where n is the number of distinct signals.Since every signal must be searched in each gate it would take:

$\Sigma(p_1+ p_2+p_3)\log(n)$ searches.
Hence time complexity is f(n)log(n).

TEST CASE USED:
PRIMARY_INPUTS A B C D
PRIMARY_OUTPUTS L
INTERNAL_SIGNALS E F G H J K I
AND2 A B E
OR2 C D H
INV D I
NOR2 D I J
INV E F
NAND2 F H G
INV J K
AND2 G K L
EXPECTD OUTPUT: L 13
GOT: L 13

A few more test cases are submitted along with this.

For the second part of the assignment , brute force search was used to search for a possible combination of delays for desired output delays. Two nested for-loops are run incrementing the input delay by 0.5 and then computation of output delays is carried. This is then matched with the required delays and if it matches the loops break. But for complication issues, this program only runs for

testcases with 2 primary inputs. There will always be a possibility of multiple answers. This program computes the one with the least change in input delays.

```
for(delays[primaryInputs[1]]=0; delays[primaryInputs[1]]<maxvalue(req_del);delays[primaryInputs[1]]+=0.5){
    for(delays[primaryInputs[0]]=0; delays[primaryInputs[0]]<maxvalue(req_del);delays[primaryInputs[0]]+=0.5){
        computation(delays);
        if(mapequality(delays,req_del)){
            break;
        }
    }
    if(mapequality(delays,req_del)){
        break;
    }
}
```

Time Complexity Analysis:
For the 2 output case, this program runs 2 nested loops. The worst case time complexity is $O(n^2)$, where n=max(required delays).

Consider the test case :
PRIMARY_INPUTS A B C
PRIMARY_OUTPUTS F G
INTERNAL_SIGNALS D E
AND2 A B D
INV C E
AND2 D E F
AND2 D E G
Clearly delay(F)==delay(G) always . Hence there exists no input delays such that delay(F)≠delay(G).
More testcases are submitted alongside.

ADITYA JHA - 2022CS11102
HARSHAL KUMAR - 2022CS11126