Date: 02.08. 2018

FIRST SEMESTER 2018-2019

In addition to Part-I (General Handout for all courses appended to the timetable) this portion gives further specific details regarding the course.

Course Handout

Course No	: CS F 215/ EEE F215 / INSTR F215
Course Title	: Digital Design
Instructor-in-charge	: Dr. Pawan K. Ajmera (pawan.ajmera@pilani.bits-pilani.ac.in)
Instructors for Lecture	: Dr. Nitin Chaturvedi, Dr. Pawan K. Ajmera.
Tutorial Instructors	: Dr. Pawan K. Ajmera, Mr. G. Sai Shesha Chalapathi Mr. Ashish Patel, Mr. Tejasvi Alladi
Practical Instructors	: Tulsi Ram Sharma, Abheek Gupta, Prateek Bindra, Punit Khatri, Teena Gakhar, Ankita Dixit.

Scope and Objective: The objective of the course is to impart knowledge of the basic tools for the design of digital circuits and to provide methods and procedures suitable for a variety of digital design applications.

Text Books :

T1: M. Moris Mano and Michael D. Ciletti "Digital Design", PHI, 5th Edition, 2013.

T2: G. Raghurama, S. Gurunarayanan, S. Mohan, Karthik, "Laboratory Manual", EDD notes 2007.

Reference Books:

R1: Ronald J. Tocci and Neal S. Widmer, "Digital Systems-Principles and Application", Pearson, 10th Edition, 2007.

R2: Thomas l. Floyd, "Digital Fundamentals," Pearson, 9th Edition, 20

R2: Donald D. Givonne, "Digital Principles and Design" TMH, 2003

Course Plan

Lecture No.	Main Topic	Contents	Reference
01	Introduction	Introduction to Digital systems and characteristics	
02	Number systems and codes	Digital, Binary, Octal and Hexadecimal, Number-Base Conversions, Complements, Signed Binary Numbers.	T1:1.1-1.9
03	Logic Gates and Boolean Algebra	Digital Logic Gates, Truth Table, Boolean Algebra, Theorems and Properties, Boolean Functions, Canonical and Std. forms.	T1:2.1-2.8
04-05	Minimization Techniques	Gate-Level Minimization, The Karnaugh Map Method, Quine-McCluskey Method	T1:3.1-3.8
06	Simulation and synthesis	Hardware Description Language (Verilog HDL)	T1:3.11
07-10	Combinational Logic Circuits	Introduction, Analysis and Design Procedure, Binary Adder-Subtractor, Decimal Adder, Binary Multiplier, HDL Models of Combinational Circuits.	T1:4.1-4.7 T1:4.12
11-14	MSI Logic Circuits	Magnitude Comparator, Decoders, Encoders, Multiplexers, HDL Models of Combinational Circuits.	T1:4.8-4.12
15-17	Sequential Logic Circuits	Introduction, Storage Elements: Latches and Flip-Flops.	T1:5.1-5.4
18-22	Registers and Counters	Registers, Shift Registers, Ripple Counters, Synchronous Counters, HDL for Registers and Counters	T1:6.1-6.5
23-25	Memory and PLD's	Introduction, Random-Access Memory, Memory Decoding, Error Detection and Correction, Read-Only Memory, Programmable Logic Array, Programmable Array Logic	T1:7.1-7.8
26-31	Synchronous Sequential circuits	Analysis of Clocked Sequential Circuits, State Reduction and Assignment, Design Procedure, HDL Models of Sequential Circuits	T1:5.5-5.8
32-36	Design of Digital Systems	Register Transfer Level (RTL) Notation, Algorithmic State Machines (ASMs), HDL description.	T1:8.1-8.8
37-40	Digital Integrated Circuits	TTL, MOS Logic families and characteristics.	T1:10.1-10.9

Evaluation Scheme:

EC No.	Evaluation Component	Duration	Marks	Date and Time	Nature of Component
1	Weekly Quiz	10 Min	45	Continuous	Close Book
2	Laboratory (Attendance + Lab exam)	180 Min	12 + 33	Continuous	Close Book
3	Mid-Semester Exam	90 Min	90	14/10 2:00 - 3:30 PM	Close Book
4	Comprehensive Exam	180 Min	120	14/12 FN	Open/Close Book

Total	**300**	

Practical

S.No.	**Name of experiment**
1.	Familiarization of bench equipment
2.	Boolean functions implementation
3.	Design of arithmetic circuits (Adder and Subtractors)
4.	Implementation of BCD adder
5.	Decoders, multiplexers and de-multiplexers
6.	Latches and Flip-Flops
7.	Counter design
8.	Operation of a 4-bit counter
9.	Shift registers
10.	Design of sequence detector
11.	Comparators and arithmetic logic unit
12.	Memories and FPGAs

Assignments: There will be simulation based assignments, which will be as take home assignments.

Chamber Consultation Hours: To be announced in the class.

Notices: Notices regarding the course will be displayed only on the EEE (FD II) notice board/NALANDA.

Makeup Policy: Makeup will be granted to ***extremely genuine*** cases only, *provided the IC has been informed.*

Instructor - in - charge
CS F215/ EEE F215 / INSTR F215