Digital Logic Families

- ICs are also classified based on their specific circuit technology, known as ***digital logic family***.
- Each family has its own basic electronic components (NAND, NOR, and NOT gates), used to build complex digital circuits.
- Various digital logic families have been introduced and used over the years.

Digital Logic Families (in chronological order)

- RTL: Resistor-Transistor Logic
- DTL: Diode-Transistor Logic

earliest, now obsolete

- I^2L: Integrated-Injection Logic
- TTL: Transistor-Transistor Logic → widely used
- ECL: Emitter-coupled Logic → high-speed operation
- MOS: Metal-Oxide Semiconductor → compact
- CMOS: Complementary MOS
  - Low power dissipation, currently the MOST DOMINANT
- BiCMOS: Bipolar CMOS
  - CMOS and TTL for additional current/speed
- GaAs: Gallium-Arsenide → very high-speed operation

Defining Characteristics of Digital Logic Families

- ***Fan-in:*** # of gate inputs.
- ***Fan-out:*** # of standard loads a gate's output can drive.
- ***Noise margin:*** max external noise tolerated.
- ***Power dissipation:*** power consumed by the gate (dissipated as heat).
- ***Propagation delay:*** time required for an input signal change to be observed at an output line.

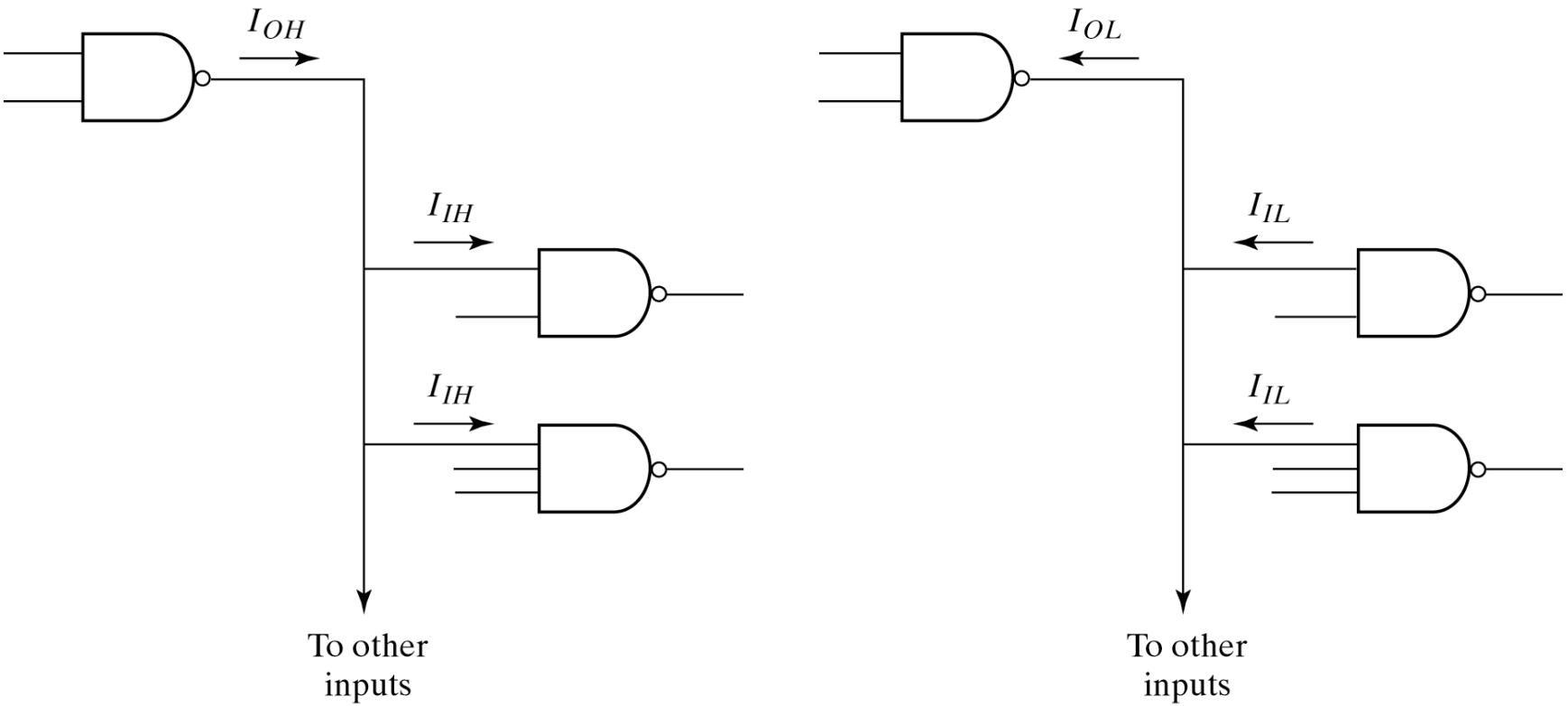


Fig. 10-3 Fan-Out Computation

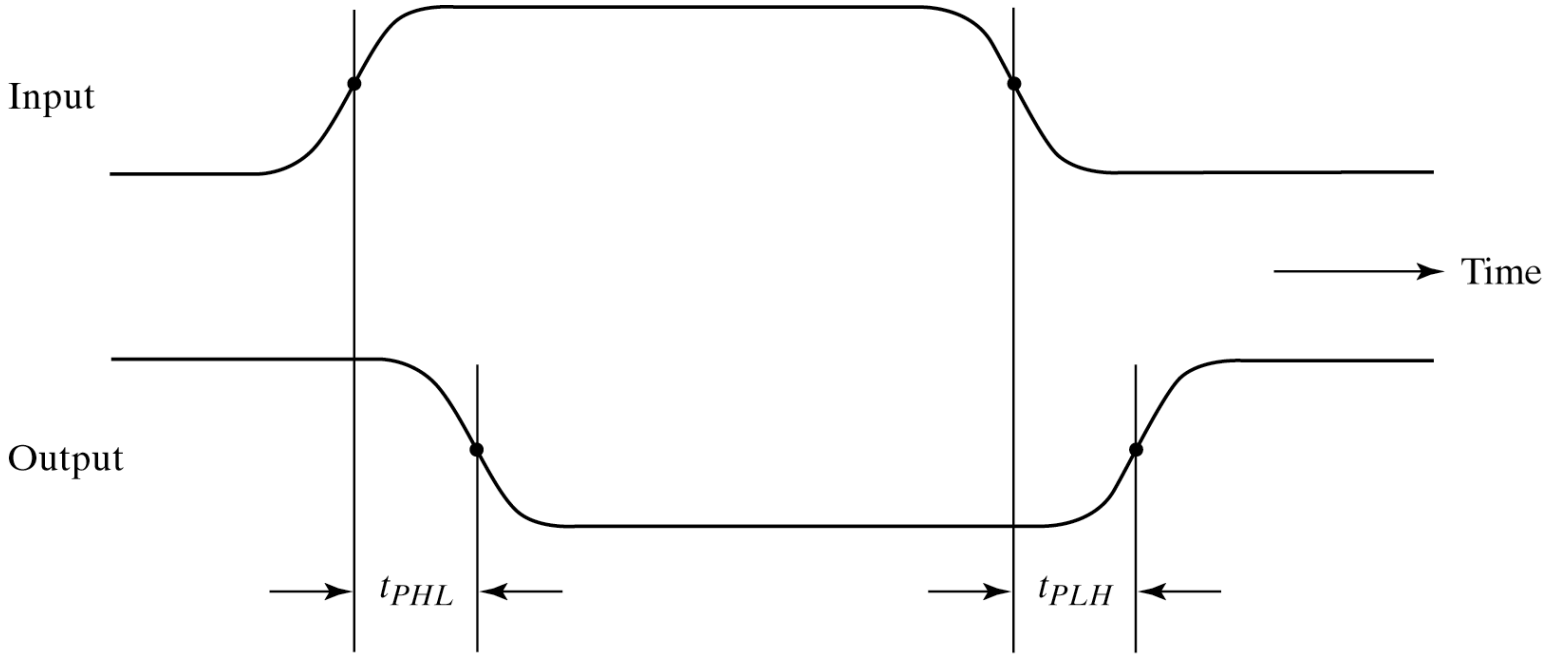
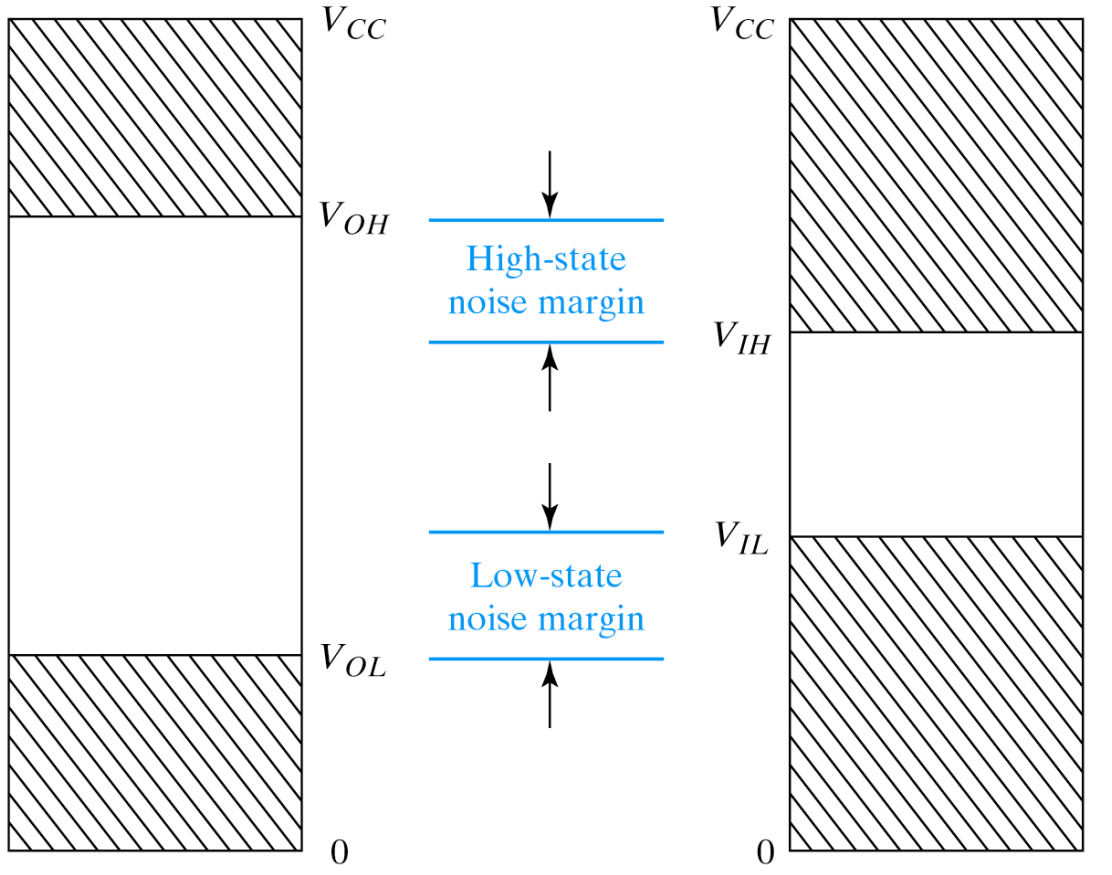


Fig. 10-4 Measurement of Propagation Delay



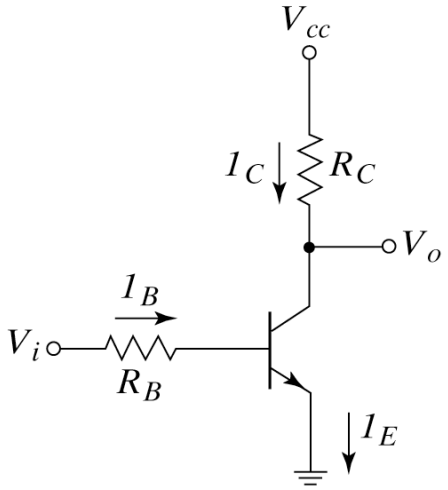
(a) Output voltage range (b) Input voltage range

Fig. 10-5 Signals for Evaluating Noise Margin

TTL LOGIC FAMILY

BJT

Characteristics



Base-Emitter voltage less than 0.6V => $I_B = 0$

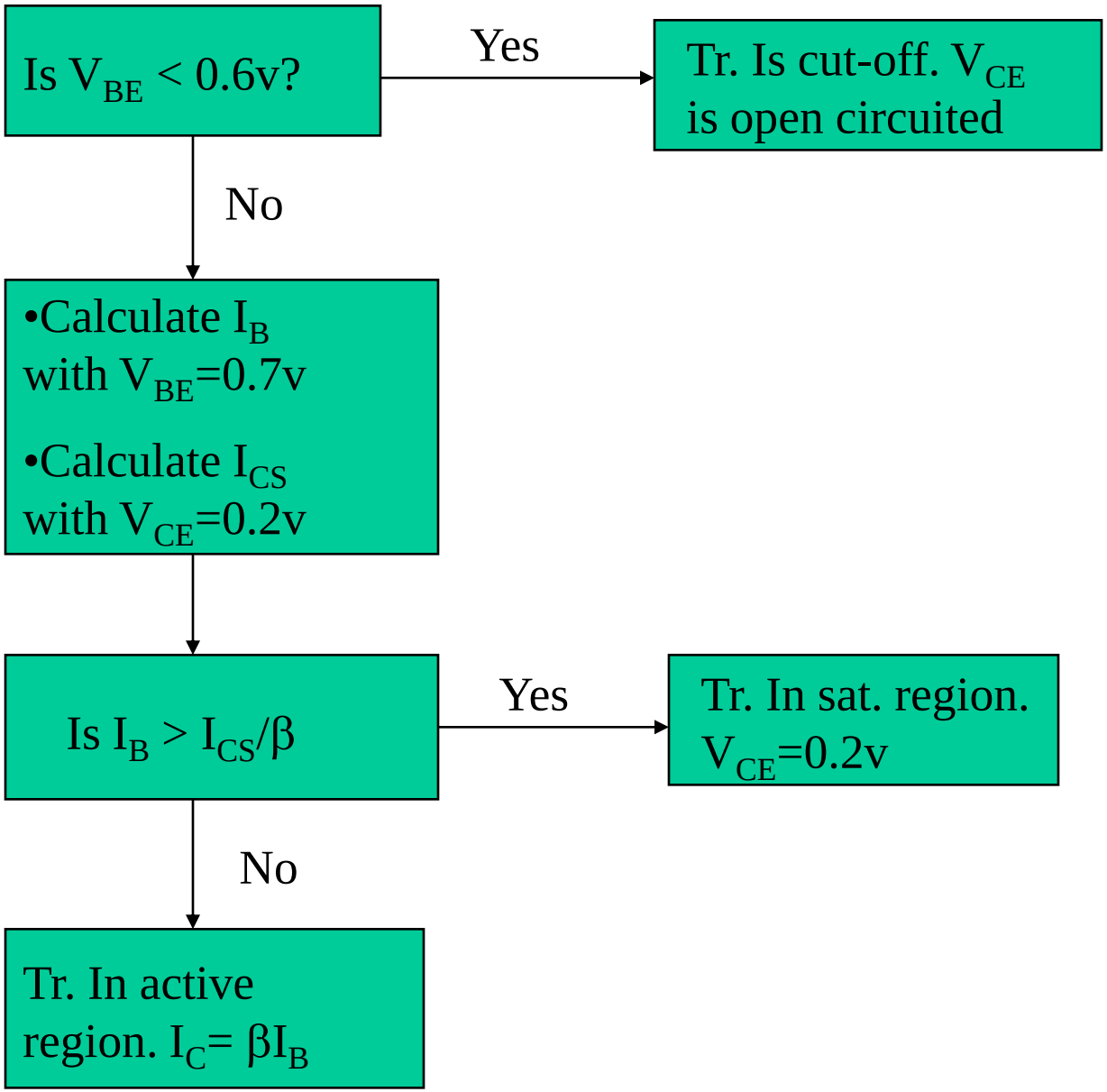
Cut-Off region

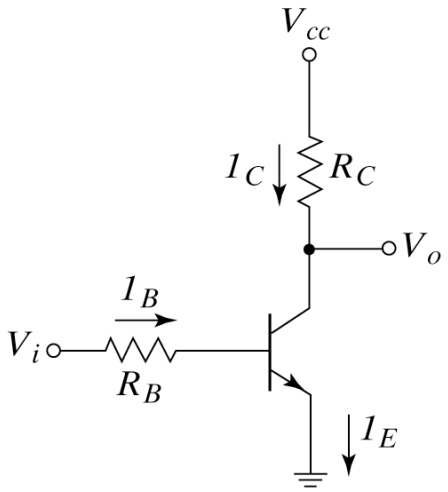
Base-Emitter voltage more than 0.6V, transistor starts Conducting -

active region $I_C = \beta I_B$

Maximum collector current $I_C = V_{CC}/R_C$

BJT operation analysis



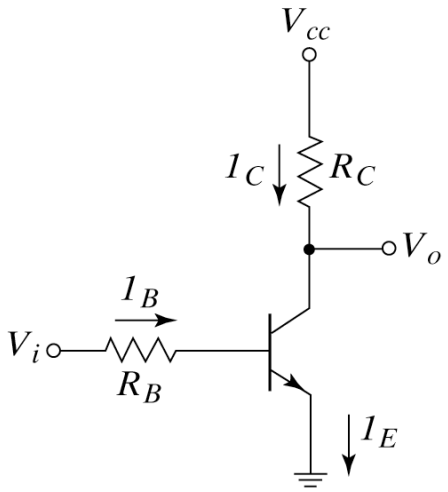


(a) Inverter circuit

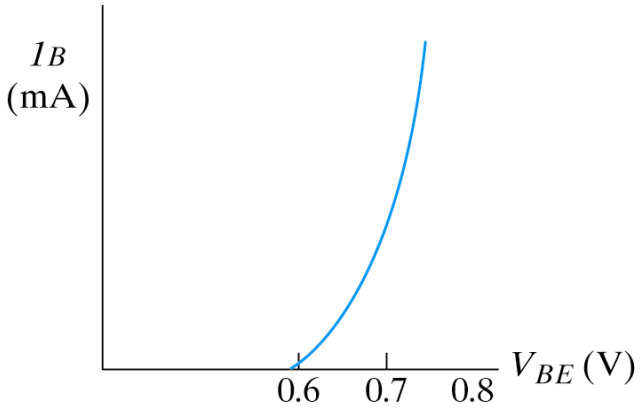
$R_C = 1k\Omega$, $R_B = 22k\Omega$, $\beta = 50$

$V_{CC} = 5V$, find V_O for

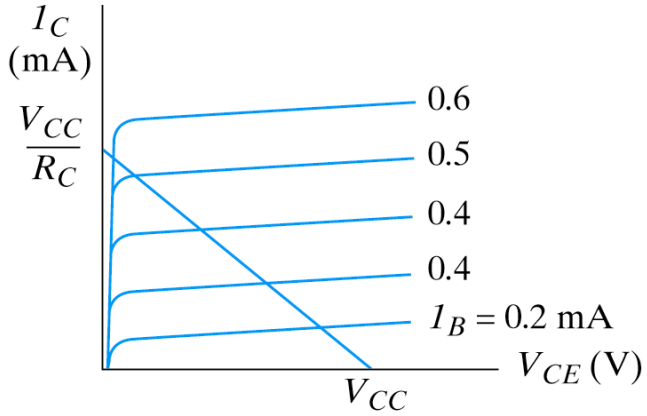
Vi = 0.2V and Vi = 5V



(a) Inverter circuit



(b) Transistor-base characteristic



(c) Transistor-collector characteristic

Fig. 10-6 Silicon *npn* Transistor Characteristics

In the cut-off region $V_{BE} < 0.6V$,
V_{CE} – open circuit, I_C, I_B negligible

In the active region V_{BE} about 0.7
V_{CE} wide range and $I_C = \beta I_B$

In the saturation region V_{BE} hardly changes,
$V_{CE} = 0.2V$

TTL Series name	Prefix
Standard	74
Low-power	74L
High-speed	74H
Schottky	74S
Low-power Schottky	74LS
Advanced Schottky	74AS
Advanced Low power- Schottky	74ALS
Fast	74F

Three Types of TTL gates

- Open - collector output

- Totem- pole output

- Three- state output

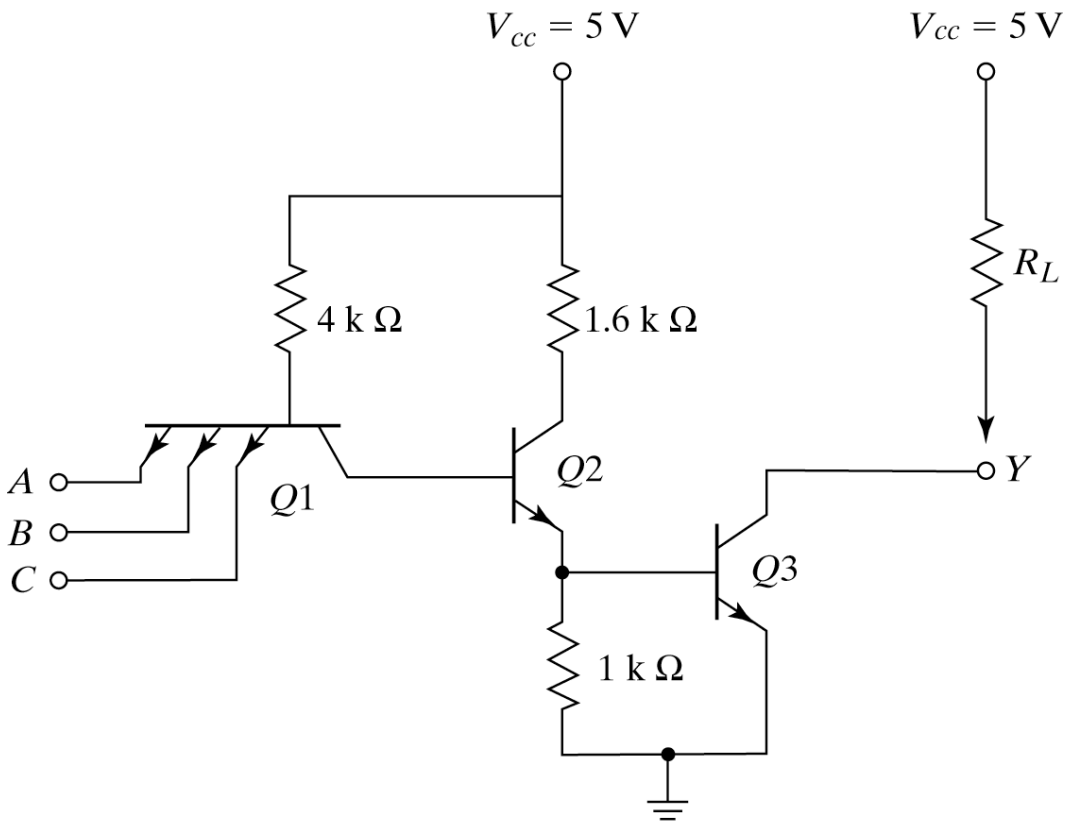


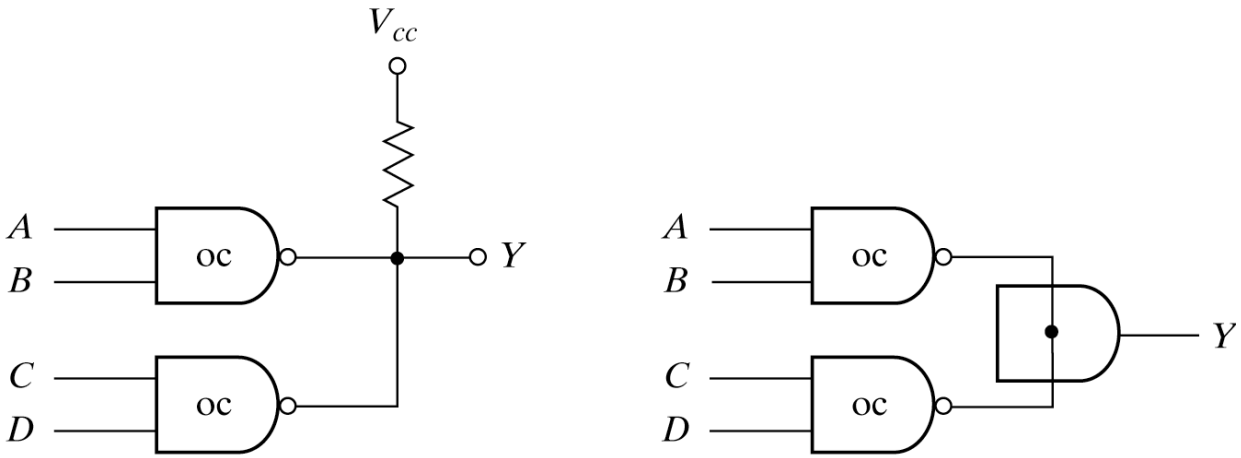
Fig. 10-11 Open-Collector TTL Gate

Open Collector gates are used

-Driving relays and lamps

-Wire ANDing

-Construction of common bus system



(a) Physical connection (b) Wired-logic graphic symbol

Fig. 10-12 Wired-AND of two Open-Collector (oc) Gates, $Y = (AB + CD)'$

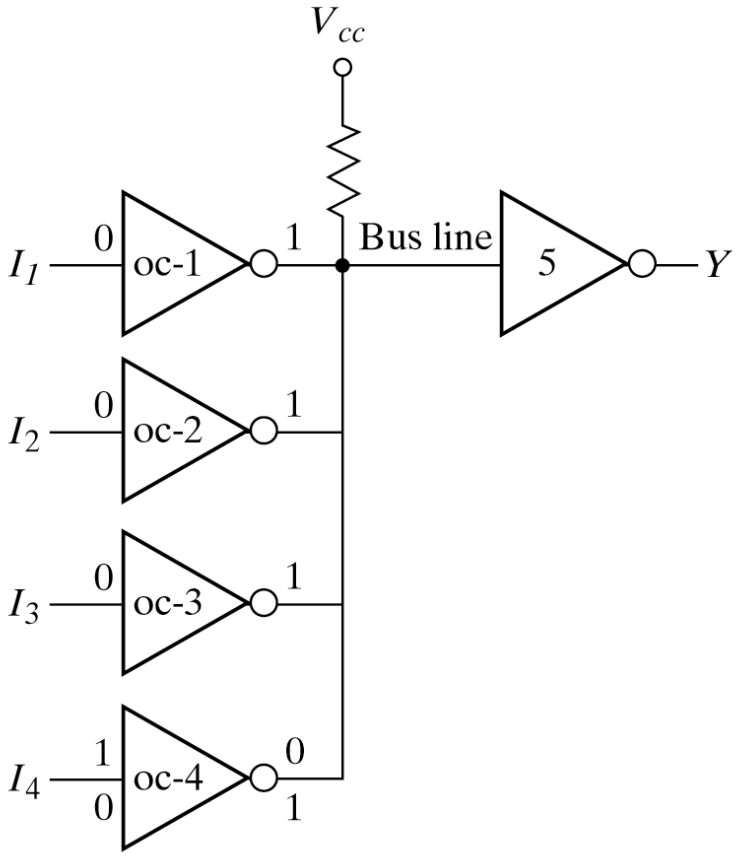


Fig. 10-13 Open-Collector Gates Forming a Common Bus Line

Output impedance of a gate is resistive plus Capacitive load

For output low to high transition C charges Exponentially through RC

R is R_L (external) in open collector

With active pull-up delay can be reduced

Totem Pole

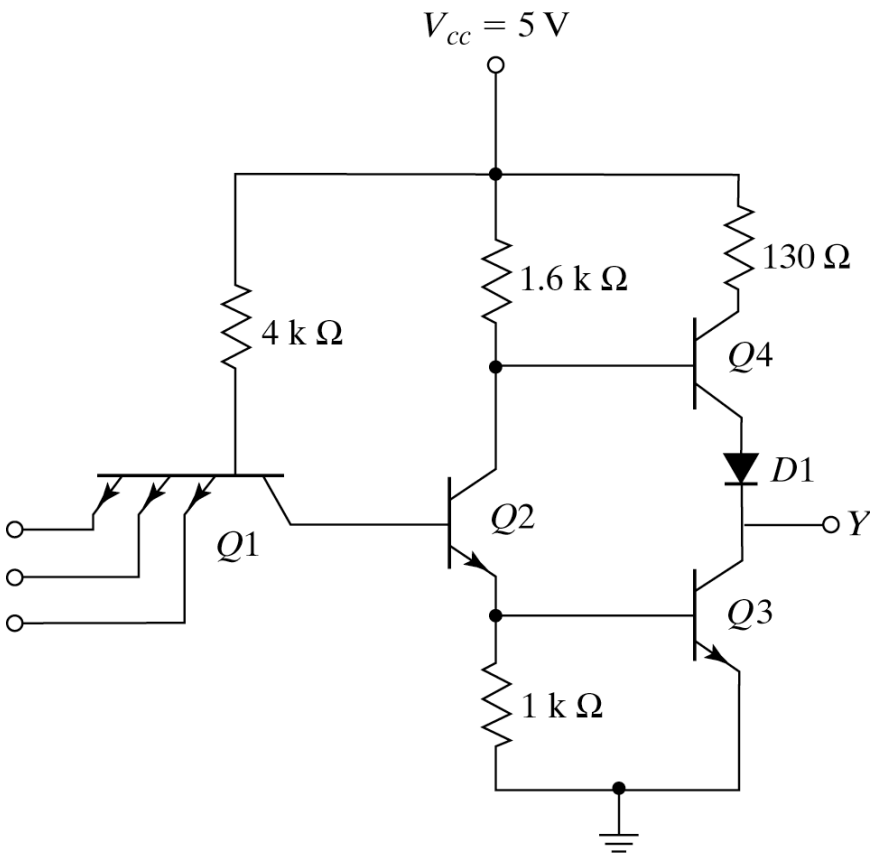


Fig. 10-14 TTL Gate with Totem-Pole Output

Wired Logic not allowed in Totem pole gates

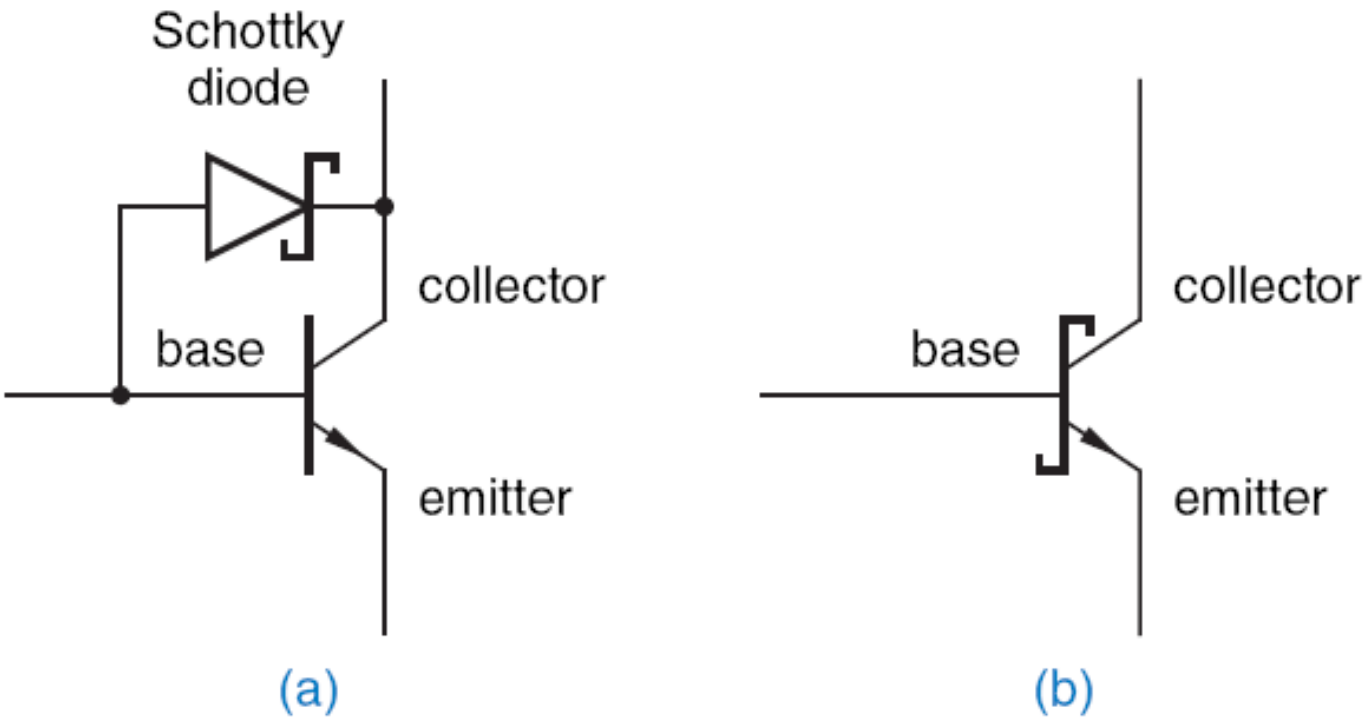
-excessive current drawn by one gate can damage it

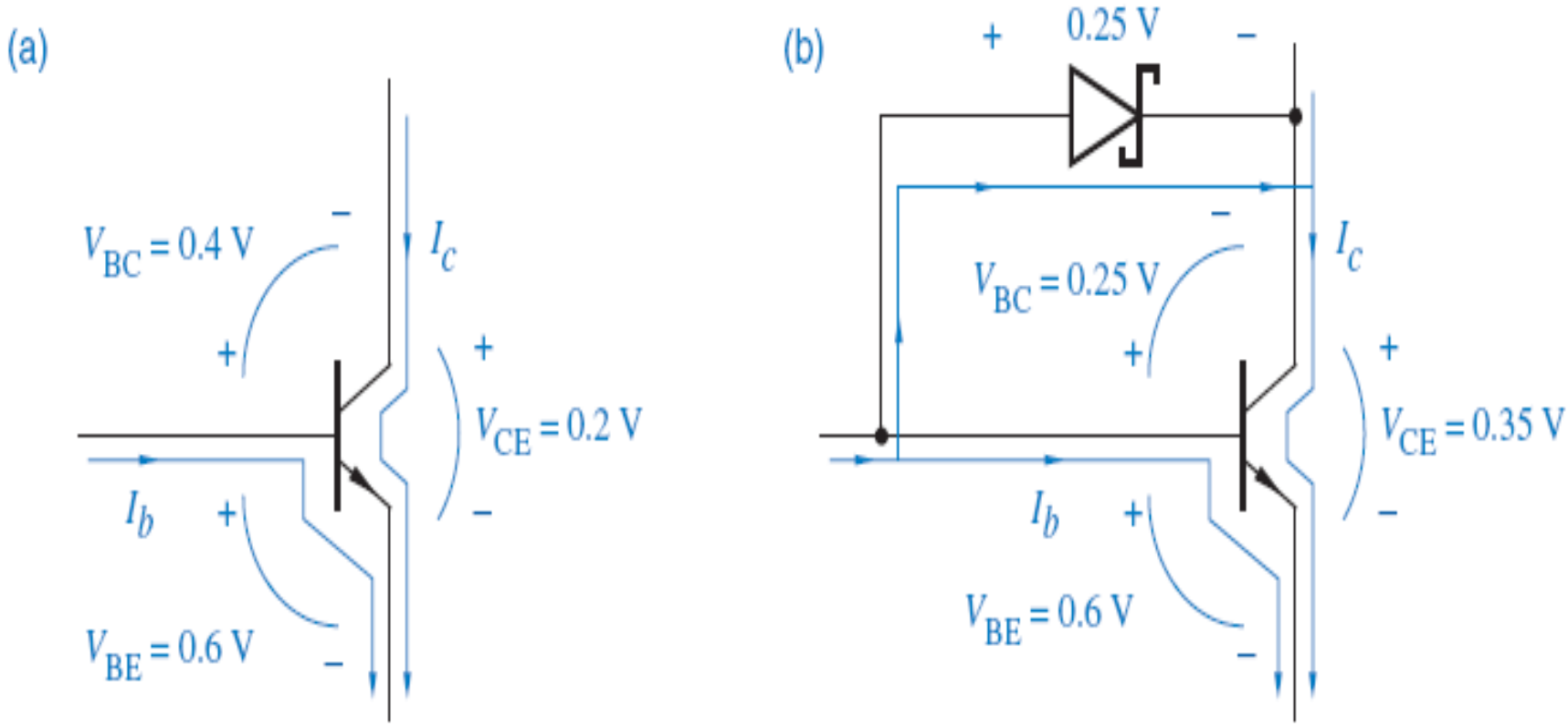
- **Reduction in storage time –reduction in Propagation delay**

- **Schottky diode- metal semiconductor junction**

- **Schottky transistor- Schottky diode between base and collector**

- **Schottky TTL**


Schottky
diode
collector
base
emitter
(a)
collector
base
emitter
(b)


(a)
$V_{BC} = 0.4$ V
I_c
$V_{CE} = 0.2$ V
I_b
$V_{BE} = 0.6$ V
(b)
0.25 V
$V_{BC} = 0.25$ V
I_c
$V_{CE} = 0.35$ V
I_b
$V_{BE} = 0.6$ V

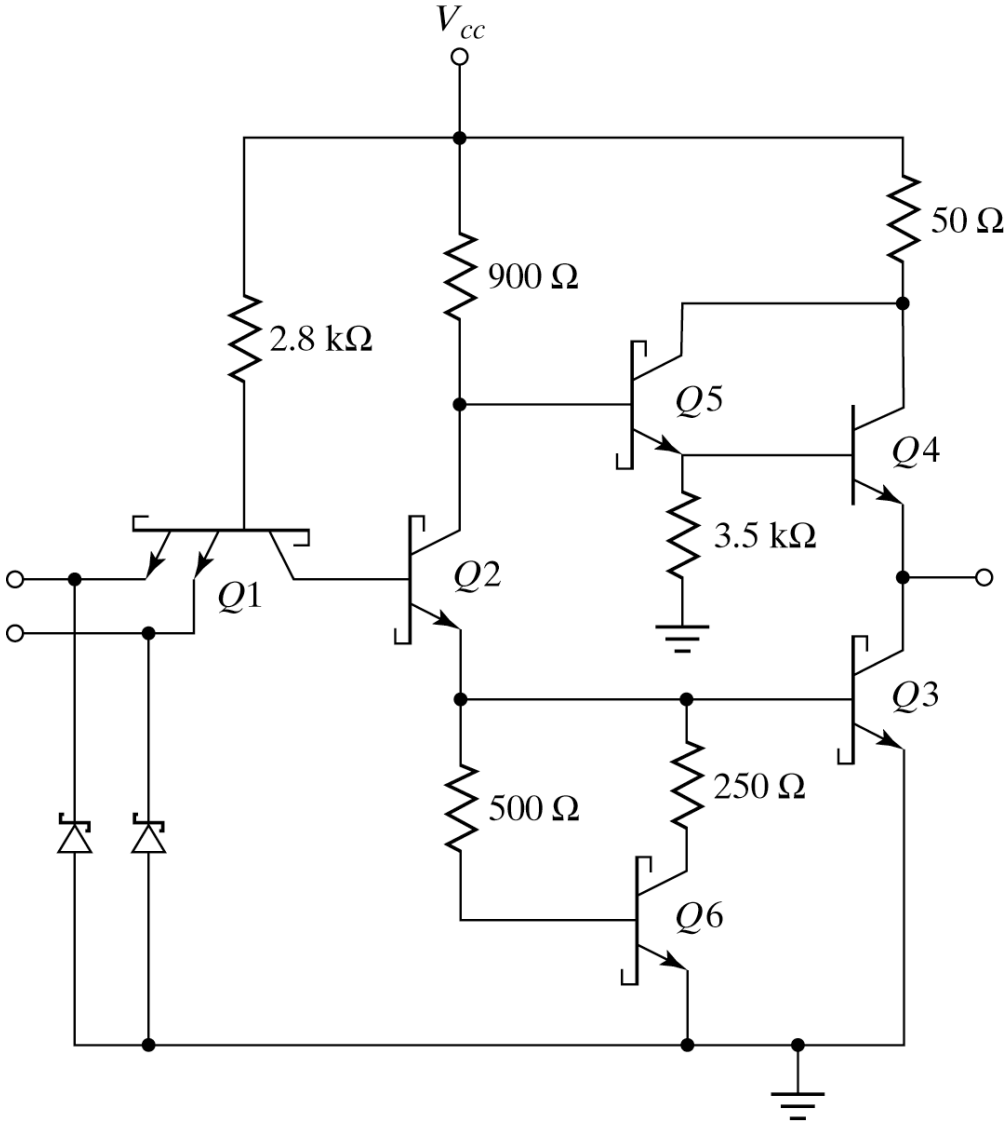
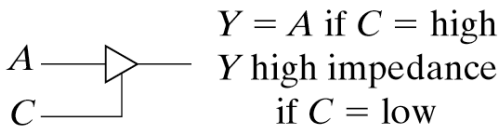
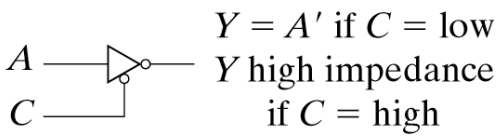


Fig. 10-15 Schottky TTL Gate

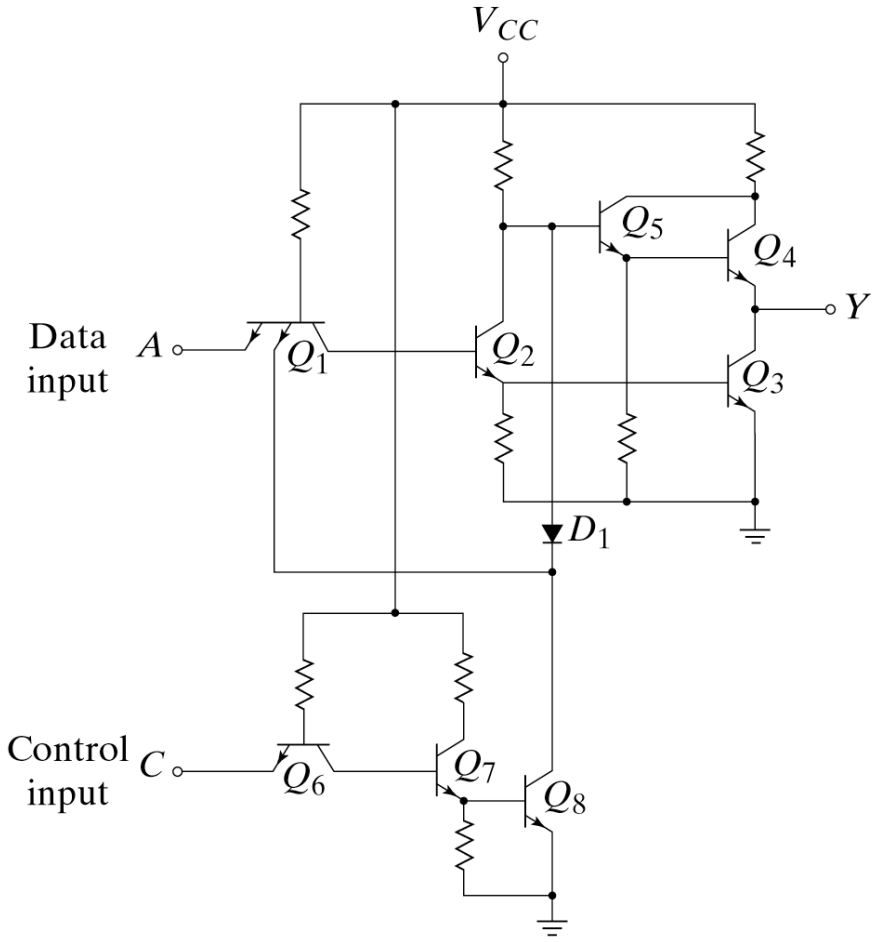
M. Morris Mano
DIGITAL DESIGN, 3e.



(a) Three-state buffer gate

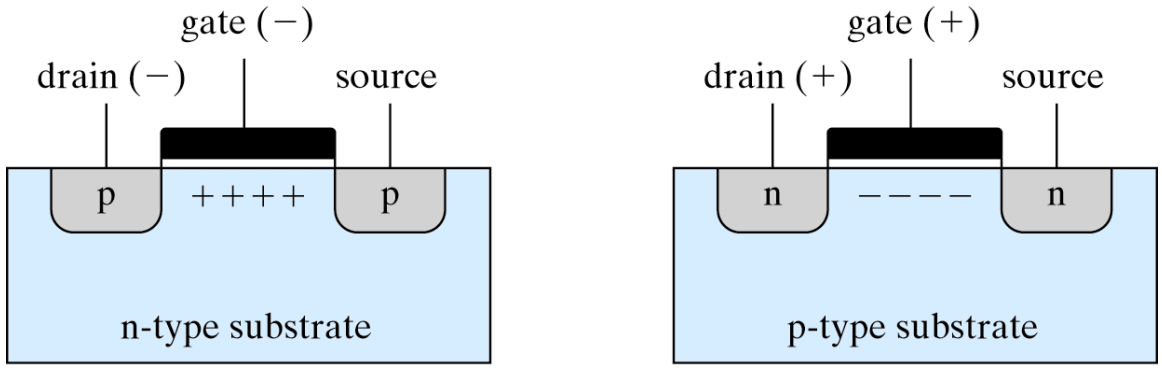


(b) Three-state inverter gate



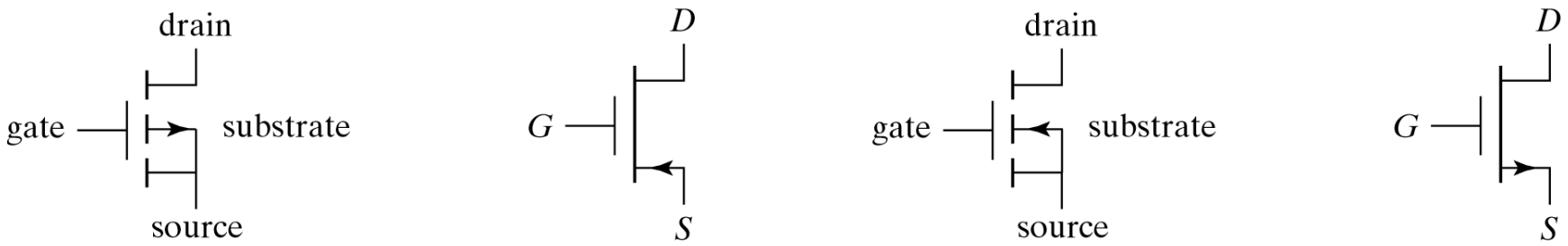
(c) Circuit diagram for the three-state inverter of (b)

Fig. 10-16 Three-State TTL Gate



(a) p-channel (b) n-channel

Fig. 10-19 Basic Structure of MOS Transistor



(a) p-channel (b) n-channel

Fig. 10-20 Symbols for MOS Transistors

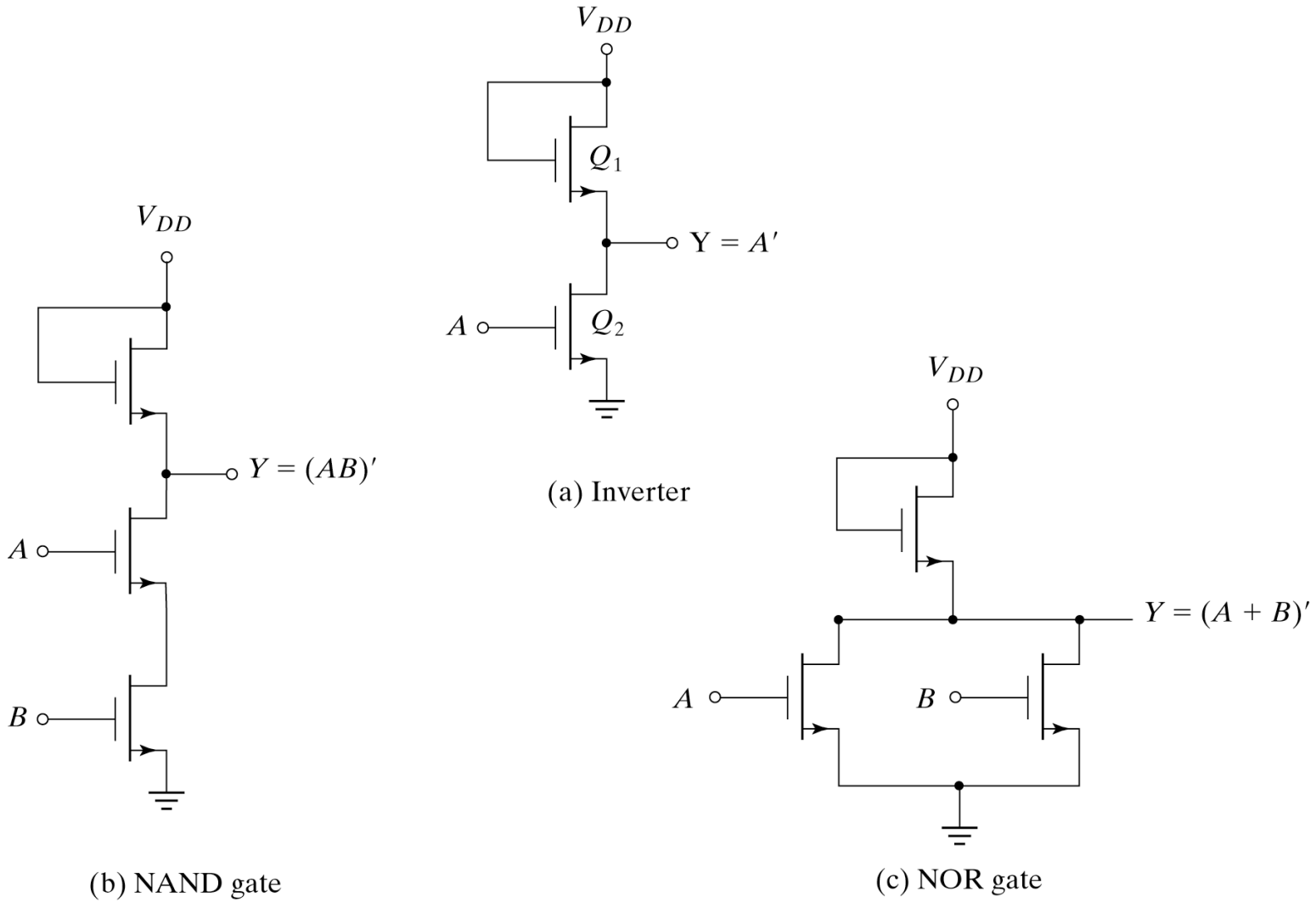
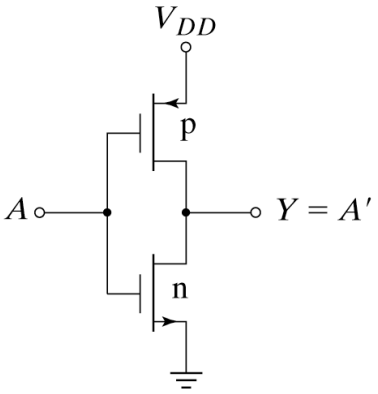
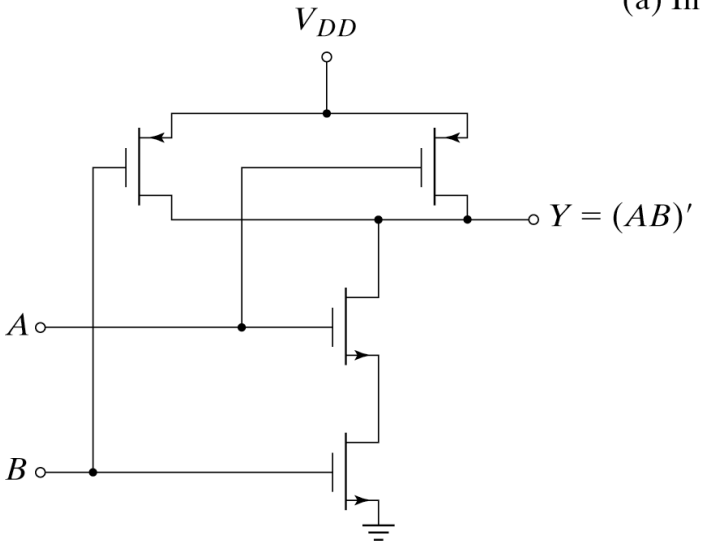


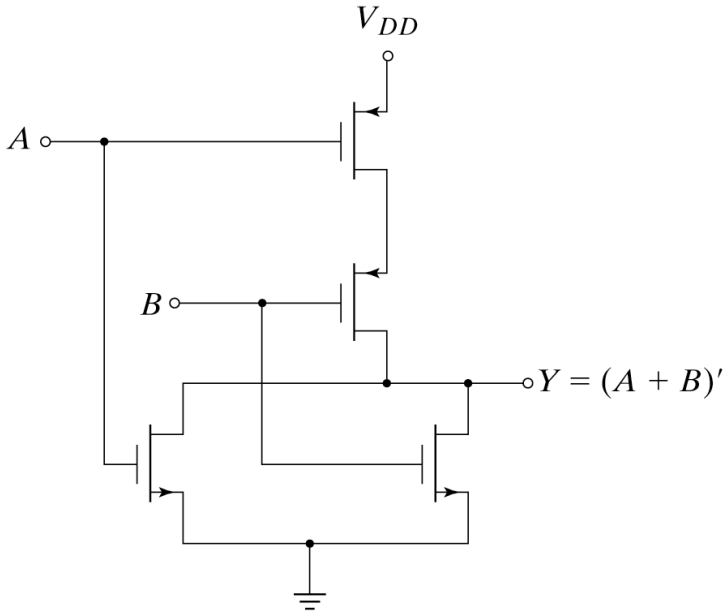
Fig. 10-21 n-channel MOS Logic Circuits



(a) Inverter

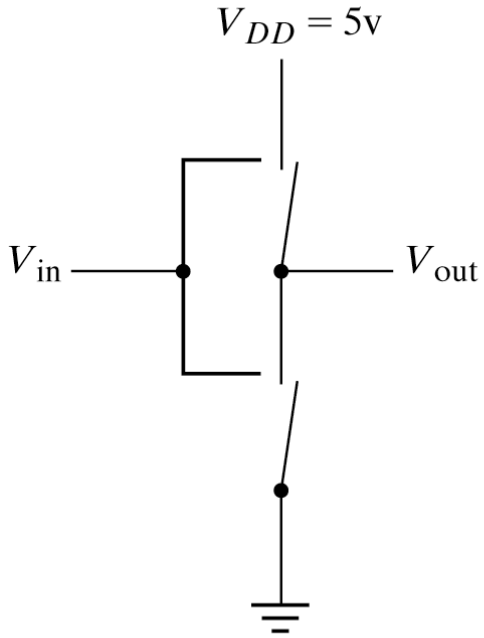


(b) NAND gate

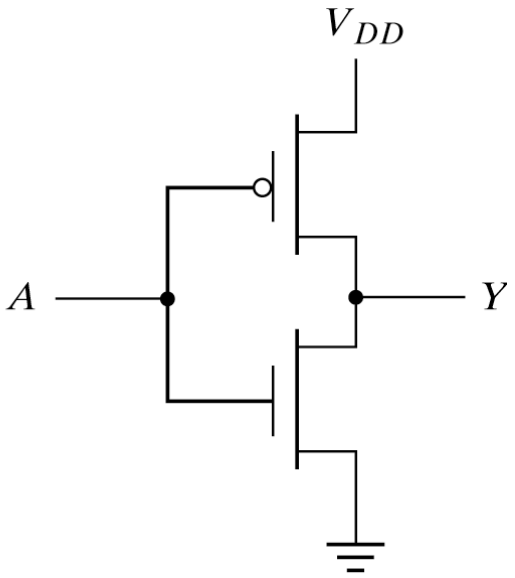


(c) NOR gate

Fig. 10-22 CMOS Logic Circuits



(a) Switch model



(b) Logical model

Fig. 10-23 *CMOS* inverter

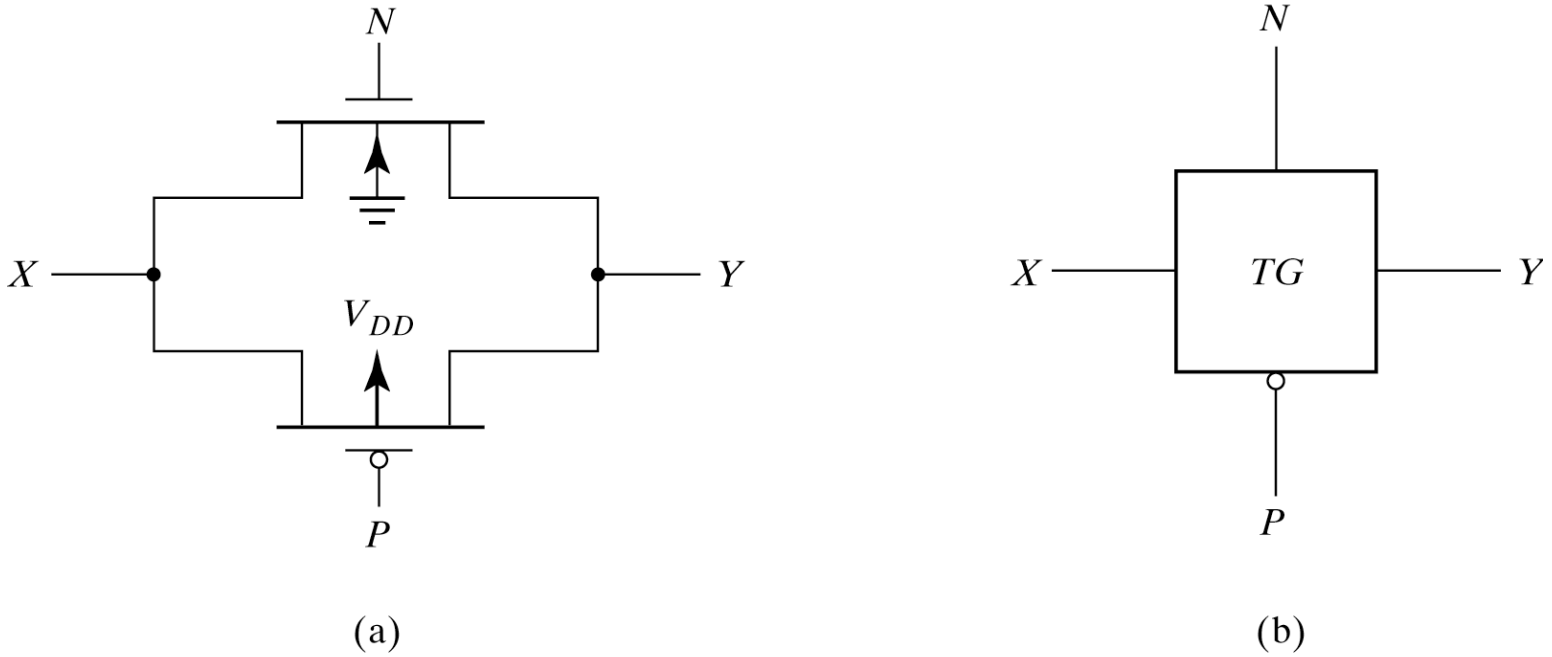


Fig. 10-24 Transmission Gate (TG)

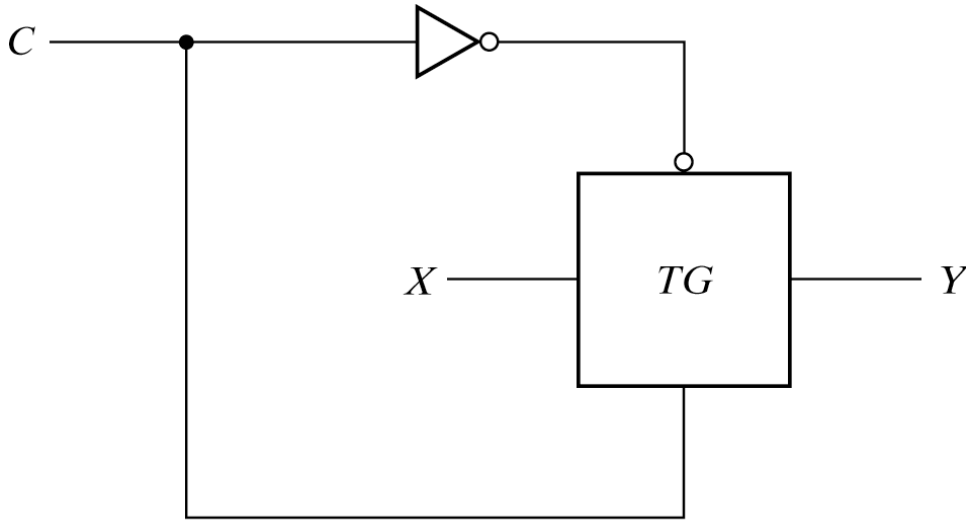
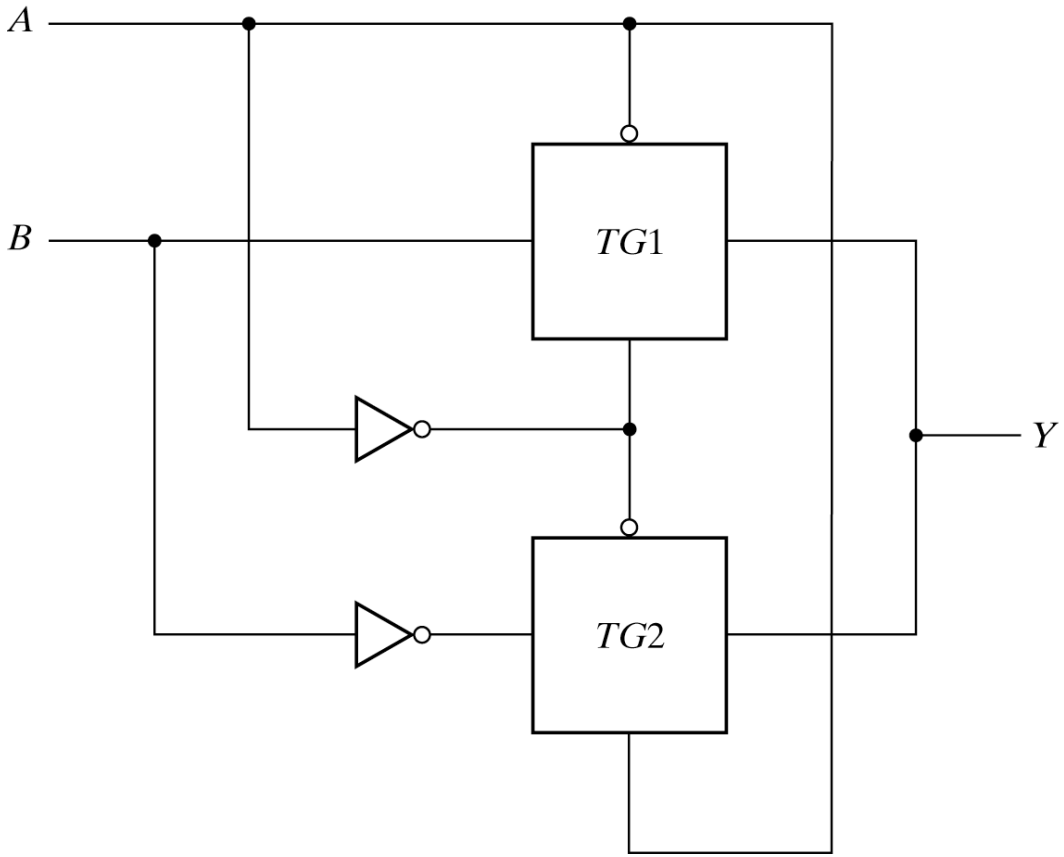


Fig. 10-25 Bilateral Switch



A	B	TG1	TG2	Y
0	0	close	open	0
0	1	close	open	1
1	0	open	close	1
1	1	open	close	0

Fig. 10-26 Exclusive-OR Constructed with Transmission Gates

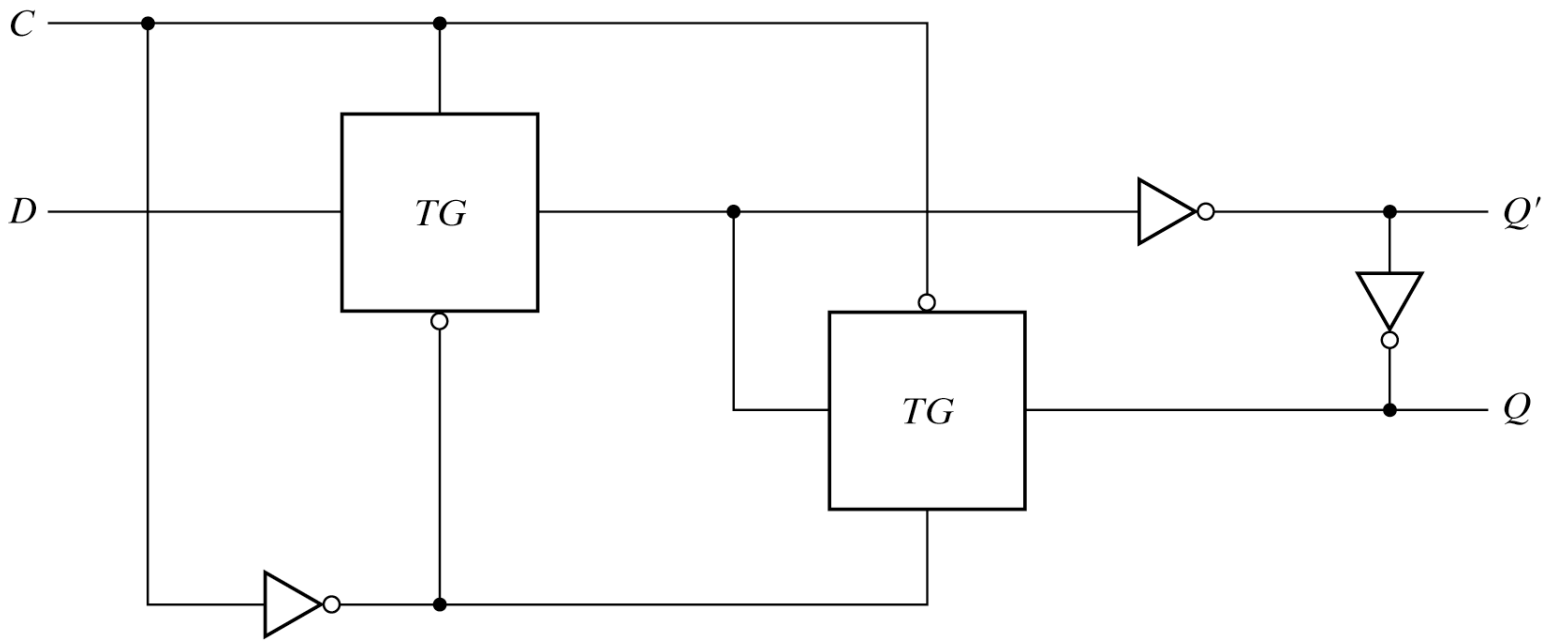


Fig. 10-28 Gated *D* Latch with Transmission Gates

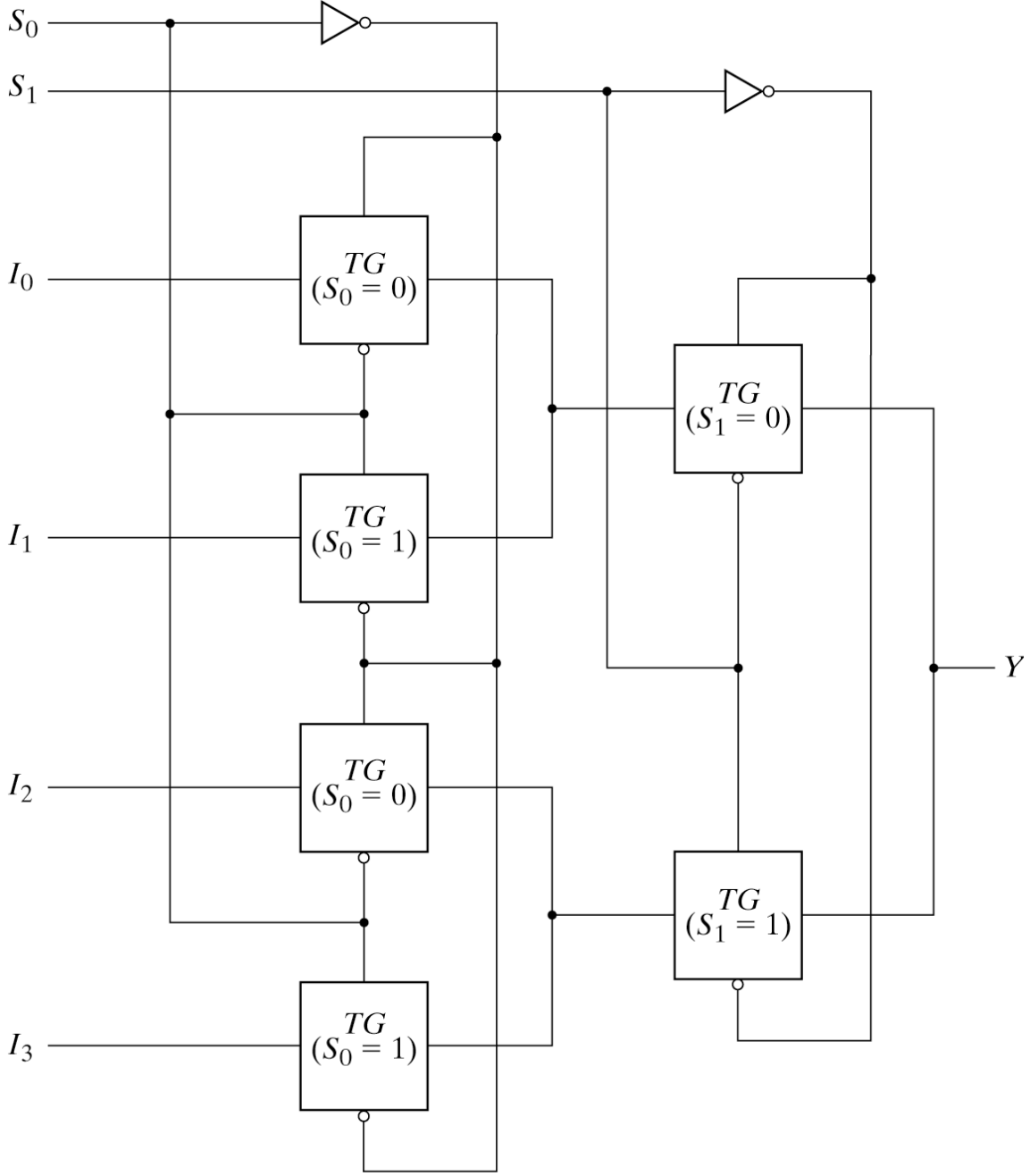


Fig. 10-27 Multiplexer with Transmission Gates