MEMORY HIERARCHY

Memory Hierarchy

- Registers
  - In CPU
- Primary Memory
  - May include one or more levels of cache
  - “RAM”
- Secondary memory
  - Magnetic/Optical

CACHE:

-High Speed Memory (SRAMs)

-Small in Size

-High cost

MAIN MEMORY

-High density (DRAMs)

-Low cost

-Slower than Cache.

RAM

Static RAM

- Bits stored as on/off switches
- No charges to leak
- No refreshing needed when powered
- More complex construction
- Larger per bit
- More expensive
- Does not need refresh circuits
- Faster
- Cache

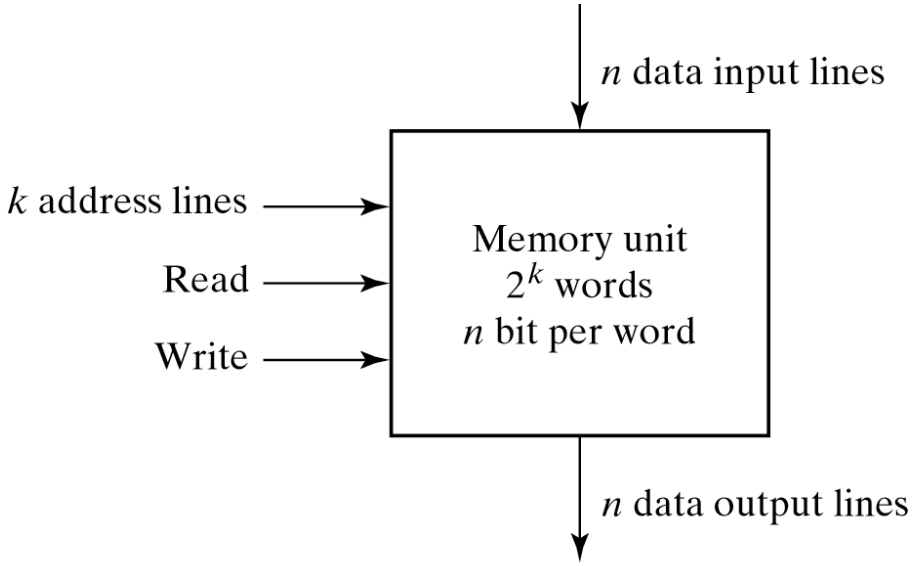
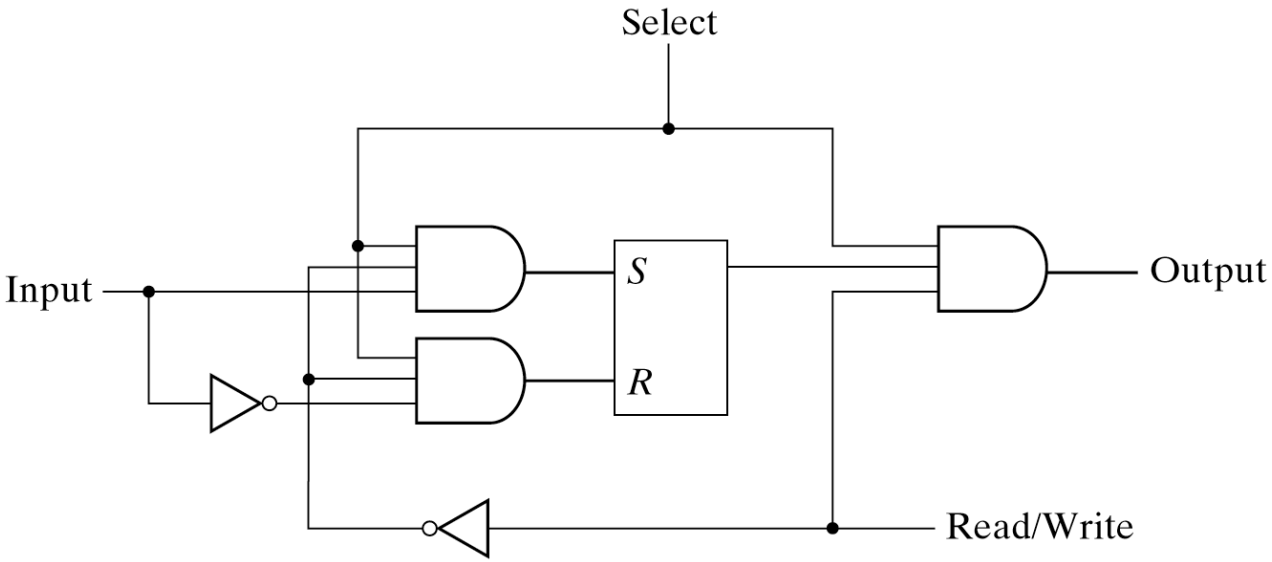


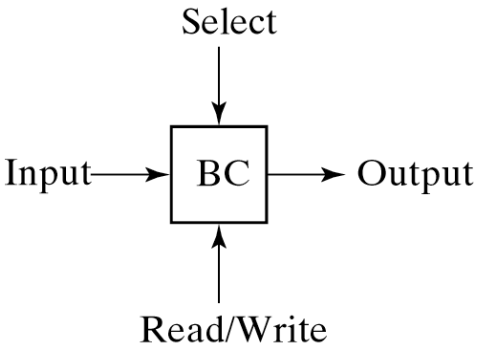
Fig. 7-2 Block Diagram of a Memory Unit

Memory address		
Binary	decimal	Memory contest
0000000000	0	1011010101011101
0000000001	1	1010101110001001
0000000010	2	0000110101000110
⋮	⋮	⋮
1111111101	1021	1001110100010100
1111111110	1022	0000110100011110
1111111111	1023	1101111000100101

Fig. 7-3 Content of a 1024 × 16 Memory



(a) Logic diagram



(b) Block diagram

Fig. 7-5 Memory Cell

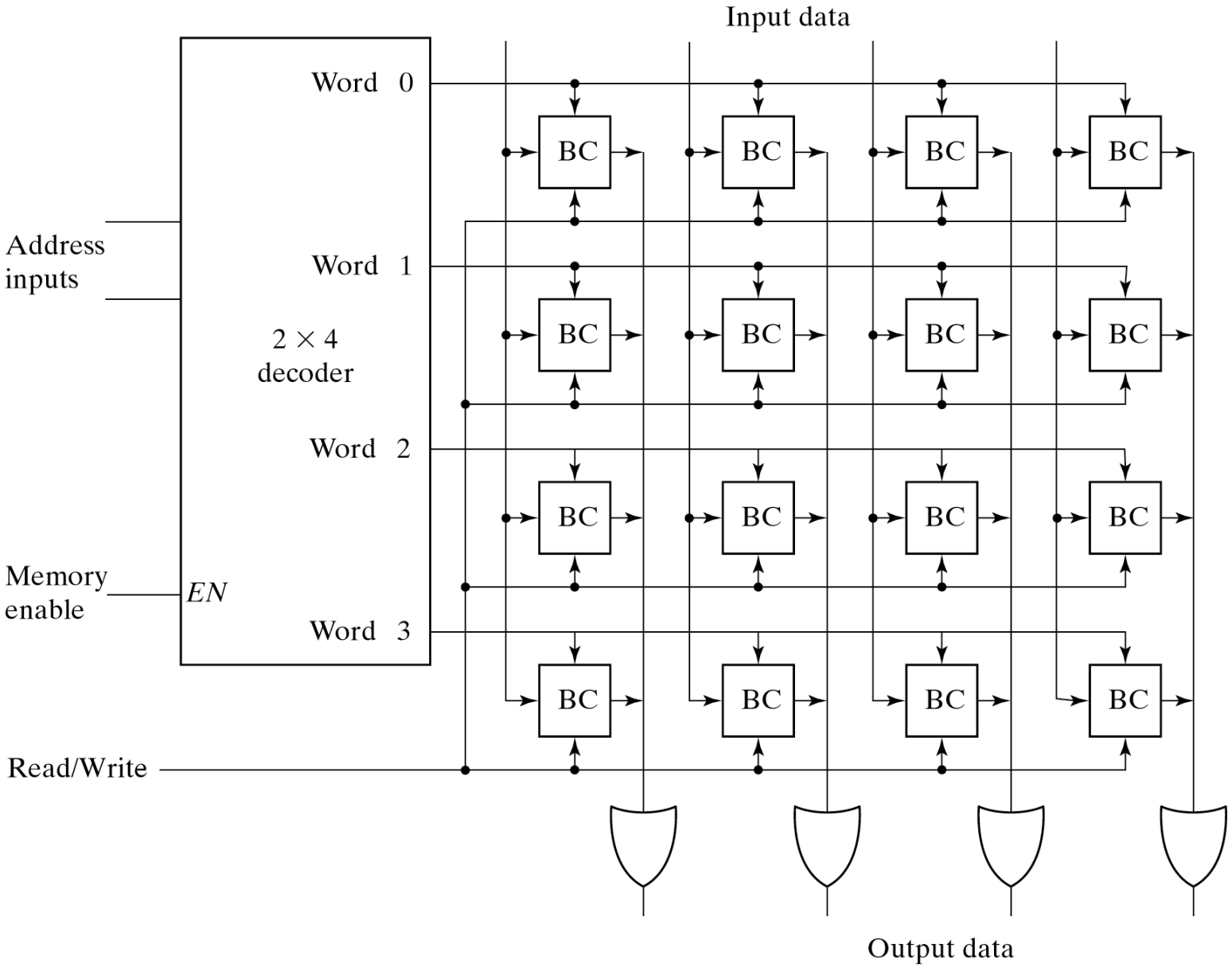
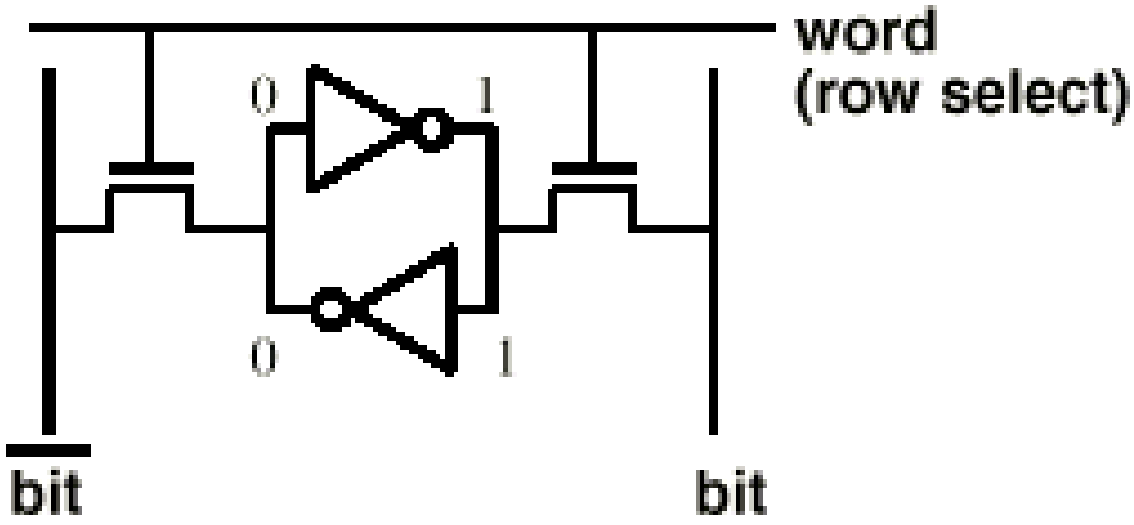
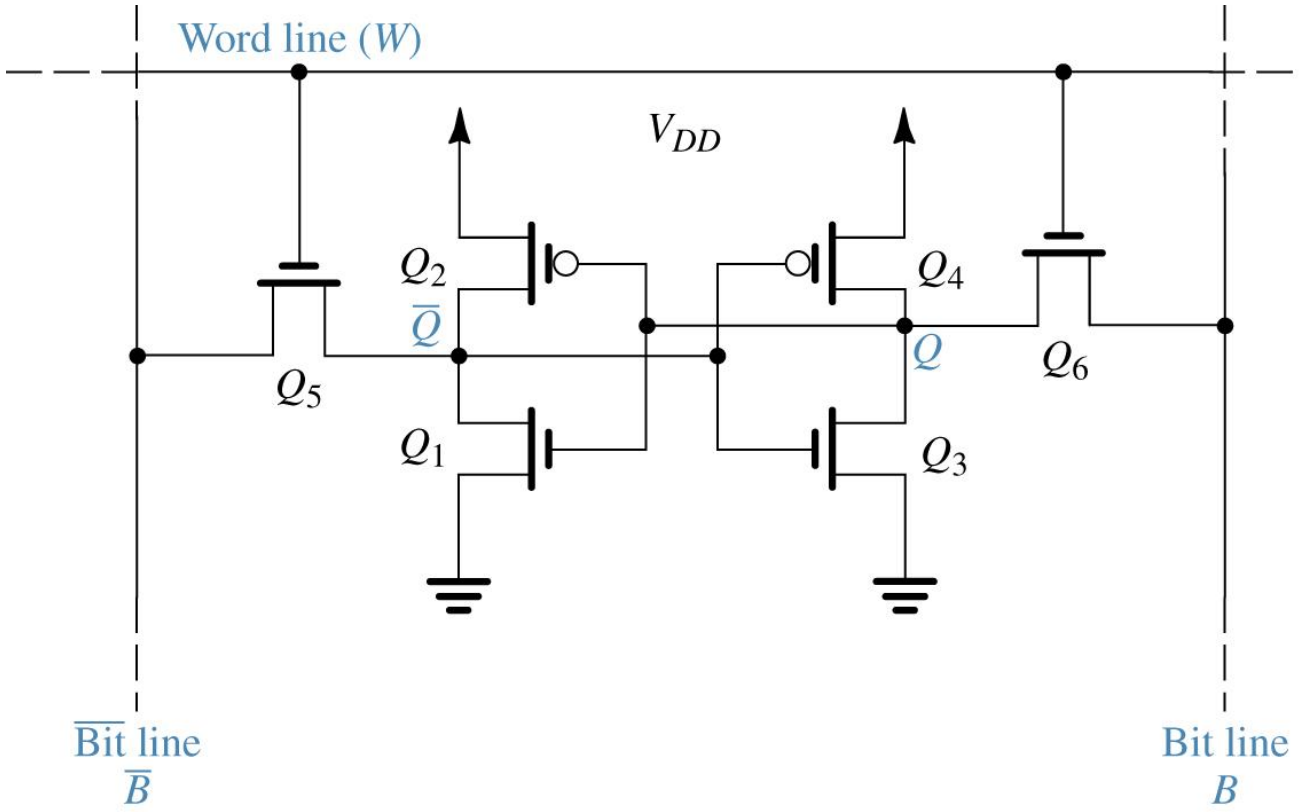


Fig. 7-6 Diagram of a 4 × 4 RAM

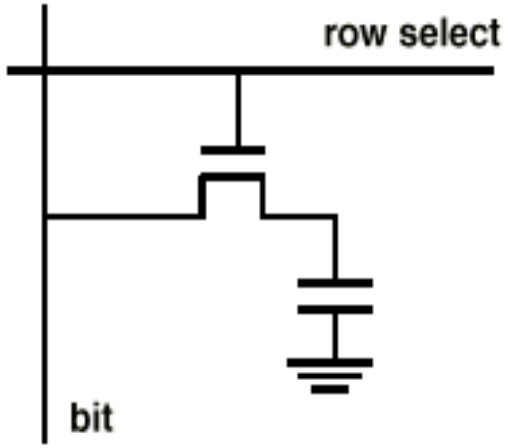
Static RAM Cell

6-Transistor SRAM Cell

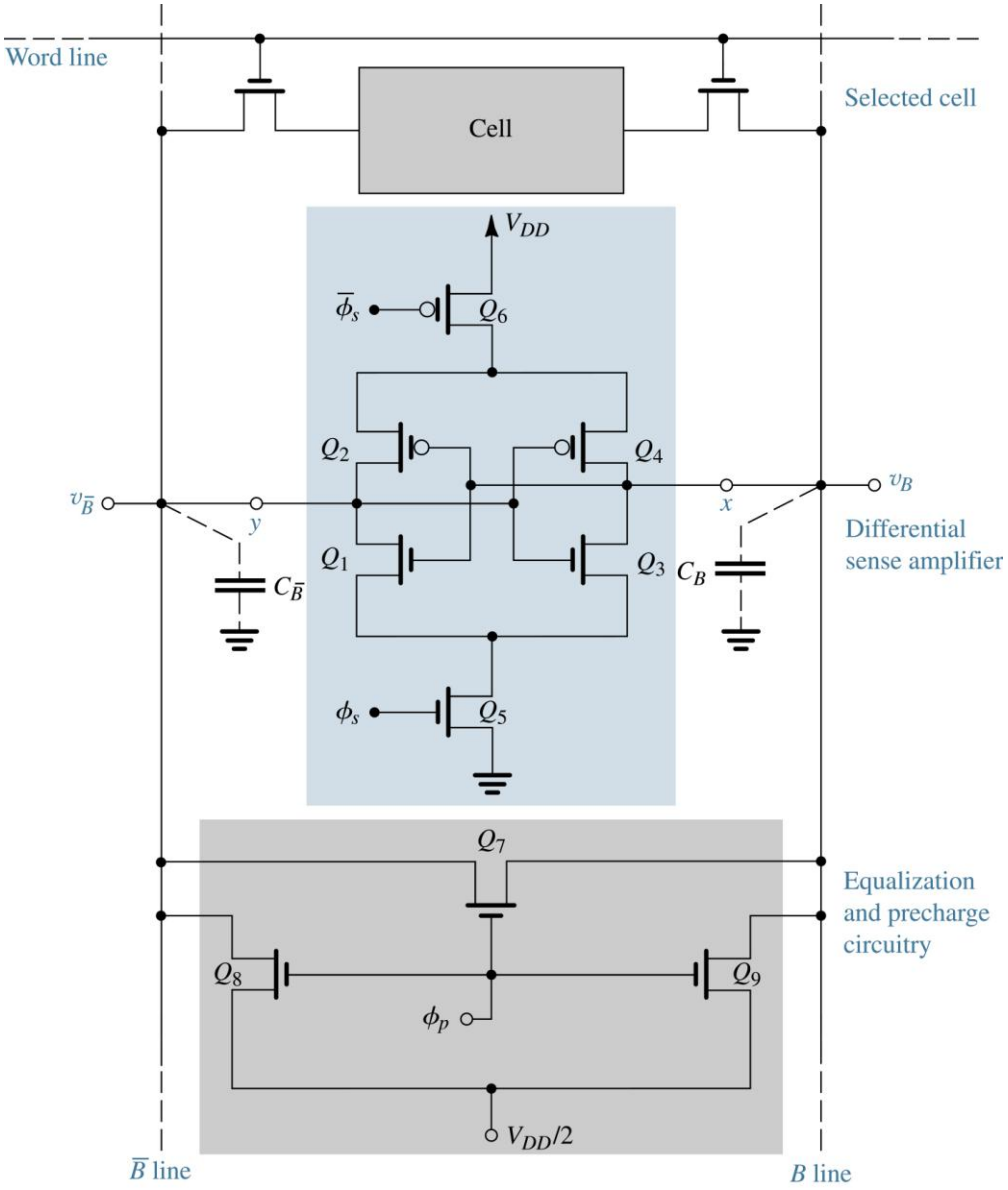


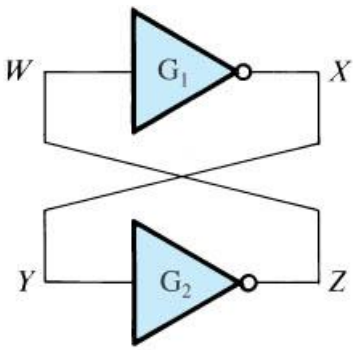

Word line (W)
V_{DD}
Q_2
$\overline{Q}$
Q_4
Q
Q_5
Q_6
Q_1
Q_3
$\overline{\text{Bit line}}$
$\overline{B}$
Bit line
B

1-Transistor Memory Cell (DRAM)

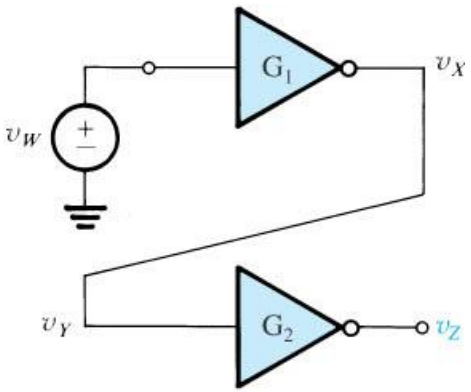


- Write:
  1. Drive bit line
  2. Select row
- Read:
  1. Precharge bit line to Vdd
  2. Select row
  3. Cell and bit line share charges
     Very small voltage changes on the bit line
  4. Sense (fancy sense amp)
  5. Write: restore the value
- Refresh
  1. Just do a dummy read to every cell.

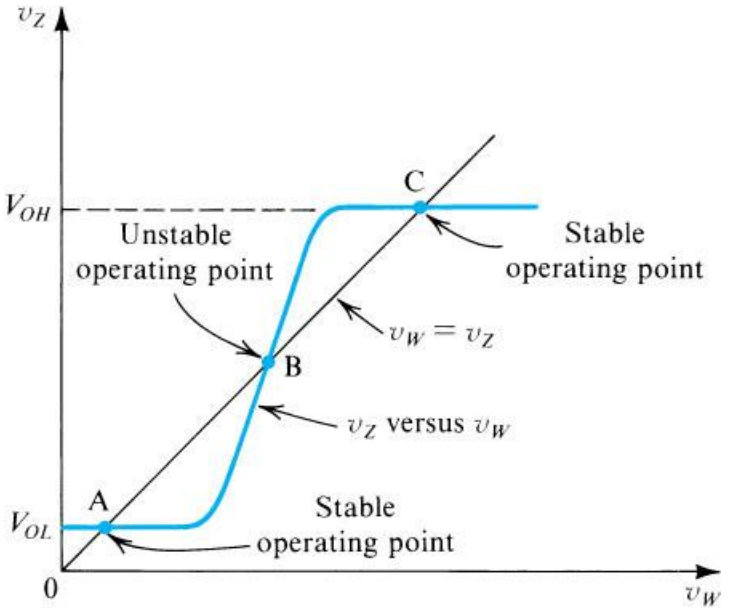

Word line
Cell
Selected cell
V_{DD}
$\overline{\phi}_s$
Q_6
Q_2
Q_4
$v_{\overline{B}}$
y
x
v_B
Differential sense amplifier
Q_1
Q_3
$C_{\overline{B}}$
C_B
ϕ_s
Q_5
Q_7
Equalization and precharge circuitry
Q_8
Q_9
ϕ_p
$V_{DD}/2$
$\overline{B}$ line
B line


W
G1
X
Y
G2
Z

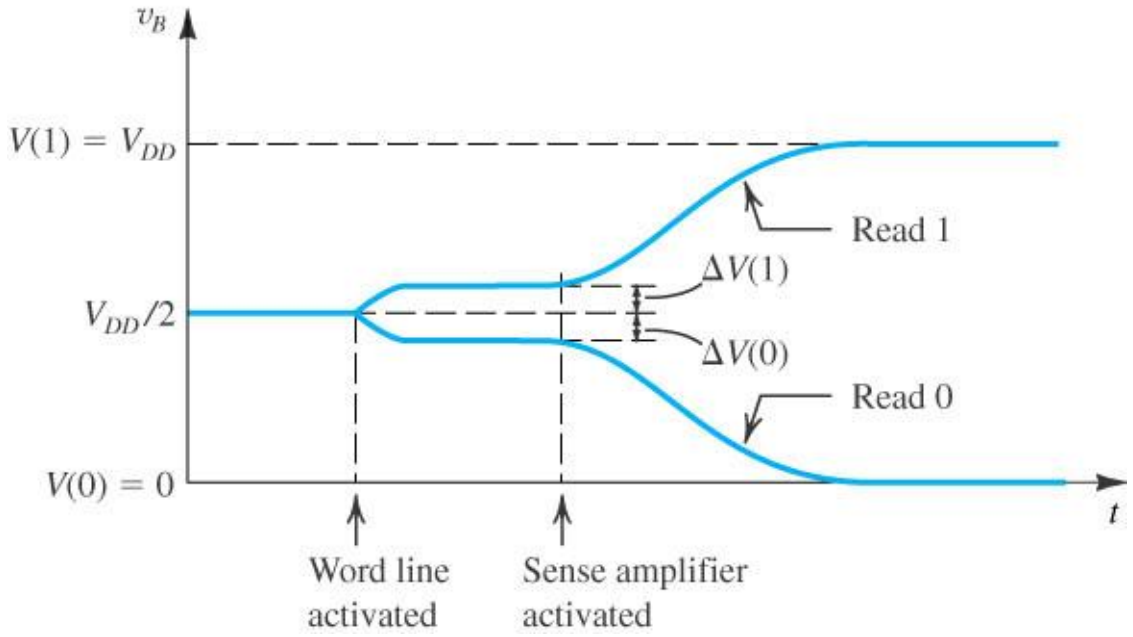
(a)


G1
vX
vW
+
−
vY
G2
vZ

(b)


vZ
VOH
C
Unstable
operating point
Stable
operating point
vW = vZ
B
vZ versus vW
A
VOL
Stable
operating point
0
vW

(c)


v_B
$V(1) = V_{DD}$
$V_{DD}/2$
$V(0) = 0$
Read 1
$\Delta V(1)$
$\Delta V(0)$
Read 0
t
Word line activated
Sense amplifier activated