iOBC-DB Interface Control Document: HOOPOE

ISIS.iOBC-DB.HOOPOE.ICD.001

Issue 1.0

Release information

Written by:	V. Karunanithi	2015-06-15
Checked by:	E. Bertels	2015-06-16
Approved by:	A.R. Bonnema	2015-06-16

Distribution List:

Change log

Date	Issue	Modified by	Section / Pages Affected	Reason for Change
2015-06-16	1.0	V.Karunanithi	All	First Release

Disclaimer

The contents of this document are subject to the relevant provisions in the contract concluded between the parties. ISIS – Innovative Solutions In Space B.V. (“ISIS”) shall not be liable, in full or in part, for any damage arising out from the application or use of any product or circuit described herein, in case such application or use are carried out in a manner not in line with the instructions and warranties provided in the User Manual, Safety Manual, product information sheets or any other document provided by ISIS upon the delivery of the product (“Documents”). Further, ISIS shall not be liable for any damage caused by any use which exceeds the function(s) of the product, or does not conform to such function(s) as described in the Documents. ISIS shall not be liable for any damage arising from a use which is not carried out in a manner conforming to acceptable practices in the aerospace industry.

ISIS warrants that the product is supplied after relevant tests had shown the product is in good order and functioning, as far as these tests may indicate and predict product functionality.

List of Acronyms

1/2/3U	1-Unit, 2-Unit, 3-Unit; commonly referring to the singles and multiples of the commercially available CubeSat sizes
ABF	Apply Before Flight
ADC	Analog Digital Conversion
ADCS	Attitude Determination and Control Subsystem
CDR	Critical Design Review
GND	Ground
GPIO	General Purpose Input Output
ICD	Interface Control Document
INMS	Ion/Neutral Mass Spectrometer
INTR	Interrupt
ISIS	Innovative Solutions In Space B.V.
MSSL	Mullard Space Science Laboratory
PWM	Pulse Width Modulation
RTD	Resistance Temperature Detectors
SPI	Serial Peripheral Interface
TBD	To Be Determined
TRX	Transmit
UART	Universal asynchronous receiver/transmitter
USB	Universal Serial Bus
VBAT	Battery voltage
VBUS	Bus Voltage

Table of Content

Table of Figures

Table of Tables

1 Introduction

1.1 Purpose and Scope of Document

This document describes the hardware interface connections and electrical characteristics of the ISIS On-board Computer Daughter Board (iOBC-DB). The daughter board is customized to the requirements of the QB50 payloads.

2 iOBC DB System interface overview

The figure below shows the block diagram of the functional blocks in the iOBC-DB. Following are the different functional units:

- Temperature measurement.
- 3.3V switch/regulator with current monitor.
- 5.0V switch/regulator with current monitor.
- ABF Schmitt trigger.

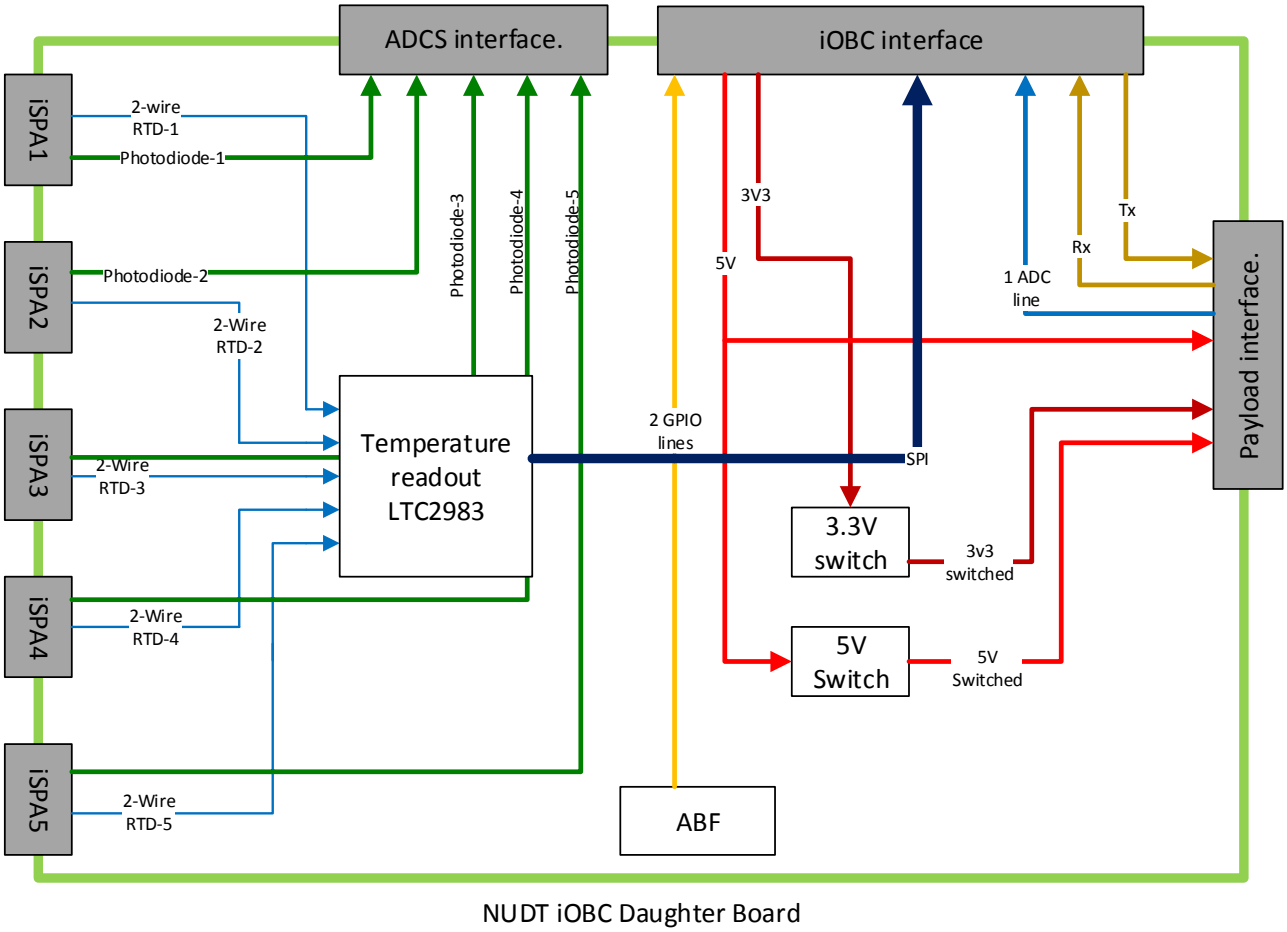

Figure 2-1: iOBC DB functional block diagram.

2.1 Temperature measurement sensor.

The need for an accurate temperature measurement and reducing the number of wires in the interface between iSPA and the iOBC has led to the design modification on the new iOBC daughterboard. The new daughter board design makes use of LTC2983 and 2-wire RTDs (Resistance Temperature Detector) to measure the panel's temperature. The LTC2983 cyclically measures the temperature from each of the RTD mounted on the iSPA and a single SPI line goes to the iOBC with temperature information. This is a centralized approach compared to the previous design where individual temperature sensors were mounted on the iSPA and they were accessible individually through I^2C.

2.2 3V3 & 5V switch and current monitor.

According to the QB50 payload requirements the payload needs to be powered through the iOBC and the current & voltage levels need to be monitored by the iOBC. The most stringent requirements are those applicable to the INMS. The requirements stated in document: “QB50-INMS-MSSL-ID-12001 Issue 10” that apply to this design are, Req ref: “INMS-I-110”, “INMS-I-115” and “INMS-I-114”. The designs for switches were reused from the daughter-board design for QB50p mission (flight-tested).

The Payload ICD specifies an inrush peak current of 4.02A on the 5V line, which was higher than what MAX890L (regulator) can provide. The maximum short circuit current the regulator is designed for is 1.3 A on the 5V line. The inrush current values mentioned in the INMS ICD were not stated as a requirement and there was ambiguity in the setup used to measure this.

Together with the payload provider it was decided to verify this situation using the QB50p EM setup and probe the voltage lines to see if there is a dip in the voltage due to the inrush and to check if the inrush current specified in the payload ICD is required to turn ON the payload.

The following figure shows the 5V line that was probed through a breakout.

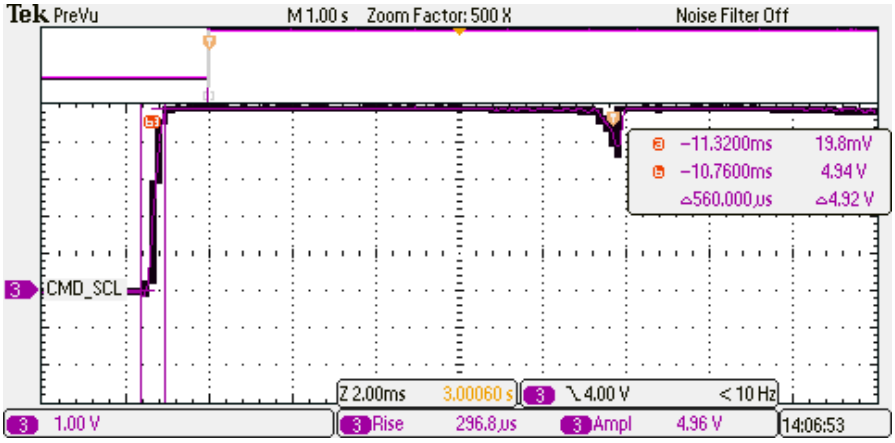

Figure 2-2: 5V switched line going to the INMS payload.

The payload turned ON without any issues and as it can be seen from the figure, the rise time was ~560 uSec (this could be due to the two 4.7uF capacitors C22 and C23 at the input of the payload). Together with the payload provider it was found the complete setup (QB50p EM with EM INMS) was representative enough for the actual flight hardware of all QB50 payloads.

3 Pinout and interface details.

3.1 Connectors and pinouts

The following figure provides a top-view of the board with different connector placements:

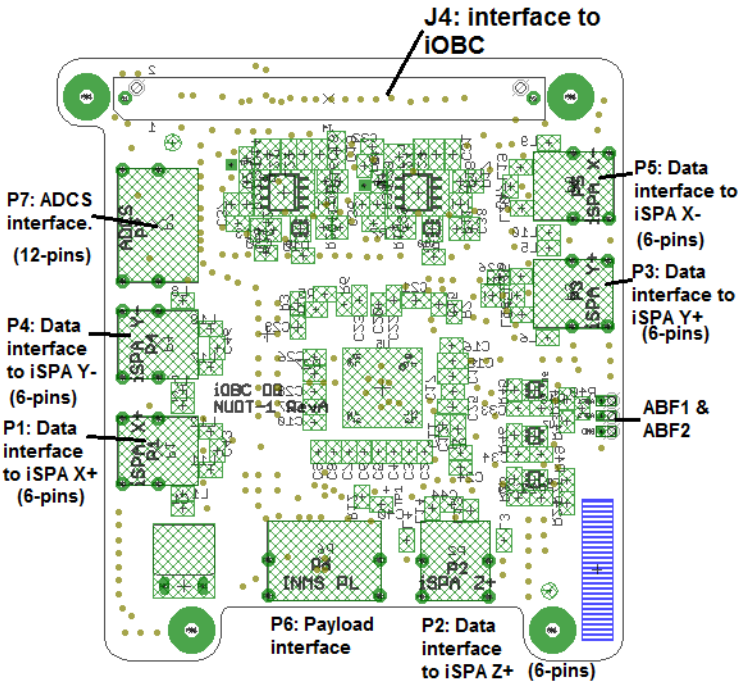

Figure 3-1: Top-view of the daughter board with connector positions.

The pinout of each of these connectors is as follows:

Table 3-1: iOBC interface: ERM8-060-05.0-S-DV-TR: J4

iOBC interface: ERM8-060-05.0-S-DV-TR: J4 (120 pins)				
Pin number	**Input or Output**	**Pin name**	**Function**	
3	Input	AN0	Not used	**ADC**
4	Input	AN1	Not used	
7	Input	AN2	Not used	
8	Input	AN3	3V3 switched line current	
11	Input	AN4	5V switched line current	
12	Input	AN5	QB50 payload: Pin-6	
15	Input	AN6	3V3 switched voltage (0.5 times 3.3V)	
16	Input	AN7	5V switched voltage (0.333 times 5V)	

19	Output	SPI1_NPCS0	Chip select 0	SPI
20	Output	SPI1_NPCS1	Chip select 1	
23	Output	SPI1_NPCS2	Chip select 2	
24	Output	SPI_SPCK	Clock	
27	Output	SPI1_MOSI	Master output	
28	Input	MISO	Temperature input	
31	I/O	GPIO0	Interrupt	GPIO
32	I/O	GPIO01	ABF1	
35	I/O	GPIO02	ABF2	
36	I/O	GPIO03	ABF3	
39	I/O	GPIO04	3V3 switch	
40	I/O	GPIO05	5V Switch	
43	I/O	GPIO06	3V3 switch fault	
44	I/O	GPIO07	5V switch fault	
47	I/O	GPIO08		
48	I/O	GPIO09		
51	I/O	GPIO10		
52	I/O	GPIO11		
55	I/O	GPIO12		
56	I/O	GPIO13		
59	I/O	GPIO14		
60	I/O	GPIO15		
63	I/O	GPIO16		
64	I/O	GPIO17		
67	I/O	GPIO18		
68	I/O	GPIO19		
71	I/O	GPIO20		
72	I/O	GPIO21		
75		PWM0/TC0	Not used	PWM
76		PWM1	Not used	
79		PWM2/TC1	Not used	
80		PWM3	Not used	
83		PWM4/TC2	Not used	
84		PWM5	Not used	
87		RX0	INMS payload pin-7	UART

88		TX0	INMS payload pin-9	
91		RX2/RX+	Not used	
92		TX2/TX+/TRX+	Not used	
93		CTS2/RX-	Not used	
94		RTS2/TX-/TRX-	Not used	
97	I/O	USBD_DP	Not used	**USB A&B**
98	I/O	USBH_DP	Not used	
99	I/O	USBD_DM	Not used	
100	I/O	USBH_DM	Not used	
103	N.A	USBD_VBUS	Not used	
104	N.A	USBH_VBUS	Not used	
107	Output	+5V	5V Supply line	**Power supply lines**
108	Output	+5V	5V Supply line	
109	Input	+3V3_IN	3V3 switched line, (In case a switch is used)	
110	Input	+3V3_IN	3V3 switched line, (In case a switch is used)	
111	Output	+3V3	3V3 supply line	
112	Output	+3V3	3V3 supply line	
115	Input	+5V_SW1	5V switched line, (In case a switch is used)	
116	Input	+5V_SW1	5V switched line, (In case a switch is used)	
117	Output	VBAT	Battery bus voltage	
118	Input	VBAT_Switched	Switched battery bus voltage (In case a switch is used)	
119	Output	VBAT	Battery bus voltage	
120	Input	VBAT_Switched	Switched battery bus voltage (In case a switch is used)	
1,2,5,6,9,10,13,14,17,18,21,22,25,26,29,30,33,34,37,38,41,42,45,46,49,50,53,54,57,58,61,62,65,66,69,70,73,74,77,78,81,82,85,86,89,90,95,96,101,102,105,106,113,114	N.A	GND		**Ground**

Table 3-2: iSPA data interface

iSPA data interface: P1, P2…., P5 (6-Pins)				
Pin number	**Input or Output**	**Pin name**	**Function**	**Connector**
1	N.A	RTD(-Ve)		M80-6670642
2	N.A	N.C		
3	N.A	RTD(+Ve)		
4	N.A	Anode (Photo diode)	Anode from the photo diode	
5	N.A	N.C		
6	N.A	Cathode (Photo diode)	cathode from the photo diode	

Table 3-3: iOBC DB to INMS payload interface.

iOBC DB -> INMS payload interface: 12-pin connector: P6				
Pin number	**Input or Output**	**Pin name**	**Function**	
1	Output	+5V Switched	5V switched line	M80-6671245
2	Output	+5V Switched	5V switched line	
3	Output	3V3 Switched	3V3 switched line	
4	Output	3V3 Switched	3V3 switched line	
5	Output	5V line	5V un-switched line	
6	input	AN6 (TBD)	ADC input	
7	Output	RX0	UART INMS payload	
8	N.A	GND		
9	input	TX0	UART INMS payload	
10	N.A	GND		
11	N.A	GND		
12	N.A	GND		

In the case of ADCS interface, Anode and Cathode of the photo-diodes from 5 iSPA are routed to the ADCS subsystem through the daughter board.

Table 3-4: Daughter board to ADCS interfaces.

iOBC DB -> ADCS board interface: 12-pin connector: P7				
Pin number	**Input or Output**	**Pin name**	**Function**	
1	N.A	Cathode X+	Cathode of X+ to ADCS board	M80-6671245

2	N.A	Anode X+	Anode of X+ to ADCS board	
3	N.A	Cathode X-	Cathode of X- to ADCS board	
4	N.A	Anode X-	Anode of X- to ADCS board	
5	N.A	Cathode Y+	Cathode of Y+ to ADCS board	
6	N.A	Anode Y+	Anode of Y+ to ADCS board	
7	N.A	Cathode Y-	Cathode of Y- to ADCS board	
8	N.A	Anode Y-	Anode of Y- to ADCS board	
9	N.A	Cathode Z+	Cathode of Z+ to ADCS board	
10	N.A	Anode Z+	Anode of Z+ to ADCS board	
11	N.A	N.C		
12	N.A	N.C		

3.2 Switch/regulator and current sensor interface details (Internal interface)

The daughter board provides two switched lines: 3V3 and 5V lines. Both lines are provided to the payload. The switches can be controlled by the iOBC through GPIOs. Provision is made to monitor voltage and current on these switched lines. Following are the lines interfacing the Switch/regulator and current sensor to iOBC.

Table 3-5: 3V3 switch interface lines.

3V3 switched line			
Line	**Input/output**	**Function**	**Remark**
GPIO4 (J4: Pin39)	Input	3V3 Switch	High: ON, Low: OFF
GPIO6 (J4: Pin 43)	Output	3V3 Switch fault	High: No Fault, Low: Fault.
AN6 (J4: Pin 15)	ADC input to iOBC	Voltage level on the 3V3 line	0.5 V/V variation.
AN3 (J4: Pin 8)	ADC input to iOBC	Current consumed on the 3V3 line	245mA correspond to 2.5V (98mA/V)

Table 3-6: 5V switch interface lines.

5V switched line			
Line	**Input/output**	**Function**	**Remark**
GPIO5 (J4: Pin 40)	Input	5V Switch	High: ON, Low: OFF
GPIO7 (J4: Pin	Output	5V Switch fault	High: No Fault, Low: Fault.

44)			
AN7 (J4: Pin 16)	ADC input to iOBC	Voltage level on the 5V line	0.333V/V variation.
AN4 (J4: Pin 11)	ADC input to iOBC	Current consumed on the 5V line	625mA corresponding to 2.5V (250mA/V)

3.3 Temperature measurement sensor interface (Internal interface)

The temperature sensor is interfacing to the iOBC through SPI lines. Apart from the SPI lines, it is possible to reset the temperature sensor using a GPIO line and an interrupt (active high) from the temperature sensor. This can be monitored by the iOBC.

Following are the list of interface lines used to control the temperature sensor:

Table 3-7: LTC2983 internal interface.

Line	Pin number	Input/output	Function
SPI1_SPCK	J4 (Pin: 24)	Input	Clock from the iOBC.
SPI1_MISO	J4 (Pin: 28)	Output	Temperature sensor output.
SPI1_MOSI	J4 (Pin: 27)	Input	Temperature sensor input.
SPI1_NPCS0	J4 (Pin: 19)	Input	Chip select. Active low
GPIO08/TEMP_RESET	J4 (Pin: 47)	Input	Trigger reset: High on GPIO08 [The reset pin of LTC2983 is pulled-up to 3V3 for normal operation, to initiate a reset, switch U11 is used to pull-down the reset pin. This is done by providing a high on GPIO08]
GPIO0/LTC2983_INTR	J4 (Pin: 31)	Output	Interrupt: LOW when device is busy either during start-up or while a conversion cycle is in progress. HIGH at the conclusion of the start-up state or conversion cycle.

4 Electrical characteristics

The electrical characteristics of external and internal interface are discussed in this section.

4.1 Temperature readout sensor.

The temperature readout sensor is operated at 3V3 in this design. It is powered using a continuous 3V3 line. When no measurements are performed, it is possible to put the sensor to sleep mode where the current consumption is very low.

Table 4-1: LTC2983 electrical characteristics.

Parameter	Value	Remark
Supply voltage	3.3V DC (2.85V to 5.25V)	In the design, operated at 3V3, supply routed through J4 (pin: 111,112)
Supply current	15 to 20 mA	
Sleep mode current	<15 uA (datasheet: 25 to 60 uA)	

4.2 3V3 and 5V switched line

The 3V3 and 5V switched lines are used to power-up the INMS payload (most stringent QB50 payload), following are the electrical characteristics of the switched lines:

Table 4-2: Switched line electrical characteristics.

Parameter	Value [3V3 switched line]	Value [5V switched line]
Current limit	245mA	625mA
Short circuit current	510mA	1.3A
Nominal current consumed by the payload [INMS-E-115]	15mA	140mA
Specified in-rush current [INMS-E-115]	830mA	4.02A

More information about the payload ICD can be found in the document: **QB50-INMS-MSSL-ID-12001 Issue 10.** Section 2.2 describes about the tests/measurements that were performed to validate and over-rule the in-rush current specified in the ICD of INMS. It was possible to turn-on the INMS payload with the regulators that were placed on QB50-DB (The same design has been re-used in this design).

4.3 ABF interface

The ABF system has 3 Schmitt-triggers that are internally powered by 3V3 continuous line. This design was re-used from QB-50p daughter board design.