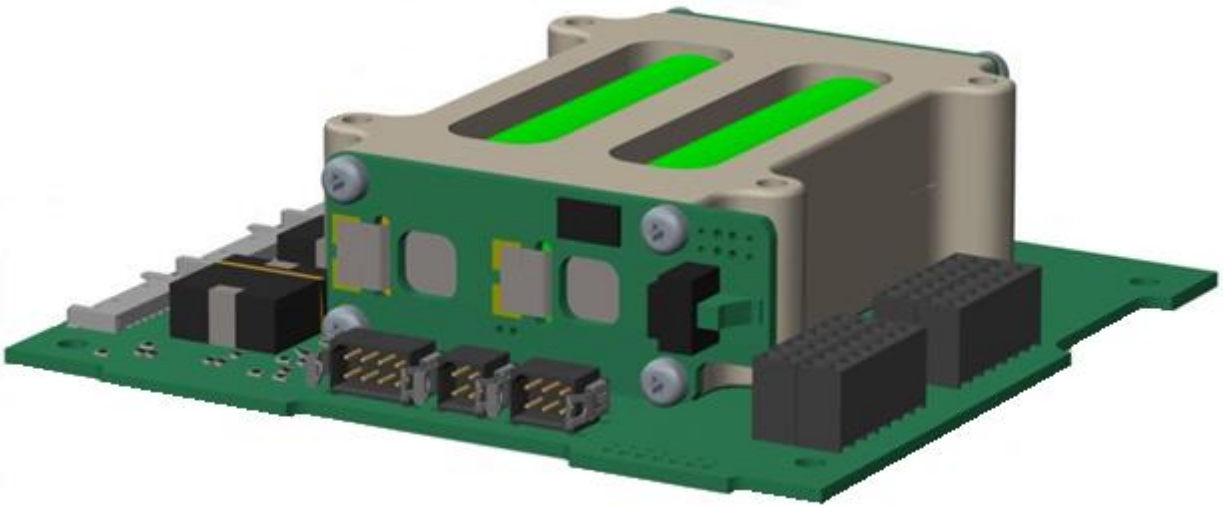


iEPS 2.0 Datasheet

ISIS.EPS.DS.001, version 1.0

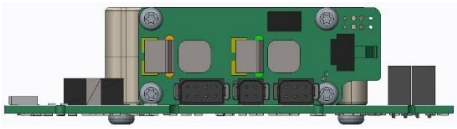
The second-generation of an in-house power system for nanosatellite 1U, 2U, 3U, 3U XL and 6U.

Applications

The ISIS Electrical Power System 2.0 is the second-generation EPS designed and manufactured by ISIS. The power system is a stackable EPS targeting nano-satellites from 1U up to 6U and might be used for 3U XL, 6U and 8U. Using recent high-performance technology, the EPS provides good efficiency with minimal EMI. The architecture allows to be adapted to the needs of the platform by customizing the size of the elements such PV input channels and battery capacitance, yielding benefits in mass and volume expenditure, reliability while increasing the overall robustness of the product.

The design philosophy that underpins the iEPS 2.0 allows flexibility in output bus count and voltage, and allows tailorable redundancy to be applied for selectable parts of the platform, depending on the needs of the mission. The approach is therefore the customer select the most suitable configuration (A, B or C) depending of the power requirements with the use of custom modules.

A



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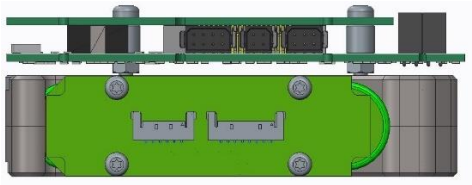

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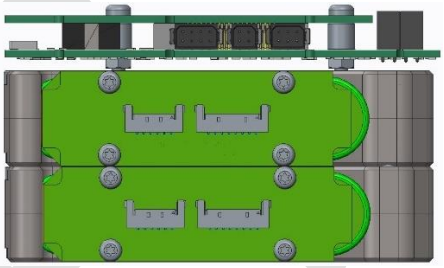


Product Features

- 3x input channels with independent MPPT boost and half bridge conversion (max 2,5A).
- 9x configurable and controlled switches with a latching current limiter. which 3 of them can be configured as permanent
- Two regulated output power buses 3V3@4A and 5V@4A.
- GaN FETs in the power conditioning power switches and FRAM in the MCU.
- On board housekeeping measurements, and I2C interface.
- Separation switch interface.
- Onboard lithium ion battery with heater, Battery under and over voltage protection.

Optional Features

- 2 extra MPPTs and extra custom voltage output regulator.
- 4 deployment lines to deploy solar panels.
- ISS compatible, battery 2 cells, 4 cells and 8 cells version.

General Description

The iEPS has been designed for small and low-cost satellites, it is able to handle different configurations with a variable number of solar panels input and batteries. The main board is the central controller with maximum 3 MPPTs, connection to the satellite bus and stackable configuration of the power systems in three different ways. The systems feature three power solutions: Model A (2 battery cells), Model B (4 cells and provision) and Model C (8 cells in two strings increasing capacitance and/or provide a redundant battery string).

Compatibility

- Compatible with ISIS products and recent Pumpkin and Gomspace products. Compliant to Cubesat standard.
- ISS and Nanoracks requirements compatible.

Flight heritage and quality assurance

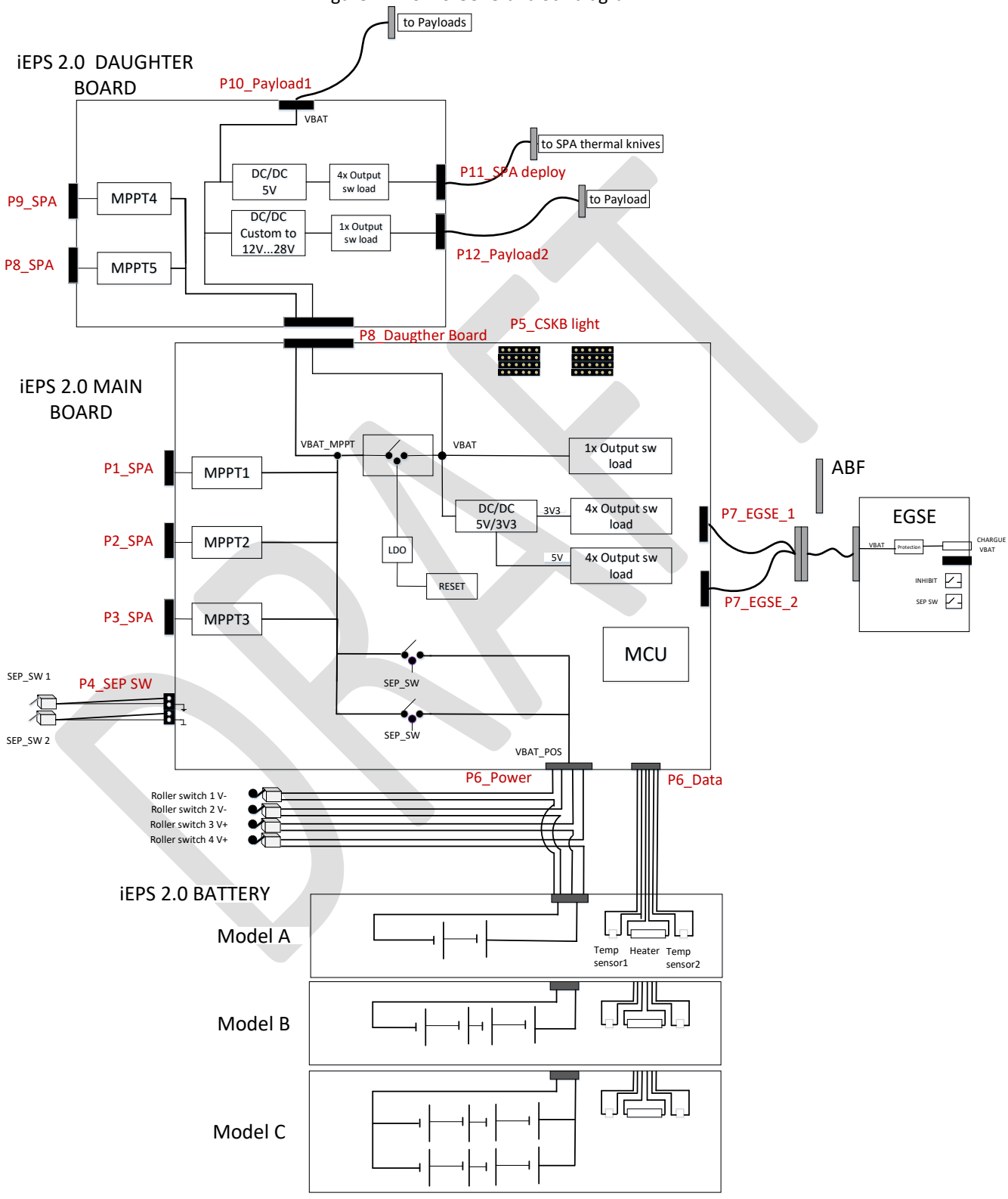
- Design based on heritage from PEASSS Cubesat (2016). Flight heritage since February 2016.
- Qualification Thermal Testing -40 to +80C.
- Sine and Random Vibration ASAPS Qualifications levels.
- IPC-A-610 Class 3 PCB and assembly, flight units thermally acceptance tested.

Ordering information

Please contact sales@isispace.nl for ordering information

Block Diagram

Figure 1 iEPS 2.0 General block diagram



Specification

Parameter	Typical Value
Operational temperature range	-20 to +60C
Storage temperature range	-30 to +70C (RH<60%)
Main Bus organization	Unregulated bus
Main Bus Voltage	Model A: 6V – 8V (battery voltage) Model B and C: 12V – 16V (battery voltage)
Output Regulator Topology	Buck only
Output Regulator Modes	Fixed frequency (loads >= 1A) Burst mode (loads < 1A)
Output Voltage Domains	VD0: 5V VD1: 3V3 VD2: user selectable (only model B and C with Daughter board)
Output Channels	VD0: 2x VD1: 3x VD2: 3x
Output Maximum Current	max 2A per channel max 4A total for VD0, VD1, VD2
Electrical Protection	- overcurrent/thermal limit on Unit input - overvoltage protection on all domains on each output bus channel: - overcurrent/thermal protection - voltage ramp slew rate control - reverse current protection
Functional Protection	- Emergency Low Power Mode (when Bus voltage low) - Hardware Supervisor including Watchdog - I2C Watchdog (stack reset on comms failure) - Firecode stack reset capability
Monitoring	- MCU/PCB temperature voltage, current and (high precision) power measurements on: - each output bus channel - total unit input - total output for VD0 regulator - total output for VD1 regulator
Communication Bus	I2C and UART for AIV testing
Unit Output Enable	yes, logic low activation for use with separation switch during deployment and/or EGSE during AIV
Battery Cell Type	Panasonic NCR18650B
Battery Cell Chemistry	Lithium-Ion
Battery Cell Nominal Voltage	3.6 V
Battery Cell Min/Max Voltage	2.5 V, 4.2 V (absolute maximum)
Battery Cell Nominal Capacity	3200 mAh
Battery Pack Configuration	Model A: 2 cells in series. Model B: 4 cells in series. Model C: 2 strings 4 cells in series.
Battery Pack Nominal Voltage	Model A: 7,2V Model B and C: 14,4V
Battery Pack Min/Max Voltage	Model A: 6V, 8.4V (absolute maximum) Model B and C: 10 V, 16.8 V (absolute maximum)

Parameter	Typical Value
Battery Pack Operating Voltage	Model A: 6.5– 8.0V (reduced range enhances longevity) Model B and C 12.8 V – 16.0V (reduced range enhances longevity)
Battery Pack Nominal Capacity	3200 mAh
Battery Pack Max Input Current	3 A (below 10 degC: 1.5A; below 0 degC: 0A) enforced by current limit for cell longevity
Battery Pack Max Output Current	4 A enforced by current limit for cell longevity
Electrical Protection	- auto-retry overcurrent limit for in and output - optional cell balancing
Functional Protection	- Emergency Low Power Mode (when string voltage low) - I2C Watchdog (Unit reset on comms failure, does not interrupt power provision)
Monitoring	- per cell voltage - total input/output current, voltage and (high precision) power - 2x temperature each pack
Battery Heating	yes, per pack closed loop controlled, in orbit configurable: enable/disable, temperature thresholds
Unit Output Enable	yes, logic low activation for use with separation switch during deployment and/or EGSE during AIV
Stowed Lifetime	>1 year
Mass	Type A 133 grams (without pcb) Type B 268 grams (without pcb)
Volume	Type A 96 x 92 x 25 mm (with pcb and top mounted) Type A 96 x 92 x 33.1 mm (with pcb and bottom mounted) Type B 94.5 x 89.3 x 21 (without PCB)

Functional Description

The Electrical Power System is a component of the ISIS platform and is responsible of harvesting, conditioning, storing and distributing the maximum amount of energy from solar panels to the platform.

The iEPS 2.0 is configurable in three configurations depending of the demand in number of PV input channels and the dimension of the battery. The following table is defined the main features of each model.

Table 1 iEPS Models overview

Feature	Model A	Model B	Model C
MPPTs	3	5	5
Number battery cells	2	4	8
Custom regulator	No	Yes	Yes
HDRM (deploy SPA)	No	Yes	Yes
CSKB light	Yes	Yes	Yes

The new and second generation of ISIS power system is targeted for sizes of 1U, 2U, 3U, 3UXL and 6U, it allows to control more power than a standard CubeSat, and increase the robustness and the reliability of the power system.

The integration of Model A can be done with the battery pack top mounted (see Figure 2)

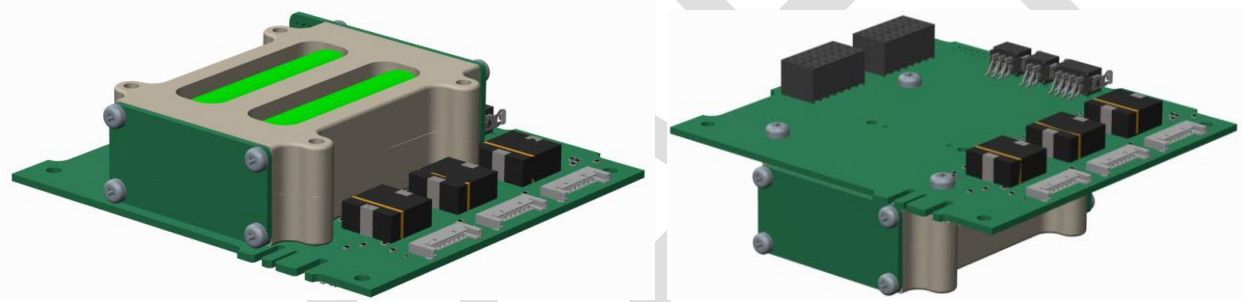


Figure 2 Model A: at left battery module top mounted and at right bottom mounted.

On the onter have for Model B and C the integration includes a daughter board top mounted and the optio to stack 4 cells or 8 cells. Note that the location of the battery module can be in a diffent stack of the nanosatellite by just specigfing the lengh of the harnness that interconnect Battey module and Mother board. See Figure 3 a render of both configurations.

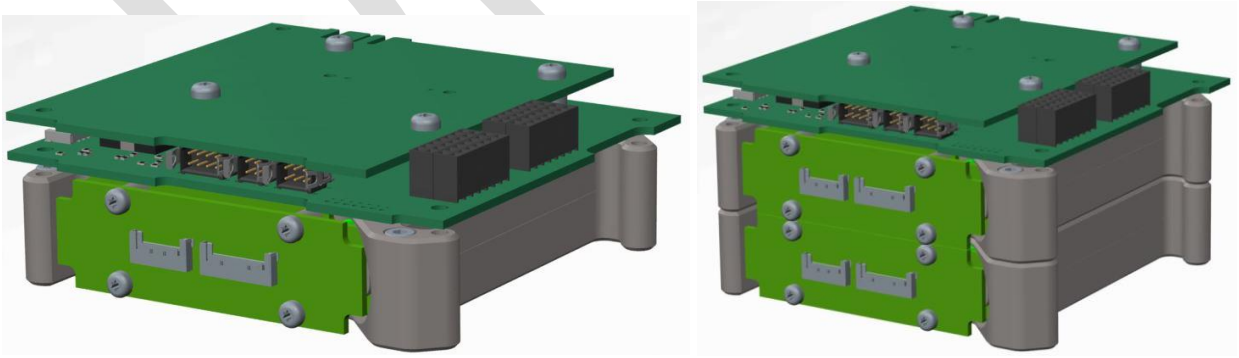


Figure 3 Model B left and Model C right

Electrical Interfaces

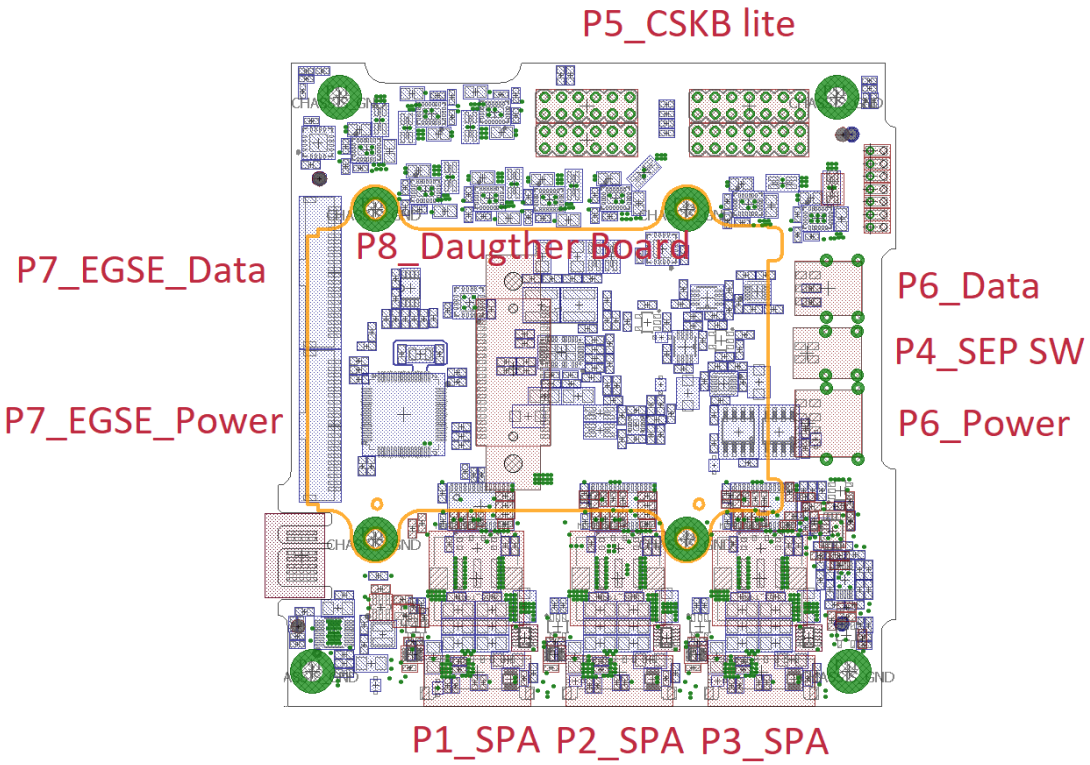
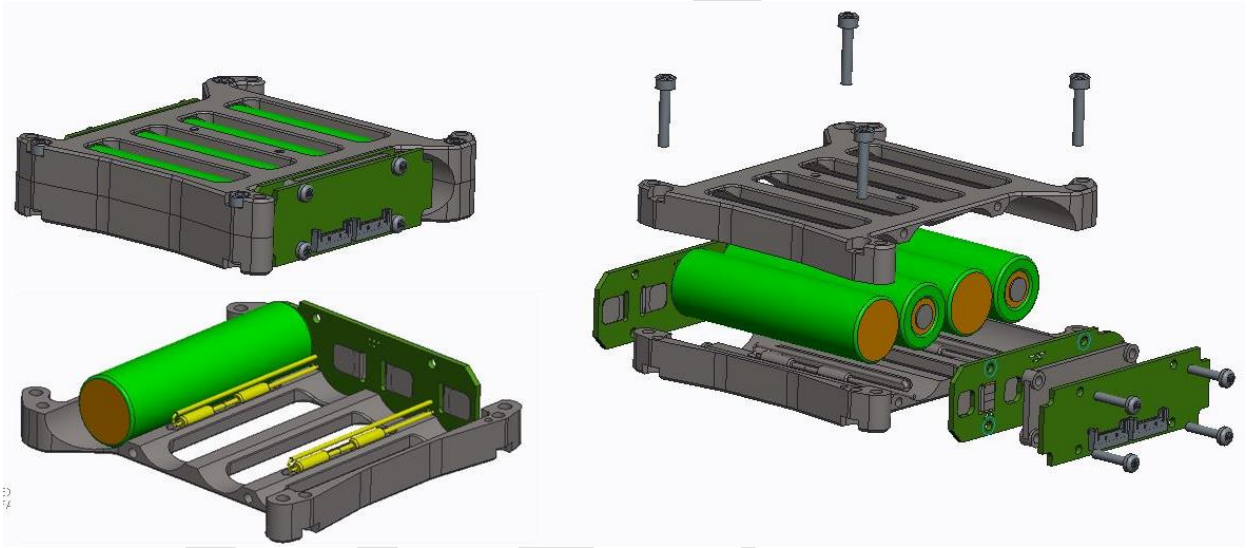


Figure 4 Interface overview mother board

Mechanical Description

For the mechanical design of the battery holders the following functions are applicable:

- Constrain the batteries in all direction.
- Contain batteries with original sleeves.
- Isolate electrically the contained batteries and allow interface to the stack according to PCB104 standard
- Harbor the electrical connection pcb / contact-strips
- Constrain the thermal heaters against the batteries
- Withstand dynamic acceleration loads according to ISIS standard loads
- Withstand thermal loads according to the applicable requirements
- Able to operate in vacuum according to the applicable requirements
- Low outgassing

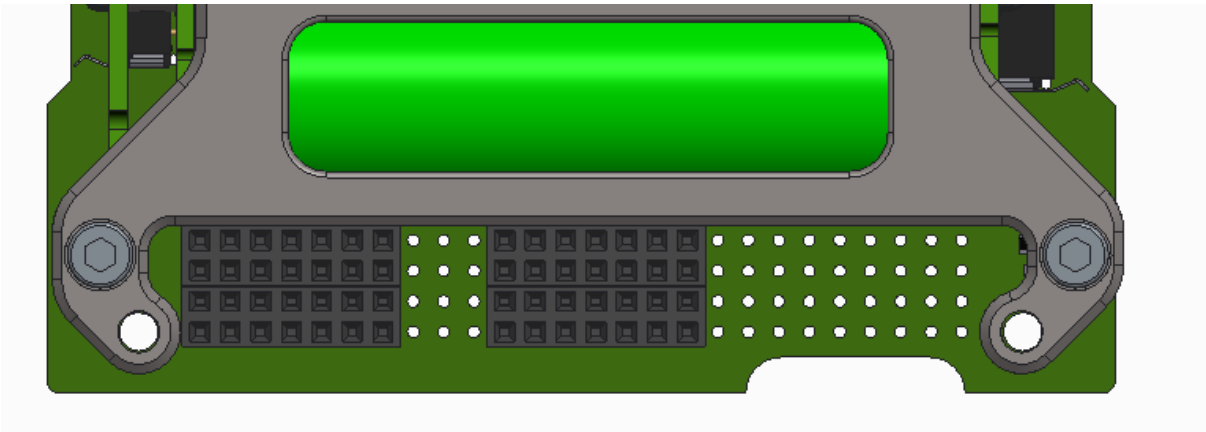


The resulting Battery holder design:

- Rotated battery orientation 90 degrees for optimizing the use of space
- The Batteries were put close together and were shifted sideways to make room for a CSKB-lite feedthrough.
- Top- bottom shell design came in to fulfil the need for removing the shells after the welding of the tabs (in case of damaged cells). Also, the structures inside the holder can easily reached to add components like heaters and thermistors.

> **Note:** For integrity of the shell combination, M3 screws were introduced at the four corners of the battery pack. The size M3 is chosen for a solid grip on the structure and for interchangeability with standard stack rods. These

- For integrity of the shell combination, M3 screws were introduced at the four corners of the battery pack. The size M3 is chosen for a solid grip on the structure and for interchangeability with standard stack rods. These rods are then used for stacking the battery holder to a type C. (Two battery-holders on top of each other.)
- For the type A these four screws are used to mount on the daughter-board interface.



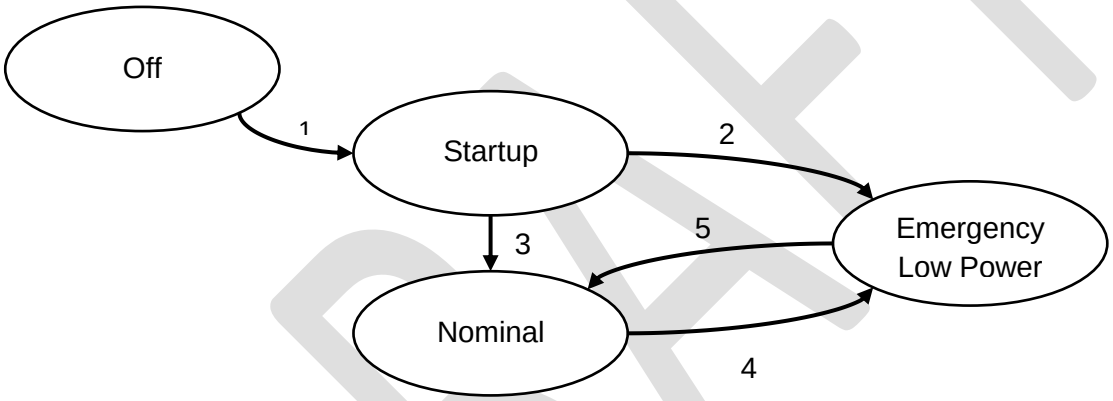
Software

The system has three main operational modes described in **Error! Reference source not found.**.

Table 2: System Operational Modes

Operation Mode	Core Function	Comments
Startup	initializes the system	system will not be responsive on external communication bus during this mode.
Emergency low power mode	protects the batteries from excessive depletion by turning off all supply channels	The system automatically enters and exits this mode depending on the measured battery voltage. All supply channels are turned off.
Nominal	provide full functionality	nominal mode allows commanding and full EPS functionality

The mode transition diagram is given in Figure with trigger information in **Error! Reference source not found.**. Note that a return to Off mode is possible from all other modes, and is implied.



Transition	From	To	Trigger
	any	off	internal power bus voltage falls below minimal voltage or reset of the PDU micro-controller
1	off	startup	internal power bus voltage exceeds power-on threshold
2	startup	emlopo	end of startup & internal power bus voltage too low
3	startup	nominal	end of startup & internal power bus voltage sufficient
4	nominal	emlopo	internal power bus voltage falls below low threshold
5	emlopo	nominal	internal power bus voltage rises above high threshold

Mode Startup

During startup mode the system will (re-)initialize all its internal components and loads the configuration parameters from non-volatile memory. In addition the reset counters are loaded/updated & saved during this mode. The system cannot be commanded during this mode. This mode lasts 500 ms and will then switch to idle mode.

Startup mode is normally not observed by the parent system, because the main I^2C interface is not enabled until the end of the startup mode.

Mode Emergency-Low-Power (emlopo)

Emergency low power mode is entered once the MCU has detected the internal power bus voltage to be too low for continued operation. This is triggered when the measured voltage drops below a voltage-low threshold. To protect the attached batteries from being excessively drained, which would cause accelerated battery degradation, the MCU switches off all output power bus channels to minimize power consumption and extend operational time of the MCU. The MCU will remain active and monitor the internal power bus voltage level. Once the internal power bus voltage has risen above a voltage-high threshold the system is returned to nominal operation. From perspective of the platform, the transition to and from emergency low power mode will resemble a power cycle.

Mode Nominal

During nominal mode the control loop awaits parent system commands while acquiring housekeeping data. Configuration parameter updates can be performed in this mode.

SW Watchdog

The system is equipped with watchdog functionality to safeguard the system from uncontrollability in the case of communication loss with its master. There are two mechanisms implemented, a full reset and a peripheral reset, which are described below.

Note: To keep the watchdog mechanism from triggering, frequent enough communication needs to be performed with the system. Alternatively, the watchdog can be disabled through configuration parameters.

To maximize recovery chances without causing a watchdog trigger it is recommended that the frequency of (regular) communication is kept at least four times larger than the frequency of the watchdog timeout.

TTC Watchdog Reset

The tracking, telemetry and commanding (TTC) watchdog is implemented as an inactivity timer that is reset when commands are received over the command interface. When the timer reaches a hard coded pre-set time threshold (i.e. a timeout occurs), the system is reset.

The timeout value is provided as a read/write parameter and can be updated or retrieved over the command interface.

TTC Peripheral Reset

An additional mechanism is in place that tries to restore communication with the master. This mechanism is triggered when the watchdog timer reaches 0.65 x watchdog timeout. When triggered only the communication peripheral internal to the system microcontroller is reset.

The peripheral reset will:

- cause unavailability of the subsystem during the peripheral reset (in the order of microseconds)
- cause loss of any ongoing transaction that started microseconds before the moment of reset
- not cause any change on the activity performed by the system

If the MCU peripheral caused the communication failure, communication will be restored by the peripheral reset. Reception of the next command will reset the watchdog timer, resulting in a more graceful recovery of the system compared to performing a full reset. To allow for graceful recovery the commanding frequency should be at least 4 times the frequency of the watchdog timeout to allow a command to fall between the peripheral reset and the system reset.

The reset timing is schematically represented in **Error! Reference source not found.**, where the last transfer causes a reset of the watchdog timer, in turn circumventing the need for a system reset.

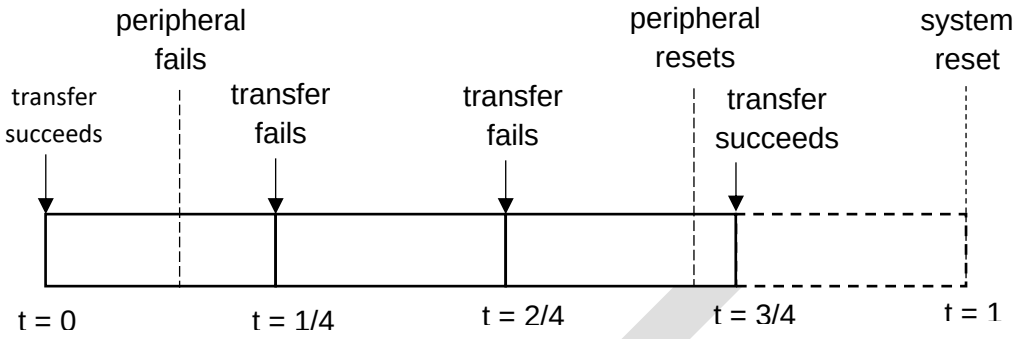


Figure 5 Peripheral Reset and Commanding Frequency

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