UCSD CSE140L Spring 2014

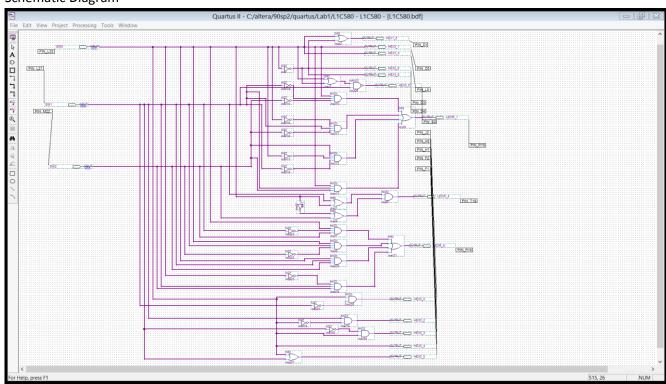
LAB#1 Report

Demonstration Date: 4/15/14		Student CID	580
Student Name:Adrian_Jimenez first		M.I.	Last
Submission Date & Time: 4 / 15 / 14 10:15 AM			
	(FILLED BY Student BEFORE DEMO)	(*** FILLED BY TUTOR/INSTRUCTOR ***)	
	Self-test Report	Demo Reviewer Name :	
	Working Not working	Demo score	Report score
Part1:	x	/1	a)/1
Part2:	x	/1	b)/1
Part3:	x	/1	c)/1
Part4:	x		d)/1
Part5:	x	/1 Subtotal	e)/1 Subtotal
		/5	

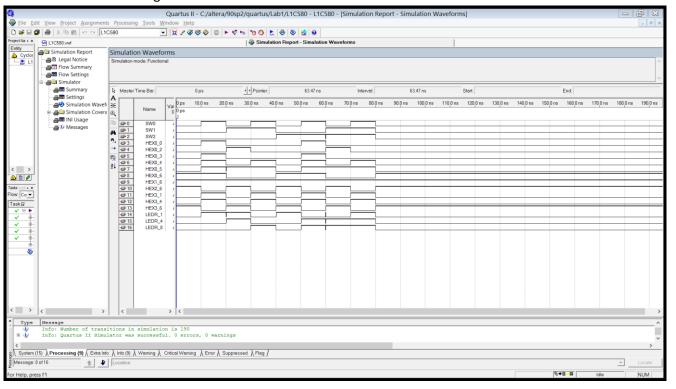
a) Description:

- a. In part one, I used SWO as my input and logic gates to alter what I needed to change on the HEX Digits which where my outputs.
- b. In part two, I used SW0, SW1, and SW2 as my inputs and used the sum of product from my minterms in order to construct my logic gates in the correct way consistent with the truth table.
- c. In part three, I used SW0, SW1, and SW2 as my inputs and used the sum of product from my minterms from my truth table to construct my logic gates in the correct way.
- d. In part four, I used SW0, SW1, and SW2 as my inputs and used the sum of product from my minterms from my truth table to construct my logic gates in the correct way.
- e. In part five, I used SWO and SW1 as my inputs and used the truth table for each output that needed to be modified to determine whether to use the sum of product, product of sum or with a logic gate that represented the truth table.

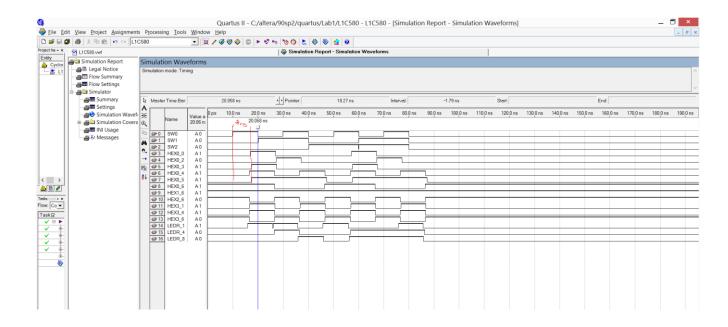
b) Schematic Diagram



c) Functional simulation diagram



d) Timing simulation diagram



e) Timing Analyzer Summary

