UCSD CSE140L Spring 2014

**LAB#1 Report**

Demonstration Date : 4 / 15 / 14 Student CID\_\_\_\_\_\_\_\_580\_\_\_\_\_\_\_\_\_

Student Name: \_\_\_\_\_Adrian\_Jimenez\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

first M.I. Last

**Submission Date & Time : 4 / 15 / 14 10:15 AM**

(FILLED BY Student BEFORE DEMO) (\*\*\* FILLED BY TUTOR/INSTRUCTOR \*\*\*)

**Self-test Report** Demo Reviewer

Name : \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Working Not working **Demo** score **Report** score

**Part1**: \_\_\_\_X\_\_\_\_\_ \_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_/1 a) \_\_\_\_\_\_/1

**Part2**: \_\_\_\_X\_\_\_\_\_ \_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_/1 b)\_\_\_\_\_\_\_/1

**Part3**: \_\_\_\_X\_\_\_\_\_ \_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_\_/1 c) \_\_\_\_\_\_\_/1

**Part4**: \_\_\_\_X\_\_\_\_\_ \_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_\_/1 d) \_\_\_\_\_\_\_/1

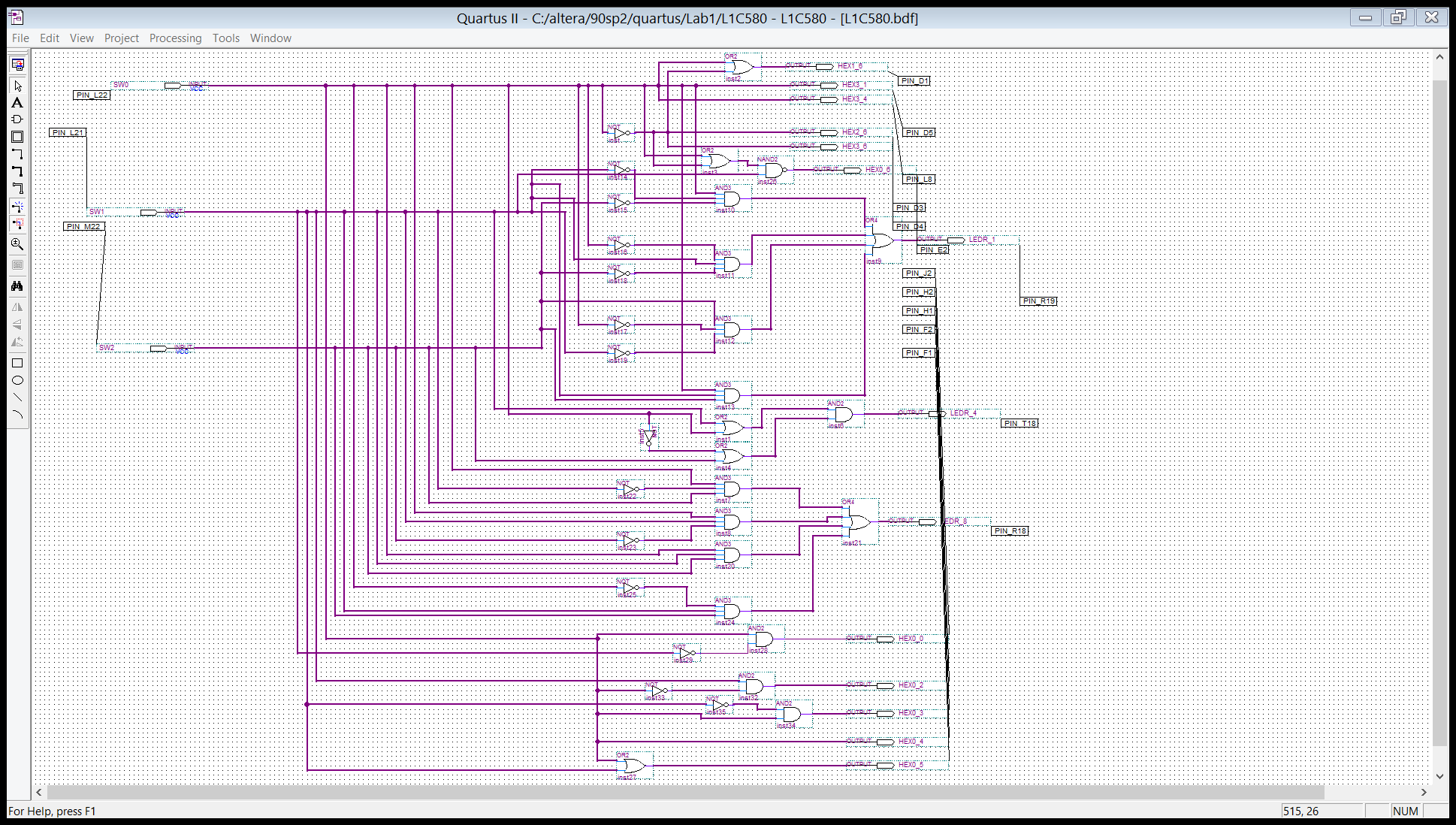
**Part5**: \_\_\_\_X\_\_\_\_\_ \_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_ /1 e) \_\_\_\_\_\_\_\_/1

**Subtotal**  **Subtotal**

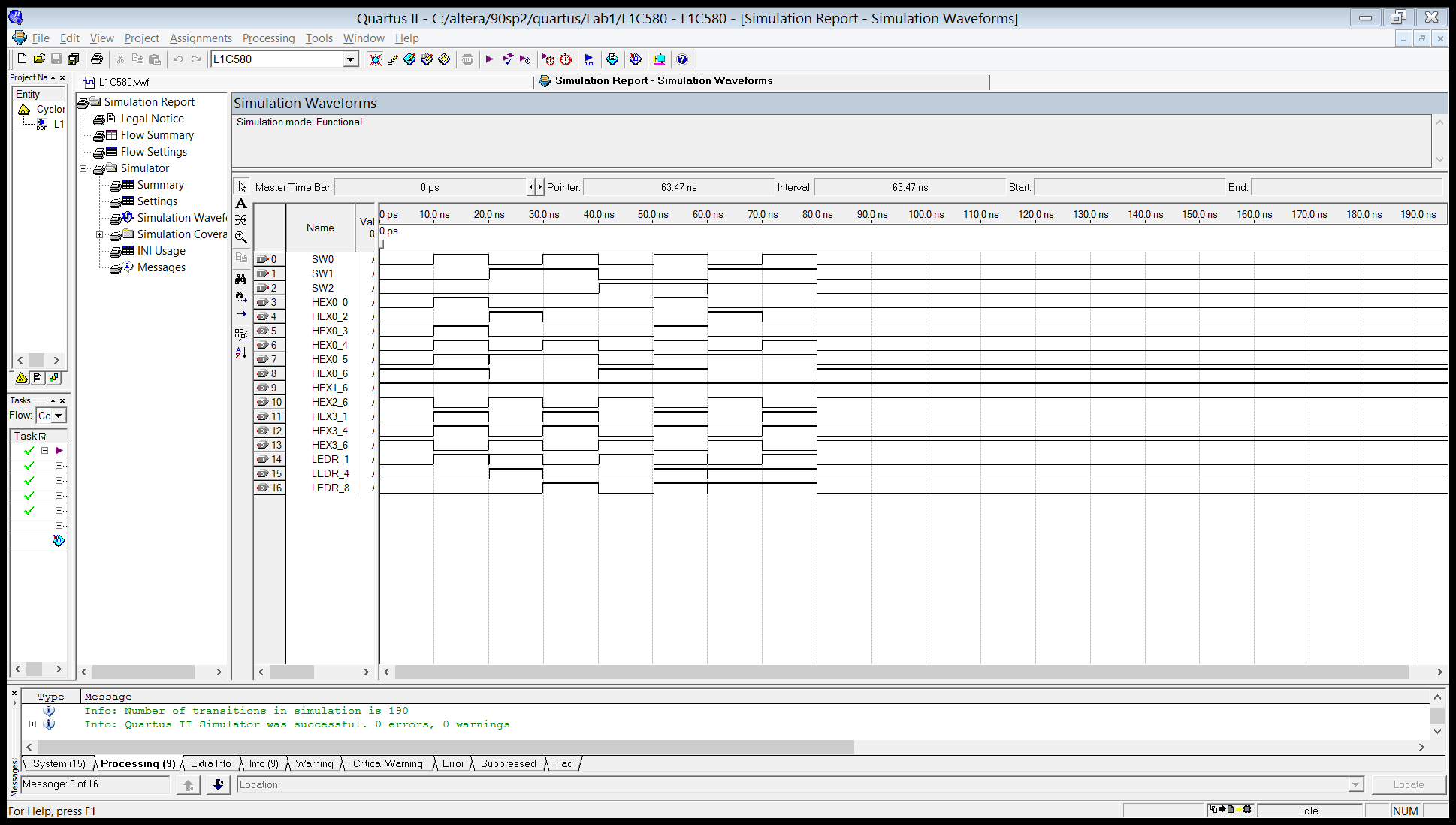
\_\_\_\_\_\_\_\_\_\_\_/**5** \_\_\_\_\_\_\_\_\_\_\_\_\_/**5**

**TOTAL Score:** **\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_/10**

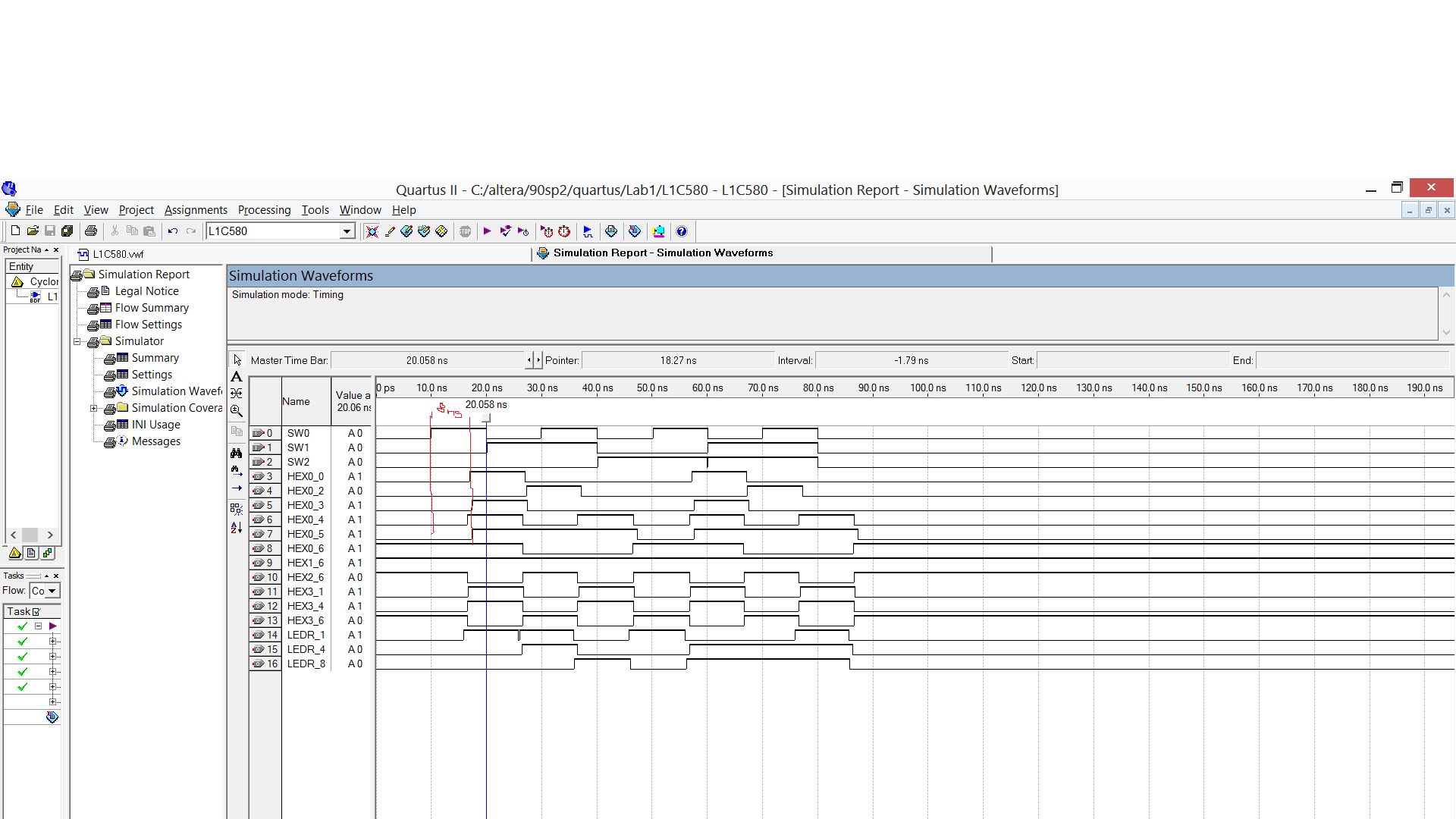
1. Description:
   1. In part one, I used SW0 as my input and logic gates to alter what I needed to change on the HEX Digits which where my outputs.
   2. In part two, I used SW0, SW1, and SW2 as my inputs and used the sum of product from my minterms in order to construct my logic gates in the correct way consistent with the truth table.
   3. In part three, I used SW0, SW1, and SW2 as my inputs and used the sum of product from my minterms from my truth table to construct my logic gates in the correct way.
   4. In part four, I used SW0, SW1, and SW2 as my inputs and used the sum of product from my minterms from my truth table to construct my logic gates in the correct way.
   5. In part five, I used SW0 and SW1 as my inputs and used the truth table for each output that needed to be modified to determine whether to use the sum of product, product of sum or with a logic gate that represented the truth table.
2. Schematic Diagram



1. Functional simulation diagram



1. Timing simulation diagram



1. Timing Analyzer Summary

