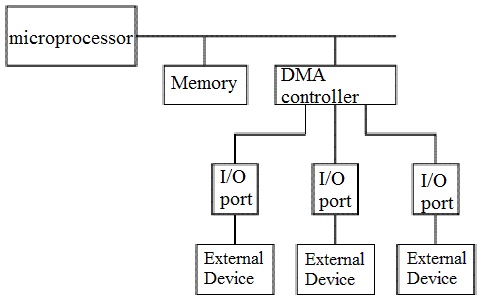
**4620218**

**Direct Access Media (DMA) :**

DMA Controller could be a hardware device that permits I/O devices to directly access memory with less participation of the processor. DMA management desires constant previous circuits of AN interface to speak with the central processing unit and Input/Output devices.

Fig-1 below shows the diagram of the DMA controller. The unit communicates with the CPU through knowledge bus and control lines. Through the utilization of the address bus and permitting the DMA and RS register to pick out inputs, the register among the DMA is chosen by the CPU. RD and WR are two-way inputs. once BG (bus grant) input is 0, the central processing unit will communicate with DMA registers. once BG (bus grant) input is 1, the CPU has relinquished the buses and DMA can communicate directly with the memory.

**DMA Controller Diagram in Computer Architecture**

**DMA controller registers**

**Address register –**It contains the address to specify the required location in memory.  
**Word count register –**It contains the amount of words to be transferred.  
**Control register –**It specifies the transfer mode.

**Note –** All registers within the DMA seem to the CPU as I/O interface registers. Therefore, the C.P.U. will each scan and write into the DMA registers beneath program management via the information bus.

**Working of DMA Controller**

DMA Controller must share the bus with the processor to form the info transfer. The device that holds the bus at a given time is termed bus master. once a transfer from I/O device to the memory or vice verse has to be made, the processor stops the execution of this program, increments the program counter, moves data over stack then sends a DMA choose signal to DMA controller over the address bus.

If the DMA controller is free, it requests the control of bus from the processor by raising the bus request signal. Processor grants the bus to the controller by raising the bus grant signal, currently DMA controller is that the bus master. The processor initiates the DMA controller by causing the memory addresses, variety of blocks of knowledge to be transferred and direction of data transfer. when assignment the info transfer task to the DMA controller, rather than waiting ideally until completion of data transfer, the processor resumes the execution of the program after retrieving directions from the stack.

DMA controller currently has the complete control of buses and might move directly with memory and I/O devices freelance of central processor. It makes the information transfer in step with the control directions received by the processor. once completion of information transfer, it disables the bus request signal and CPU disables the bus grant signal thereby moving control of buses to the CPU.

When an I/O device needs to initiate the transfer then it sends a DMA request signal to the DMA controller, that the controller acknowledges if it’s free. Then the controller requests the processor for the bus, raising the bus request signal. once receiving the bus grant signal it transfers the information from the device. For n channeled DMA management n variety of external devices is connected.

**The DMA transfers the data in 3 modes that embrace the following.**

**a) Burst Mode:** during this mode DMA relinquishing the buses to central processor solely after completion of whole data transfer. Meanwhile, if the CPU needs the bus it’s to remain ideal and look forward to data transfer.

**b) Cycle Stealing Mode:** during this mode, DMA offers control of buses to CPU after transfer of each byte. It incessantly problems asking for bus control, makes the transfer of 1 computer memory unit and returns the bus. By this central processor doesn’t have to be compelled to look forward to an extended time if it desires a bus for higher priority task.

**c) Transparent Mode:** Here, DMA transfers data only if CPU is death penalty the instruction that doesn’t need the utilization of buses.

**Advantages and Disadvantages of DMA controller**

**Advantages:**  
1)Transferring the info while not the involvement of the processor will speed up the scan-write task.  
2)DMA reduces the clock cycle requires to read or write a block of data.  
3)Implementing DMA also reduces the overhead of the processor.  
**Disadvantages :**1)As it’s a hardware unit, it would cost to implement a DMA controller within the system.  
2)Cache coherence problem can occur whereas mistreatment DMA controller.