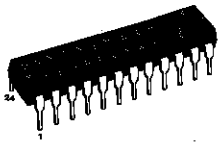
SGS-THOMSON MICROELECTRONICS

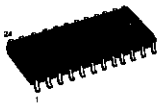
M74HC4514
M74HC4515

HC4514: 4 TO 16 LINE DECODER/LATCH
HC4515: 4 TO 16 LINE DECODER LATCH (INV.)

- HIGH SPEED
  t_{PD} = 18 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC}(OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 4514B/4515B



B1R
(Plastic Package)

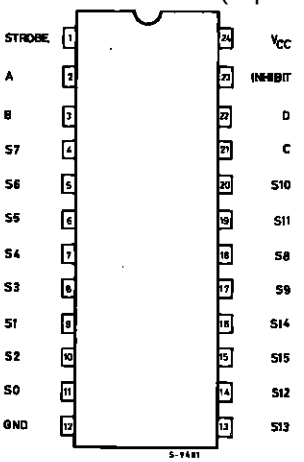


M1R
(Micro Package)

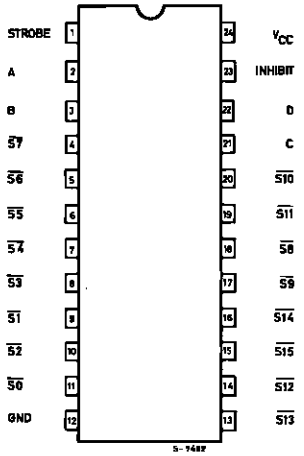
ORDER CODES :
M74HCXXXXM1R M74HCXXXXB1R

PIN CONNECTIONS (top view)

HC4514



HC4515

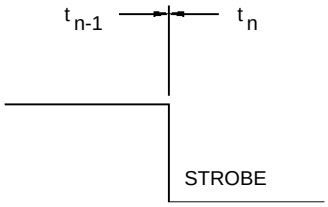


DESCRIPTION

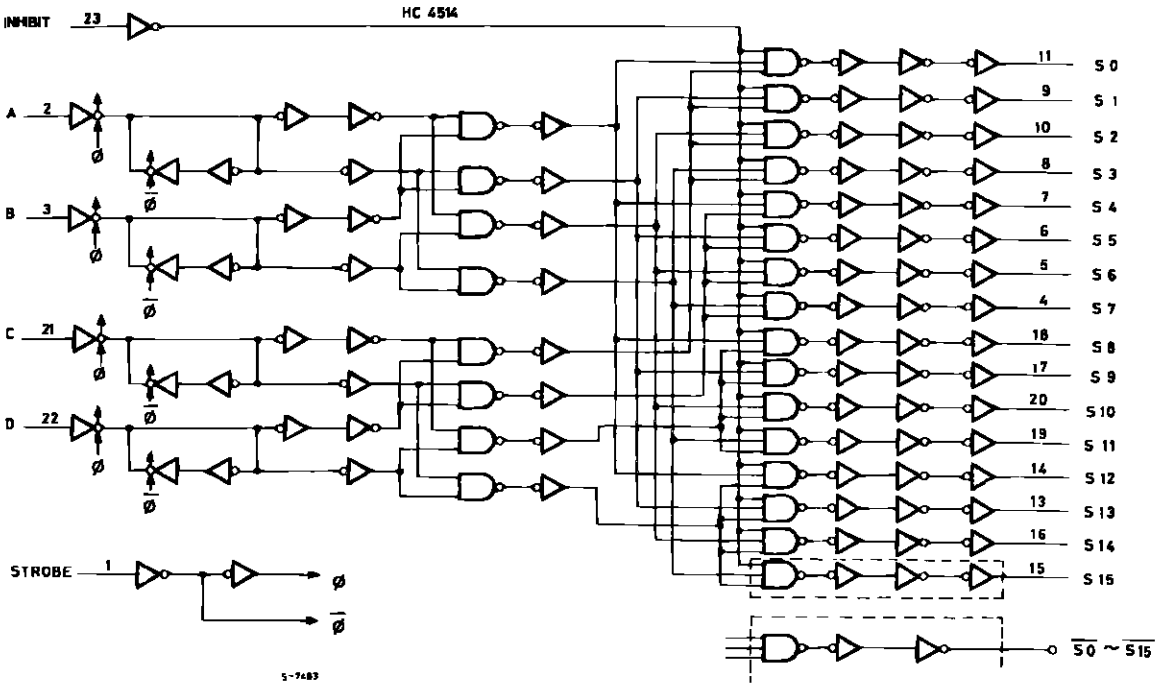
The 74HC4514 and the 74HC4515 are high speed CMOS 4-LINE TO 16-LINE DECODERS WITH LATCHED INPUTS fabricated in silicon gate C^2MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption.

A binary code stored in the four input latches (A to D) provides a high level (HC4514) or a low level (HC4515) at the selected one of sixteen outputs excluding the other fifteen outputs, when the inhibit input (INHIBIT) is held low. When the inhibit input is held high, all outputs are kept low level (HC4514) or high level (HC4515), while the latch function is available. The data applied to the data inputs are transfered to the Q outputs of latches when the strobe input is held high. When the strobe input is taken low, the information data applied to the data input at a time is retained at the output of the latches. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

INPUTS					STROBE	SELECT OUTPUT HC4514 - 'H' (HC4515 - 'L')
INHIBIT	A	B	C	D		
L	L	L	L	L	STROBE = 'H' Refer to truth table STROBE = 'L' Data at the negative going transition of strobe shall be provided on the each output while strobe is held low. 	S0 ($\overline{S0}$)
L	H	L	L	L		S1 ($\overline{S1}$)
L	L	H	L	L		S2 ($\overline{S2}$)
L	H	H	L	L		S3 ($\overline{S3}$)
L	L	L	H	L		S4 ($\overline{S4}$)
L	H	L	H	L		S5 ($\overline{S5}$)
L	L	H	H	L		S6 ($\overline{S6}$)
L	H	H	H	L		S7 ($\overline{S7}$)
L	L	L	L	H		S8 ($\overline{S8}$)
L	H	L	L	H		S9 ($\overline{S9}$)
L	L	H	L	H		S10 ($\overline{S10}$)
L	H	H	L	H		S11 ($\overline{S11}$)
L	L	L	H	H		S12 ($\overline{S12}$)
L	H	L	H	H		S13 ($\overline{S13}$)
L	L	H	H	H		S14 ($\overline{S14}$)
L	H	H	H	H		S15 ($\overline{S15}$)
H	X	X	X	X		HC4514 - ALL OUTPUTS 'L' (HC4515 - ALL OUTPUTS 'H')

LOGIC DIAGRAM (HC4514)



FOR HC4515 DEVICE LOGIC DIAGRAM SHOWN AT THE BOTTOM SHALL TAKE THE PLACE OF OUTPUT CIRCUITS.

PIN DESCRIPTION (HC4514)

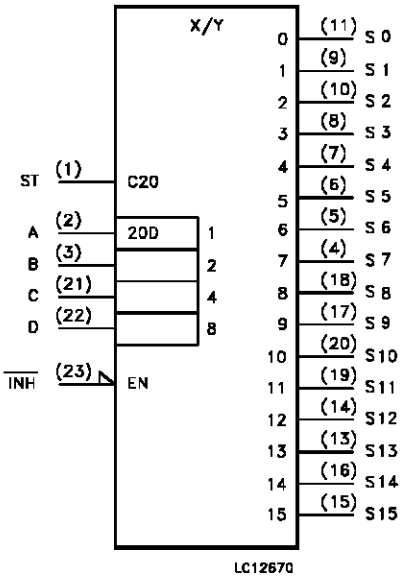
PIN No	SYMBOL	NAME AND FUNCTION
1	STROBE	Strobe Input
2, 3, 21, 22	A to D	Address Inputs
11, 9, 10, 8, 7, 6, 5, 4, 18, 17, 20, 19, 14, 13, 16, 15	S0 to S15	Multiplexer Outputs (Active HIGH)
23	INHIBIT	Enable Input
12	GND	Ground (0V)
24	V_{CC}	Positive Supply Voltage

PIN DESCRIPTION (HC4515)

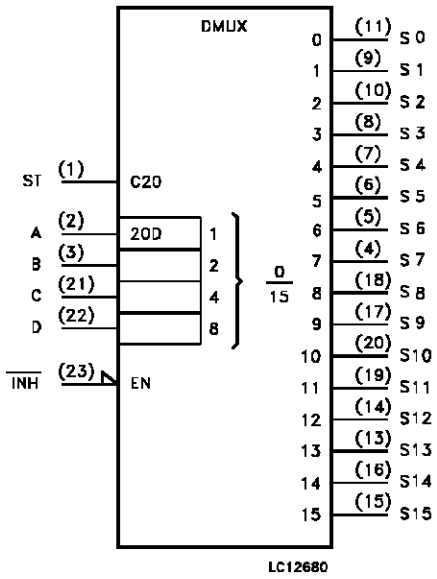
PIN No	SYMBOL	NAME AND FUNCTION
1	STROBE	Strobe Input
2, 3, 21, 22	A to D	Address Inputs
11, 9, 10, 8, 7, 6, 5, 4, 18, 17, 20, 19, 14, 13, 16, 15	$\overline{S0}$ to $\overline{S15}$	Multiplexer Outputs (Active LOW)
23	INHIBIT	Enable Input
12	GND	Ground (0V)
24	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS

HC4514

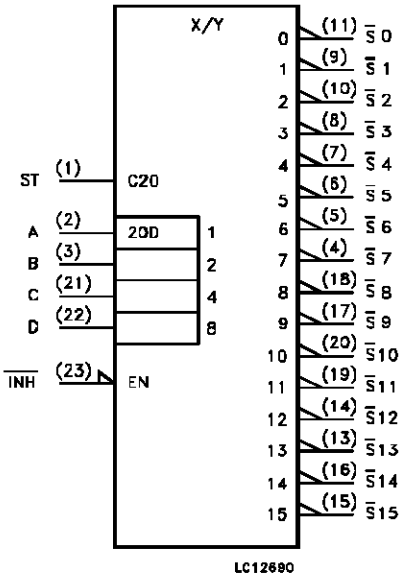


LC12670

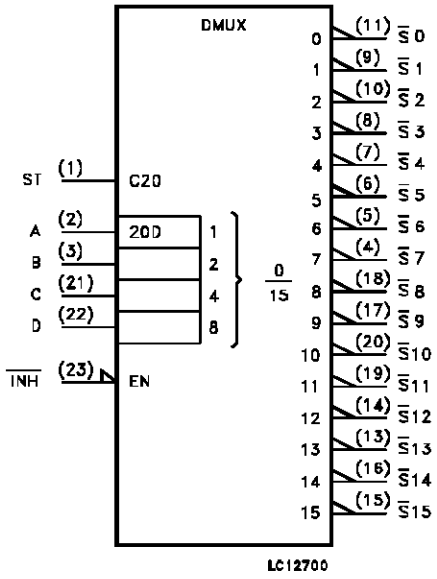


LC12680

HC4515

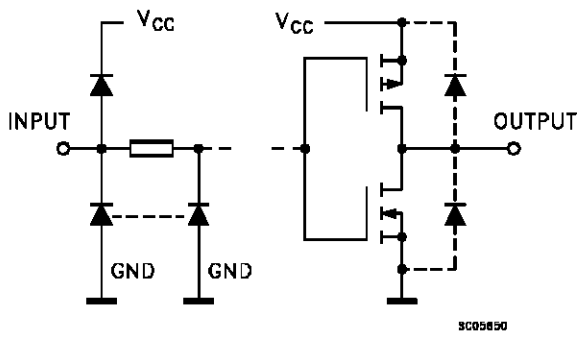


LC12690



LC12700

INPUT AND OUTPUT EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

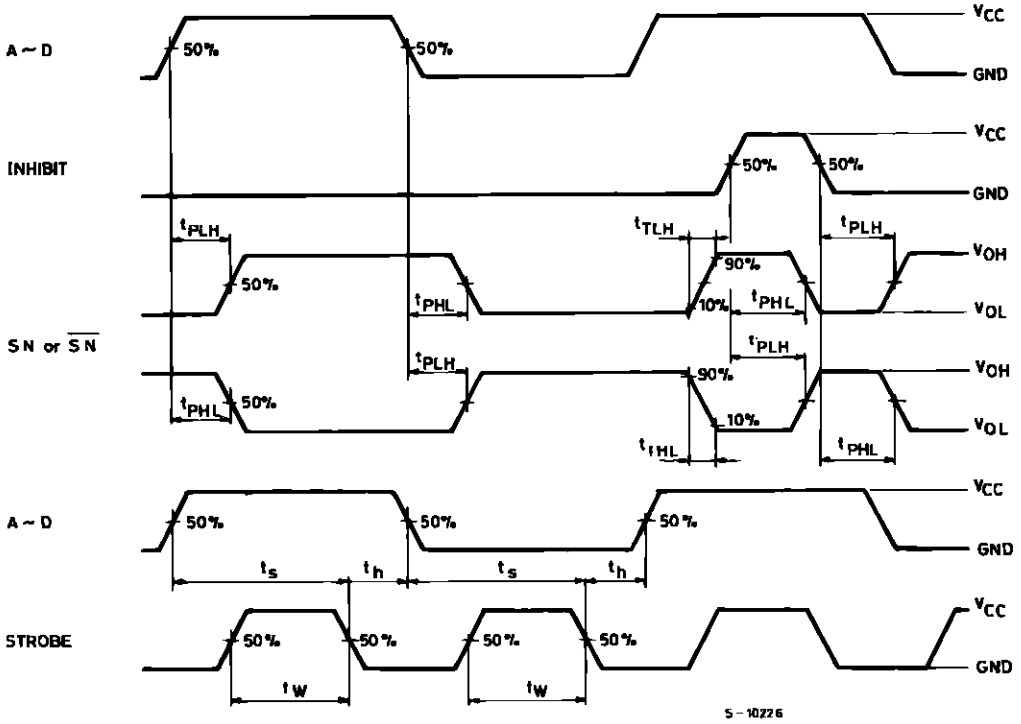
Symbol	Parameter	Test Conditions			Value					Unit
		V_{CC} (V)			T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		V
		4.5			3.15			3.15		
		6.0			4.2			4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5	V
		4.5					1.35		1.35	
		6.0					1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		V
		4.5			4.4	4.5		4.4		
		6.0			5.9	6.0		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1	V
		4.5				0.0	0.1		0.1	
		6.0				0.0	0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5.0	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

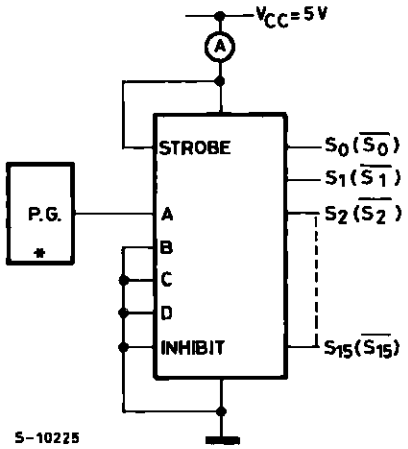
Symbol	Parameter	Test Conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
t_{PLH} t_{PHL}	Propagation Delay Time (DATA - Sn, $\overline{Sn}$)	2.0			65	175		220	ns
		4.5			22	35		44	
		6.0			19	30		37	
t_{PHL} t_{PLH}	Propagation Delay Time (STROBE - Sn, $\overline{Sn}$)	2.0			75	175		220	ns
		4.5			24	35		44	
		6.0			20	30		37	
t_{PHL} t_{PLH}	Propagation Delay Time (INHIBIT - Sn, $\overline{Sn}$)	2.0			60	175		220	ns
		4.5			20	35		44	
		6.0			17	30		37	
$t_{W(L)}$	Minimum Pulse Width (STROBE)	2.0			14	75		95	ns
		4.5			6	15		19	
		6.0			6	13		16	
t_s	Minimum Set-up Time (DATA)	2.0			10	50		65	ns
		4.5			2	10		13	
		6.0			2	9		11	
t_h	Minimum Hold Time (DATA)	2.0				5		5	ns
		4.5				5		5	
		6.0				5		5	
C_{IN}	Input Capacitance				5	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				61				pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



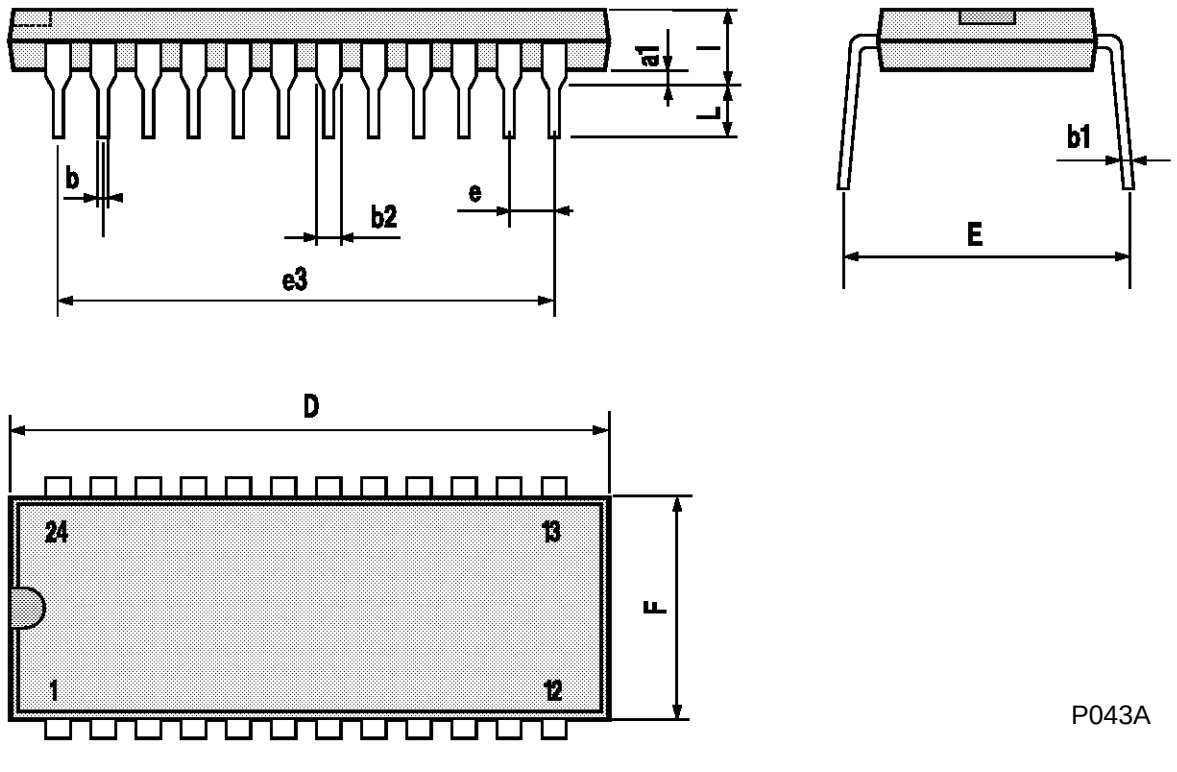
TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

Plastic DIP24 (0.25) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			32.2			1.268
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		27.94			1.100	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	



P043A

SO24 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45° (typ.)					
D	15.20		15.60	0.598		0.614
E	10.00		10.65	0.393		0.420
e		1.27			0.05	
e3		13.97			0.55	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
S	8° (max.)