ECE 6130: Advanced VLSI Systems

Project Report
Phase 2

Submitted by
Project Group 3
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Report Organization:

This report presents an implementation of a 4 tap FIR filter as per the Phase 2 Project statement. We present the Adder arithmetic circuitry and its layout used for the FIR Filter initially. This is followed by a description of the Multiplier Block used in our implementation. Finally, the FIR Filter schematic, its functionality and its further analysis is reported.

Adder Block:

A 6-bit adder has been implemented using wide carry look ahead (CLA) topology. Two 3-bit CLA adder has been cascaded in ripple carry fashion. This scheme of adder has been chosen to get better speed than a traditional ripple carry adder. In CLA adder each carry adder each carry bit is generated directly from the inputs and generator/propagator block. As a result, there is no necessity of carry propagation in CLA adder which gives it a faster response. But in CLA adders having large inputs it requires high fan-in and/or gates which increases its delay. So, we have made a tradeoff here and cascaded two 3-bit CLA adders instead of making 6-bit CLA adder so that we do not need very high fan-in logic gates as well as we can minimize the time required for carry propagation. *All AND, OR and XOR gates used in the following implementation have been made from NOT, NAND and NOR gates made in Phase1 of the Project.*

The schematic diagrams and layouts for the 6-bit adders are given below:

Generator/Propagator block:

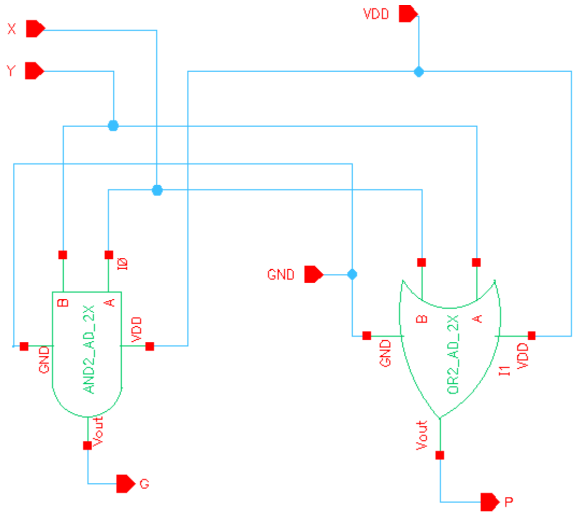


Fig 1: Schematic of Generator/Propagator block

The logic expressions for generator/propagator block is:

$g_n = x_n y_n$

$p_n = x_n + y_n$

Where x_n and y_n are inputs to the adder and g_n / p_n is the generation/ propagation bits.

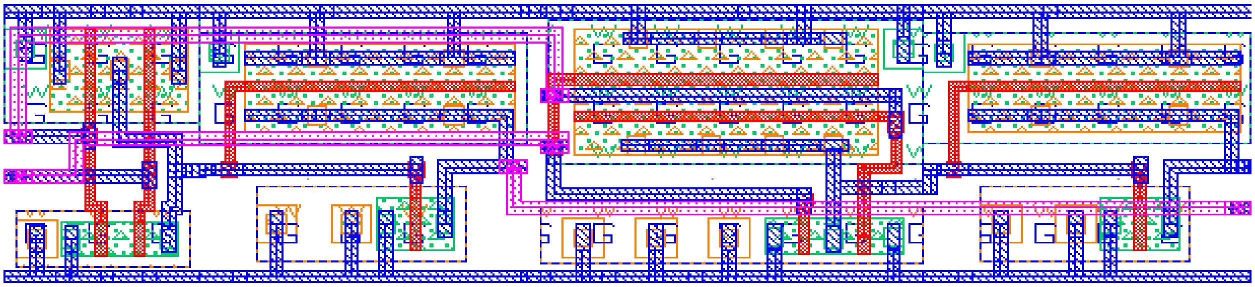


Fig 2: Layout of the Generator/Propagator block

Sum block

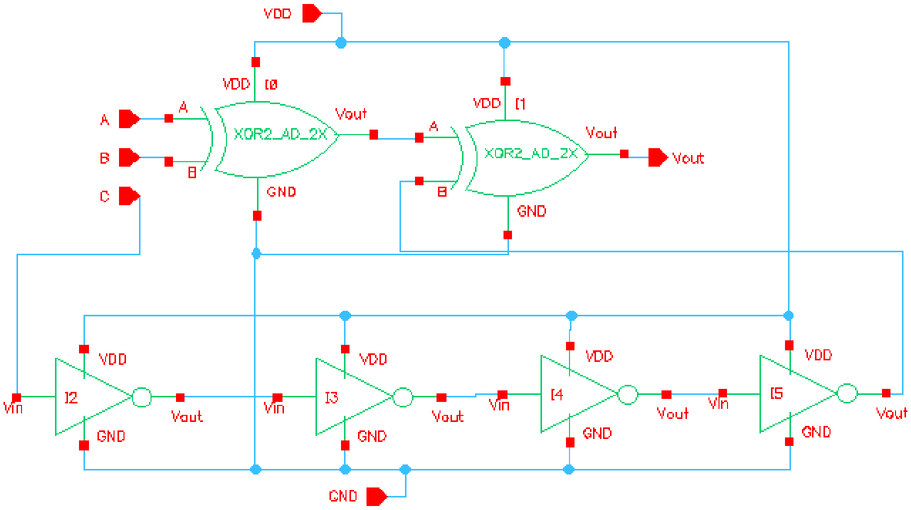


Fig 3: Schematic of sum block

The sum block is a three input xor gate made by cascading two 2 input xor gates. The buffer chain in the schematic is used to adjust the delay between the inputs of xor gates. The logical expression for the sum block is

$s_n = x_n \oplus y_n \oplus c_n$

where x_n , y_n are inputs and c_n is the carry generated from previous bits.

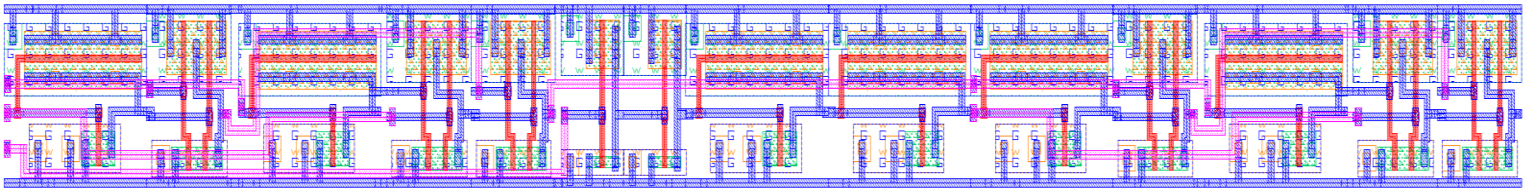


Fig 4: Layout of the sum block

Carry blocks:

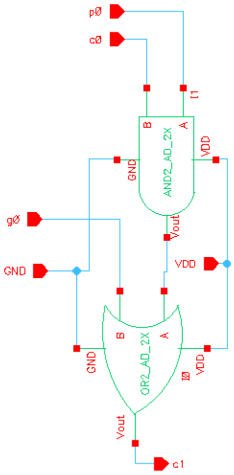


Fig 5: Schematic of C_1 (carry from the first input bits x_o , y_o) block

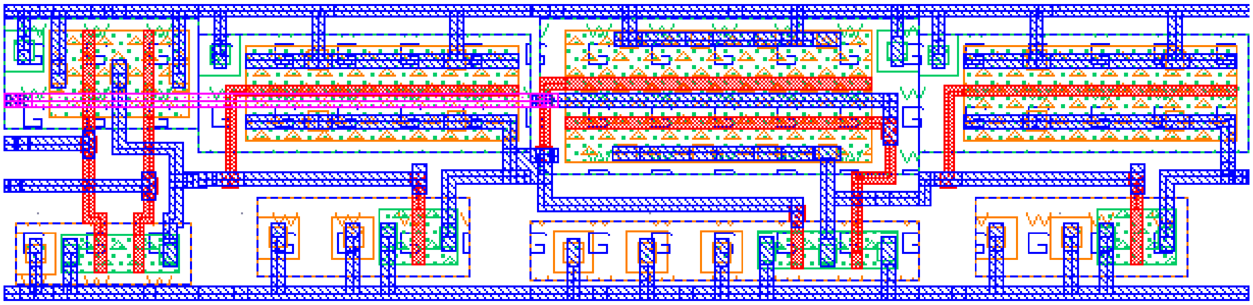


Fig 6: Layout of C_1 (carry 1) block

Logical expression of C_1 block

$C_1 = g_o + p_o c_o$

Where g_o , p_o are outputs of generator/ propagator block and c_o is the input carry.

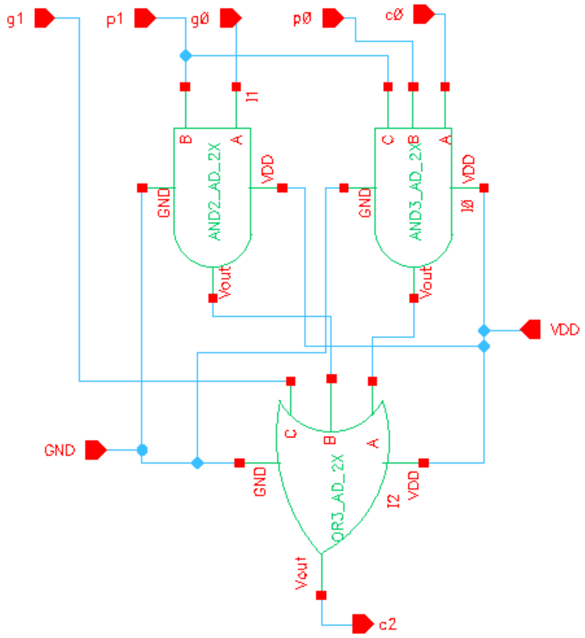


Fig 7: Schematic of C_2 block

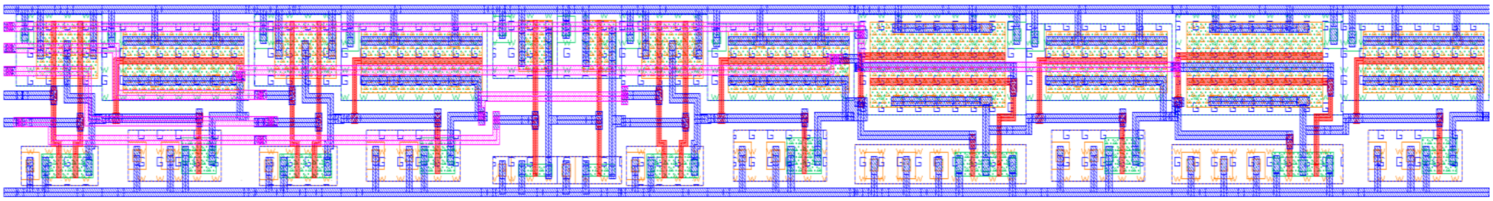


Fig 8: Layout of C_2 block

Logical expression of C_2 block

$C_2 = g_1+p_1\ g_o\ +p_1\ p_oc_o$

Where g, p are outputs of generator/ propagator block and c_o is the input carry.

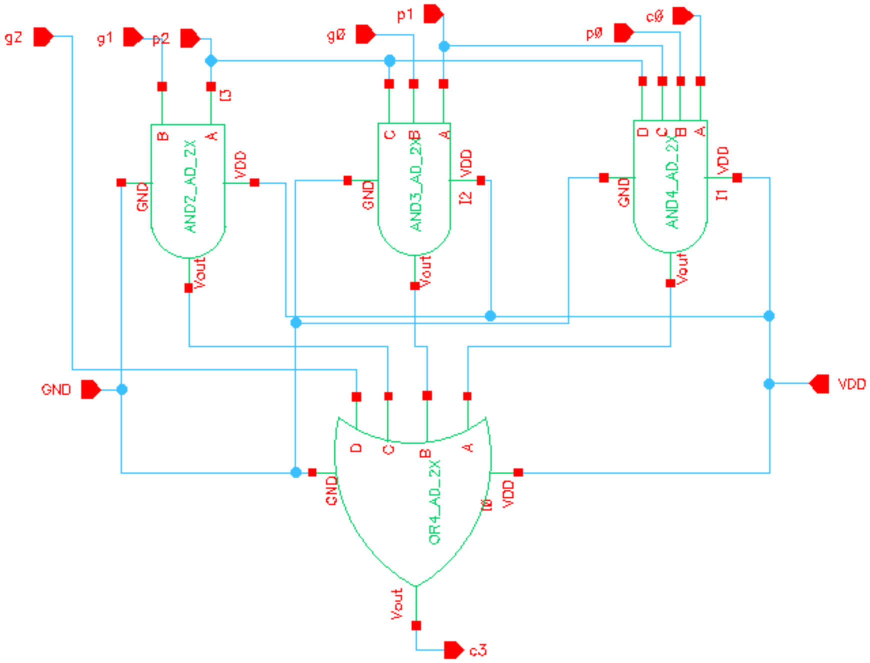


Fig 9: Schematic of C_3 block

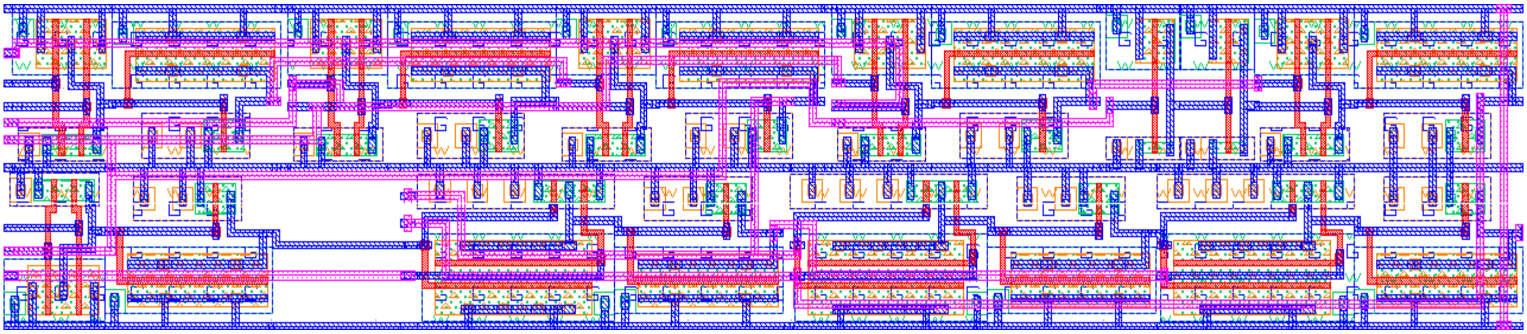


Fig 10: Layout of C_3 block

Logical expression of C_3 block

$C_3 = g_2 + p_2 g_1 + p_2 p_1 g_o + p_2 p_1 p_o c_o$

Where g, p are outputs of generator/ propagator block and c_o is the input carry.

Carry Look Ahead Block:

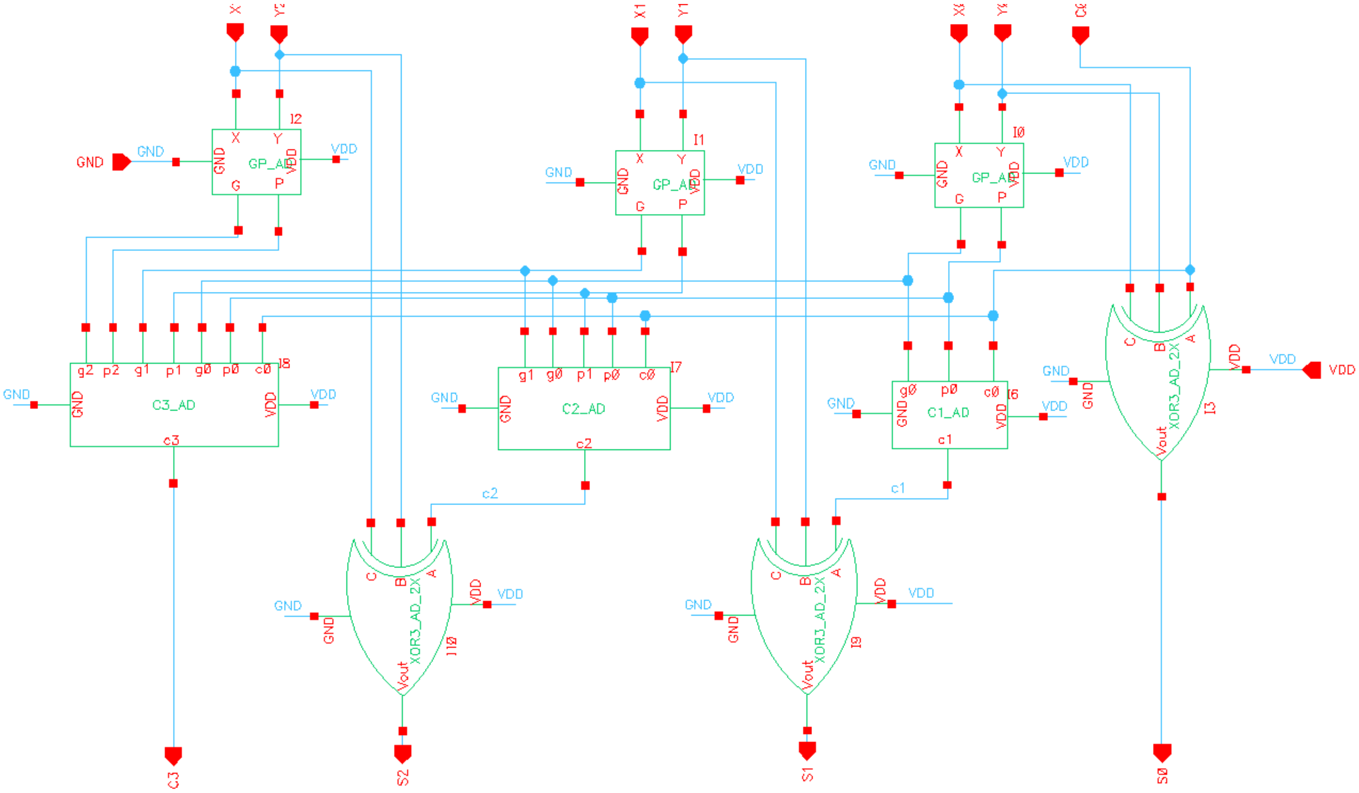


Fig 11: Schematic of 3bit CLA block

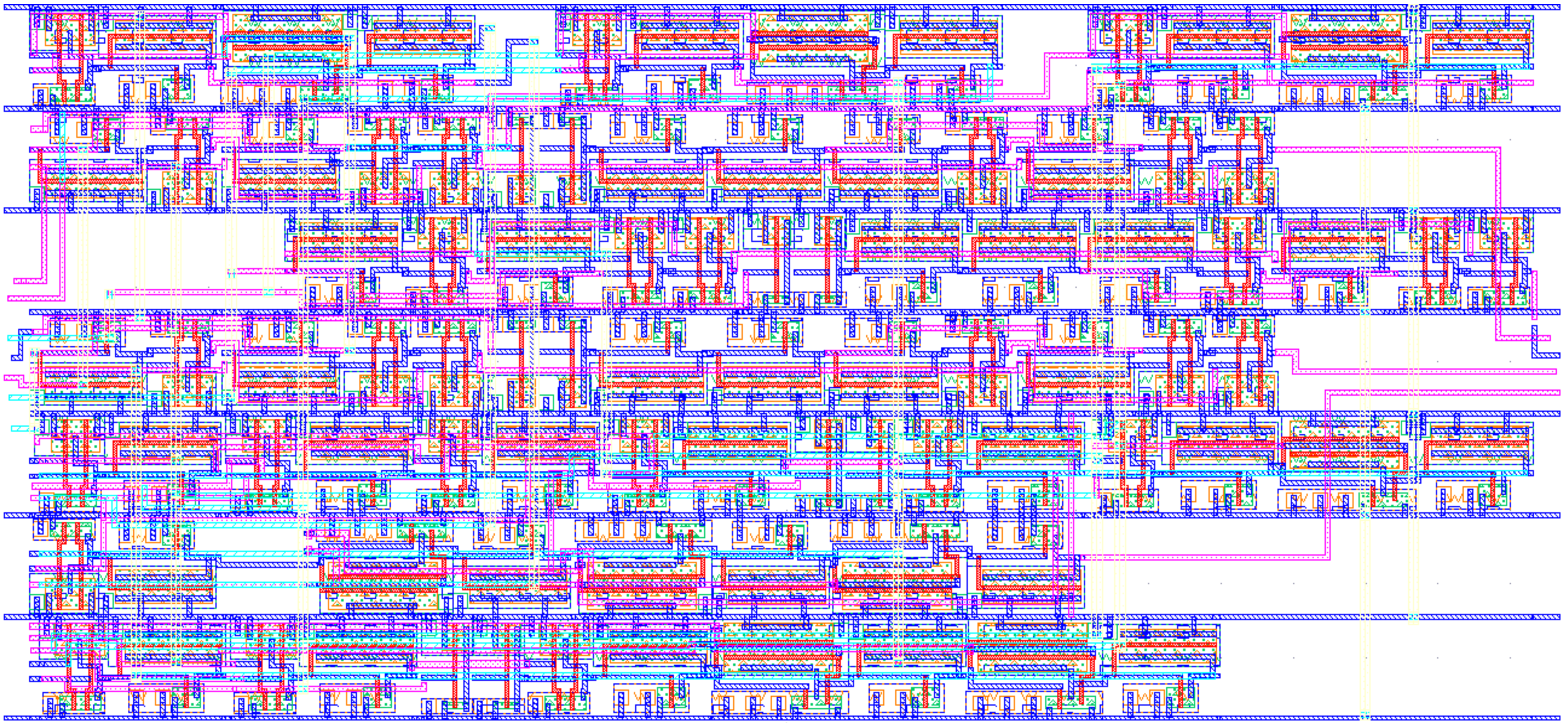


Fig: 12 Layout of 3bit CLA block

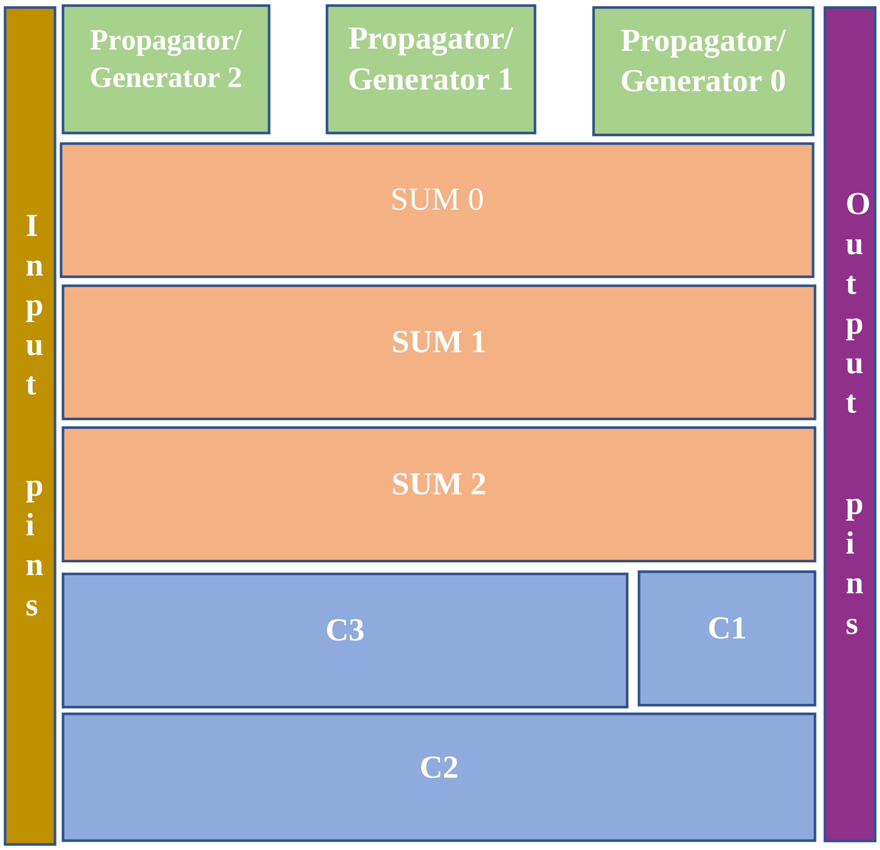


Fig 13: Floor plan of the 3 bit CLA layout

Final 6 bit adder:

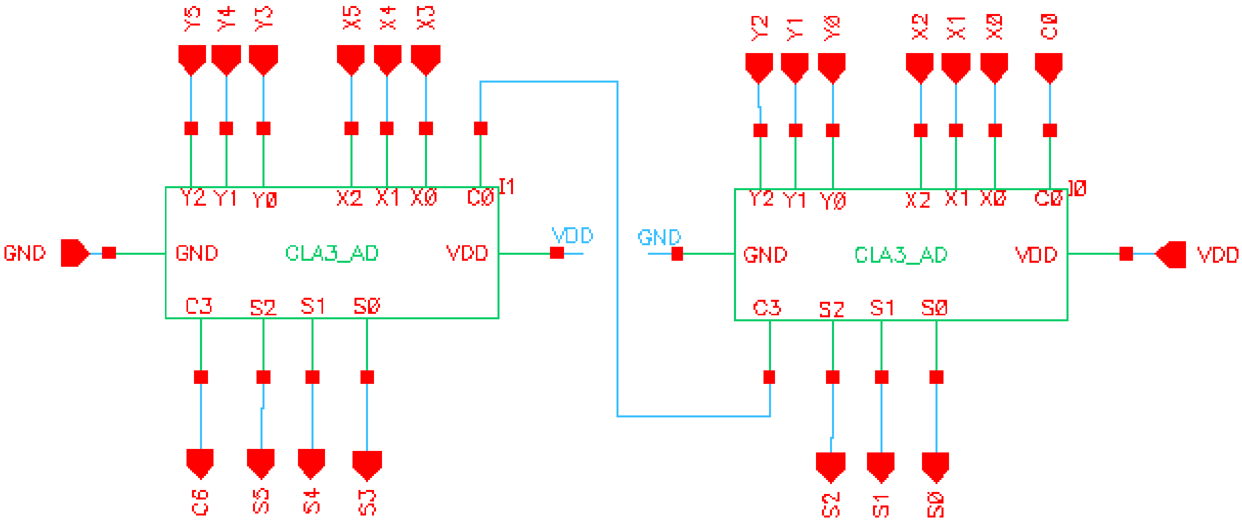


Fig 14: Schematic of 6-bit adder

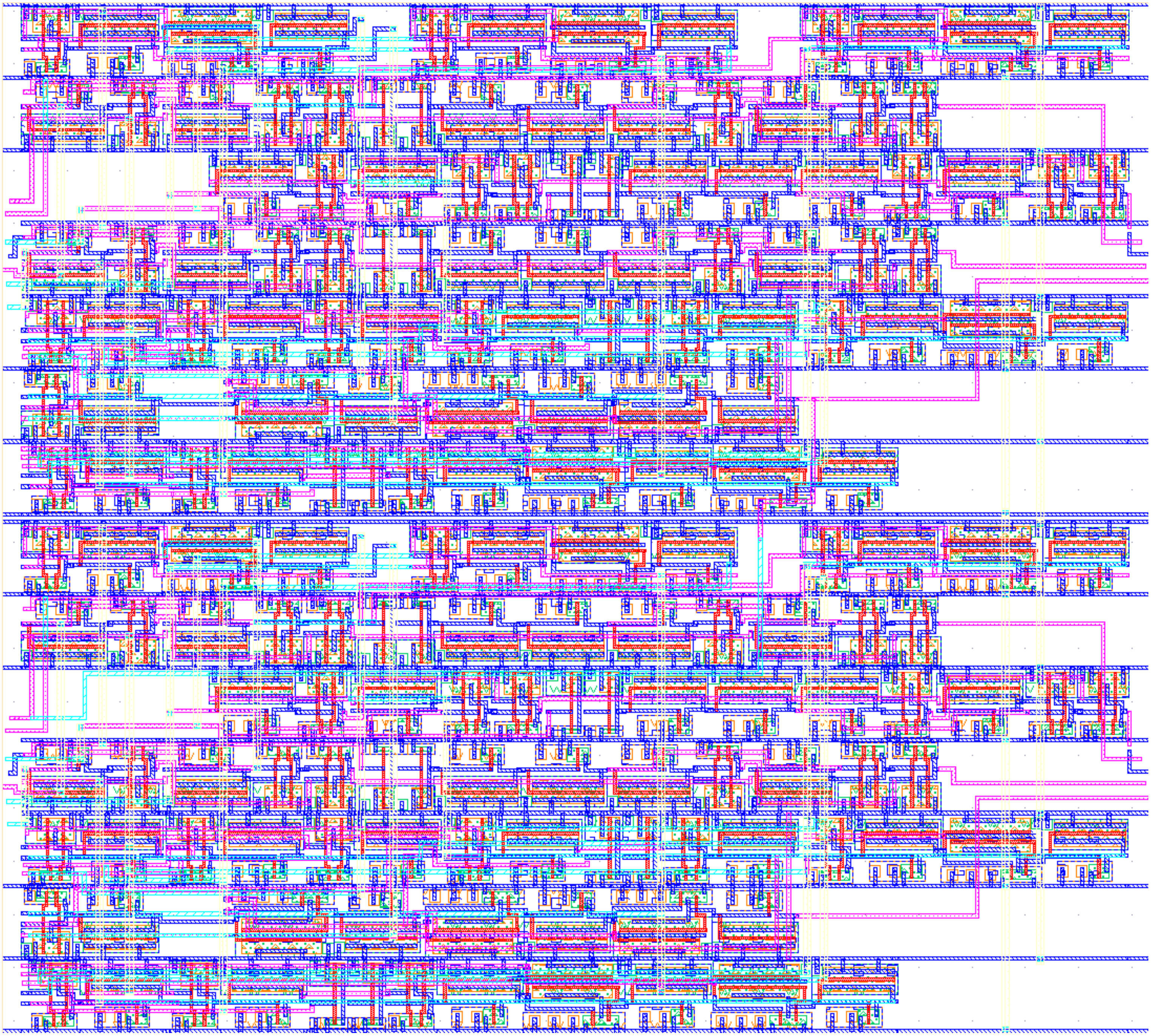


Fig 15: Layout of 6 bit adder

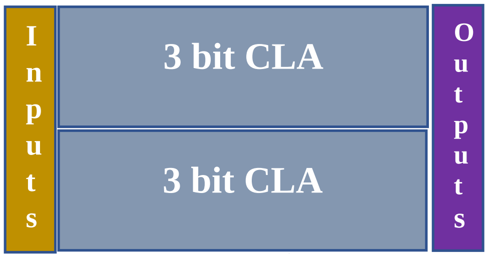


Fig 16: Floorplan of 6 bit adder

Adder with sleep transistor:

Two sleep transistors were included in two 3-bit CLA slices of the adder. The width of the sleep transistors of the adder are chosen to be 2.8um which degrades the F_{max} of the circuit by 4.47% at 1V VDD.

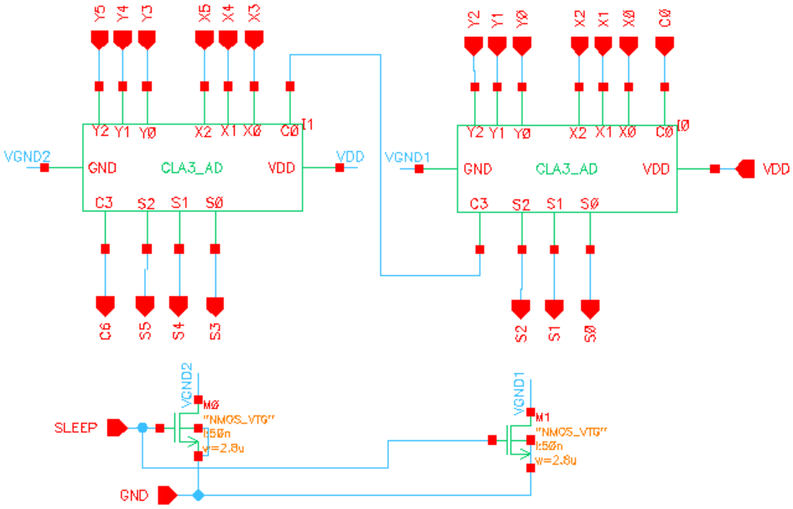


Fig 17: Schematic of 6-bit adder with sleep transistors

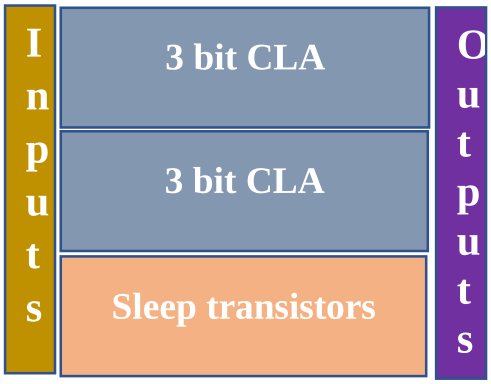


Fig 18: Floorplan of 6-bit adder

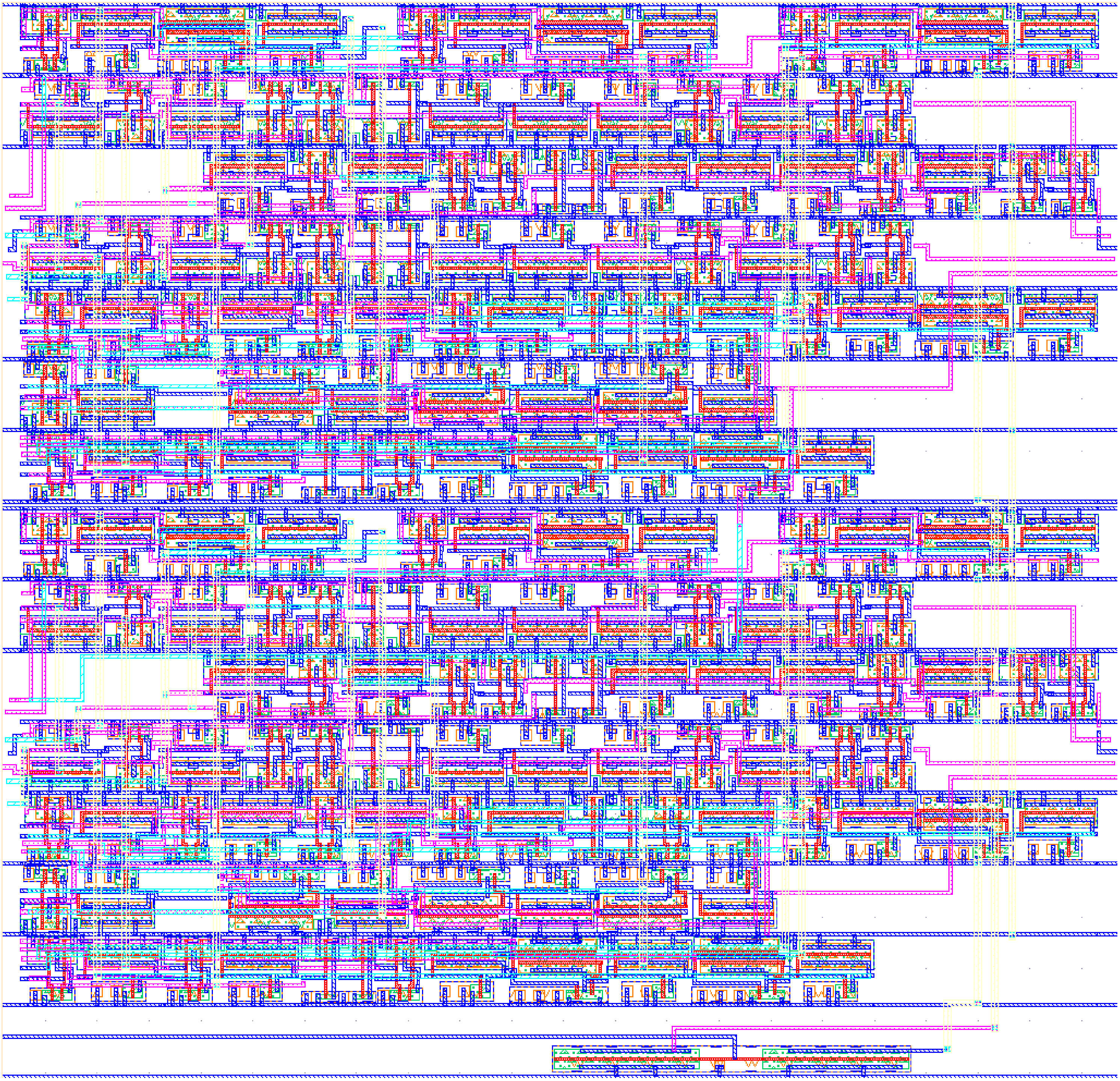
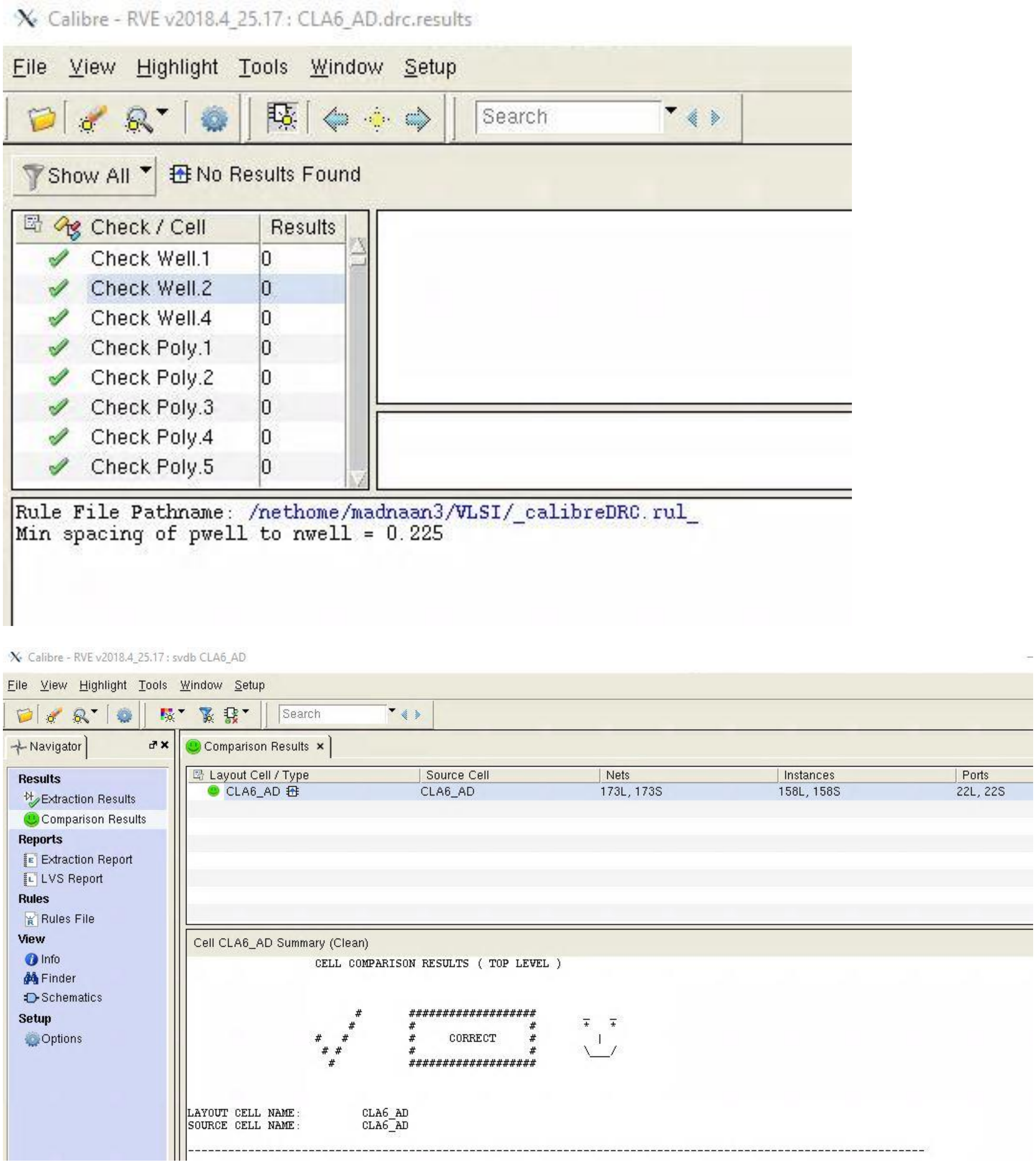


Fig 19: Layout of 6-bit adder with sleep transistor

DRC and LVS Summary of Adder layout:


Calibre - RVE v2018.4_25.17 : CLA6_AD.drc.results
File View Highlight Tools Window Setup
Search
Show All
No Results Found

Check / Cell	Results
✓ Check Well.1	0
✓ Check Well.2	0
✓ Check Well.4	0
✓ Check Poly.1	0
✓ Check Poly.2	0
✓ Check Poly.3	0
✓ Check Poly.4	0
✓ Check Poly.5	0

```
Rule File Pathname: /nethome/madnaan3/VLSI/_calibreDRC.rul_
Min spacing of pwell to nwell = 0.225
```

Layout Cell / Type	Source Cell	Nets	Instances	Ports
CLA6_AD	CLA6_AD	173L, 173S	158L, 158S	22L, 22S

Cell CLA6_AD Summary (Clean)

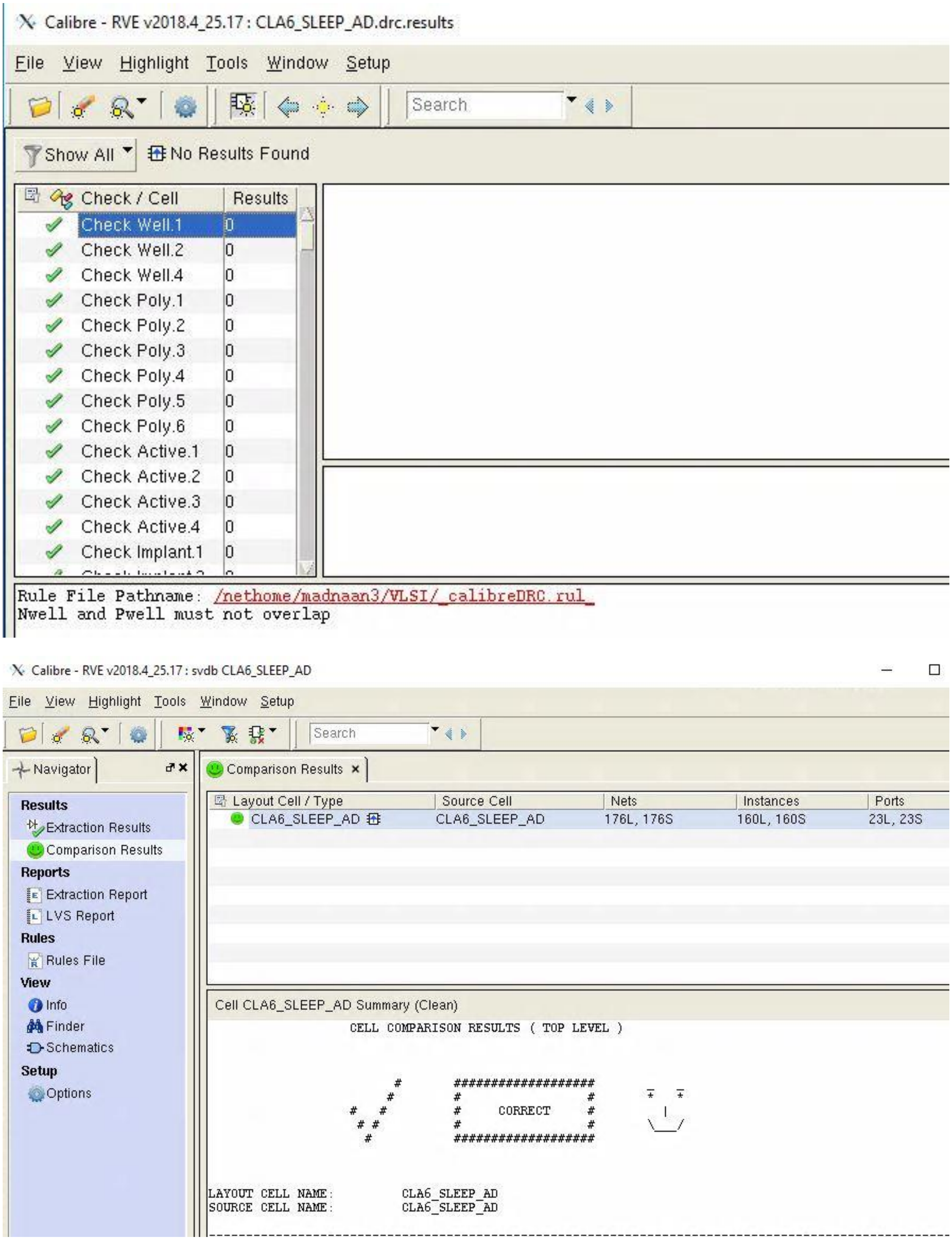
```
                    CELL COMPARISON RESULTS ( TOP LEVEL )


                         #         ###################
                        #          #                 #
                    #   #          #     CORRECT     #
                     # #           #                 #
                      #            ###################


LAYOUT CELL NAME:          CLA6_AD
SOURCE CELL NAME:          CLA6_AD

--------------------------------------------------------------------------------------------------------------
```

Fig 20: DRC and LVS reports of adder layout



Calibre - RVE v2018.4_25.17 : CLA6_SLEEP_AD.drc.results

Check / Cell	Results
✓ Check Well.1	0
✓ Check Well.2	0
✓ Check Well.4	0
✓ Check Poly.1	0
✓ Check Poly.2	0
✓ Check Poly.3	0
✓ Check Poly.4	0
✓ Check Poly.5	0
✓ Check Poly.6	0
✓ Check Active.1	0
✓ Check Active.2	0
✓ Check Active.3	0
✓ Check Active.4	0
✓ Check Implant.1	0

```
Rule File Pathname: /nethome/madnaan3/VLSI/_calibreDRC.rul_
Nwell and Pwell must not overlap
```

Calibre - RVE v2018.4_25.17 : svdb CLA6_SLEEP_AD

Layout Cell / Type	Source Cell	Nets	Instances	Ports
CLA6_SLEEP_AD	CLA6_SLEEP_AD	176L, 176S	160L, 160S	23L, 23S

Cell CLA6_SLEEP_AD Summary (Clean)

```
                    CELL COMPARISON RESULTS ( TOP LEVEL )


                         #        ###################       _   _
                        #         #                 #        *   *
                    #   #         #     CORRECT     #          |
                     # #          #                 #        \___/
                      #           ###################


LAYOUT CELL NAME:         CLA6_SLEEP_AD
SOURCE CELL NAME:         CLA6_SLEEP_AD
--------------------------------------------------------------------------------------------------
```

Fig 21: DRC and LVS reports of adder layout with sleep transistors

MULTIPLIER

The 4-bit unsigned multiplier that has been used here is based on Carry Save adder (CSA) based partial product (PP) reduction. We have used Dadda tree method of partial product reduction.

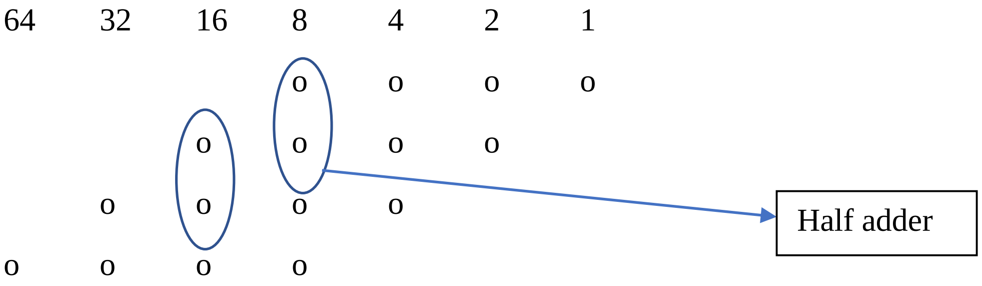
Wallace tree method applies the 3:2 carry save reduction to all the weight positions taking sets of 3 PPs in a weight concurrently (Here maximum four PPs are there in a weight so no concurrency to exploit within 1 weight). Dadda tree in contrast looks up the number of reductions steps for a range of number of PPs and reduces only up to the maximum number in that range. For example, if there are 10 partial products and 7,8 and 9 all three PPs would require 5 steps of reduction if concurrent CSA reduction were done, it will reduce only till 9. This would reduce the resources used and could also reduce delay for a few reduction steps if only half adders are needed in that step.

Operation

First the partial product generation is done using 2 NAND gates (doing an AND operation) for all 4×4 combinations. The multiplier reduces partial products as follows-

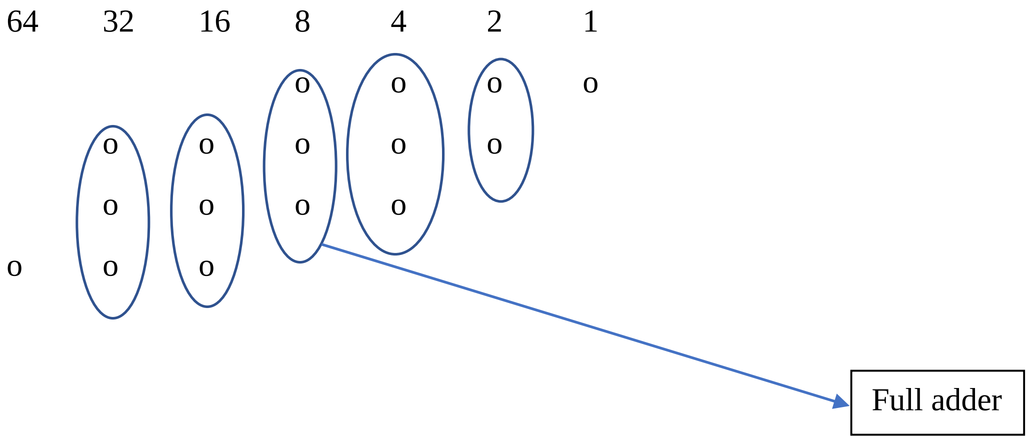
Partial products here are represented by “o” and the numbers above them represent the weights.

Reduction step 1

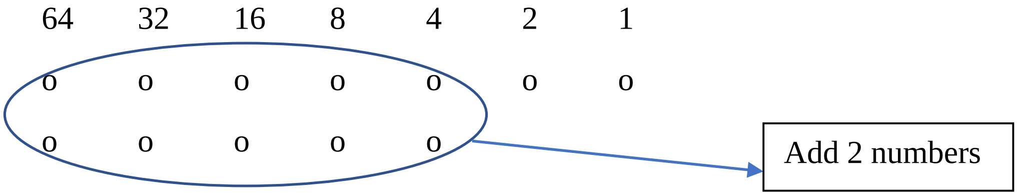


First step (diagram shown above) is reducing all the weights to 3 partial products because a full adder can easily add 3 terms, so we apply one half adder to two weight-8 PPs and two weight-16 PPs, so the weight-8 would reduce to 3 PPs and weight-16 should reduce to 2PPs but a carry from weight-8 computation makes it 3PPs and weight-32 will also have 3PPs due to a carry from weight-16

Reduction step 2



Second step (diagram shown above) is applying one full adder (or half adder if 2 PPs are there) to inputs of each weight concurrently. Now we get two inputs which can be summed by a carry propagate adder so a half adder at weight-4 and full adders at weights-8,16,32 and 64.



So, in all, weight-1 is directly the partial product. Weight-2 requires one half adder for two of its inputs. Weight-4 uses a full adder and a half adder. Similarly, weight-8 and weight-16 use 1 half adder and 2 full adders for each weight. Weight-32 uses 2 full adders and Weight-64 uses 1 full adder. Schematic and block level schematic are made based on that.

By doing carry save reduction, we save a lot of time as we can reduce different weight PPs concurrently (but there is no concurrency within 1 weight PPs).

The worst-case (longest path) delay of the circuit is $2t_{NAND} + 2t_{HA} + 4t_{FA}$

This delay is as good as an adder and hence CSA based reduction is beneficial.

The schematic of the multiplier is as follows-

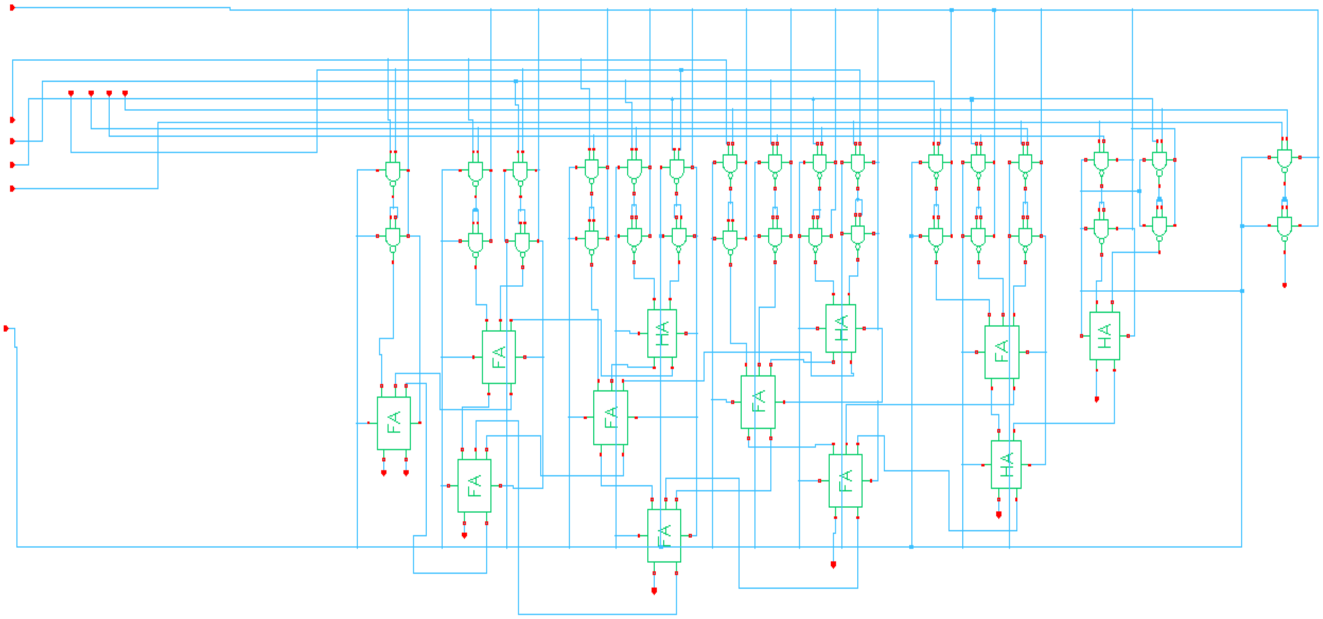


Fig 22: Multiplier Schematic

4-TAP FIR FILTER

FIR Filter Schematic:

The schematic of the FIR filter is as follows-

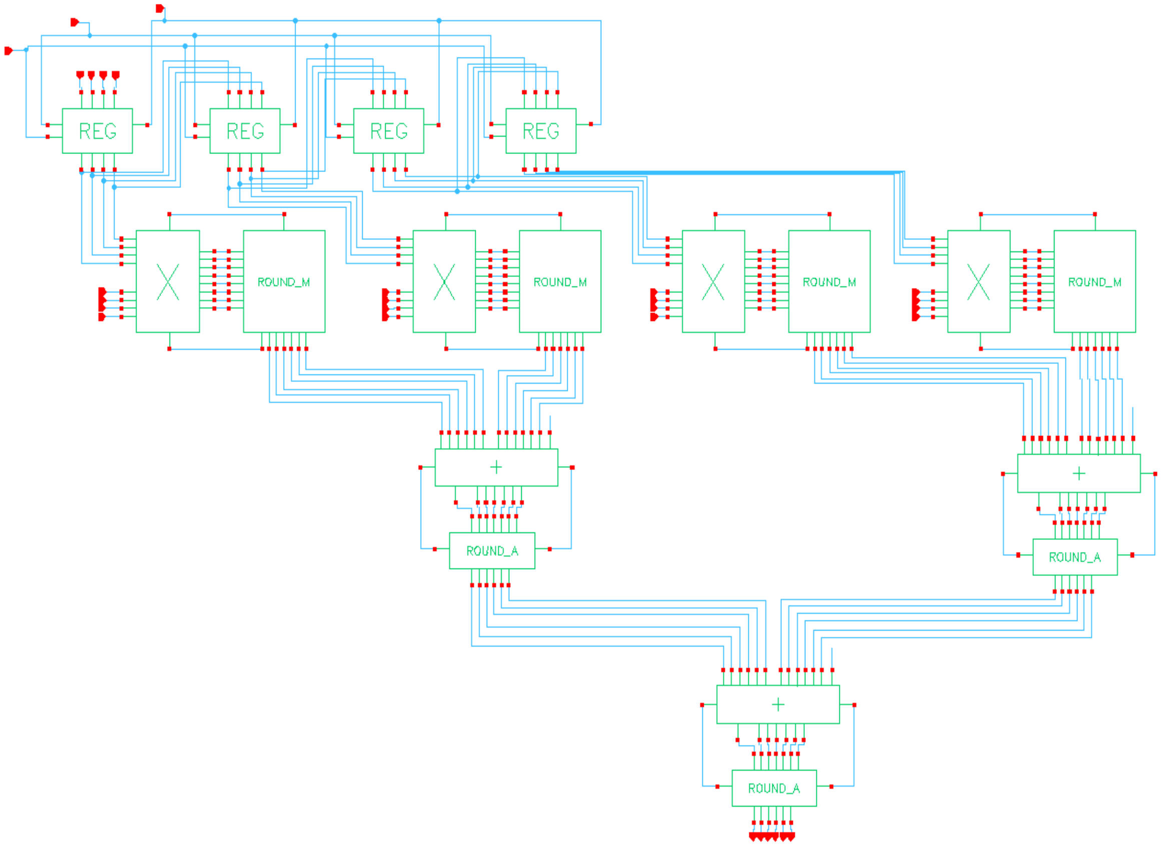


Fig 23: FIR Filter Schematic

The 4-TAP FIR filter operates as follows-

$$\boldsymbol{y = b_o x[n] + b_1 x[n-1] + b_2 x[n-2] + b_3 x[n-3]}$$

The circuit implements the functionality of the 4-TAP FIR filter. The data encoding used here is **4-bit unsigned integer**. Also, since the datapath has to be 6-bit, there are special rounding units which force the result to 111111 (i.e. 63 in decimal) if the result is greater than 63 at every stage.

So the circuit consists of a 4-bit shift register that keeps 4 values. The $\boldsymbol{x[n]}$ data arrives sufficiently before the positive clock edge so that it is captured properly. So the first Register returns the $\boldsymbol{x[n]}$**,** and next 3 registers return $\boldsymbol{x[n-1]}$, $\boldsymbol{x[n-2]}$ and $\boldsymbol{x[n-3]}$

These values are multiplied by the coefficients and then the 8-bit result is rounded using the rounding unit whose schematic is as follows-

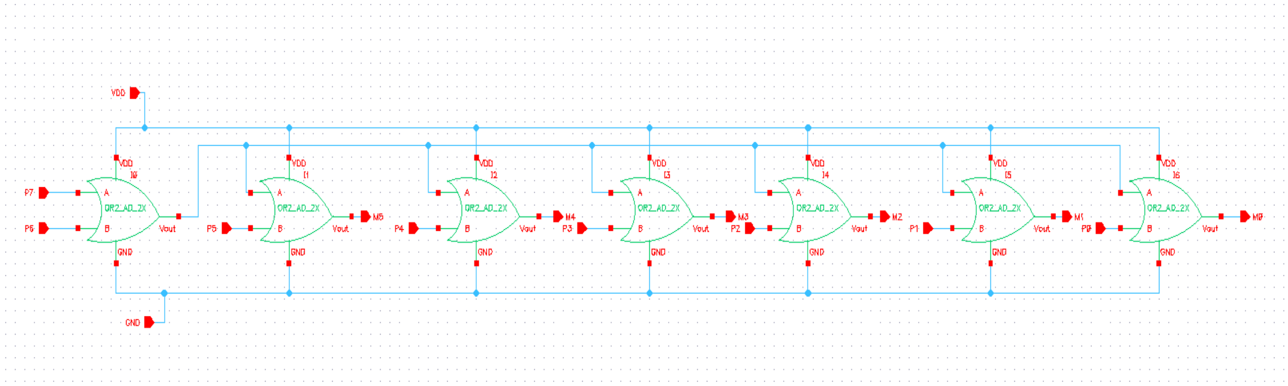


Fig 24: Multiplier Output Rounding Circuitry

Basically P6 and P7 are the extra bits and if any of them is 1, then everything else should be 1 so their OR is ORRed with the other bits.

Then the 4 results are passed to a 4 adders connected in a tree fashion that adds those 4 numbers.

The 7-bit result at each stage of addition is rounded to 6-bits and basically the carry is ORRed with every other bit, so if the carry is 1, all the bits are forced to 1.

The schematic of adder rounding unit is as follows

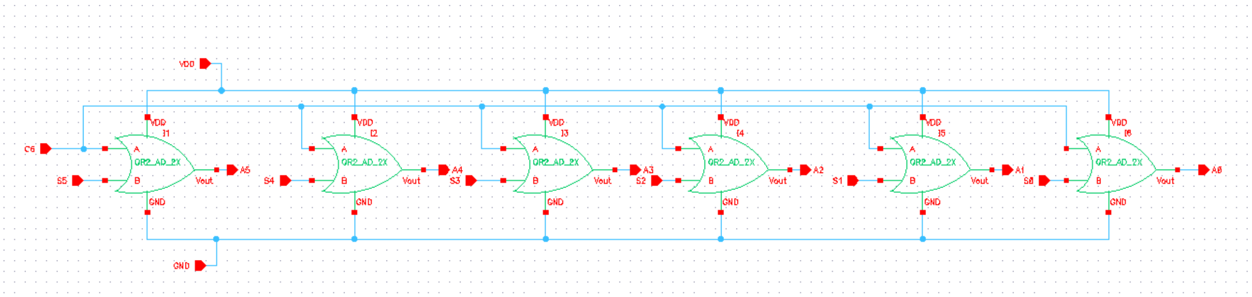


Fig 25: Adder Output Rounding Circuitry

FIR Filter Functionality:

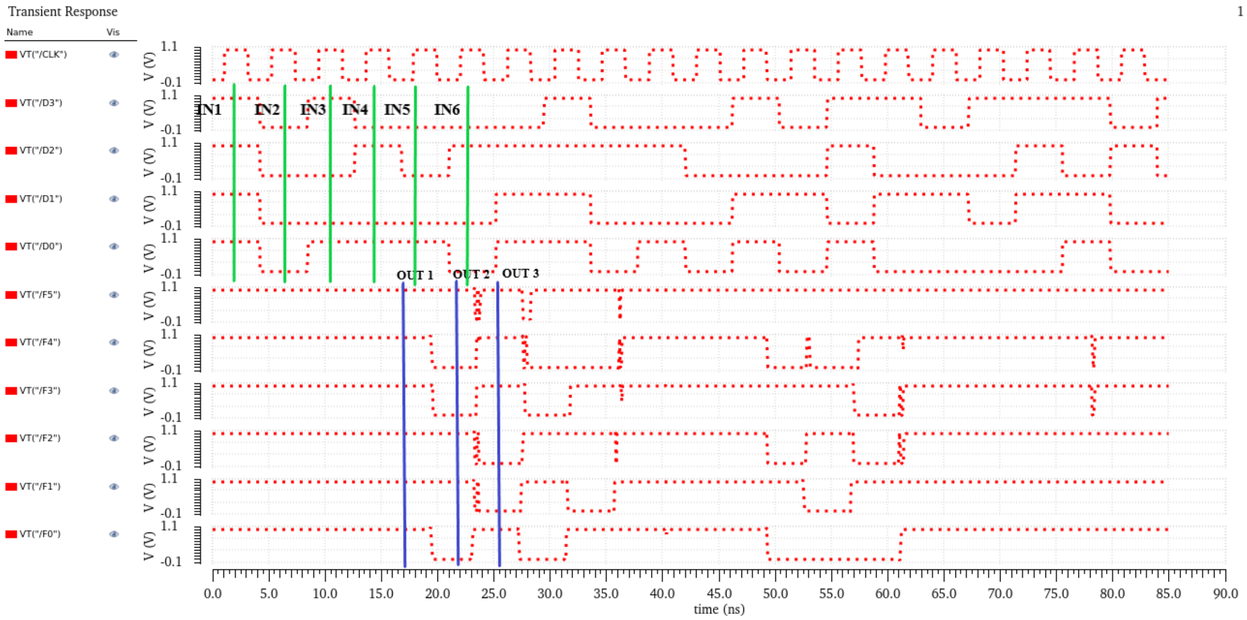


Fig 26: Input and Output for the FIR Filter at VDD = 1V, Frequency of Operation = F_{MAX} = 242.42MHz

To test the functionality, we fixed the weights to arbitary values i.e. W0 = 4'b0001, W1 = 4'b0010, W2 = 4'b0011 and W3 = 4'b0100.

The above figure shows the waveforms snapshot for a simulation of 20 random input strings and their corresponding outputs. As we have implemented a 4-Tap FIR filter, the correct output starts arriving after the 4th Clock.

As per the above snapshot of the simulation, IN1 = 4'b1111='d15, IN2 = 4'b0000 = 'd0, IN3 = 4'b1001='d9, IN4 = 4'b0101='d5, IN5 = 4'b0001='d1, IN6 = 4'b0100='d4.

Now for the First Correct Output (OUT1 in Fig):

$$\boldsymbol{OUT1 = 1 \times IN4 + 2 \times IN3 + 3 \times IN2 + 4 \times IN1}$$

$$\boldsymbol{OUT1 \ = 1 \times 5 + 2 \times 9 + 3 \times 0 + 4 \times 15 = {}'d83}$$

We observe that OUT1 = 6'b111111 which is what we expected. (Actual output value = 'd83 rounded to 'd63 = 6'b111111 as per our rounding logic for a 6-bit Datapath)

Similarly we have:

$$\boldsymbol{OUT2 = 1 \times IN5 + 2 \times IN4 + 3 \times IN3 + 4 \times IN2}$$

$$\boldsymbol{OUT2 = 1 \times 1 + 2 \times 5 + 3 \times 9 + 4 \times 0 \ \ = {}'d38 \ \ = 6'b100110}$$

Similarly,

$$\boldsymbol{OUT3 = 1 \times IN6 + 2 \times IN5 + 3 \times IN4 + 4 \times IN3}$$

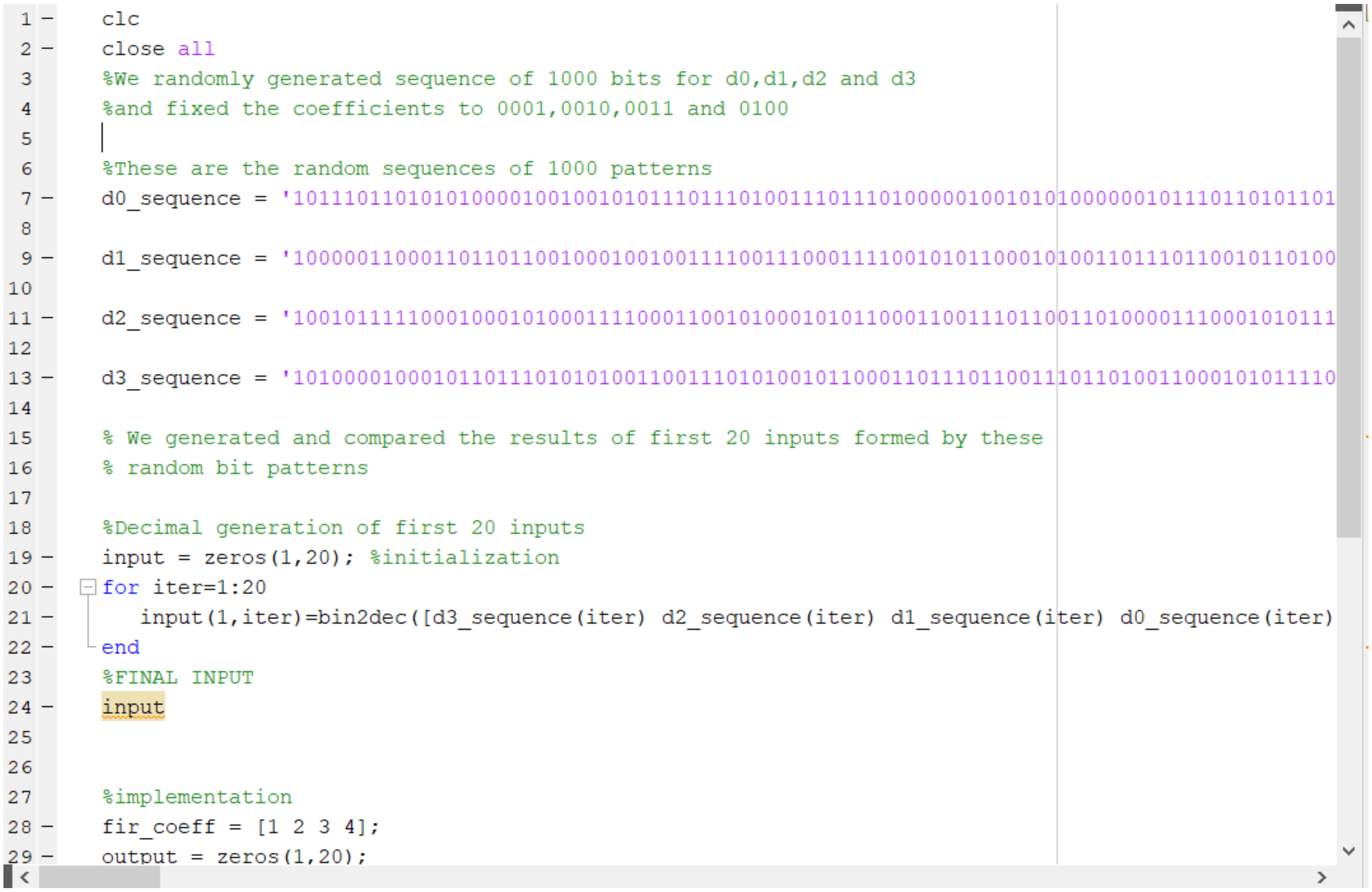
$$\boldsymbol{OUT3 = 1 \times 4 + 2 \times 1 + 3 \times 5 + 4 \times 9 = {}'d57 = 6'b111001}$$

From the above snapshot we can observe OUT2 = 6’b100110 and OUT3 = 6’b111001, which is correct. Similarly, rest of the outputs in the simulation can be verifed. Therefore, we see that the functionality of our implementation of the FIR filter meets the expected behaviour.

Note: *The arriving data was given sufficiently before the positive edge of the clock so that it was captured at the edge*

The values can also be verified by computing the function mathematically on MATLAB.

MATLAB code screenshots are as follows-



```
clc
close all
%We randomly generated sequence of 1000 bits for d0,d1,d2 and d3
%and fixed the coefficients to 0001,0010,0011 and 0100

%These are the random sequences of 1000 patterns
d0_sequence = '1011101101010100001001001010111011101001110111010000010010101000000101110110101101

d1_sequence = '1000001100011011011001000100100111100111000111100101011000101001101110110010110100

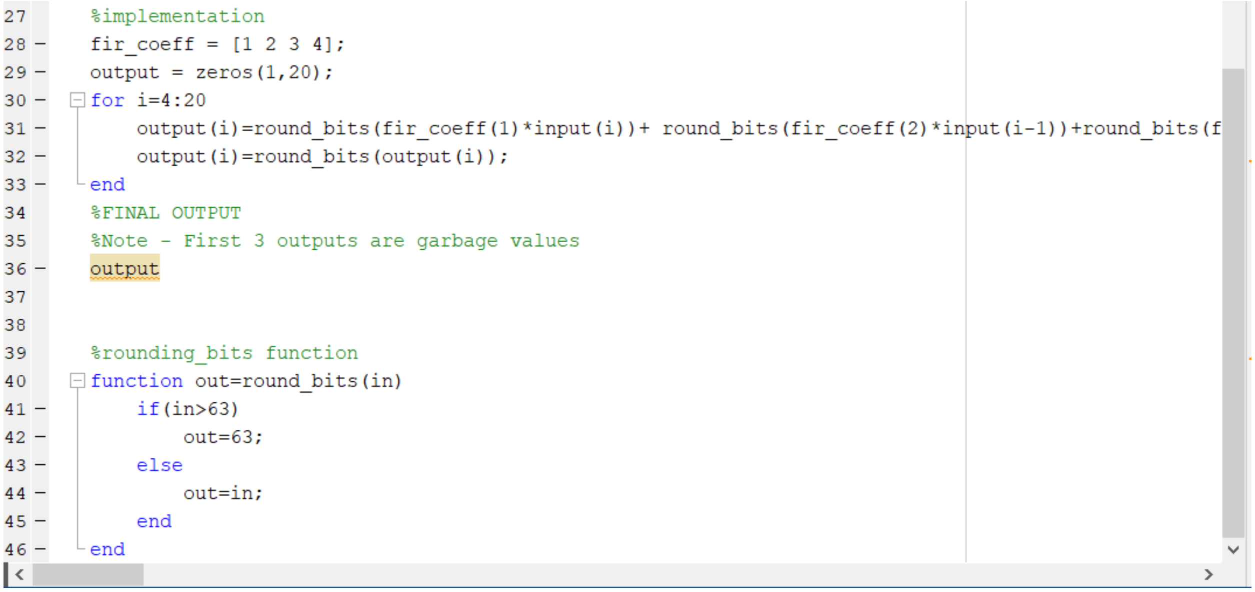
d2_sequence = '1001011111000100010100011110001100101000101011000110011101100110100001110001010111

d3_sequence = '1010000100010110111010101001100111010100101100011011101100111011010011000101011110

% We generated and compared the results of first 20 inputs formed by these
% random bit patterns

%Decimal generation of first 20 inputs
input = zeros(1,20); %initialization
for iter=1:20
   input(1,iter)=bin2dec([d3_sequence(iter) d2_sequence(iter) d1_sequence(iter) d0_sequence(iter)
end
%FINAL INPUT
input

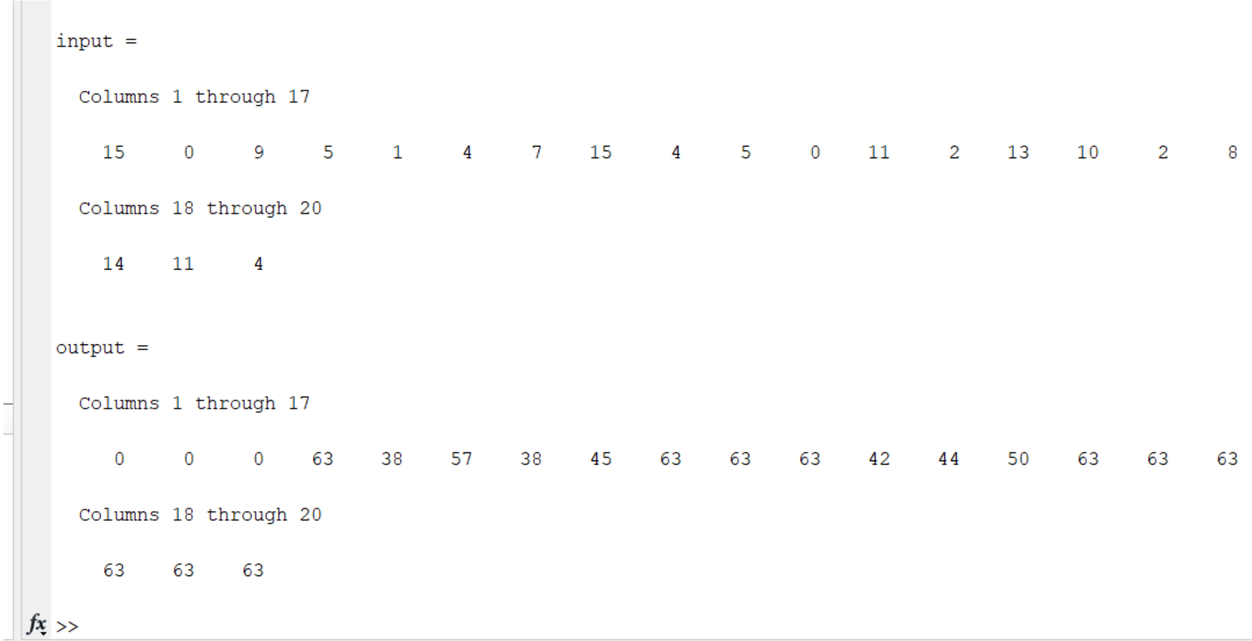

%implementation
fir_coeff = [1 2 3 4];
output = zeros(1,20);
```



```
%implementation
fir_coeff = [1 2 3 4];
output = zeros(1,20);
for i=4:20
    output(i)=round_bits(fir_coeff(1)*input(i))+ round_bits(fir_coeff(2)*input(i-1))+round_bits(f
    output(i)=round_bits(output(i));
end
%FINAL OUTPUT
%Note - First 3 outputs are garbage values
output


%rounding_bits function
function out=round_bits(in)
    if(in>63)
        out=63;
    else
        out=in;
    end
end
```

We displayed the inputs and the outputs which are as follows-



```
input =

  Columns 1 through 17

    15     0     9     5     1     4     7    15     4     5     0    11     2    13    10     2     8

  Columns 18 through 20

    14    11     4


output =

  Columns 1 through 17

     0     0     0    63    38    57    38    45    63    63    63    42    44    50    63    63    63

  Columns 18 through 20

    63    63    63

fx >>
```

FIR Filter Analysis:

The FIR Filter circuit is tested for its Maximum Frequency of operation, Active Dynamic and Active Leakage Power consumtion. As per the Project Statement, we further report the Energy consumption for a 1000 string input and its point of maximum energy efficiency. Sleep transistors are added further into the analysis and the circuit is tested for its Standby Power consumption with the new additions.

Maximum Frequency of Operation:

To test the circuit for its maximum frequency of operation, we followed a systematic apporach. We initially calculated the individual critical path worst case delays for all the logic blocks in the datapath by simulating them individually. We then calculated the total time delay for the complete FIR filter. This provided us with a starting point to further simulate the complete FIR filter circuit. We then simulated the FIR filter with frequency equal to the inverse of the total delay of the individual blocks in the FIR datapath.

The above analysis was performed for VDD ranging from 1V to 0.2V to get the maximum frequency of operation as a function of VDD.

Table 1. F_{MAX} vs VDD

VDD (V)	F_{MAX} for FIR Filter
1	242.4242 MHz
0.9	167.5182 MHZ
0.8	95.4271 MHz
0.7	39.0166 MHz
0.6	10.3407 MHz
0.5	1.9890 MHz
0.4	0.3292 MHz
0.3	0.05137 MHz
0.2	0.0084 MHz

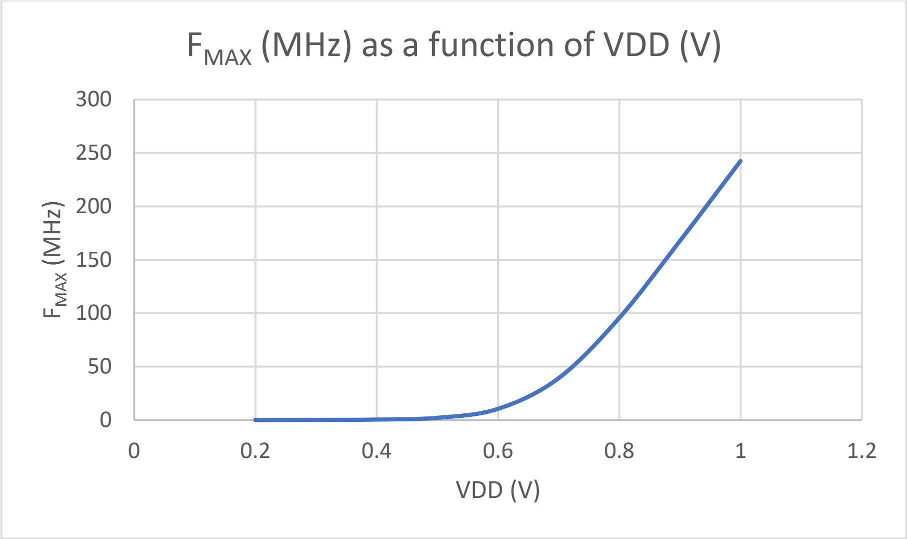


Fig 27. F_{MAX} (MHz) vs VDD (V)

Active Dynamic and Leakage Power:

The Active Power as a function of VDD was evaluated. We used a random pattern as the input to induce switching in the FIR Filter circuit. We report the Active Leakage power, Average Dynamic Power consumed as well the Peak Power consumption for our input test pattern.

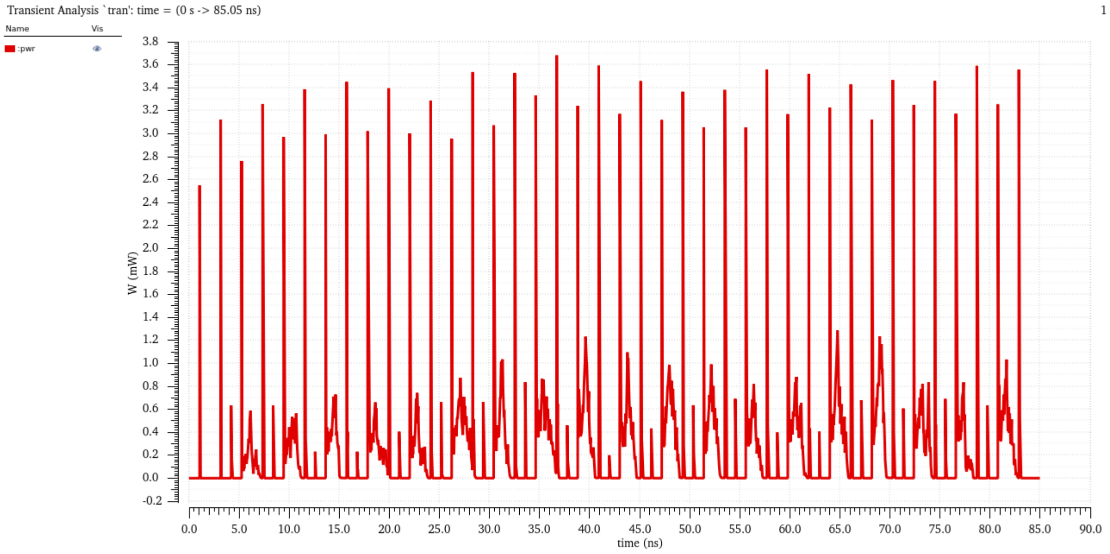


Fig 28: Transient Analysis Simulation for Active Power for a random input string of 20 values for VDD =1 V

Table 2. Active Leakage Power vs VDD

VDD (V)	Active Leakage Power (nW)
1	265.35
0.9	170.69
0.8	100.53
0.7	62.31
0.6	38.55
0.5	21.36
0.4	12.38
0.3	6.72
0.2	3.16

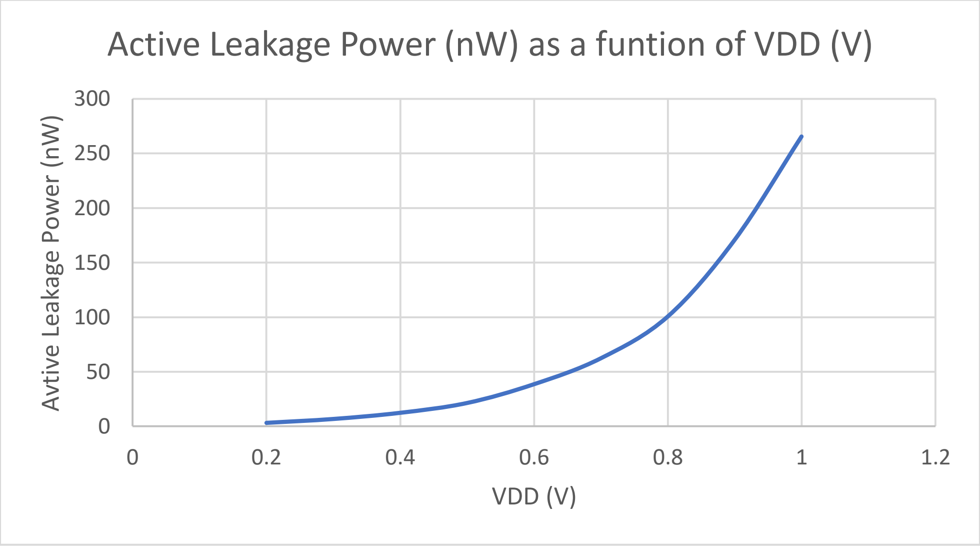


Fig 28. Active Leakage Power (nW) vs VDD (V)

Table 3. Average and Peak Dynamic Power vs VDD

VDD (V)	Average Dynamic Power	Peak Dynamic Power
1	191.0 uW	3.682 mW
0.9	121.6 uW	2.267 mW
0.8	53.39 uW	1.227 mW
0.7	16.78 uW	467.2 uW
0.6	3.23 uW	119.8 uW
0.5	451.3 nW	16.03 uW
0.4	58.47 nW	1.418 uW
0.3	10.57 nW	107.9 nW
0.2	3.45 nW	8.916 nW

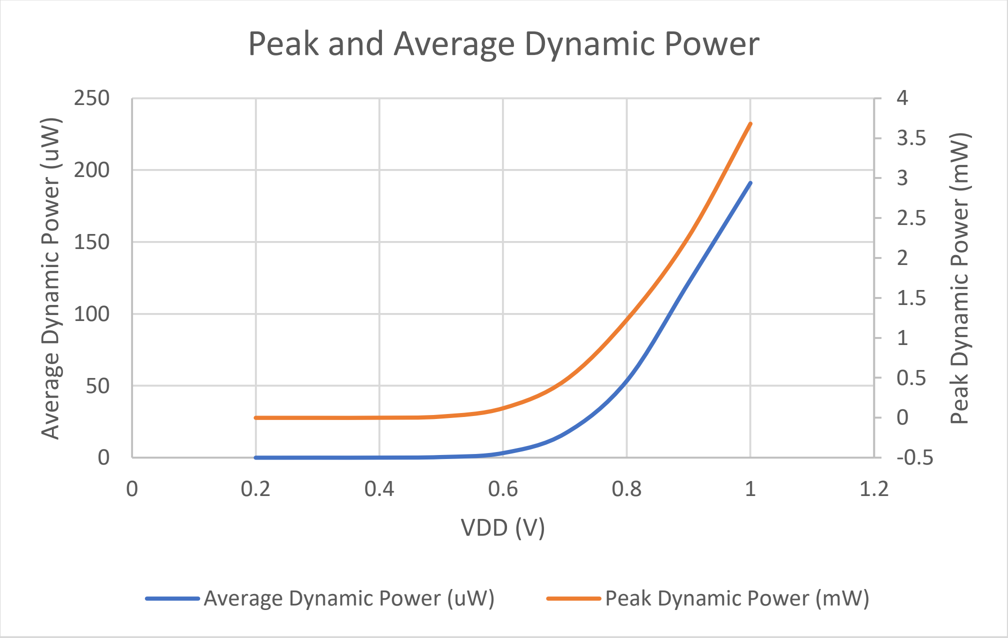


Fig. 29 Peak (mW) and Average (uW) Dynamic Power vs VDD (V)

Energy Consumption:

The energy consumption of the filter for 1000 strings is tabulated as follows. Maximum frequency of operation at each VDD voltage was considered.

Table 4: VDD vs Energy Consumption

VDD(V)	Energy Consumption for 1000 input strings
1	877.5 pJ
0.9	718.9 pJ
0.8	565.8 pJ
0.7	432.6 pJ
0.6	316.7 pJ
0.5	228.8 pJ
0.4	178.0 pJ
0.3	208.8 pJ
0.2	413.6 pJ

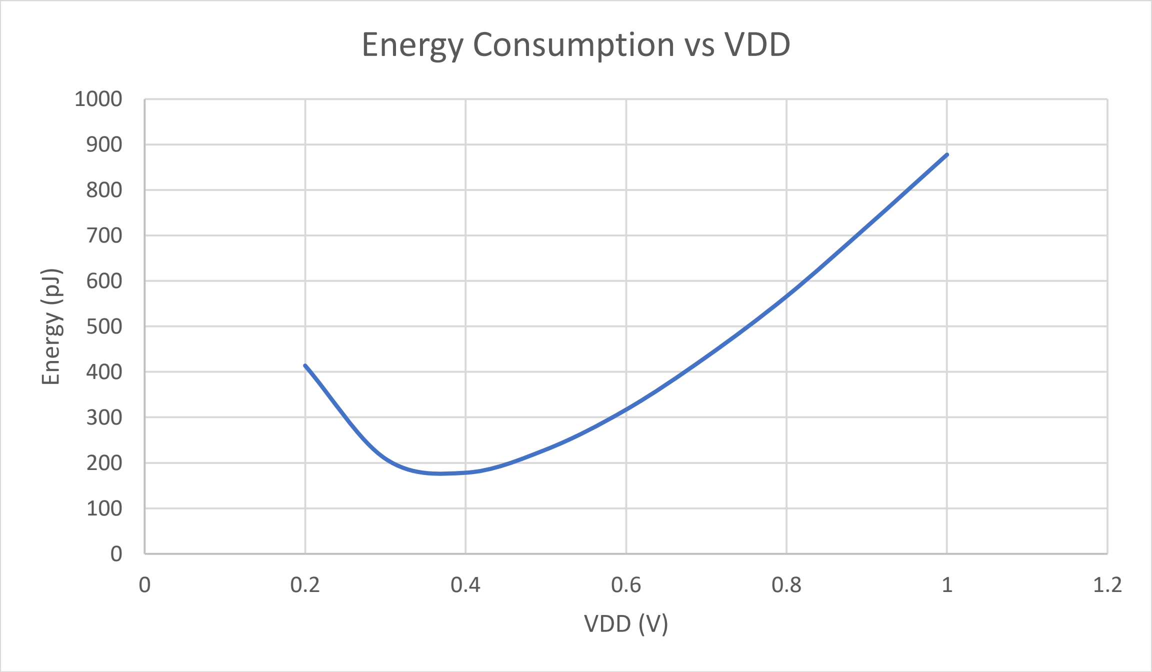


Fig 30: VDD (V) vs Energy Consumption (pJ) for 1000 input strings

From the above plot, the point of maximum energy efficiency is at VDD = 0.38V.

Standby Leakage Power with Sleep Transistors:

We used sleep transistors for supply gating. Each 4-Bit Register is supply gated with a sleep transistor. For our 6-Bit adder, each 3-Bit CLA slice was given its own sleep transistor. Each Multiplier unit was provided with a sleep transistor. The rounding units for each Multiplier were also connected with individual sleep transistors. The widths of the NMOS sleep transistors used for VDD = 1V are as follows:

$$W_{Sleep\_Dff} = 200nm$$
$$W_{Sleep\_Mult\_round\_unit} = 350nm$$
$$W_{Sleep\_Multiplier} = 1525nm$$
$$W_{Sleep\_3\text{-}bit\_CLA} = 2800nm$$

The usage of Sleep transistors introduces a trade-off between standby leakage power and maximum frequency of operation. While their addition does decrease the leakage power however, the maximum frequency of operation also decreases. We made sure that we fix the size of the sleep transistors in a way such that the max frequency of operation doesn't decrease by more than 5%.

The maximum frequency of operation of the FIR Filter with the above configuration of Sleep Transistors at VDD=1V is 230.73MHz. This is a 4.82% degradation from a F_{MAX} = 242.42MHz without Sleep Transistors for our design.

We evaluated standby leakage power when the sleep transistor was ON and OFF

Plots for sleep transistor -

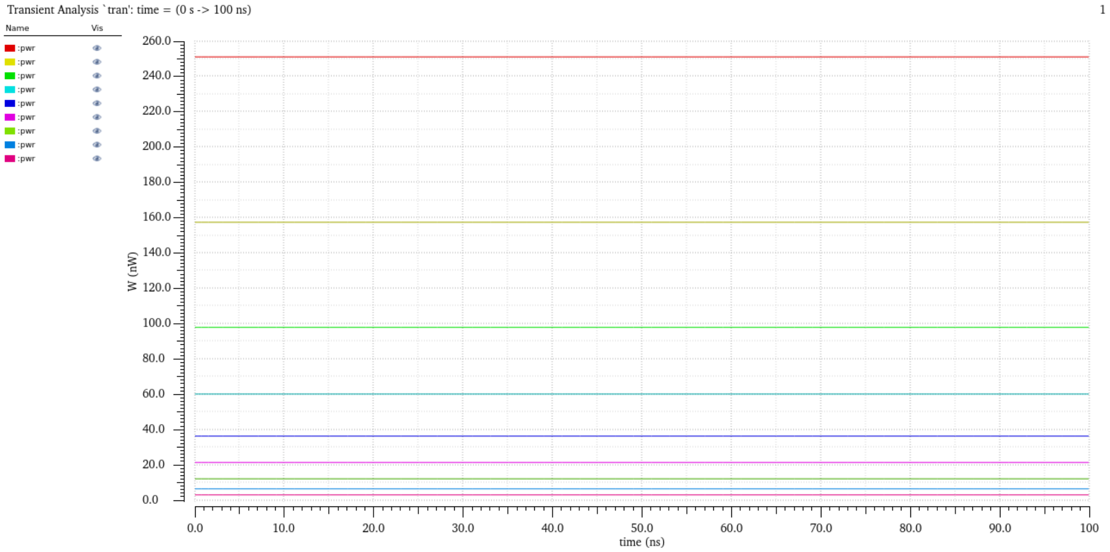


Fig 31: Transient Analysis Simulations for Standby Leakage (Sleep ON) for VDD in range (0.2V – 1V, 0.1V steps).

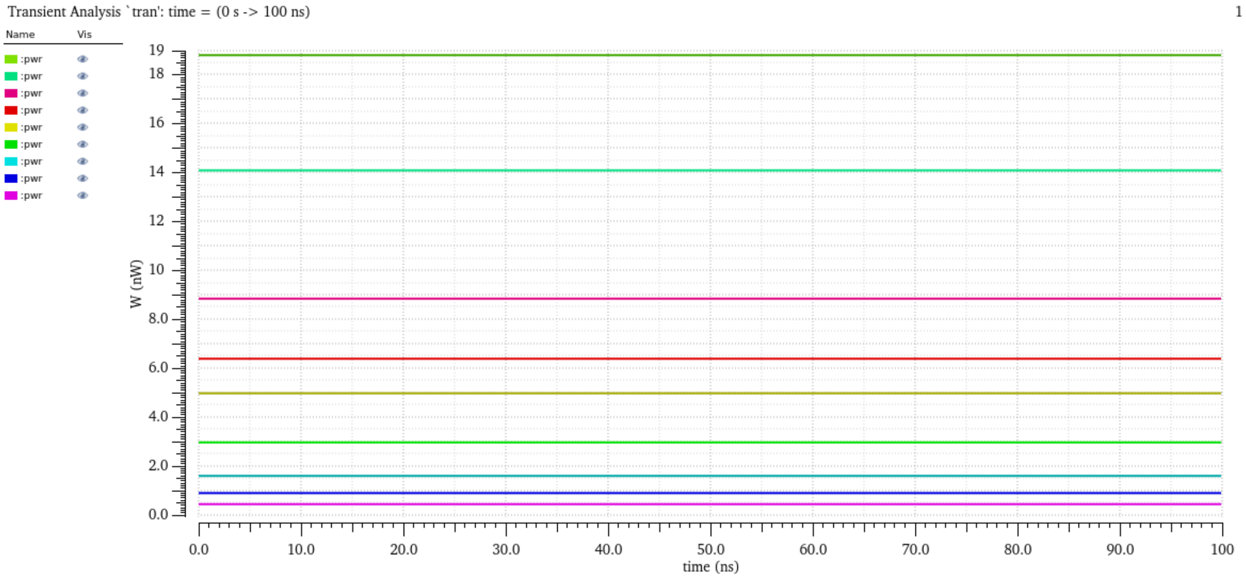


Fig 32: Transient Analysis Simulations for Standby Leakage (Sleep OFF) for VDD in range (0.2V – 1V, 0.1V steps).

Table 5. Standby Leakage Power vs VDD

VDD	Leakage with Sleep Transistor “On”	Leakage with Sleep Transistor “Off”
1	251.15 nW	18.82 nW
0.9	157.46 nW	14.1 nW
0.8	97.91 nW	8.86 nW
0.7	60.15 nW	6.40 nW
0.6	36.33 nW	4.98 nW
0.5	21.40 nW	2.97 nW
0.4	12.14 nW	1.60 nW
0.3	6.46 nW	0.9 nW
0.2	3.04 nW	0.447 nW

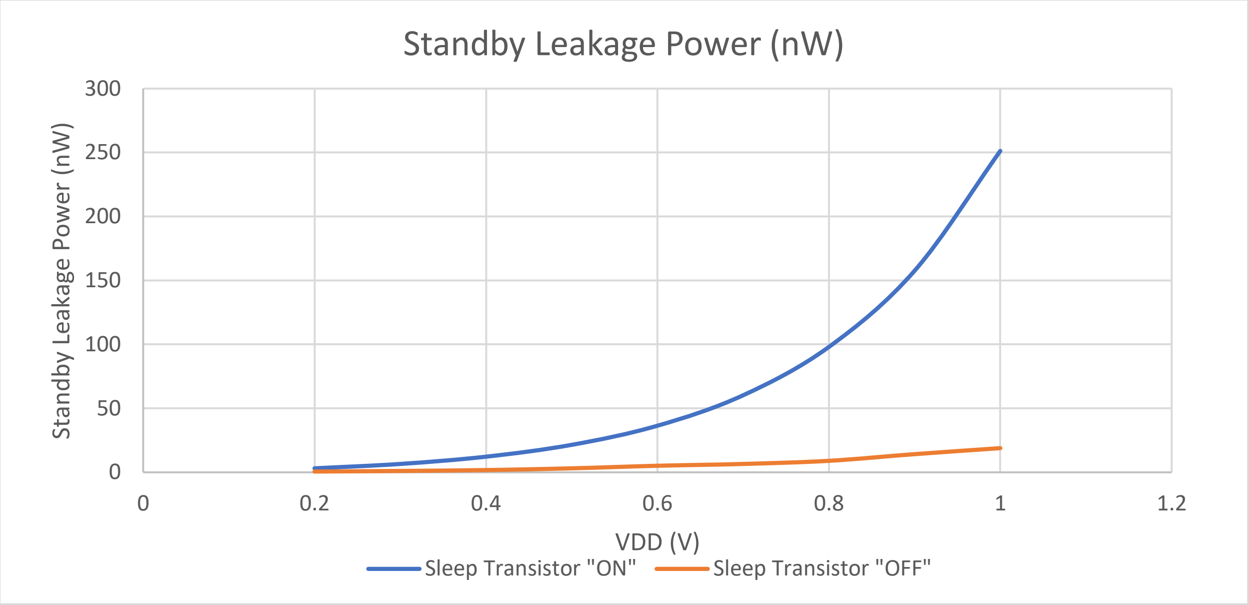


Fig 33: Standby Leakage Power vs VDD with Sleep Transistor “ON” and “OFF”

Conclusion:

In our design we have tried to optimize the performance by choosing suitable topology for multiplier and adder. Besides, we have tried to minimize the area of physical layout of the adder by placing the blocks as close as possible. After implementing a functionally accurate 4 tap FIR filter we have performed simulations to measure its various performance metrics. From the simulations we can observe that fmax of the circuit and power consumption (both dynamic and static) increases with increasing the supply voltage which are in accordance with theoretical predictions. In case of consumed energy to filter a particular number of inputs we have seen that energy consumption at first decreases as we increase the supply voltage. Then after reaching a minimum value it starts to increase with increasing supply voltage. The intuition behind this scenario is- energy consumption depends on two factors: time required to filter the inputs and power consumed during the process. When we decrease the supply voltage beyond the value of the voltage which gives minimum energy consumption, though the power consumption is less, it takes a long time to do the filtering which ultimately increases its energy consumption. On the other hand, at high supply voltage power consumption is higher and time required to do the filtering is less. But the increase of power consumption dominates over the reduction of time in filtering which causes the increase in energy consumption. Finally, we have also observed the effect of sleep transistors and verified that incorporating sleep transistors in the design reduces the leakage power to a great extent.

DRC and LVS Reports of ADDER

```
================================================================================
==
=== CALIBRE::DRC-H SUMMARY REPORT
===
Execution Date/Time:       Sun Nov 10 23:49:27 2019
Calibre Version:           v2018.4_25.17    Thu Nov 1 16:52:36 PDT 2018
Rule File Pathname:        /nethome/madnaan3/VLSI/_calibreDRC.rul_
Rule File Title:
Layout System:             GDS
Layout Path(s):            CLA6_AD.calibre.db
Layout Primary Cell:       CLA6_AD
Current Directory:         /nethome/madnaan3/VLSI
User Name:                 madnaan3
Maximum Results/RuleCheck: 1000
Maximum Result Vertices:   4096
DRC Results Database:      CLA6_AD.drc.results (ASCII)
Layout Depth:              ALL
Text Depth:                PRIMARY
Summary Report File:       CLA6_AD.drc.summary (REPLACE)
Geometry Flagging:         ACUTE = NO  SKEW = NO  ANGLED = NO  OFFGRID = NO
                           NONSIMPLE POLYGON = NO  NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping:         COMMENT TEXT + RULE FILE INFORMATION
Layers:                    MEMORY-BASED
Keep Empty Checks:         YES
--------------------------------------------------------------------------------
--
--- RUNTIME WARNINGS
---
--------------------------------------------------------------------------------
--
--- ORIGINAL LAYER STATISTICS
---
LAYER pwell ...... TOTAL Original Geometry Count = 5   (476)
LAYER nwell ...... TOTAL Original Geometry Count = 5   (360)
LAYER active ..... TOTAL Original Geometry Count = 12  (1824)
LAYER poly ....... TOTAL Original Geometry Count = 21  (1236)
LAYER pimplant ... TOTAL Original Geometry Count = 6   (1126)
LAYER nimplant ... TOTAL Original Geometry Count = 6   (698)
LAYER vth ........ TOTAL Original Geometry Count = 0   (0)
LAYER vtg ........ TOTAL Original Geometry Count = 8   (360)
LAYER metal1 ..... TOTAL Original Geometry Count = 269 (6144)
LAYER contact .... TOTAL Original Geometry Count = 11  (1942)
LAYER metal2 ..... TOTAL Original Geometry Count = 54  (561)
LAYER metal3 ..... TOTAL Original Geometry Count = 26  (253)
LAYER metal4 ..... TOTAL Original Geometry Count = 23  (138)
LAYER metal5 ..... TOTAL Original Geometry Count = 0   (0)
LAYER metal6 ..... TOTAL Original Geometry Count = 0   (0)
LAYER metal7 ..... TOTAL Original Geometry Count = 0   (0)
LAYER metal8 ..... TOTAL Original Geometry Count = 0   (0)
LAYER metal9 ..... TOTAL Original Geometry Count = 0   (0)
LAYER metal10 .... TOTAL Original Geometry Count = 0   (0)
LAYER via1 ....... TOTAL Original Geometry Count = 2   (292)
LAYER via2 ....... TOTAL Original Geometry Count = 1   (110)
LAYER via3 ....... TOTAL Original Geometry Count = 1   (96)
LAYER via4 ....... TOTAL Original Geometry Count = 0   (0)
LAYER via5 ....... TOTAL Original Geometry Count = 0   (0)
LAYER via6 ....... TOTAL Original Geometry Count = 0   (0)
LAYER via7 ....... TOTAL Original Geometry Count = 0   (0)
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LAYER via9 ....... TOTAL Original Geometry Count = 0   (0)
--------------------------------------------------------------------------------
```

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RULECHECK Antenna.metal9 .... TOTAL Result Count = 0 (0)
RULECHECK Antenna.metal10 ... TOTAL Result Count = 0 (0)
--------------------------------------------------------------------------------
--
--- RULECHECK RESULTS STATISTICS (BY CELL)
---
--------------------------------------------------------------------------------
--
--- SUMMARY
---
TOTAL CPU Time:                  0
TOTAL REAL Time:                 0
TOTAL Original Layer Geometries: 450 (15616)
TOTAL DRC RuleChecks Executed:   167
TOTAL DRC Results Generated:     0 (0)
```

```
                  ##################################################
                  ##                                              ##
                  ##         C A L I B R E    S Y S T E M         ##
                  ##                                              ##
                  ##             L V S   R E P O R T              ##
                  ##                                              ##
                  ##################################################


REPORT FILE NAME:         CLA6_AD.lvs.report
LAYOUT NAME:              /nethome/madnaan3/VLSI/CLA6_AD.sp ('CLA6_AD')
SOURCE NAME:              /nethome/madnaan3/VLSI/CLA6_AD.src.net ('CLA6_AD')
RULE FILE:                /nethome/madnaan3/VLSI/_calibreLVS.rul_
RULE FILE TITLE:          LVS Rule File for FreePDK45
CREATION TIME:            Sun Nov 10 23:59:37 2019
CURRENT DIRECTORY:        /nethome/madnaan3/VLSI
USER NAME:                madnaan3
CALIBRE VERSION:          v2018.4_25.17    Thu Nov 1 16:52:36 PDT 2018



                               OVERALL COMPARISON RESULTS



                         #       ###################       _   _
                        #        #                 #       *   *
                   #   #         #     CORRECT     #         |
                    # #          #                 #       \___/
                     #           ###################



********************************************************************************
******************************
                                      CELL  SUMMARY
********************************************************************************
******************************

  Result         Layout                         Source
  -----------    -----------                    --------------
  CORRECT        CLA6_AD                        CLA6_AD



********************************************************************************
******************************
                                      LVS PARAMETERS
********************************************************************************
******************************


o LVS Setup:

   LVS COMPONENT TYPE PROPERTY            element
   LVS COMPONENT SUBTYPE PROPERTY         model
   // LVS PIN NAME PROPERTY
   LVS POWER NAME                         "VDD"
   LVS GROUND NAME                        "VSS" "GROUND"
   LVS CELL SUPPLY                        NO
   LVS RECOGNIZE GATES                    ALL
   LVS IGNORE PORTS                       NO
   LVS CHECK PORT NAMES                   NO
   LVS IGNORE TRIVIAL NAMED PORTS         NO
   LVS BUILTIN DEVICE PIN SWAP            YES
   LVS ALL CAPACITOR PINS SWAPPABLE       NO
   LVS DISCARD PINS BY DEVICE             NO
   LVS SOFT SUBSTRATE PINS                NO
   LVS INJECT LOGIC                       YES
   LVS EXPAND UNBALANCED CELLS            YES
   LVS FLATTEN INSIDE CELL                NO
   LVS EXPAND SEED PROMOTIONS             NO
   LVS PRESERVE PARAMETERIZED CELLS       NO
   LVS GLOBALS ARE PORTS                  YES
   LVS REVERSE WL                         NO
   LVS SPICE PREFER PINS                  NO
   LVS SPICE SLASH IS SPACE               YES
   LVS SPICE ALLOW FLOATING PINS          YES
   // LVS SPICE ALLOW INLINE PARAMETERS
   LVS SPICE ALLOW UNQUOTED STRINGS       NO
   LVS SPICE CONDITIONAL LDD              NO
   LVS SPICE CULL PRIMITIVE SUBCIRCUITS   NO
   // LVS SPICE EXCLUDE CELL SOURCE
   // LVS SPICE EXCLUDE CELL LAYOUT
   LVS SPICE IMPLIED MOS AREA             NO
   // LVS SPICE MULTIPLIER NAME
   LVS SPICE OVERRIDE GLOBALS             NO
   LVS SPICE REDEFINE PARAM               NO
   LVS SPICE REPLICATE DEVICES            NO
   LVS SPICE SCALE X PARAMETERS           NO
   LVS SPICE STRICT WL                    NO
   // LVS SPICE OPTION
   LVS STRICT SUBTYPES                    NO
   LVS EXACT SUBTYPES                     NO
   LAYOUT CASE                            NO
   SOURCE CASE                            NO
   LVS COMPARE CASE                       NO
   LVS DOWNCASE DEVICE                    NO
   LVS REPORT MAXIMUM                     50
   LVS PROPERTY RESOLUTION MAXIMUM        32
   // LVS SIGNATURE MAXIMUM
   // LVS FILTER UNUSED OPTION
   LVS REPORT OPTION                      N
   LVS REPORT UNITS                       YES
   // LVS NON USER NAME PORT
   // LVS NON USER NAME NET
   // LVS NON USER NAME INSTANCE
   // LVS IGNORE DEVICE PIN
   // LVS PREFER NETS FILTER SOURCE
   // LVS PREFER NETS FILTER LAYOUT

   // Reduction

   LVS REDUCE SERIES MOS                  YES
   LVS REDUCE PARALLEL MOS                YES
   LVS REDUCE SEMI SERIES MOS             YES
   LVS REDUCE SPLIT GATES                 YES
   LVS REDUCE PARALLEL BIPOLAR            YES
   LVS REDUCE SERIES CAPACITORS           YES
   LVS REDUCE PARALLEL CAPACITORS         YES
   LVS REDUCE SERIES RESISTORS            YES
   LVS REDUCE PARALLEL RESISTORS          YES
   LVS REDUCE PARALLEL DIODES             YES
```

```
   LVS REDUCTION PRIORITY                 PARALLEL

   LVS SHORT EQUIVALENT NODES             NO

   // Trace Property

   TRACE PROPERTY  mn(nmos_vtl)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vtl)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtl)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtl)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vth)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vth)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vth)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vth)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vtg)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vtg)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtg)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtg)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_thkox)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_thkox)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_thkox)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_thkox)  w w 4e-09 ABSOLUTE


                   CELL COMPARISON RESULTS ( TOP LEVEL )


                         #       ###################       _   _
                        #        #                 #       *   *
                   #   #         #     CORRECT     #         |
                    # #          #                 #       \___/
                     #           ###################


LAYOUT CELL NAME:         CLA6_AD
SOURCE CELL NAME:         CLA6_AD

--------------------------------------------------------------------------------
------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:             22        22

 Nets:             275       275

 Instances:        260       260         MN (4 pins)
                   260       260         MP (4 pins)
                ------    ------
 Total Inst:       520       520


NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:             22        22
 Nets:             173       173

 Instances:         68        68         _invv (4 pins)
                     4         4         _invx2v (4 pins)
                     6         6         _invx4v (4 pins)
                    62        62         _nand2v (5 pins)
                    18        18         _nor2v (5 pins)
                ------    ------
 Total Inst:       158       158


********************************************************************************
******************************
                               INFORMATION AND WARNINGS
********************************************************************************
******************************


                  Matched    Matched    Unmatched    Unmatched    Component
                   Layout     Source       Layout       Source    Type
                  -------    -------    ---------    ---------    ---------
   Ports:              22         22            0            0

   Nets:              173        173            0            0

   Instances:          68         68            0            0    _invv
                        4          4            0            0    _invx2v
                        6          6            0            0    _invx4v
                       62         62            0            0    _nand2v
                       18         18            0            0    _nor2v
                  -------    -------    ---------    ---------
   Total Inst:        158        158            0            0


o Initial Correspondence Points:

   Ports:        VDD Y5 X0 X5 Y3 X4 X1 X2 Y2 Y0 X3 C0 Y1 Y4 GND S1 S5 S2 C6 S4
S3 S0


********************************************************************************
******************************
                                         SUMMARY
********************************************************************************
******************************

Total CPU Time:      0 sec
Total Elapsed Time:  0 sec
```

```
================================================================================
==
=== CALIBRE::DRC-H SUMMARY REPORT
===
Execution Date/Time:       Mon Nov 11 00:04:40 2019
Calibre Version:           v2018.4_25.17    Thu Nov 1 16:52:36 PDT 2018
Rule File Pathname:        /nethome/madnaan3/VLSI/_calibreDRC.rul_
Rule File Title:
Layout System:             GDS
Layout Path(s):            CLA6_SLEEP_AD.calibre.db
Layout Primary Cell:       CLA6_SLEEP_AD
Current Directory:         /nethome/madnaan3/VLSI
User Name:                 madnaan3
Maximum Results/RuleCheck: 1000
Maximum Result Vertices:   4096
DRC Results Database:      CLA6_SLEEP_AD.drc.results (ASCII)
Layout Depth:              ALL
Text Depth:                PRIMARY
Summary Report File:       CLA6_SLEEP_AD.drc.summary (REPLACE)
Geometry Flagging:         ACUTE = NO  SKEW = NO  ANGLED = NO  OFFGRID = NO
                           NONSIMPLE POLYGON = NO  NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping:         COMMENT TEXT + RULE FILE INFORMATION
Layers:                    MEMORY-BASED
Keep Empty Checks:         YES
--------------------------------------------------------------------------------
--
--- RUNTIME WARNINGS
---
--------------------------------------------------------------------------------
--
--- ORIGINAL LAYER STATISTICS
---
LAYER pwell ...... TOTAL Original Geometry Count = 6   (478)
LAYER nwell ...... TOTAL Original Geometry Count = 5   (360)
LAYER active ..... TOTAL Original Geometry Count = 14  (1843)
LAYER poly ....... TOTAL Original Geometry Count = 24  (1240)
LAYER pimplant ... TOTAL Original Geometry Count = 6   (1127)
LAYER nimplant ... TOTAL Original Geometry Count = 8   (716)
LAYER vth ........ TOTAL Original Geometry Count = 0   (0)
LAYER vtg ........ TOTAL Original Geometry Count = 9   (361)
LAYER metal1 ..... TOTAL Original Geometry Count = 281 (6177)
LAYER contact .... TOTAL Original Geometry Count = 11  (1960)
LAYER metal2 ..... TOTAL Original Geometry Count = 56  (569)
LAYER metal3 ..... TOTAL Original Geometry Count = 28  (259)
LAYER metal4 ..... TOTAL Original Geometry Count = 25  (141)
LAYER metal5 ..... TOTAL Original Geometry Count = 0   (0)
LAYER metal6 ..... TOTAL Original Geometry Count = 0   (0)
LAYER metal7 ..... TOTAL Original Geometry Count = 0   (0)
LAYER metal8 ..... TOTAL Original Geometry Count = 0   (0)
LAYER metal9 ..... TOTAL Original Geometry Count = 0   (0)
LAYER metal10 .... TOTAL Original Geometry Count = 0   (0)
LAYER via1 ....... TOTAL Original Geometry Count = 2   (295)
LAYER via2 ....... TOTAL Original Geometry Count = 2   (114)
LAYER via3 ....... TOTAL Original Geometry Count = 2   (98)
LAYER via4 ....... TOTAL Original Geometry Count = 0   (0)
LAYER via5 ....... TOTAL Original Geometry Count = 0   (0)
LAYER via6 ....... TOTAL Original Geometry Count = 0   (0)
LAYER via7 ....... TOTAL Original Geometry Count = 0   (0)
LAYER via8 ....... TOTAL Original Geometry Count = 0   (0)
LAYER via9 ....... TOTAL Original Geometry Count = 0   (0)
--------------------------------------------------------------------------------
```

```
--
--- RULECHECK RESULTS STATISTICS
---
RULECHECK Well.1 ............ TOTAL Result Count = 0 (0)
RULECHECK Well.2 ............ TOTAL Result Count = 0 (0)
RULECHECK Well.4 ............ TOTAL Result Count = 0 (0)
RULECHECK Poly.1 ............ TOTAL Result Count = 0 (0)
RULECHECK Poly.2 ............ TOTAL Result Count = 0 (0)
RULECHECK Poly.3 ............ TOTAL Result Count = 0 (0)
RULECHECK Poly.4 ............ TOTAL Result Count = 0 (0)
RULECHECK Poly.5 ............ TOTAL Result Count = 0 (0)
RULECHECK Poly.6 ............ TOTAL Result Count = 0 (0)
RULECHECK Active.1 .......... TOTAL Result Count = 0 (0)
RULECHECK Active.2 .......... TOTAL Result Count = 0 (0)
RULECHECK Active.3 .......... TOTAL Result Count = 0 (0)
RULECHECK Active.4 .......... TOTAL Result Count = 0 (0)
RULECHECK Implant.1 ......... TOTAL Result Count = 0 (0)
RULECHECK Implant.2 ......... TOTAL Result Count = 0 (0)
RULECHECK Implant.3 ......... TOTAL Result Count = 0 (0)
RULECHECK Implant.4 ......... TOTAL Result Count = 0 (0)
RULECHECK Implant.6 ......... TOTAL Result Count = 0 (0)
RULECHECK Contact.1 ......... TOTAL Result Count = 0 (0)
RULECHECK Contact.2 ......... TOTAL Result Count = 0 (0)
RULECHECK Contact.3 ......... TOTAL Result Count = 0 (0)
RULECHECK Contact.4 ......... TOTAL Result Count = 0 (0)
RULECHECK Contact.5 ......... TOTAL Result Count = 0 (0)
RULECHECK Contact.6 ......... TOTAL Result Count = 0 (0)
RULECHECK Metal1.1 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal1.2 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal1.3 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal1.4 .......... TOTAL Result Count = 0 (0)
RULECHECK Via1.1 ............ TOTAL Result Count = 0 (0)
RULECHECK Via1.2 ............ TOTAL Result Count = 0 (0)
RULECHECK Via1.3 ............ TOTAL Result Count = 0 (0)
RULECHECK Via1.4 ............ TOTAL Result Count = 0 (0)
RULECHECK Metal2.1 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal2.2 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal2.3 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal2.4 .......... TOTAL Result Count = 0 (0)
RULECHECK Via2.1 ............ TOTAL Result Count = 0 (0)
RULECHECK Via2.2 ............ TOTAL Result Count = 0 (0)
RULECHECK Via2.3 ............ TOTAL Result Count = 0 (0)
RULECHECK Via2.4 ............ TOTAL Result Count = 0 (0)
RULECHECK Metal3.1 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal3.2 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal3.3 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal3.4 .......... TOTAL Result Count = 0 (0)
RULECHECK Via3.1 ............ TOTAL Result Count = 0 (0)
RULECHECK Via3.2 ............ TOTAL Result Count = 0 (0)
RULECHECK Via3.3 ............ TOTAL Result Count = 0 (0)
RULECHECK Via3.4 ............ TOTAL Result Count = 0 (0)
RULECHECK Metal4.1 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal4.2 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal4.3 .......... TOTAL Result Count = 0 (0)
RULECHECK Via4.1 ............ TOTAL Result Count = 0 (0)
RULECHECK Via4.2 ............ TOTAL Result Count = 0 (0)
RULECHECK Via4.3 ............ TOTAL Result Count = 0 (0)
RULECHECK Via4.4 ............ TOTAL Result Count = 0 (0)
RULECHECK Metal5.1 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal5.2 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal5.3 .......... TOTAL Result Count = 0 (0)
RULECHECK Via5.1 ............ TOTAL Result Count = 0 (0)
RULECHECK Via5.2 ............ TOTAL Result Count = 0 (0)
RULECHECK Via5.3 ............ TOTAL Result Count = 0 (0)
RULECHECK Via5.4 ............ TOTAL Result Count = 0 (0)
RULECHECK Metal6.1 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal6.2 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal6.3 .......... TOTAL Result Count = 0 (0)
RULECHECK Via6.1 ............ TOTAL Result Count = 0 (0)
RULECHECK Via6.2 ............ TOTAL Result Count = 0 (0)
RULECHECK Via6.3 ............ TOTAL Result Count = 0 (0)
RULECHECK Via6.4 ............ TOTAL Result Count = 0 (0)
RULECHECK Metal7.1 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal7.2 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal7.3 .......... TOTAL Result Count = 0 (0)
RULECHECK Via7.1 ............ TOTAL Result Count = 0 (0)
RULECHECK Via7.2 ............ TOTAL Result Count = 0 (0)
RULECHECK Via7.3 ............ TOTAL Result Count = 0 (0)
RULECHECK Via7.4 ............ TOTAL Result Count = 0 (0)
RULECHECK Metal8.1 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal8.2 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal8.3 .......... TOTAL Result Count = 0 (0)
RULECHECK Via8.1 ............ TOTAL Result Count = 0 (0)
RULECHECK Via8.2 ............ TOTAL Result Count = 0 (0)
RULECHECK Via8.3 ............ TOTAL Result Count = 0 (0)
RULECHECK Via8.4 ............ TOTAL Result Count = 0 (0)
RULECHECK Metal9.1 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal9.2 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal9.3 .......... TOTAL Result Count = 0 (0)
RULECHECK Via9.1 ............ TOTAL Result Count = 0 (0)
RULECHECK Via9.2 ............ TOTAL Result Count = 0 (0)
RULECHECK Via9.3 ............ TOTAL Result Count = 0 (0)
RULECHECK Via9.4 ............ TOTAL Result Count = 0 (0)
RULECHECK Metal10.1 ......... TOTAL Result Count = 0 (0)
RULECHECK Metal10.2 ......... TOTAL Result Count = 0 (0)
RULECHECK Metal10.3 ......... TOTAL Result Count = 0 (0)
RULECHECK Metal1.5 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal1.6 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal1.7 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal1.8 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal1.9 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal2.5 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal2.6 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal2.7 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal2.8 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal2.9 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal3.5 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal3.6 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal3.7 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal3.8 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal3.9 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal4.5 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal4.6 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal4.7 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal4.8 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal5.5 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal5.6 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal5.7 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal5.8 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal6.5 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal6.6 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal6.7 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal6.8 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal7.5 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal7.6 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal7.7 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal8.5 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal8.6 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal8.7 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal9.5 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal9.6 .......... TOTAL Result Count = 0 (0)
RULECHECK Metal10.5 ......... TOTAL Result Count = 0 (0)
RULECHECK Metal10.6 ......... TOTAL Result Count = 0 (0)
RULECHECK Grid.1 ............ TOTAL Result Count = 0 (0)
RULECHECK Grid.2 ............ TOTAL Result Count = 0 (0)
RULECHECK Grid.3 ............ TOTAL Result Count = 0 (0)
RULECHECK Grid.4 ............ TOTAL Result Count = 0 (0)
RULECHECK Grid.5 ............ TOTAL Result Count = 0 (0)
RULECHECK Grid.6 ............ TOTAL Result Count = 0 (0)
RULECHECK Grid.7 ............ TOTAL Result Count = 0 (0)
RULECHECK Grid.8 ............ TOTAL Result Count = 0 (0)
RULECHECK Grid.9 ............ TOTAL Result Count = 0 (0)
RULECHECK Grid.10 ........... TOTAL Result Count = 0 (0)
RULECHECK Grid.11 ........... TOTAL Result Count = 0 (0)
RULECHECK Grid.12 ........... TOTAL Result Count = 0 (0)
RULECHECK Grid.13 ........... TOTAL Result Count = 0 (0)
RULECHECK Grid.14 ........... TOTAL Result Count = 0 (0)
RULECHECK Grid.15 ........... TOTAL Result Count = 0 (0)
RULECHECK Grid.16 ........... TOTAL Result Count = 0 (0)
RULECHECK Grid.17 ........... TOTAL Result Count = 0 (0)
RULECHECK Grid.18 ........... TOTAL Result Count = 0 (0)
RULECHECK Grid.19 ........... TOTAL Result Count = 0 (0)
RULECHECK Grid.20 ........... TOTAL Result Count = 0 (0)
RULECHECK Grid.21 ........... TOTAL Result Count = 0 (0)
RULECHECK Grid.22 ........... TOTAL Result Count = 0 (0)
RULECHECK Grid.23 ........... TOTAL Result Count = 0 (0)
RULECHECK Grid.24 ........... TOTAL Result Count = 0 (0)
RULECHECK Grid.25 ........... TOTAL Result Count = 0 (0)
RULECHECK Grid.26 ........... TOTAL Result Count = 0 (0)
RULECHECK Antenna.poly ...... TOTAL Result Count = 0 (0)
RULECHECK Antenna.metal1 .... TOTAL Result Count = 0 (0)
RULECHECK Antenna.metal2 .... TOTAL Result Count = 0 (0)
RULECHECK Antenna.metal3 .... TOTAL Result Count = 0 (0)
RULECHECK Antenna.metal4 .... TOTAL Result Count = 0 (0)
RULECHECK Antenna.metal5 .... TOTAL Result Count = 0 (0)
RULECHECK Antenna.metal6 .... TOTAL Result Count = 0 (0)
RULECHECK Antenna.metal7 .... TOTAL Result Count = 0 (0)
RULECHECK Antenna.metal8 .... TOTAL Result Count = 0 (0)
RULECHECK Antenna.metal9 .... TOTAL Result Count = 0 (0)
RULECHECK Antenna.metal10 ... TOTAL Result Count = 0 (0)
--------------------------------------------------------------------------------
--
--- RULECHECK RESULTS STATISTICS (BY CELL)
---
--------------------------------------------------------------------------------
--
--- SUMMARY
---
TOTAL CPU Time:                  0
TOTAL REAL Time:                 0
TOTAL Original Layer Geometries: 479 (15738)
TOTAL DRC RuleChecks Executed:   167
TOTAL DRC Results Generated:     0 (0)
```

```
                  ##################################################
                  ##                                              ##
                  ##         C A L I B R E    S Y S T E M         ##
                  ##                                              ##
                  ##             L V S   R E P O R T              ##
                  ##                                              ##
                  ##################################################


REPORT FILE NAME:         CLA6_SLEEP_AD.lvs.report
LAYOUT NAME:              /nethome/madnaan3/VLSI/CLA6_SLEEP_AD.sp
('CLA6_SLEEP_AD')
SOURCE NAME:              /nethome/madnaan3/VLSI/CLA6_SLEEP_AD.src.net
('CLA6_SLEEP_AD')
RULE FILE:                /nethome/madnaan3/VLSI/_calibreLVS.rul_
RULE FILE TITLE:          LVS Rule File for FreePDK45
CREATION TIME:            Mon Nov 11 00:07:43 2019
CURRENT DIRECTORY:        /nethome/madnaan3/VLSI
USER NAME:                madnaan3
CALIBRE VERSION:          v2018.4_25.17    Thu Nov 1 16:52:36 PDT 2018


                               OVERALL COMPARISON RESULTS



                         #       ###################       _   _
                        #        #                 #       *   *
                   #   #         #     CORRECT     #         |
                    # #          #                 #       \___/
                     #           ###################



********************************************************************************
******************************
                                      CELL  SUMMARY
********************************************************************************
******************************

  Result         Layout                        Source
  -----------    -----------                   --------------
  CORRECT        CLA6_SLEEP_AD                 CLA6_SLEEP_AD



********************************************************************************
******************************
                                      LVS PARAMETERS
********************************************************************************
******************************


o LVS Setup:

   LVS COMPONENT TYPE PROPERTY               element
   LVS COMPONENT SUBTYPE PROPERTY            model
   // LVS PIN NAME PROPERTY
```

```
LVS POWER NAME                         "VDD"
LVS GROUND NAME                        "VSS" "GROUND"
LVS CELL SUPPLY                        NO
LVS RECOGNIZE GATES                    ALL
LVS IGNORE PORTS                       NO
LVS CHECK PORT NAMES                   NO
LVS IGNORE TRIVIAL NAMED PORTS         NO
LVS BUILTIN DEVICE PIN SWAP            YES
LVS ALL CAPACITOR PINS SWAPPABLE       NO
LVS DISCARD PINS BY DEVICE             NO
LVS SOFT SUBSTRATE PINS                NO
LVS INJECT LOGIC                       YES
LVS EXPAND UNBALANCED CELLS            YES
LVS FLATTEN INSIDE CELL                NO
LVS EXPAND SEED PROMOTIONS             NO
LVS PRESERVE PARAMETERIZED CELLS       NO
LVS GLOBALS ARE PORTS                  YES
LVS REVERSE WL                         NO
LVS SPICE PREFER PINS                  NO
LVS SPICE SLASH IS SPACE               YES
LVS SPICE ALLOW FLOATING PINS          YES
// LVS SPICE ALLOW INLINE PARAMETERS
LVS SPICE ALLOW UNQUOTED STRINGS       NO
LVS SPICE CONDITIONAL LDD              NO
LVS SPICE CULL PRIMITIVE SUBCIRCUITS   NO
// LVS SPICE EXCLUDE CELL SOURCE
// LVS SPICE EXCLUDE CELL LAYOUT
LVS SPICE IMPLIED MOS AREA             NO
// LVS SPICE MULTIPLIER NAME
LVS SPICE OVERRIDE GLOBALS             NO
LVS SPICE REDEFINE PARAM               NO
LVS SPICE REPLICATE DEVICES            NO
LVS SPICE SCALE X PARAMETERS           NO
LVS SPICE STRICT WL                    NO
// LVS SPICE OPTION
LVS STRICT SUBTYPES                    NO
LVS EXACT SUBTYPES                     NO
LAYOUT CASE                            NO
SOURCE CASE                            NO
LVS COMPARE CASE                       NO
LVS DOWNCASE DEVICE                    NO
LVS REPORT MAXIMUM                     50
LVS PROPERTY RESOLUTION MAXIMUM        32
// LVS SIGNATURE MAXIMUM
// LVS FILTER UNUSED OPTION
LVS REPORT OPTION                      N
LVS REPORT UNITS                       YES
// LVS NON USER NAME PORT
// LVS NON USER NAME NET
// LVS NON USER NAME INSTANCE
// LVS IGNORE DEVICE PIN
// LVS PREFER NETS FILTER SOURCE
// LVS PREFER NETS FILTER LAYOUT

// Reduction

LVS REDUCE SERIES MOS                  YES
LVS REDUCE PARALLEL MOS                YES
LVS REDUCE SEMI SERIES MOS             YES
LVS REDUCE SPLIT GATES                 YES
LVS REDUCE PARALLEL BIPOLAR            YES
LVS REDUCE SERIES CAPACITORS           YES
LVS REDUCE PARALLEL CAPACITORS         YES
LVS REDUCE SERIES RESISTORS            YES
```

```
   LVS REDUCE PARALLEL RESISTORS          YES
   LVS REDUCE PARALLEL DIODES             YES
   LVS REDUCTION PRIORITY                 PARALLEL

   LVS SHORT EQUIVALENT NODES             NO

   // Trace Property

   TRACE PROPERTY  mn(nmos_vtl)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vtl)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtl)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtl)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vth)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vth)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vth)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vth)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vtg)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vtg)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtg)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtg)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_thkox)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_thkox)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_thkox)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_thkox)  w w 4e-09 ABSOLUTE


                   CELL COMPARISON RESULTS ( TOP LEVEL )


                         #       ###################        _   _
                        #        #                 #        *   *
                   #   #         #     CORRECT     #          |
                    # #          #                 #        \___/
                     #           ###################


LAYOUT CELL NAME:         CLA6_SLEEP_AD
SOURCE CELL NAME:         CLA6_SLEEP_AD

--------------------------------------------------------------------------------
------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:             23        23

 Nets:             278       278

 Instances:        262       262         MN (4 pins)
                   260       260         MP (4 pins)
                ------    ------
 Total Inst:       522       522


NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:             23        23

 Nets:             176       176

 Instances:          2         2         MN (4 pins)
                    68        68         _invv (4 pins)
                     4         4         _invx2v (4 pins)
                     6         6         _invx4v (4 pins)
                    62        62         _nand2v (5 pins)
                    18        18         _nor2v (5 pins)
                ------    ------
 Total Inst:       160       160


********************************************************************************
******************************
                               INFORMATION AND WARNINGS
********************************************************************************
******************************


                  Matched    Matched    Unmatched    Unmatched    Component
                   Layout     Source       Layout       Source    Type
                  -------    -------    ---------    ---------    ---------
   Ports:              23         23            0            0

   Nets:              176        176            0            0

   Instances:           2          2            0            0    MN(NMOS_VTG)
                       68         68            0            0    _invv
                        4          4            0            0    _invx2v
                        6          6            0            0    _invx4v
                       62         62            0            0    _nand2v
                       18         18            0            0    _nor2v
                  -------    -------    ---------    ---------
   Total Inst:        160        160            0            0


o Initial Correspondence Points:

   Ports:        VDD Y5 X0 X5 Y3 X4 X1 X2 Y2 Y0 X3 C0 Y1 Y4 SLEEP GND S1 S5 S2
C6 S4 S3 S0


********************************************************************************
******************************
                                         SUMMARY
********************************************************************************
******************************

Total CPU Time:      0 sec
Total Elapsed Time:  0 sec
```