

Assignment - 2

Q.1) Flag register of 80386

Flag	Bit No.	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F	Reserved	V	R	O	N	T	O	P	D	O	D	I	T	S	Z	O	A	O	P	I
L	for INTEL	M	F	T		E	F	F	F	F	F	F	F	F	F	F	F	F	F	
A																				
GS																				

FLAG REGISTER OF 80386

Flags:-

- ① C (Carry) :- It holds the carry after calculations
- ② P (Parity) :- Parity is a logic 0 for odd parity and a logic 1 for even parity. Parity is a count of ones in a number expressed as even or odd.
- ③ A (Auxiliary Carry) :- Carry occurs bits positions 3 and 5 of the results.
- ④ Z (Zero) :- The zero flag shows that the result of an arithmetic or logical operation is zero. When $Z=1$, the result is zero, when $Z=0$, the result was non-zero.
- ⑤ T (Trap) :- Enables trapping through an on-chip debugging facility.

⑥ S(sign):- The sign flag holds the arithmetic sign after an arithmetic or a logical operation. If $S=1$ the sign bit is set and the result is negative. If $S=0$, the sign bit is not set & the result is positive.

⑦ I(Interrupt):- The interrupt flag controls the operations of the INTR (Interrupt request) input pin. If $I=1$, the INTR pin is enabled; if $I=0$, the INTR pin is disabled.

⑧ VM(Virtual mode):- If this flag set, the 80386 enters the virtual mode within the protected mode. In this mode, if any privileged instruction is executed, an exception 13 is generated.

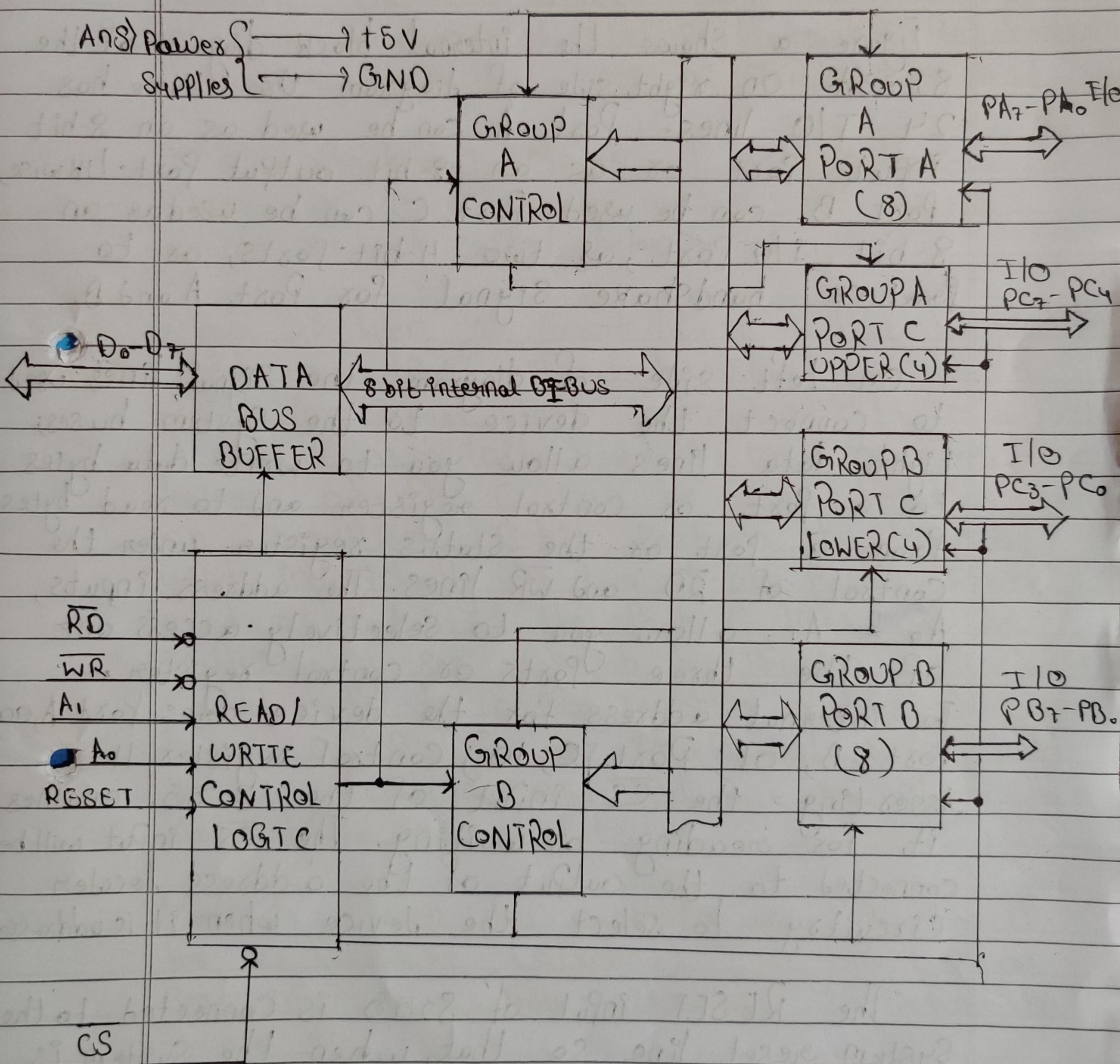
⑨ RF(Resume):- Used by the debug registers DR6 and DR7. It enables you to ~~turn off~~ turn off certain exceptions while debugging code.

⑩ NT(Nested task):- The nested task flag is used to indicated that the current task is nested within another task in protected mode operation. This flag can be manipulated for multitasking.

⑪ TOPL(I/O privilege level):- TOPL is used in in protected mode operation to select the privilege level for I/O devices. If the current privilege level is higher or more trusted than the TOPL, I/O executed without hindrance. If the TOPL is lower than the current privilege level, an interrupt occurs.

Q.2) 8255 block diagram.

Ans) Power Supplies → +5V → GND



8255 Block diagram

Figure a.

? Internal Block diagram and System Connections of 8255-

Figure a Shows the internal block diagram of the 8255A. On right side of diagram the device has 24 I/O lines. Port A can be used as an 8-bit input port or as an 8-bit output port. Likewise, Port B can be used. Port C can be used as an 8-bit I/O port, as two 4-bit ports, or to produce handshake signal for Port A and B.

On left side of diagram, the signal lines used to connect the device to the system buses. Eight data lines allow you to write data bytes to a port or control register and to read bytes from a port or the status register under the control of RD and WR lines. The address inputs, A₀ & A₁, allow you to selectively access one of the three ports or control register.

The internal address for the device are: Port A, 00; Port B, 01; Port C, 10; Control registers 11. Asserting the CS input of the 8255 enables it for reading or writing. The CS input will be connected to the output of the address decoder circuitry to select the device when it is addressed.

The RESET input of 8255 is connected to the system reset line so that, when the system is reset, all the port lines are initialized as outputs after a power-up or reset input lines. If port lines were initialized as outputs after a power-up or reset, the port might try to output to the output

of a device connected to the port. The possible argument between the two outputs might destroy one or both of them. Therefore, all the programmable port devices initialize their port lines as inputs when reset.

8255 Operational Modes and Initialization:-

There are 3 different modes of 8255 which are described below:-

Mode 0:- When you want to use a port for simple input or output without handshaking, you initialize that port in mode 0. If both port A and B are initialized in mode 0, then two halves of Port C can be used together as an additional 8-bit port, or they can be used individually as two 4-bit ports. When used as outputs, the Port C lines can be individually set or reset by sending a special control word to Control register address. The two halves of Port C are independent, so one half can be initialized as input, & the other half initialized as output.

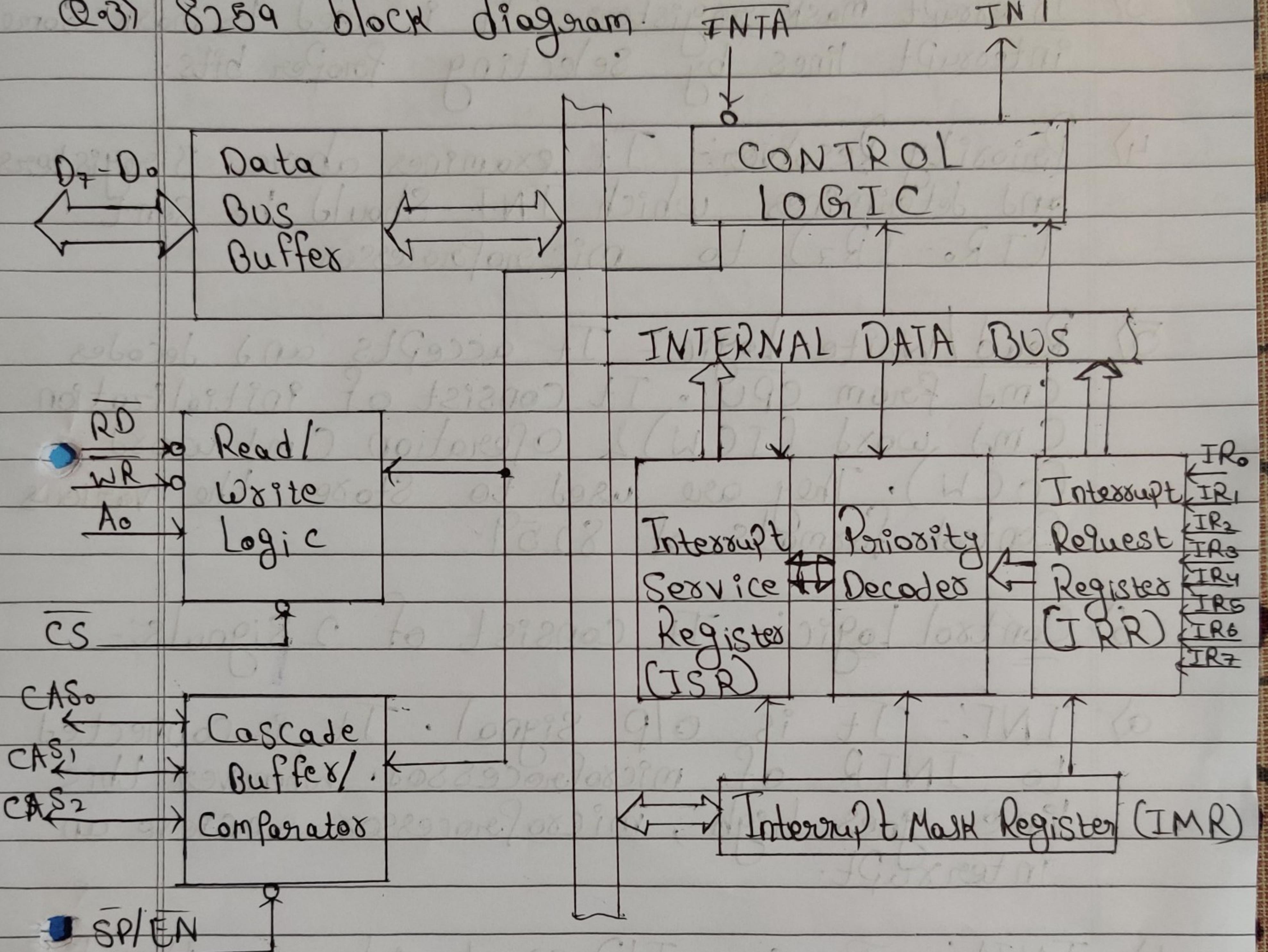
Mode 1:- When you want to use Port A or B for a handshake (strobed) I/O operation as seen in Mode 0, you initialize that port in mode 1.

In this mode, some of the pins of Port C function as handshake lines. Pins PC₀, PC₁, & PC₂ function as handshake lines for Port B if it is initialized in mode 1. If Port A is initialized as

a handshake (mode 1) input port, then pins PC₃, PC₄ and PC₅ function as handshake signals. Pins PC₆ and PC₇ are available for use as input lines or output lines. If Port A is initialized as a handshake signals. Port C output port, then Port C pins PC₃, PC₆, and PC₇ function as handshake signals. Port C pins PC₄ and PC₅ are available for use as input or output lines.

MODE 2: Only Port A can be initialized in mode 2. In mode 2, Port A can be used for bidirectional handshake data transfer. This means that data can be output or input on the same eight lines. The 8255 might be used in this mode to extend the system bus to a slave microprocessor or to transfer data bytes to and from a floppy disk controller board. If Port A is initialized in mode 2, then pins PC₃ through PC₇ are used as handshake lines for Port A. The other three pins, PC₀ through PC₂, can be used for I/O if Port B is in mode 0. The three pins will be used for Port B handshake lines if Port B is initialized in mode 1.

Q.3) 8259 block diagram.



1) Interrupt Request Register: - It has 8 input lines IR₇-IR₀. Peripheral devices are connected to these lines. When these lines goes high the requests are stored in this register.

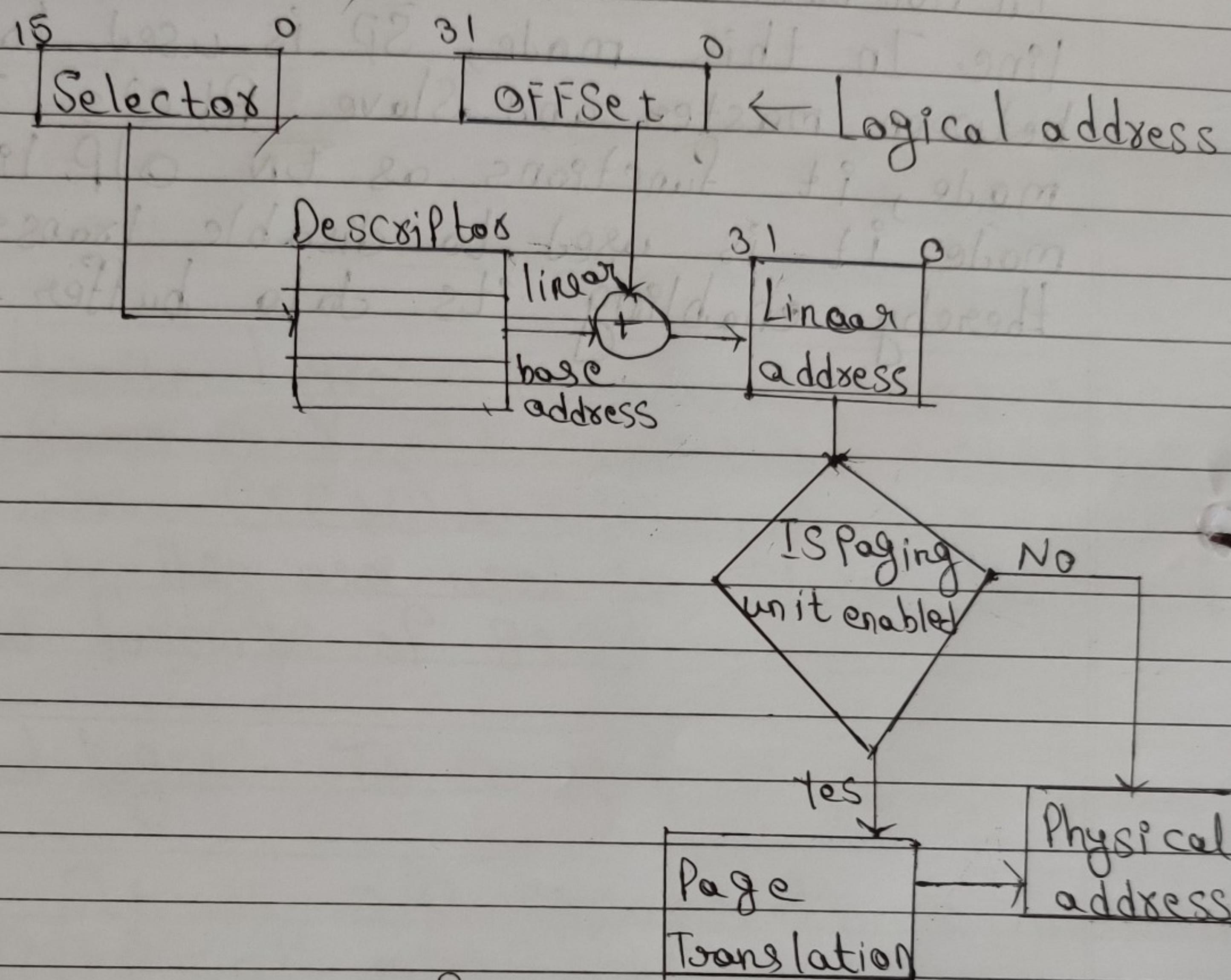
2) Interrupt Service Register: - It is used to store all the lines which are being serviced.

- 3) Interrupt mask register: - It is used to mask some interrupt lines by selecting proper bits.
- 4) Priority Resolver: - It examines above 3 registers and determines which INT should be sent (IR₀-IR₇) to microprocessor.
- 5) Read/Write Logic: - It accepts and decodes cmd from CPU. It consists of initialization Cmd word (TCW) & Operation Cmd word (OCW). They are used to store the various control formats of 8259.
- 6) Control Logic: - It consists of 2 signals:
 - a) INT: - It is o/p signal. It is connected to INTR of microprocessor. Whenever this line goes high, microprocessor receives an interrupt.
 - b) INTA: - It is I/P signal. Whenever this line goes active low microprocessor acknowledges the arrival of interrupt request to 8259.
- 7) Data bus buffer: - It is 8-bit bidirectional buffer. It is used to interface the 8259 to system bus.
- 8) Cascade buffer/Comparator: - It is used in cascade mode. It is used to increase no. of interrupt levels by cascading many 8259. It uses cascade lines CAS₂, CAS₁, CAS₀ & SP/EN.

q) SP1EN: It is active low bidirectional control line. In non-buffered mode it functions as SP input line. In this mode, SP is used to distinguish between master and Slave PIC's. In buffered mode, it functions as EN O/P line. In this mode it is used to disable transceiver & thereby enabling its data buffer.

4) Address translation of 80386.

Ans)

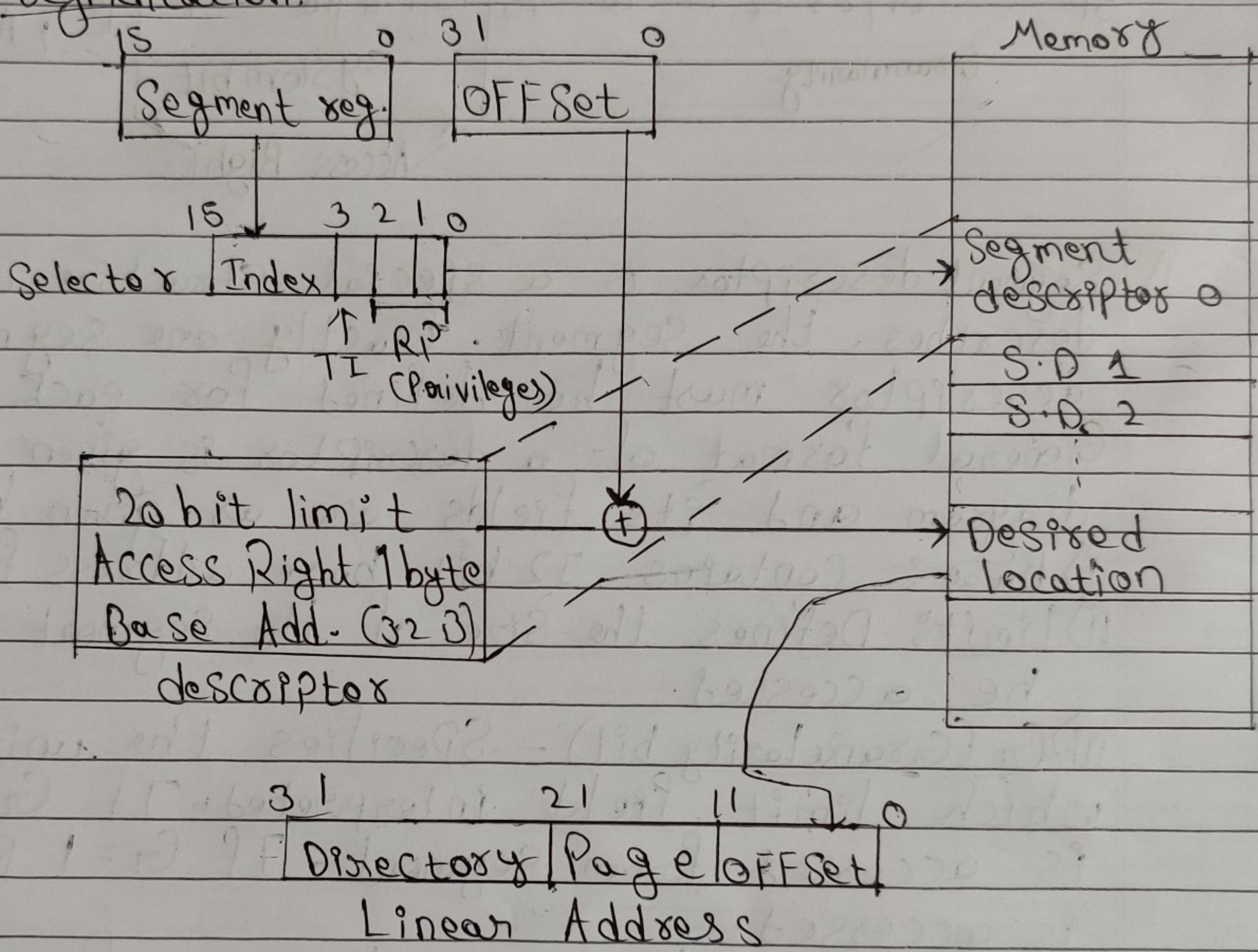


Overview of address translation

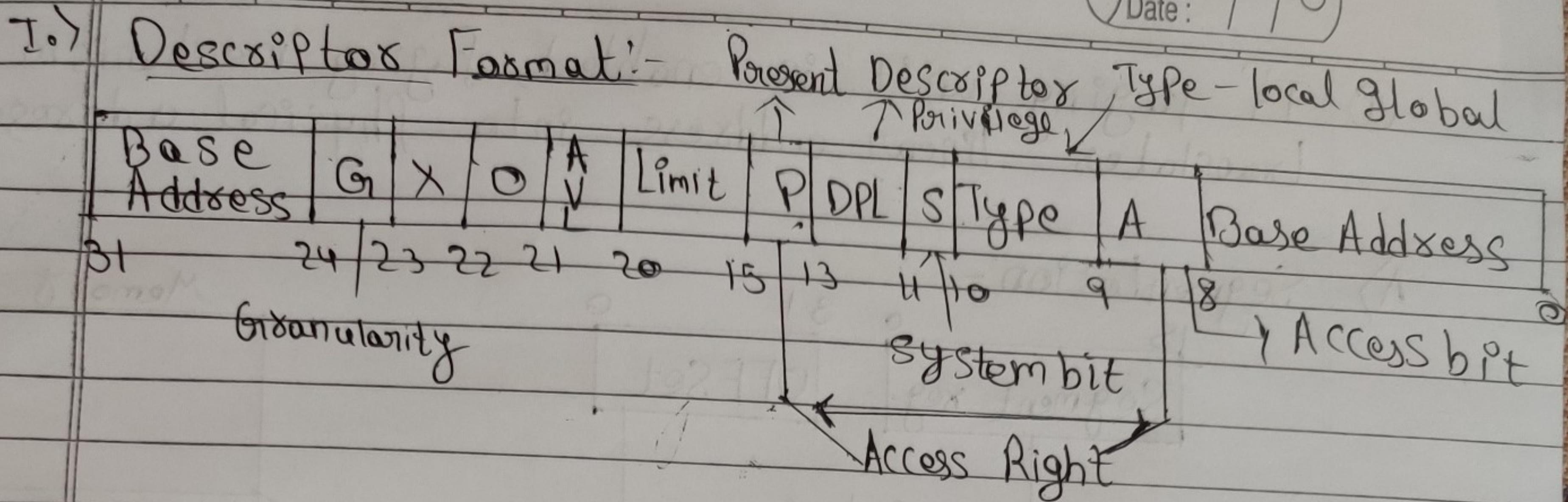
- ① The 80386 has three distinct address:
 - i) Logical
 - ii) Linear
 - iii) Physical
- ② Logical address consists of a selector & offset.
- ③ In real mode, the segmentation unit adds the selector with offset to form linear address while in protected mode, every segment has linear base address which is stored in segment descriptor.
- ④ The linear base address from the descriptor is added to offset address to generate 32-bit linear address. This process is called Segmentation.

- ④ If Paging unit is enabled, Paging mechanism translates linear address into physical address.

A) Segmentation:-



- 1) The Selector component of each logical address contains 2 bit of privilege level of a program.
- 2) The descriptor of each Segment also contains 2 bit of privilege level of that segment.
- 3) If the privilege of each segment also contain
- 3) If the privilege level in Selector is greater than privilege level of descriptor, then MMU allows the program to access the segment.
- 4) If IT=0, then global descriptor table is used, else local descriptor is used.



- I) Segment descriptor is a special structure which describes the segment. Exactly one segment descriptor must be defined for each program.
- General format of a descriptor is given in above diagram and its fields are as given below:
- i) Base: Contains 32-bit base address for a segment.
 - ii) Limit: Defines the size of the segment that can be accessed.
 - iii) G (Granularity bit):- Specifies the unit with which limit field interpreted. If $G=0$, byte is accessed from segment. If $G=1$ page (4 KB) is accessed.
 - iv) AVL:- This bit is completely undefined & 80386 ignores it.
- v) Access Right bytes:-
- a) P:- Present bit. If $P=1$, segment is loaded in physical memory.
 - b) DPL:- Descriptor privilege level - Defines the level of privilege associated with descriptor.
- $DPL = 00$ (most privileged)
 $DPL = 11$ (least privileged)
- c) System bit: S:- If $S=0$, then System Segment is accessed.
 $S=1$, Code/ Data Segment is accessed.

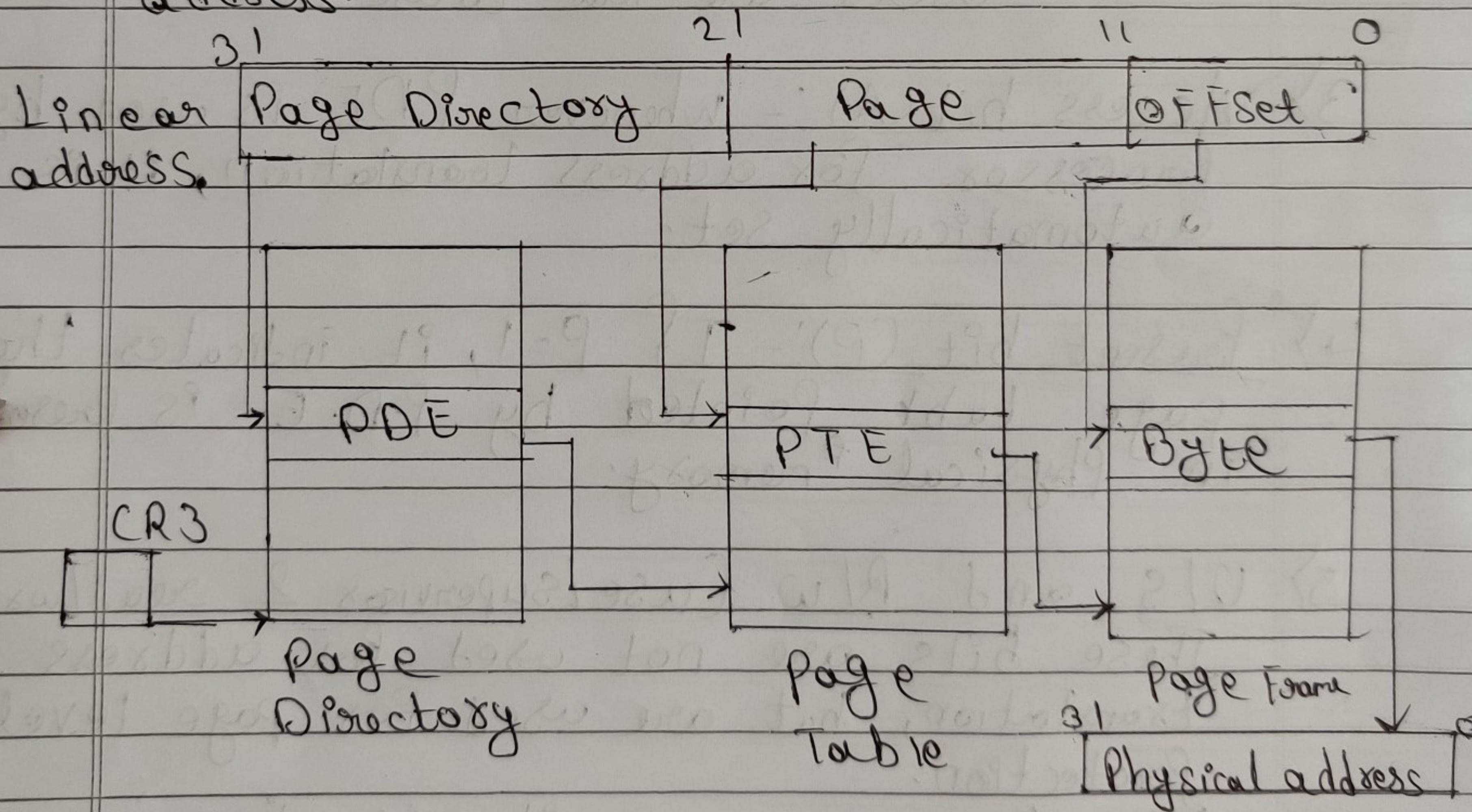
d) Type: It defines the type of descriptor being used.

e) A (Accessbit): It is automatically set to 1 when descriptor is accessed.

b) Paging:-

This is the second phase of address translation. The

In this phase, 80386 transforms linear address generated by segmentation to physical address.



Page Directory Table Format:-

1. PDE Format:

31	2	1	0
Page table base address	User	A	DS User Super read write R/W P

U/S	R/W	Privilege All	Privilege to P1 to L2
0	0	None	R/W
0	1	None	R/W
1	0	Readonly	R/W
1	1	Read only	R/W

1) Page Table Address

Specifies Physical Starting address or base address of page table.

2) User:- Bit 9-11 are not used by 80386
Users are free to use them.

3) Access bit (A) :- whenever PDE is used by processor for address translation, it is automatically set.

4) Present bit (P):- If P=1, it indicates the page table pointed by P.D.E is present in physical memory.

5) U/S and R/W (User/Supervisor & read/write):-
These bits are not used for address translation, but are used for page level protection.

When U/S=0, only privilege levels 0,1,2 are accessible to data.

When U/S=1, then all privilege levels can access the data.

PTE (Page Table Format):-

Page table Frame	User	D	A	U/S	R/W	P
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6) Dirty bit (D):- The dirty bit is ~~set~~ automatically set whenever page frame is written into. From this, user can keep track of most often written pages of memory.