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## APPENDIX 2: REGISTER AND INSTRUCTION SET SUMMARIES

### 1. CONTROL REGISTER SUMMARY

Register	Address	D7	D6	D5	D4	D3	D2	D1	D0	Comment
P1  Port P15- P10	FF00	/	/	P15	P14	P13	P12	P11	P10	R/W Control of transfer data by P14, P15
SB  Serial transfer register	FF01									R/W  Transfer data
SC  Serial control	FF02	Transfer start 0: No start 1: Start	/	/	/	/	/	Clock speed 0: 8 KHz 1: 256 KHz	Shift clock 0: External 1: Internal	R/W In double- speed mode clock speed also doubled
DIV  Divider	FF04	$f2^{18}$  64Hz	$f2^{18}$  128Hz	$f2^{14}$  256Hz	$f2^{13}$  512Hz	$f2^{12}$  1024Hz z	$f2^{11}$  2048Hz z	$f2^{10}$  4096Hz z	$f2^9$  8192Hz z	R/W With clear normal by LD instruction: $f=4194304$ Double speed: $f=8388608$
TIMA  Timer	FF05									R/W Timer unit Operates at double-speed in double- speed mode
TMA  Timer modulo	FF06									R/W Preset register for timer
TAC  Timer control	FF07	/	/	/	/	/	Timer stop 0: Stop 1: Operate	Frequency selection bit 00: $f2^{10}$ 10: $f2^9$ 01: $f2^4$ 11: $f2^3$		R/W Normal-speed: $f=4194304$ Double-speed: $f=8388608$
IF  Interrupt request flag	FF0F	/	/	/	Terminals P10-P13 HIGH	End of serial transfer	Timer overflow	LCDC Controller STAT	V-blank	R/W Bit reset valid
IE  Interrupt enable flag	FFFF				Terminals P10-P13 LOW	End of serial transfer	Timer overflow	LCDC Controller STAT	V-blank	R/W 0: Disabled 1: Enabled
IME  Interrupt master enable		/	/	/	/	/	/	/		Reset with DI; set with EI 0: Disable interrupts 1: Enable interrupts

**Appendix 2: Register and Instruction Set Summaries**


Register	Address	D7	D6	D5	D4	D3	D2	D1	D0	Comment
LCDC LCDC Control	FF40	Controller 0: Stop 1: Operate	WIN Area 0: 9800- 1: 9C00-	Window 0: OFF 1: ON	BG Characters 0: 8800- 1: 8000-	BG Area 0: 9800- 1: 9C00-	OBJ Block 0: 8x8 1: 8x16	OBJ Display 0: OFF 1: ON	BG Display 0: OFF 1: ON	RAM Bit 0 fixed to display BG ON in CGB mode only
STAT LCDC status information	FF41		LCDC status interrupt selection flags				LYC agreement 0: 1: LYC=LY	Mode 00: RAM access 10: OBJ search 01: V-blank 11: LCD transfer		RAM Bits 3-6 Interrupt 0: Not selected 1: Selected
			Agreement flag selection	Mode 10 selection	Mode 01 selection	Mode 00 selection				
SCY Scroll Y register	FF42									RAM 0x00 – 0xFF
SCX Scroll X register	FF43									RAM 0x00 – 0xFF
LY LCDC y- coordinate	FF44									R y-coordinate during display
LYC LY compare register	FF45									RAM Agreement flag set with LYC=LY
DMA DMA Transfer	FF46									W 0x00 – 0xDF Transfer starts at the same time as address set

Register	Address	D7	D6	D5	D4	D3	D2	D1	D0	Comment
BGP BG Palette Data	FF47	Palette data for character dot data 11 in DMG mode.		Palette data for character dot data 10 in DMG mode.		Palette data for character dot data 01 in DMG mode.		Palette data for character dot data 00 in DMG mode.		W
OBP0 OBJ palette data 0	FF48	Palette data for character dot data 11 in DMG mode.		Palette data for character dot data 10 in DMG mode.		Palette data for character dot data 01 in DMG mode.		Palette data for character dot data 00 in DMG mode.		W When attribute bit4 is 0.
OBP1 OBJ palette data 1	FF49	Palette data for character dot data 11 in DMG mode.		Palette data for character dot data 10 in DMG mode.		Palette data for character dot data 01 in DMG mode.		Palette data for character dot data 00 in DMG mode.		W When attribute bit4 is 1.
WY Window y-coordinate	FF4A									R/W 0 - 143 Top edge when WY=0
WX Window x-coordinate	FF4B									R/W 7 - 165 Left edge when WX=7
KEY1 CPU speed switching	FF4D	Current speed: 0: Normal 1: Double speed							Enable speed switching	R/W Switch by setting bit0 to 1 and issuing a STOP instruction
VBK VRAM bank specification	FF4F								Bank 0: Bank0 1: Bank1	R/W Bank0 selected immediately after a reset signal.
HDMA1 Higher-order address of HDMAtransfer source	FF51									W 0x00 - 0x7F (ROM) 0xA0 - 0xDF (VRAM)
HDMA2 Lower-order address of HDMAtransfer source	FF52									W 0x00 - 0xFF
HDMA3 Higher-order address of HDMAtransfer destination	FF53									W 0x00 - 0x1F
HDMA4 Lower-order address of HDMAtransfer destination	FF54									W 0x00 - 0xFF

**Appendix 2: Register and Instruction Set Summaries**

Register	Address	D7	D6	D5	D4	D3	D2	D1	D0	Comment
HDMA5 H-blank and general- purpose DMA control	FF55	DMA selection 0: General purpose 1: H- blank	$0 \leq n \leq 127$ Total number of transferred bytes: $16 \times (n+1)$							W H-blanking stopped by setting bit 7 to 0; General- purpose stopped by resetting
RP  Infrared communication port	FF56	Data read-enable flag 00: Disable 11: Enable						Read data 0: LED-ON 1: LED-OFF	Write data 0: LED-OFF 1: LED-ON	R/W
BCPS Color palette BG write specification	FF68	Increment 0: OFF 1: ON		Palette No. 0 - 7			Palette No. 0 - 3		H/L specification 0: L 1: H	R/W Not incremented automatically with a read
BCPD Color palette BG write data	FF69									R/W
OCPS Color palette OBJ write specification	FF6A	Increment 0: OFF 1: ON		Palette No. 0 - 7			Palette No. 0 - 3		H/L specification 0: L 1: H	R/W Not incremented automatically with a read
OCPD Color palette OBJ write data	FF6B									R/W

Register	Address	D7	D6	D5	D4	D3	D2	D1	D0	Comment
SVBK WRAM Bank specification	FF70						Banks specification 0,1: Specifies bank 1 2-7: Specifies banks 2-7			R/W
<u>OBJ0</u> <sup>*1</sup> LCD y- coordinate	FE00									R/W 0x00—0xFF Top edge when Y=0x10
LCD x- coordinate	FE01									R/W 0x00—0xFF Left edge when X=0x08
Character code	FE02									R/W 0x00—0xFF
Attribute flag	FE03	Display priority 0: OBJ 1: BG	Vertical flip 0: Normal 1: Flip	Horizontal flip 0: Normal 1: Flip	Palette specification for DMG mode	VRAM bank 0: bank0 1: bank1	Color Palette No. 0 - 7			R/W
<sup>*1</sup> OBJ1 - OBJ39 same as OBJ0										

The dark frame  indicates a flag or register unique to CGB.

## 2. SOUND REGISTER SUMMARY

All values shown in the following table apply to normal mode. The values for double-speed mode should be calculated by doubling the system clock frequency.

calculated by doubling the system clock frequency.

	Register	Address	D7	D6	D5	D4	D3	D2	D1	D0	Comment		
S O U N D  1	NR10	FF10		Sweep time: 010:15.6ms 101:39.1ms 000:OFF 011:23.4ms 110:46.9ms 001:7.8ms 100:31.3ms 111:54.7ms			Sweep increase /decrease 0: + f <sub>hi</sub> 1: - f <sub>low</sub>	Number of sweep shifts: 0 - 7			R/W f <sub>128</sub> =128Hz		
	NR11 Duty cycle/sound length	FF11		Waveform duty cycle 00: 12.5% 10: 50% 01: 25% 11: 75%		Sound length data t1: 0 - 63 Sound length = (64+t1) * (1/256) sec						R/W	
	NR12 Envelope	FF12		Initial envelope value: 0x00 - 0x0F Mute when 0x00 Maximum when 0x0F				Envelope U/D 0: Attenuate 1: Amplify	Number of envelope steps N= 0 - 7 Length of 1 step = N*(1/64) sec Envelope function stopped when N=0			R/W Initial value of 00 sets to OFF when in DOWN mode	
	NR13 Lower- order frequency data	FF13		Lower order 8 bits of frequency data									W
	NR14 Higher- order frequency data/ other	FF14		Restart when initialize flag set to 1 0: Consecutive 1: NR11	Length selection 0: Consecutive 1: NR11				Higher order 3 bits of frequency data With x=11-bit frequency data, f= 4194304/(4*2 <sup>3</sup> (2048-x)) Hz			R/W f= 64Hz - 131kHz	
S O U N D  2	NR21 Duty cycle/sound length	FF16	Waveform duty cycle 00: 12.5% 10: 50% 01: 25% 11: 75%		Sound length t1: 0 - 63 Sound length = (64+t1) * (1/256) sec							R/W	
	NR22 Envelope	FF17	Initial envelope value: 0x00 - 0x0F Mute when 0x00 Maximum when 0x0F				Envelope U/D 0: Attenuate 1: Amplify	Number of envelope steps N=0-7 Length of 1 step = N*(1/64) sec Envelope function stops when N=0			R/W Initial value of 00 sets to OFF when in DOWN mode		
	NR23 Lower- order frequency data	FF18	Lower order 8 bits of frequency data,									W	
	NR24 Higher- order /other frequency data	FF19	Restart when initialize flag set to 1 0: Consecutive 1: NR21	Length selection 0: Consecutive 1: NR21				Higher order 3 bits of frequency data With x=11-bit frequency data, f= 4194304/(4*2 <sup>3</sup> (2048-x)) Hz			R/W f= 64Hz - 131kHz		

	Register	Address	D7	D6	D5	D4	D3	D2	D1	D0	Comment
S O U N D  3	NR30  Sound OFF	FF1A	Sound OFF 0: OFF 1: ON								R/W
	NR31  Sound length data	FF1B	Sound length data t1 : 0 - 255 Sound length = $(256-t1) * (1/256)$ sec								R/W
	NR32  Output level	FF1C		Output level 00: Mute 10: 1/2 01: Max 11: 1/4							R/W
	NR33  Lower- order frequency data	FF1D	Lower-order 8 bits of frequency data								W
	NR34  Higher- order frequency data/other	FF1E	Restart when initialize flag set to 1	Length selection 0: Consecutive 1: NR31				Higher-order 3 bits of frequency data With x=11-bit frequency data, $f = 4194304 / (2^{(2048-x)})$ Hz			R/W f= 64Hz - 131kHz



	Register	Address	D7	D6	D5	D4	D3	D2	D1	D0	Comment
S C U N D	NR41 Sound length data	FF20			Sound length data t1 : 0 - 63 Sound length = (64-t1) * (1/256) sec						R/W
	NR42 Envelope	FF21	Initial envelope value 0x00 – 0x0F Mute when 0x00 Max when 0x0F			Envelope U/D 0: Attenuate 1: Amplify	Number of envelope steps N=0-7 Length of 1 step = N*(1/64) sec Envelope function stops when N=0				R/W Initial value of 00 sets to OFF when in DOWN mode
	NR43 Polynomial counter	FF22	Polynomial counter clock frequency selection 0000: $f_b \times 1/2$ 1100: $f_b \times 1/2^{10}$ 1110: $f_b \times 1/2^{12}$ 1111: $f_b \times 1/2^{14}$ Prohibited codes				Step no. selection 0: 15 steps 1: 7 steps	Selection of frequency dividing ratio $f_b$ 000: $f \times 1/2^{1/2}$ 110: $f \times 1/2^{1/6}$ 001: $f \times 1/2^{1/1}$ to 000: $f \times 1/2^{1/7}$			W f = 4.194304MHz
	NR44 Initialize/length	FF23	Restart when initialize flag set to 1	Length selection 0: Conservative 1: NR41							R/W
C C N T R O L	NR50 SQ1/SQ2 level	FF24	VIN input 0: SQ2 OFF 1: SQ2 output	SQ2 output level control 000 (min) – 111 (max)			VIN input 0: SQ1 OFF 1: SQ1 output	SQ1 output level control 000 (min) – 111 (max)			R/W
	NR51 Distribution to SQ1/SQ2	FF25	Sound 4 to SQ2	Sound 3 to SQ2	Sound 2 to SQ2	Sound 1 to SQ2	Sound 4 to SQ1	Sound 3 to SQ1	Sound 2 to SQ1	Sound 1 to SQ1	R/W 0: No output 1: Output
	NR52 Sound-end flag	FF26	All sounds 0: Stop 1: Play				Sound 4 ON flag	Sound 3 ON flag	Sound 2 ON flag	Sound 1 ON flag	R/W

#### Waveform RAM

Waveform RAM is made up of waveform patterns consisting of 4 bits × 32 steps.

Address	D7	D6	D5	D4	D3	D2	D1	D0
FF30	Step 0				Step 1			
FF31	Step 2				Step 3			
FF32	Step 4				Step 5			
⋮								
⋮								
⋮								
FF3F	Step 30				Step 31			

## 3. CPU INSTRUCTION SET SUMMARY

	MNEMONIC	SYMBOLIC OPERATION	FLAGS				CYCL	OP-CODE 76 543 210	COMMENT		
			CY	H	N	Z					
8-Bit Transfer/Input-Output Instructions	LD r,r'	$r \leftarrow r'$	--	--	-	--	1	01 r r'			
	LD r,n	$r \leftarrow n$	--	--	-	--	2	00 r 110			
								$\leftarrow n \rightarrow$			
	LD r,(HL)	$r \leftarrow (HL)$	--	--	-	--	2	01 r 110	Register	r,r'	
	LD (HL),r	$(HL) \leftarrow r$	--	--	-	--	2	01 110 r	A	111	
	LD (HL),n	$(HL) \leftarrow n$	--	--	-	--	3	00 110 110	B	000	
								$\leftarrow n \rightarrow$	C	001	
	LD A,(BC)	$A \leftarrow (BC)$	--	--	-	--	2	00 001 010	D	010	
	LD A,(DE)	$A \leftarrow (DE)$	--	--	-	--	2	00 011 010	E	011	
	LD A,(C)	$A \leftarrow (FF00H + C)$	--	--	-	--	2	11 110 010	H	100	
	LD (C),A	$(FF00H + C) \leftarrow A$	--	--	-	--	2	11 100 010	L	101	
	LD A,(n)	$A \leftarrow (n)$	--	--	-	--	3	11 110 000			
								$\leftarrow n \rightarrow$			
	LD (n),A	$(n) \leftarrow A$	--	--	-	--	3	11 100 000			
								$\leftarrow n \rightarrow$			
	LD A,(nn)	$A \leftarrow (nn)$	--	--	-	--	4	11 111 010			
								$\leftarrow n \rightarrow$			
								$\leftarrow n \rightarrow$			
	LD (nn),A	$(nn) \leftarrow A$	--	--	-	--	4	11 101 010			
								$\leftarrow n \rightarrow$			
								$\leftarrow n \rightarrow$			
	LD A,(HLI)	$A \leftarrow (HL)$ $HL \leftarrow HL + 1$	--	--	-	--	2	00 101 010			
	LD A,(HLD)	$A \leftarrow (HL)$ $HL \leftarrow HL - 1$	--	--	-	--	2	00 111 010			
	LD (BC),A	$(BC) \leftarrow A$	--	--	-	--	2	00 000 010			
	LD (DE),A	$(DE) \leftarrow A$	--	--	-	--	2	00 010 010			
	LD (HLI),A	$(HL) \leftarrow A$ $HL \leftarrow HL + 1$	--	--	-	--	2	00 100 010	Register Pair	dd	
									BC	00	

**Appendix 2: Register and Instruction Set Summaries**

16-Bit Transfer Instructions	MNEMONIC	SYMBOLIC OPERATION	CY	FLAGS H	N	Z	CYCL	OP-CODE 76 543 210	Register Pair	dd
	LD (HLD),A	(HL) ← A HL←HL-1	--	--	-	--	2	00 110 010	DE	01
									HL	10
									SP	11
	LD dd,nn	dd←nn	--	--	-	--	3	00 cd0 001		
							L-ADRS	← n →		
							H-ADRS	← n →	Register Pair	qq
	LD SP,HL	SP←HL	--	--	-	--	2	11 111 001	BC	00
	PUSH qq	(SP-1) ← qqH (SP-2) ← qqL SP←SP-2	--	--	-	--	4	11 qq0 101	DE	01
									HL	10
									AF	11
	POP qq	qqL←(SP) qqH←(SP+1) SP←SP-2	--	--	-	--	3	11 qq0 001	e=-128~+127	
	LDHL SP,e	HL←SP+e	+	+	0	0	3	11 111 000		
								← e →		
	LD (nn),SP	(nn)←SPL (nn+1) ←SPH	--	--	-	--	5	00 001 000		
							L-ADRS	← n →		
							H-ADRS	← n →		

	MNEMONIC	SYMBOLIC OPERATION	FLAGS				CYCL	OP-CODE 76 543 210	COMMENT					
			CY	H	N	Z								
8-Bit Arithmetic and Logical Operation Instructions	ADD A,r	$A \leftarrow A+r$	*	*	0	*	1	10 000 r	s is any of r,n,(HL)  CYCL 1: s is r 2: s is n or (HL)					
	ADD A,n	$A \leftarrow A+n$	*	*	0	*	2	11 000 110						
								$\longleftrightarrow n$						
	ADD A,(HL)	$A \leftarrow A+(HL)$	*	*	0	*	2	10 000 110						
	ADC A,s	$A \leftarrow A+s+CY$	*	*	0	*	1,2	-- --- ---						
	SUB s	$A \leftarrow A-s$	*	*	1	*	1,2	-- --- ---						
	SBC A,s	$A \leftarrow A-s-CY$	*	*	1	*	1,2	-- --- ---						
	AND s	$A \leftarrow A \wedge s$	0	1	0	*	1,2	-- --- ---						
	OR s	$A \vee s$	0	0	0	*	1,2	-- --- ---						
	XOR s	$A \oplus s$	0	0	0	8	1,2	-- --- ---						
	CP s	$A-s$	*	*	1	*	1,2	-- --- ---						
	INC r	$r \leftarrow r+1$	--	*	0	*	1	00 r 100						
INC (HL)	$(HL) \leftarrow (HL)+1$	--	*	0	*	3	00 110 100	<table><tr><td>Register Pair</td><td>ss</td></tr><tr><td>BC</td><td>00</td></tr><tr><td>DE</td><td>01</td></tr></table>	Register Pair	ss	BC	00	DE	01
Register Pair	ss													
BC	00													
DE	01													
	DEC r	$r \leftarrow r-1$	--	*	1	*	1	00 r 101						
	DEC (HL)	$(HL) \leftarrow (HL)-1$	--	*	1	*	3	00 110 101						
16-Bit Arithmetic Operation Instructions	ADD HL,ss	$HL \leftarrow HL+ss$	*	*	0	--	2	00 ss1 001	<table><tr><td>HL</td><td>10</td></tr></table>	HL	10			
	HL	10												
	ADD SP,e	$SP \leftarrow SP+e$	*	*	0	0	4	11 101 000	<table><tr><td>SP</td><td>11</td></tr></table>	SP	11			
	SP	11												
								$\longleftrightarrow e$						
	INC ss	$ss \leftarrow ss+1$	--	--	--	--	2	00 ss0 011	e=-128~+127					
	DEC ss	$ss \leftarrow ss-1$	--	--	--	--	2	00 ss1 011						

The flag is affected according to the result of the operation.

Z: Zero flag. z=1 if the result of the operation is 0  
 C: Carry/link flag. C=1 if the operation produced a carry from the MSB of the operand or result  
 H: Half-carry flag.  
 N: Add/Subject flag.

	MNEMONIC	SYMBOLIC OPERATION	FLAGS				CYCL	OP-CODE 76 543 210	COMMENT														
			CY	H	N	Z																	
Rotate Shift Instructions	RLCA		A <sub>7</sub>	0	0	0	1	00 000 111	<table><tr><td>Register</td><td>r</td></tr><tr><td>A</td><td>111</td></tr><tr><td>D</td><td>000</td></tr><tr><td>C</td><td>001</td></tr><tr><td>E</td><td>010</td></tr><tr><td>H</td><td>100</td></tr><tr><td>L</td><td>101</td></tr></table>	Register	r	A	111	D	000	C	001	E	010	H	100	L	101
	Register	r																					
	A	111																					
	D	000																					
	C	001																					
	E	010																					
	H	100																					
	L	101																					
	RLA		A <sub>7</sub>	0	0	0	1	00 010 111															
	RRCA		A <sub>0</sub>	0	0	0	1	00 001 111															
	RRA		A <sub>0</sub>	0	0	0	1	00 011 111															
	RLC m		m <sub>7</sub>	0	0	*	--	-- --- ---	<table><tr><td>m is any of (HL)</td><td>CYCL</td></tr><tr><td>RLC r</td><td>2</td></tr><tr><td>RLC (HL)</td><td>4</td></tr></table>	m is any of (HL)	CYCL	RLC r	2	RLC (HL)	4								
	m is any of (HL)	CYCL																					
	RLC r	2																					
RLC (HL)	4																						
RL m		m <sub>7</sub>	0	0	*	--	-- --- ---	<table><tr><td>RL r</td><td>2</td></tr><tr><td>RL (HL)</td><td>4</td></tr></table>	RL r	2	RL (HL)	4											
RL r	2																						
RL (HL)	4																						
RRC m		m <sub>0</sub>	0	0	*	--	-- --- ---	<table><tr><td>RRC r</td><td>2</td></tr><tr><td>RRC (HL)</td><td>4</td></tr></table>	RRC r	2	RRC (HL)	4											
RRC r	2																						
RRC (HL)	4																						
RR m		m <sub>0</sub>	0	0	*	--	-- --- ---	<table><tr><td>RR r</td><td>2</td></tr><tr><td>RR (HL)</td><td>4</td></tr></table>	RR r	2	RR (HL)	4											
RR r	2																						
RR (HL)	4																						
SLA m		m <sub>7</sub>	0	0	*	--	-- --- ---	<table><tr><td>SLA r</td><td>2</td></tr><tr><td>SLA (HL)</td><td>4</td></tr></table>	SLA r	2	SLA (HL)	4											
SLA r	2																						
SLA (HL)	4																						
SRA m		m <sub>0</sub>	0	0	*	--	-- --- ---	<table><tr><td>SRA r</td><td>2</td></tr><tr><td>SRA (HL)</td><td>4</td></tr></table>	SRA r	2	SRA (HL)	4											
SRA r	2																						
SRA (HL)	4																						
SRL m		m <sub>0</sub>	0	0	*	--	-- --- ---	<table><tr><td>SRL r</td><td>2</td></tr><tr><td>SRL (HL)</td><td>4</td></tr></table>	SRL r	2	SRL (HL)	4											
SRL r	2																						
SRL (HL)	4																						
SWAP m		0	0	0	*	--	-- --- ---	<table><tr><td>SWAP r</td><td>2</td></tr><tr><td>SWAP (HL)</td><td>4</td></tr></table>	SWAP r	2	SWAP (HL)	4											
SWAP r	2																						
SWAP (HL)	4																						

	MNECMONIC	SYMBOLIC OPERATION	FLAGS				CYCL	OP-CODE 76 543 210	COMMENT																																				
			C <sup>v</sup>	H	N	Z																																							
Bit Operations	BIT b,r	$Z \leftarrow \overline{b_r}$	--	1	0	$\overline{r_b}$	2	11 00' 011	<table><tr><th>R#</th><th>b</th><th>Register</th><th>r</th></tr><tr><td>0</td><td>000</td><td>A</td><td>111</td></tr><tr><td>1</td><td>001</td><td>B</td><td>000</td></tr><tr><td>2</td><td>010</td><td>C</td><td>001</td></tr><tr><td>3</td><td>011</td><td>D</td><td>010</td></tr><tr><td>4</td><td>100</td><td>E</td><td>011</td></tr><tr><td>5</td><td>101</td><td>H</td><td>100</td></tr><tr><td>6</td><td>110</td><td>L</td><td>101</td></tr><tr><td>7</td><td>111</td><td></td><td></td></tr></table>	R#	b	Register	r	0	000	A	111	1	001	B	000	2	010	C	001	3	011	D	010	4	100	E	011	5	101	H	100	6	110	L	101	7	111		
	R#	b	Register	r																																									
	0	000	A	111																																									
	1	001	B	000																																									
	2	010	C	001																																									
	3	011	D	010																																									
	4	100	E	011																																									
5	101	H	100																																										
6	110	L	101																																										
7	111																																												
BIT b,(HL)	$Z \leftarrow (HL)_b$	--	1	0	$(HL)_b$	3	11 00' 011																																						
							01 b 110																																						
SE <sup>-</sup> b,r	$b_r \leftarrow 1$	--	--	--	--	2	11 00' 011																																						
							11 b r																																						
SE b,(HL)	$(HL)_b \leftarrow 1$	--	--	--	--	4	11 UU' U11																																						
							11 b 110																																						
RES b,r	$b_r \leftarrow 0$	--	--	--	--	2	11 00' 011																																						
							10 b r																																						
RES b,(HL)	$(HL)_b \leftarrow 0$	--	--	--	--	4	11 00' 011																																						
							10 b 110																																						
Jump Instructions	JP nn	$PC \leftarrow nn$	--	--	--	--	4	11 000 011	<p>* No. of cycles is 3 when no cc agreement:</p> <table><tr><th>CC</th><th>Condition</th><th>Flag</th></tr><tr><td>00</td><td>NZ</td><td>Z=0</td></tr><tr><td>01</td><td>Z</td><td>Z=1</td></tr><tr><td>10</td><td>NC</td><td>CY=0</td></tr><tr><td>11</td><td>C</td><td>CY=1</td></tr></table> <p>e=-127~+129</p>	CC	Condition	Flag	00	NZ	Z=0	01	Z	Z=1	10	NC	CY=0	11	C	CY=1																					
	CC	Condition	Flag																																										
	00	NZ	Z=0																																										
	01	Z	Z=1																																										
	10	NC	CY=0																																										
	11	C	CY=1																																										
								$\xleftarrow{\quad n \quad} \xrightarrow{\quad}$																																					
							$\xleftarrow{\quad n \quad} \xrightarrow{\quad}$																																						
JP cc,nn	If octrue, $PC \leftarrow nn$	--	--	--	--	4/3	11 0cc 010																																						
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							$\xleftarrow{\quad n \quad} \xrightarrow{\quad}$																																						
JR c	$PC \leftarrow PC + e$					3	00 01' 000																																						
							$\xleftarrow{\quad e-2 \quad} \xrightarrow{\quad}$																																						
JR cc,e	If octrue, $PC \leftarrow PC + e$	--	--	--	--	3/2	00 1cc 000																																						
							$\xleftarrow{\quad e-2 \quad} \xrightarrow{\quad}$																																						
JP (HL)	$PC \leftarrow HL$	--	--	--	--	1	11 10' 001																																						
Call/Return Instructions	CALL nn	$(SP-1) \leftarrow PC_H$ $(SP-2) \leftarrow PC_L$ $PC \leftarrow nn$ $SP \leftarrow SP-2$	--	--	--	--	6	11 00' 101	<table><tr><th>Operands</th><th>t</th><th>(PC<sub>H</sub>)</th><th>(PC<sub>L</sub>)</th></tr><tr><td>0</td><td>000</td><td>0x00</td><td>0x00</td></tr><tr><td>1</td><td>001</td><td>0x00</td><td>0x08</td></tr><tr><td>2</td><td>010</td><td>0x00</td><td>0x10</td></tr><tr><td>3</td><td>011</td><td>0x00</td><td>0x18</td></tr><tr><td>4</td><td>100</td><td>0x00</td><td>0x20</td></tr><tr><td>5</td><td>101</td><td>0x00</td><td>0x28</td></tr><tr><td>6</td><td>110</td><td>0x00</td><td>0x30</td></tr><tr><td>7</td><td>111</td><td>0x00</td><td>0x38</td></tr></table>	Operands	t	(PC <sub>H</sub> )	(PC <sub>L</sub> )	0	000	0x00	0x00	1	001	0x00	0x08	2	010	0x00	0x10	3	011	0x00	0x18	4	100	0x00	0x20	5	101	0x00	0x28	6	110	0x00	0x30	7	111	0x00	0x38
	Operands	t	(PC <sub>H</sub> )	(PC <sub>L</sub> )																																									
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	4	100	0x00	0x20																																									
	5	101	0x00	0x28																																									
	6	110	0x00	0x30																																									
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								$\xleftarrow{\quad n \quad} \xrightarrow{\quad}$																																					
	CALL cc,nn	If octrue, $(SP-1) \leftarrow PC_H$ $(SP-2) \leftarrow PC_L$ $PC \leftarrow nn$ $SP \leftarrow SP-2$	--	--	--	--	6/3	11 0cc 100																																					
							$\xleftarrow{\quad n \quad} \xrightarrow{\quad}$																																						
							$\xleftarrow{\quad n \quad} \xrightarrow{\quad}$																																						
RET	$PC_L \leftarrow (SP)$ $PC_H \leftarrow (SP+1)$ $SP \leftarrow SP+2$	--	--	--	--	4	11 00' 001																																						
RETI	$PC_L \leftarrow (SP)$ $PC_H \leftarrow (SP+1)$ $SP \leftarrow SP+2$	--	--	--	--	4	11 011 001																																						
RET cc	If octrue, $PC_L \leftarrow (SP)$ $PC_H \leftarrow (SP+1)$ $SP \leftarrow SP+2$	--	--	--	--	5/2	11 0cc 000																																						
RST t	$(SP-1) \leftarrow PC_H$ $(SP-2) \leftarrow PC_L$ $SP \leftarrow SP-2$ $PC_H \leftarrow 0$ $PC_L \leftarrow P$	--	--	--	--	4	11 t 111																																						

	MNEMONIC	SYMBOLIC OPERATION	FLAGS				CYCL	OP-CODE 76 543 210	COMMENT
			CY	H	N	Z			
Gen-Purpose/Arithmetic/CPU Control Instructions	DAA	Decimal Adjust acc	*	0	--	*	1	00 100 111	
	CPL	$A \leftarrow \overline{A}$	- -	1	1	--	1	00 101 111	
	NOP	No operation	- -	--	--	--	1	00 000 000	
	CCF	$CY \leftarrow \overline{CY}$	$\overline{CY}$	0	0	--	1	00 111 111	
	SCF	$CY \leftarrow 1$	1	0	0	--	1	00 110 111	
	DI	$IME \leftarrow 0$	- -	--	--	--	1	11 110 011	
	EI	$IME \leftarrow 1$	- -	--	--	--	1	11 111 011	
	HALT	Halt	- -	--	--	--	1	01 110 110	
	STOP	Stop	- -	--	--	--	1	00 010 000	
								00 000 000	

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## APPENDIX 3: SOFTWARE SUBMISSION REQUIREMENTS

### 1. THE SOFTWARE SUBMISSION PROCESS

All software submissions to Nintendo of America Inc. must be forwarded to the attention of NOA Product Testing Supervisor. Otherwise, the submission's placement into the testing queue may be delayed. To help reduce a submission's turn-around time, it is suggested that licensees assign a primary contact person for each software submission. All communications with NOA concerning a submission's testing status should be forwarded through this individual. The contact person should also be responsible for notifying any other interested parties.

When a submission is approved, your company's primary contact will be notified immediately in writing.

When a submission is not approved, NOA may send a videotaped copy of the programming problem(s) which prevent(s) the submission from being approved. This is intended to assist the licensee in analyzing the cause of the software problem. It is the licensee's responsibility to send a copy of this tape to any developer(s) of the software. NOA strongly encourages that copies be sent to the software developer(s) as quickly as possible.

Software submissions should be sent to the following address:

Nintendo of America Inc.  
Attn: Product Testing Supervisor  
4820 150th Avenue NE  
Redmond, WA 98052  
Phone: (425) 861-2674  
Fax: (425) 882-3585

### 2. ITEMS REQUIRED FOR SUBMISSIONS

The following items must be submitted with each Game Boy software submission.

#### ***Specification Sheet and Check List***

The appropriate Software Specification sheet and the Software Submission Checklist must be filled out completely and must be correct for the particular program version.

#### ***ROM Data***

A copy of the ROM data must be submitted in binary format on MS-DOS® 3.5 inch disk(s). The size of the file must be equal to the size of the EP-ROM (i.e., one 4 Meg EP- ROM = one 4 Meg file). Please label each disk and include a description of its contents. (See "Storing Data to the Floppy Disk" below.)

<b>Note</b>	<b><i>For software that supports communications, when communications are delayed for more than one hour after the game starts, in addition to the above items, you must submit one set of boards with EP-ROM (or a flash board) in which the game has been advanced to the point where communication can take place.</i></b>
-------------	--

#### ***Game Play Videotape/Rating Certificate***

A video tape containing complete game play is required unless the product has been rated by the Entertainment Software Ratings Board (ESRB). If the product has been rated by the ESRB, then a copy of the rating certificate must accompany the submission and no video tape is needed.

### **Screen Text**

A printed copy of the complete screen text must be submitted.

### **Instruction Manual**

One copy of the instruction manual must be included with your game submission. If, at the time of submission the manual is not complete, (submitted as an intermediate version) then you must submit a list of known bugs.

**Note** *If any of these items are not satisfied, the program will be rejected and will not be submitted into the approval process until all criteria are met.*

## **3. SOFTWARE VERIFICATION**

The following verification process will significantly improve the probability of approval of your software.

1. The licensing screen on all submissions should state "LICENSED BY NINTENDO".
2. Confirm the Licensing Screen information is correct.
3. Check the spelling on the Licensing Screen and Title Screen, as well as the spelling and grammar on the screen text.
4. Confirm the use of a TM (™), circle R (®), or circle C (©) where applicable.
5. Run a "Bypass" Test to assure that when the game is powered up, the Licensing Screen is visible for at least one second, even if any combination of controller buttons are pressed repeatedly. Also "Power-up" the software repeatedly to assure it does so without programming failures.
6. Game characters should be moved in all possible directions or positions, regardless of whether it is required to play the game properly. For instance, if the game does not require going to a particular area to complete the game, go there anyway to assure there are no programming problems in going to that location.
7. The software should be paused many times during the test, as this often causes programming problems to surface.
8. All testing should be recorded onto a videotape, making it easier to review programming problems.
9. The entire attract mode (demo) should be viewed to assure there are no programming problems.
10. Routines designed to assist the programmer or developer in "debugging" the software should be removed from the game prior to submission. This includes routines to determine hardware type.

11. A Game Boy Color dedicated game must include a hardware check upon power-up, which will display the following message when it is connected to a device other than Game Boy Color. The official game title must also be displayed in the upper portion of the display screen.

--<Game Title>--

"This game can only be played on Game Boy Color"

#### **4. LICENSEE GAME PLAY VIDEOTAPE PASS/FAIL GUIDELINES**

1. The licensee game play videotape (if included) must be recorded on a VHS tape, Standard Play speed (SP) for clarity.
2. No editing of the tape is allowed.
3. If more than one tape is needed to show the entire piece of software, then when a second tape begins it must show that the player is in the exact same place as where the first tape left off.
4. No codes or "built-up" characters are allowed.
5. All levels or areas must be completed, in succession.
6. Screen text must have correct grammar and spelling.
7. No deviations from NOA Software Standards Policy may be present.
8. The entire ending credits (if any) must be shown.
9. If the product has been rated by the ESRB, then a copy of the rating certificate must accompany the submission and no videotape is needed.

#### **5. LICENSING SCREEN INFORMATION PASS/FAIL GUIDELINES**

The following Licensing information should be included for all software. This can be displayed on one (1) or two (2) screens.

1. Licensee's software title.
2. Licensee's trademark and copyright notice  
( \_ 19\_\_ Licensee's name or copyright owner)
3. LICENSED BY NINTENDO

##### ***Example***

Tom's Golf™ or ®

© 1992 ABC Corporation

LICENSED BY NINTENDO

If a blank screen appears for more than two seconds when powered up, Nintendo suggests placing a message or graphic on the screen so that consumers do not think their game is inoperable (e.g., -- "Please Wait"--). If a blank screen appears for more than five seconds during game play, a message or graphic should also be placed on the screen.

## 6. COMMON PROBLEMS

Some possible problems that may prevent approval of your software include, but are not limited to the following:

1. Software locks up.
2. Scrambled blocks or characters appear on the screen.
3. The software won't pause.
4. Your character can get stuck somewhere with no possible way to get out.
5. Scrambled graphics at the edges of the screen when the screen scrolls in any direction.
6. Vowels in the passwords or password entry-system.
7. Colored lines at the top or bottom of the screen.
8. Shifting of the screen in any direction.
9. Inconsistent scoring methods.
10. Flashes on screen.
11. Small flickering lines on the screen.
12. Hit or be hit by an enemy but no damage is incurred.
13. Three (3) or four (4) player game can be started without using a four player adapter.
14. Incorrect Licensing Screen; "Licensed by Nintendo" should appear for all formats.
15. Violation of any Programming Cautions in the product programming manual.
16. Communication problems on two-player linkable DMG games.
17. Horizontal or vertical black lines when switching between screens on DMG games.
18. Use of the Nintendo logo or representations of Nintendo products in software without license agreement.
19. The use of the term Super Nintendo or Nintendo when the Super Nintendo Entertainment System or Nintendo Entertainment System is the intended reference, respectively. Use of any term other than Nintendo 64 or N64 when the Nintendo 64 Entertainment System is the intended reference.
20. Character actions are inconsistent (for instance, a character that cannot fly, being able to walk off the edge of a platform and stand in midair).
21. Referring to the Nintendo Control Pad or Control Stick by an unacceptable term, such as; "joypad", "directional control", etc.
22. Referring to the Nintendo Controller by an unacceptable term, such as; "joystick", etc.
23. Referring to the Nintendo Game Pak by an unacceptable term, such as; "Game Cassette", etc.
24. Referring to the Game Boy Game Link by an unacceptable term, such as; "Video Link", etc.

**Note** *If Licensor approval is required, please assure that this has been finalized before the software submission has been made.*

## **7. A NOTE ON OBJECTIONABLE MATERIAL**

A copy of the Nintendo "Game Content Guidelines" is included at the end of this document. If you are unsure of whether an item of text or element of a game is within Nintendo Software Standards, you may contact our Engineering Department early in the development process and they will discuss questionable items over the phone. In cases concerning an extensive amount of text, please send it to the attention of NOA Product Testing Supervisor, at the address listed in below, with the questionable items highlighted. The material will be evaluated and you will be contacted within a week to ten days.

Nintendo of America Inc.  
Attn: Product Testing Supervisor  
4820 150th Avenue NE  
Redmond, WA 98052  
Phone: (425) 861-2674  
Fax: (425) 882-3585

**8. SOFTWARE SUBMISSION CHECKLIST****SOFTWARE SUBMISSION CHECKLIST**

<b>MACHINE TYPE</b>	<input type="checkbox"/> SNS	<input type="checkbox"/> NUS	<input type="checkbox"/> DMG	<input type="checkbox"/> CGB
<b>GAME NAME</b>	_____			
<b>COMPANY</b>	_____			
<b>GAME CODE</b>	SNS _ _ _ _		NUS _ _ _ _	
	DMG _ _ _ _		CGB _ _ _ _	
<b>VERSION</b>	<input type="checkbox"/> Evaluation <input type="checkbox"/> Approval Ver. ____ <input type="checkbox"/> Specification Sheet <input type="checkbox"/> 1 Set of ROMs <input type="checkbox"/> MS-DOS 3 1/2 Disk(s) (Files must be in binary format) <input type="checkbox"/> 1 copy of Custom DSP IC if applicable (Super NES submissions only) <input type="checkbox"/> 1 copy of VHS tapes or ESRB Rating Certificate <input type="checkbox"/> Screen Text <input type="checkbox"/> Instruction Manual or Game Play Instructions			
<b>REMARKS</b>	_____ _____ _____ _____			

**Note** This checklist must be included with the software submission. If any of the items are not satisfied, the program will be promptly returned and will not be submitted into the approval process until all criteria are met.

## 9. INSTRUCTIONS FOR SOFTWARE SPECIFICATION SHEET

1. Game Title  
Print the planned name for the game. You may use up to 11 characters.
2. Game Code  
Print the product code designated by Nintendo. Use "CGB-P-" for CGB-dedicated software (software that will not operate on a conventional Game Boy). Otherwise, use "DMG-P-".
3. Language  
Indicate the primary language used for messages, etc. in the game.
4. DMG Communication Mode  
Indicate whether the software has a function which uses an external expansion connector for Game Boy (or Super Game Boy), like a Game Boy communication cable.
5. Software Type  
Indicate whether the game being submitted is DMG exclusive, DMG/CGB compatible, or CGB exclusive.
6. CGB-related Functions  
Check the following items, as appropriate, if you selected "DMG/CGB compatible" or "CGB exclusive" in item 5.
  - a. Serial Transfer Speed (check all that apply)  
Check all corresponding communication speeds.
  - b. High Speed ROM Required?  
A high speed ROM is required if CPU double-speed mode (Key 1), horizontal blanking DMA, or general DMA is used.

**Note: These 3 functions cannot be used in MBC-1, 2, and 3.**

  - c. IR Communications  
If the software has CGB infrared communications capabilities, please indicate whether the function involves communications with the same game or with a different game. If you select "different game," include the game title in the parentheses.
7. Overseas Version  
If the game has been, or will be, sold in another country; indicate the product title and product code.
8. Contact  
Provide the company name, department, address, phone number, fax number, and the name of a representative that Nintendo should contact with all questions or comments about the product.



9. Submission Date

Provide the submission date and select the method used for submission.

10. Scheduled Release Date

Provide the scheduled release date for the game.

11. ROM Registration Data

Provide the contents registered in the indicated addresses of the master ROM. Refer to "ROM Registration Data Specification" for details. Enter the ASCII code for the characters in areas marked with parenthesis "( )".

12. Game Title Registration

Enter the game title registered in the master ROM using ASCII characters and their ASCII codes. Also enter the Game Code assigned by Nintendo. Refer to "Character Code List for Game Title Registration" for these entries.

13. Memory Controller

Indicate the type of memory controller used for this game. If no Memory Controller is used, mark None.

14. Memory Configuration

Indicate the memory configuration of the game, as follows.

- ◆ ROM: Indicate the ROM size.
- ◆ RAM: Indicate whether or not work RAM is installed in the Game Pak. If work RAM is installed, indicate whether it is used as an expansion device or contained inside an MBC. If it is used as an expansion device, indicate the size of the RAM in the location provided. Also indicate if work RAM requires data back-up (battery). When the MBC-3 Clock Counter function is used, check "Yes" for "Data Back-up", regardless of which box is checked for "RAM".

## 15. ROM Version

### Mask ROM Version

- ◆ Indicate "0" if submitting the first version of the game.
- ◆ Indicate the next higher number for each revised version after starting production.

### Submission ROM

- ◆ Indicate "0" for the first submission
- ◆ Indicate the next higher number each time the game contents change without updating the Mask ROM version.

Version	First	Second	Third	⇒ Change after first production	Fourth	Fifth
Mask ROM Version	0	0	0		1	1
EPROM Version	0	1	2		0	1
Version on Title Label of EPROM	0.0	0.1	0.2		1.0	1.1

↑  
First Production

	⇒ Change after second production	Sixth	Seventh	.....
		2	2	
		0	1	
		2.0	2.1	

↑  
Second Production

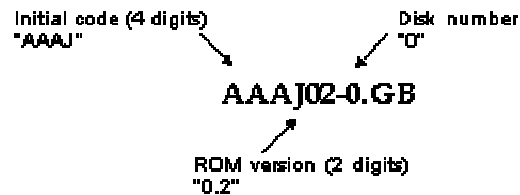
↑  
Third Production

**Example:**

## 16. File Name and Check Sums

Print the file name on each disk using the following format: \*\*\* \*\*-.GB

Example:



**Note:** *The first disk will be numbered "0."*

If the Initial code is 3 digits (prior to 1994), include an under bar (" \_ ") after the Initial code to bring it to 4 digits. The file name would appear as follows: "AAJ\_10-0.GB"

Enter the check sum of each ROM submitted. To calculate the check sum, add each byte in the ROM data. The lower 2 bytes of the resulting value is the check sum. Enter the check sum for each ROM submitted for the master program and the total of their individual check sums. The total is calculated by adding the individual check sums. This method of calculation is different from the check sum on the ROM Registration Specification.

**17. Programming Features**

Indicate if special programming is implemented for a specific purpose, such as copy protection. If special programming is implemented, it must be explained in writing.

If the software is N64 GB Pak compatible, indicate the name of the N64 game and its product code. (N64 GB Pak is a peripheral device that allows the N64 system to read data from and write to a standard Game Boy Game Pak. This device is not marketed in the U.S. For more information, please contact Nintendo Technical Support.)

**18. SGB Support**

If the software is designed to use Super Game Boy (SGB) functions, check "Yes." If the software is not specifically designed to use Super Game Boy functions, but will run on SGB, indicate "No."

If you checked "Yes" for SGB Support, the SGB Function Code (address 0146H) should contain "03H". If you checked "No", the data contained in address 0146H should read "00H".

Also, if you checked "Yes" for CGB Support, complete the following 3 items. Do not make any marks in these boxes if you checked "No".

**a. SGB Support Marking**

Check "Yes", if the SGB compatability marking needs to be displayed on product packaging. Otherwise, check "No".

**b. SGB Competition Mode**

Indicate whether the game contains a multi-player function for SGB, by checking the appropriate box.

**c. Program Transfer to Super NES**

Indicate whether or not the program is transferred to the S-CPU for execution as a unique program on the Super NES.

## 10. CHARACTER CODE LIST FOR GAME TITLE REGISTRATION

	00	10	20	30	40	50	60	70	80	~	F0
0			SP	0	@	P					
1			!	1	A	Q					
2			"	2	B	R					
3			#	3	C	S					
4			\$	4	D	T					
5			%	5	E	U					
6			&	6	F	V					
7			'	7	G	W					
8			(	8	H	X					
9			)	9	I	Y					
A			*	:	J	Z					
B			+	;	K	[					
C			,	<	L	¥					
D			-	=	M	]					
E			.	>	N	^					
F			/	?	O	_					

Note 1: Do not use characters in shaded areas.

Note 2: "SP" means space.

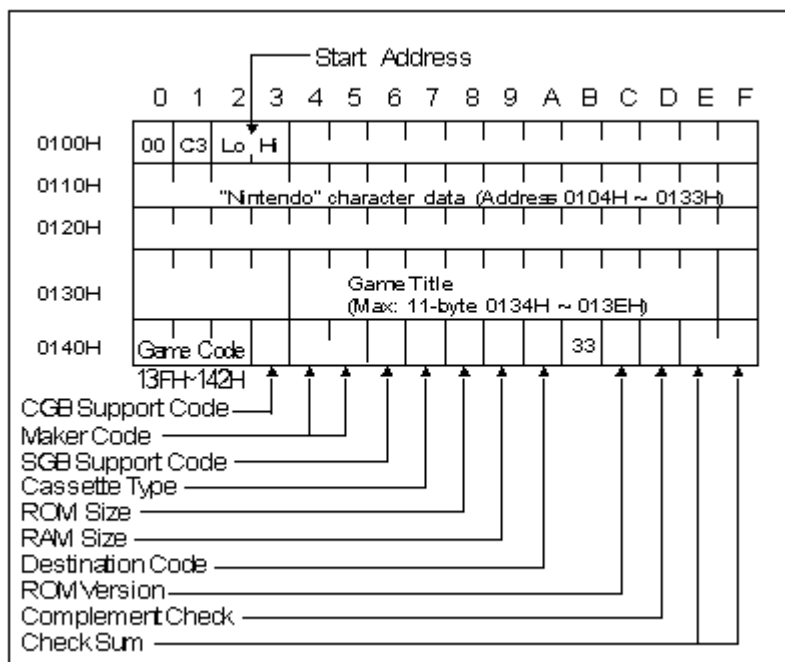
Example: If ASCII character is A, ASCII code is 41.

## 11. ROM REGISTRATION DATA SPECIFICATION

Enter information regarding the game title and Game Boy software specifications at the indicated addresses in ROM.

The ROM registration data address is 80 bytes of CPU memory (0100H ~ 014FH).

ROM registration data is stored using the following format.



**Note** The following data will be stored in Game Boy Memory for all Game Boy software.

0100H = 00H  
 0101H = C3H  
 014BH = 33H  
 0104H~0133H = "Nintendo" character data

## 11.1 Description of ROM Registration Data

1. Start Address (0102H, 0103H)  
The Game Boy (Super Game Boy) program starts after Initial Program Load (IPL) is run on the CPU. The low byte of the starting address is stored first, then the high byte.
2. "Nintendo" Character Data (0104H~0133H)  
Register the character pattern of "Nintendo" to be displayed when the Game Boy is turned on. The following hexadecimal data must be store since IPL verifies it when the program begins.
3. Game Title (0134H~013EH)  
Store the game title (up to 11 characters) using ASCII code. The table "Character Code List for Game Title Registration" is provided for your convenience. Use code 20H for a space and code 00H for all unused areas in the game title. Please use only those characters listed in the provided table when registering a game title. The game title registered should be close to the title under which the game will be marketed. Please do not register a tentative name which is used for development.
4. Game Code (013FH~0142H)  
Store the 4 character game code, assigned by Nintendo, using ASCII code from the table used in item 3. Please use only "upper case" letters, listed in the provided table, when registering a game code.  
Example:  
When the Game Code is "APCJ", the following codes would be stored.  
41H('A') → Address 013FH  
50H('P') → Address 0140H  
43H('C') → Address 0141H  
4AH('J') → Address 0142H  
This requirement only applies to new titles. If the program is changed and a master ROM resubmitted for a game title which has already been marketed, it is not necessary to insert a game code for this submission. (If the Game Code is added to an existing game, please be aware of potential problems with software verification routines in serial communication protocols or GB Pak routines. For example, the Game Titles for the old version and the new version MAY be different, causing the new version to be unrecognized by the software verification routine.)

5. CGB Support Code (0143H)

Store the code which distinguishes between games that are CGB (Game Boy Color) compatible, and those that are not.

Address 143H	Denotation
00H	CGB Incompatible
80H	CGB Compatible
C0H	CGB Exclusive

CGB Incompatible: A program which does not use CGB functions, but operates with both CGB and DMG (Monochrome).

CGB Compatible: A program which uses CGB functions, and operates with both CGB and DMG.

CGB Exclusive: A program which uses CGB functions, but will only operate on a Game Boy Color unit (not on DMG/MGB). If a user attempts to play this software on Game Boy, a screen must be displayed telling the user that the game must be played on Game Boy Color.

6. Maker Code (0144H, 0145H)

Enter the 2-digit ASCII code assigned by Nintendo. Contact Product Testing, if in doubt. All letters must be in upper case. For example;

If Maker Code is 01, the ASCII code for 0 (30H) is stored at 0144H and the ASCII code for 1 (31H) is stored at 0145H.

If Maker Code is FF, the ASCII code for F (46H) is stored at 0144H and 0145H.

7. SGB Support Code (0146H)

Store the Function Code for the game program. Use the table below.

0146H	Super Game Boy Function
00H	Game Boy (will also run on Super Game Boy)
03H	Uses Super Game Boy Functions

**Note** *In order to use Super Game Boy functions, the following data must be registered.*

0146H = 03H and 014BH = 33H



8. Cartridge Type (0147H)

Store the appropriate code for the type of cartridge (Game Pak parts configuration) being used.

Address 0147H	Parts Configuration								
	ROM	MBC-1	MBC-2	MBC-3		MBC5		SRAM	Backup Battery
				W/ RTC	No RTC	No Rumble	W/ Rumble		
00H	X								
01H	X	X							
02H	X	X						X	
03H	X	X						X	X
04H									
05H	X		X						
06H	X		X						X
07H									
08H	X							X	
09H	X							X	X
0FH	X			X					X
10H	X			X				X	X
11H	X				X				
12H	X				X			X	
13H	X				X			X	X
19H	X					X			
1AH	X					X		X	
1BH	X					X		X	X
19H	X						X		
1AH	X						X	X	
1BH	X						X	X	X

**9. ROM Size (0148H)**

Store the code for the program ROM size from the table below.

<b>0148H</b>	<b>ROM Size</b>
00H	256 KBit
01H	512 KBit
02H	1 MBit
03H	2 MBit
04H	4 MBit
05H	8 MBit
06H	16 MBit
07H	32 Mbit
08H	64 Mbit

**10. External RAM Size (0149H)**

Store the code for the size of external RAM installed in the cartridge.

<b>Address 149</b>	<b>RAM Size</b>
00H	No RAM or MBC2
01H	-----
02H	64 KBit
03H	256 KBit
04H	1 Mbit

**11. Destination Code (014AH)**

Store the code from the table below which indicates where the product will be marketed.

<b>Address 147</b>	<b>Destination</b>
00H	Japan
01H	All Others

**12. Mask ROM Version N0. (014CH)**

The mask ROM version number starts from 00 and increases by 1 for each revised version sent after starting production.

**13. Complement Check (014DH)**

After all the registration data has been entered (0134H~014CH), add 19H to the sum of the data stored at addresses 0134H through 014CH and store the complement value of the resulting sum.

$$(0134H) + (0135H) + \dots + (014CH) + 19H + (014DH) = 00H$$

**14. Check Sum Hi and Lo**

The check sum, excluding the value of 014EH and 014FH, is stored here.

Check sum Hi and Lo will be different from the Total Check Sum.

014EH = Upper

014FH = Lower

## **12. STORING DATA TO THE FLOPPY DISK**

1. Use MS-DOS® 3.5 inch, 2HD disk(s).
2. The data must be submitted in binary (ROM) format. Do not compress the data. The maximum amount of data stored on each floppy should be 8Mbit.
3. The file name should be formatted as described in item #16 of "Instructions for Game Boy Software Specification Sheet - File Name and Check Sums."
4. Place a label describing the content of each disk as shown below.

Company name: Nintendo Co., Ltd.

Product name: Mario's Pikurosu

Product code: DMG-P-APCJ (JPN)

File name: APCJ00-0.GB

Check sum: ABCD

Date: 1998/8/1

### 13. PRODUCTION SOFTWARE SELECTION

MBC	ROM SIZE SRAM SIZE		256K	512K	1M	2M	4M	8M	16 M	32 M	64M	Comments
None	None	○										
	64K	▲										With or without backup battery
MBC-1	None		○	○	○	○	○	○ <sup>*1</sup>	▲ <sup>*1</sup>			
	64K		○	○	○	○	○	○ <sup>*1</sup>	○ <sup>*1</sup>			With or without backup battery
	256K	▲	○	○	○	○						With or without backup battery
MBC-2	None	▲	○	○	○							With backup battery only
MBC-3 W/RTC	None	▲	▲	▲	▲	▲	▲	▲				With backup battery only
	64K	▲	○	○	○	○	○	▲				With backup battery only
	256K	▲	▲	▲	▲	▲	○	▲				With backup battery only
MBC-5	None		(▲)*2	(▲)*2	○	○	○	○	○	(○)		
	64K		(▲)*2	(▲)*2	○	○	○	○	○	(○)		With or without backup battery
	256K	(▲)*2	(▲)*2	(▲)*2	○	○	○	○	○	(○)		With or without backup battery
	1M	(▲)*2	(▲)*2	(▲)*2	▲	▲	▲	▲	▲	(▲)		With or without backup battery
MBC-5/ Rumble	None	(▲)*2	(▲)*2	(▲)*2	▲	○	○	▲	▲	(▲)		
	64K	(▲)*2	(▲)*2	(▲)*2	▲	○	○	○	○	(○)		With or without backup battery
	256K	(▲)*2	(▲)*2	(▲)*2	▲	○	○	▲	▲	(▲)		With or without backup battery

○ : Board Available

If a price quote is necessary, please submit a "Game Boy Price Quote Request Form" to NOA Licensing Dept.

▲ : Board Not Available

If required, please submit a "Game Boy Price Quote Request Form" to NOA Licensing Dept., approximately 5 months before scheduled software submission.

( ) : At the present time, a mask ROM cannot be prepared. If necessary, please contact NOA Licensing Dept.

[Notes] MBC-1, 2, and 3 do not support Game Boy Color double-speed mode (including H-DMA and General Purpose DMA. Please refer to your Programming Manual.

<sup>\*1</sup> There are some restrictions in memory mapping when MBC-1 ROM Size is 8M or larger. Please refer to "Memory Controllers" in your Programming Manual.<sup>\*2</sup> For MBC-5 with ROM of 1M or less, a mask ROM supporting CGB double-speed mode can not be prepared. Double-speed mode is supported by ROM of 2M or larger.

## 14. DEVELOPMENT SOFTWARE SELECTION

ROM SIZE MBC SRAM SIZE		256K	512K	1M	2M	4M	8M	16M	32M	Comments
None	None	1								
MBC-1	None		2	3						
	64K/None				4					<ul style="list-style-type: none"> <li>Built-in 64K SRAM With or without backup battery</li> </ul>
	256K/64K/None		5				6			
					7					<ul style="list-style-type: none"> <li>Built-in 256K SRAM With or without backup battery</li> </ul>
MBC-2	None			8						
MBC-3	256K/64K/None				9					<ul style="list-style-type: none"> <li>RTC Function</li> <li>Built-in 256K SRAM With or without backup battery</li> </ul>
MBC-5	1M/256K/64K/None					10				<ul style="list-style-type: none"> <li>Built-in 32M Flash ROM</li> <li>Built-in 1M SRAM With or without backup battery</li> </ul>
	256K/64K/None					11				<ul style="list-style-type: none"> <li>Built-in 32M Flash ROM</li> <li>Rumble Function</li> <li>Built-in 256K SRAM With or without backup battery</li> </ul>

	Product Names (*1)		Memory Specifications (*2)	Comments
	Board Name	Product Code		
1	DMG-256K-EPROM	E200225	EPROM : 27C256	EPROM not included
2	MBC1-512K-EPROM	E200241	EPROM : 27C512	
3	MBC1-1M to 2M-EPROM	E200233	EPROM : 27C101/27C2001 (Can use 301 type) (*3)	
4	MBC1-1M to 2M-EPROM+64K	E200530	EPROM : 27C101/27C2001/27C4001	
5	MBC1-Multichecker	E200191	EPROM : 27C256/27C512/27C101/27C301	
6	MBC1-4M to 16M-EPROM+64K	E200654	EPROM : 27C4001	
7	MBC1-1M to 4M-EPROM+256K	E200605	EPROM : 27C101/27C2001/27C4001	
8	MBC2-1M to 2M-EPROM	E200258	EPROM : 27C101/27C2001 (Can use 301 type) (*3)	
9	MBC3-4M-ROM2-256K	E201025	EPROM : 27C101/27C2001/27C4001/27C8001	

## Game Boy Programming Manual

	Product Names (*1)		Memory Specifications (*2)	Comments
	Board Name	Product Code		
10	DMG-MBC5-32M-FLASH	E201264	Built-in 32M Flash Memory + 1MRAM	Requires DMG Falsh ROM Gang Writer or CGB Emulator
11	DMG-MBC5-32M-R-FLASH	E201272	Built-in 32M Flash Memory (with Rumble Pak) +256KRAM	

[Notes] MBC-1, 2, and 3 do not support Game Boy Color double-speed mode (including H-DMA and General Purpose DMA. Please refer to your Programming Manual.

There are some restrictions in memory mapping when MBC-1 ROM size is 1M or larger. Please refer to "Memory Controllers" in your Programming Manual.

\*1 : When ordering, please indicate both the board name and product code to NOA Licensing Dept.

\*2 : For the EPROM specification, please use the described specification, above, or something with the same pin configuration.

\*3 : Can support both types for land switching on the board.

## **15. GAME CONTENT GUIDELINES**

The following Game Content Guidelines are presented for assistance in the development of authorized game paks (i.e., both Nintendo and licensee game paks) by defining the types of themes inconsistent with Nintendo's corporate philosophy. Exceptions may be made when an objectional item is necessary to maintain the integrity of the product or the games' theme. Nintendo will only approve products (i.e., audio-visual work, packaging and instruction manuals) which do not:

- contain sexually explicit content including but not limited to nudity, rape, sexual intercourse and sexual touching; for instance, Nintendo does not allow bare-breasted women in its games, however, mild displays of affection such as kissing or hugging are acceptable.
- contain language or depictions which specifically denigrate members of any race, gender, ethnicity, religion or political group.
- depict gratuitous or excessive blood or violence. Nintendo does not permit depictions of animal cruelty or torture.
- depict verbal or physical spousal or child abuse.
- permit racial, gender, ethnic, religious or political stereotypes; for example religious symbols such as crosses will be acceptable when fitting into the theme of the game and not promoting a specific religious denomination.
- use profanity, obscenity or incorporate language or gestures that are offensive by prevailing public standard and tastes.
- promote the use of illegal drugs, smoking materials, tobacco and/or alcohol; for example Nintendo does not allow an unnecessary beer or cigarette advertisement anywhere in a product, however Sherlock Holmes smoking a pipe would be acceptable as it fits the theme of the game.

## 16. GAME BOY PRICE QUOTE REQUEST FORM

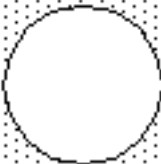
Please FAX this form to Nintendo of America Inc., Attn.: Juana Tingdale, Licensing Department, (206) 861-2173.

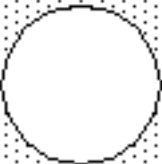
Today's Date (M/D/Y)	/ /	Licensee	
Release Date(M/D/Y)	/ /	Game Title	
Quantity		Contact	
<b>Specification</b>		Telephone No.	
<ROM> _____ Bit <RAM> _____ Bit/no RAM <Backup> Yes/ No			
<MBC> <u>MBC -</u>			
Others: Please specify if you are inquiring other than standard specification.			

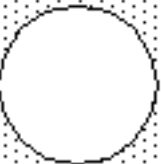
This area will be completed by Nintendo:

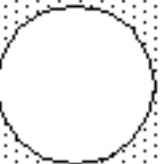
Received by NOA Engineering	Signature _____	Date _____
Received by NCL Licensing	Signature _____	Date _____
Received by NCL Engineering	Signature _____	Date _____
Received by NCL R & D	Signature _____	Date _____

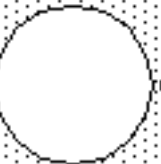
Estimated Completion Date(M/D/Y)	/ /	Resource	
Comments: EPROM PCB development, etc.			

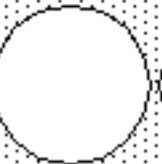
  
 NCL Licensing

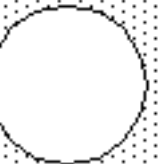
  
 NCL Engineering

  
 NCL R & D

  
 Resource

  
 Checked

  
 Checked

  
 Approved