APPENDIX 1: PROGRAMMING CAUTIONS

1. USING THIS APPENDIX

Purpose and Scope

These programming notes provide information on how to avoid easily made mistakes during program development, information on unique Game Boy programming issues that require special attention, and special issues regarding peripheral devices.

Items Covered in this Manual

Many of the topics covered in this appendix also are covered elsewhere in different chapters of this manual. This appendix consolidates the discussion of these topics. Topics that would be more easily comprehensible to the reader when presented separately will also be discussed in another chapter, even though this may duplicate the discussion in this appendix.

Note: Although these notes were created to make every effort to eliminate potential sources of trouble at market, they do not represent a guarantee that various potential problems on the market can be absolutely avoided.

2. PROGRAMMING CAUTIONS REGARDING GAME BOY

Covers:
DMG: DMG, MGB, and MGL
SGB: SGB and SGB2
CGB: CGB

2.1 LCDC/VRAM

2.1.1 Setting the LCDC to OFF (Recommended)

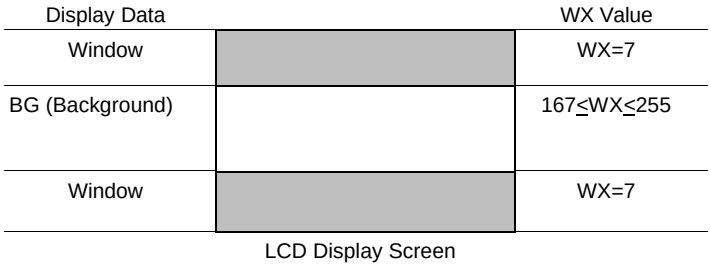
Covers: DMG and CGB
In early DMGs, a black horizontal line appears on the screen if the LCDC is stopped (LCDC register bit 7 ← 0) at any time other than during vertical blanking. Therefore, the LCDC should be set to OFF during V-blanking. If the occurrence of V-blanking cannot be confirmed, the LCDC should be set to OFF when the value of the LY register is 145 (0x91) or greater. These restrictions do not apply in CGB. Thus, when creating software for use on CGB only, the timing of setting the LCDC to OFF need not be considered.

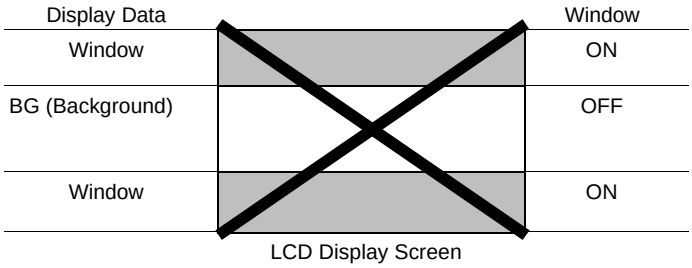
2.1.2 Window x-coordinate Register (Required)

Covers: DMG, SGB, and CGB
When the window is displayed, the window x-coordinate register (register WX, address 0xFF4B) must be set in the range 7-165. A setting of 0-6 or 166 is prohibited. Specifying a value of 167 or greater causes the window not to be displayed.

2.1.3 Displaying Multiple Windows (Required)

Covers: CGB
Multiple windows that divide the screen horizontally into upper and lower areas can be displayed by setting the window x-coordinate register (WX) to a value of 167 or greater during a horizontal blanking period. Attempting to display multiple windows by switching the window ON and OFF during H-blanking may result in the lower window not being displayed.





Reference Notes:

1. Accessing VRAM Outside of a V-blanking period
   In early DMGs, accessing VRAM outside of a V-blanking period would corrupt the screen.
2. Length of H-blanking
   The length of the H-blanking period changes depending on the conditions of OBJ use, so caution is recommended when using H-blanking.

2.2 Communication

2.2.1 Communication Rate *(Required)*

Covers: DMG, SGB2, and CGB
Data may be corrupted if the data transfer rate is too high.
The maximum external clock setting should be 512KHz between CGBs.
It should be 500KHz for others including DMG and SGB2.
Also, it should be 256KHz for communication between CGB and DMG.

2.2.2 Communication Errors (Recommended)

Covers: DMG, SGB2, and CGB
When using the communication function (infrared), the communicating data may be corrupted by noise and such. Therefore, the program should not go out of control by such data corruption on both the sending and receiving side.
When using the communication function (serial), depending on how program is made, it is confirmed that communication errors happen rarely.
SIO interrupt processing may be delayed by factors such as the processing of other interrupts. This type of error should be avoided by establishing a proper communication interval that allows a problem-free exchange of data.

2.2.3 Effects of Other Infrared Devices (Recommended)

Covers: CGB
Adequate care should be taken to ensure against faulty operation and loss of program control even when infrared communication signal input is received from other game software and devices. Note that such problems may particularly occur in communication between multiple games that use the same subroutines. (Before performing data communication, use means such exchanging a unique key code to check whether the same game is on the other hardware.)

2.3 Sound

2.3.1 Using Sounds 1, 2 , and 3 (Required)

Covers: CGB
With continuous operation mode selected (bit 6 of NR*4 set to 0) for sounds 1, 2, and 3, if the higher-order frequency data (lower-order 3 bits of NR*4) are changed, the sound length (bits 0-5 of NR*1) must to set to 0 after the frequency data is set. If the sound length is not set to 0, the sound may stop during playback.

2.3.2 Using Sound 3 (Required)

Covers: DMG, SGB, and CGB
When sound 3 is used, data should always first be specified for addresses 0xFF30-0xFF3F of waveform RAM. If the initial flag is set during sound 3 operation (sound 3 ON flag = 1), the contents of waveform RAM will be destroyed.

2.4 Miscellaneous Notes

2.4.1 Using Interrupts (Required)

Covers: DMG, SGB, and CGB
When interrupts are used, the IF register should be cleared before the IE register is set. If the IF register is not first cleared, an interrupt may be generated immediately after interrupts are enabled.

2.4.2 Reading Keys (Required)

Covers: DMG
An interval of approximately 18 cycles should be used between output from P14 and P15 and reading of input. Without this interval, normal key input cannot be read.

2.4.3 Using the Timer (Required)

Covers: DMG, SGB, and CGB
The timer should be started (TAC start flag set) after the count-up pulse is selected. Starting the timer before or at the same time as the pulse is selected may result in an extra count-up operation at the time of pulse selection.

Example:

```
LD   A,3      ;Selects f/256 as the count-up pulse.
LD   (07),A   ;Sets TAC ← 3
LD   A,7      ;Starts the timer
LD   (07),A
```

If a write instruction is executed for the modulo register TMA with the same timing as the contents of that register are transferred to TIMA as a result of a timer overflow, the same write data also will be transferred to TIMA..

2.4.4 Using STOP Mode (Required)

Covers: DMG, SGB, and CGB
When STOP mode is used, all interrupt-enable (IE) flags should be reset before execution of a STOP instruction. Otherwise, if an interrupt is generated during the period of oscillation stabilization (HALT mode) following STOP mode cancellation, HALT mode will immediately be canceled, preventing a stable system clock from being provided.

2.4.5 Using Paired Registers (Required)

Covers: DMG, SGB, and CGB
With instructions that use paired registers BC, DE, and HL, such as the following, there is some chance that OAM RAM may be destroyed. Therefore, ensure that these paired registers are not set to a value in the range 0xFE00-0xFE9E.

```
INC   ss              ; ss : BC, DE, HL
DEC   ss
LD    A,(HLI)
LD    A,(HLD)
LD    (HLI),A
LD    (HLD),A
```

2.4.6 Using the HALT Instruction (Required)

Covers: DMG, SGB, and CGB
When using a HALT instruction, always add an NOP instruction immediately after the HALT instruction. Not adding the NOP instruction may in rare cases cause the instruction after the HALT instruction not to be executed.

2.4.7 Switching the CPU Operating Speed (Recommended)

Covers: CGB
When switching the CPU operating speed, first confirm the current speed by checking the speed flag (bit 7 of register KEY1). In double-speed mode, both the divider (DIV) and timer (TIMA) registers will also be set for double-speed operation.

2.4.8 Using Horizontal Blanking DMA (Required)

Horizontal blanking DMA should always be started (bit 7 of HDMA5 set to 1) when the STAT mode is not set to 00. If horizontal blanking DMA is started when STAT mode is 00, depending on the timing, the data in LCD display RAM may be destroyed. In addition, execution of a HALT instruction during horizontal blanking DMA may prevent normal cancellation of the HALT mode or DMA. Therefore, HALT instructions should not be used while horizontal blanking DMA is being started.

2.4.9 Using General-Purpose DMA (Required)

General-purpose DMA should be started (bit 7 of HDMA5 set to 0) with the LCDC off or during V-blanking. However, when transferring data during V-blanking, ensure that the transfer period does not overlap with STAT modes 10 or 11.

2.4.10 DMA Transfers to OAM (Required)

In DMG and in CGB in DMG mode, when transferring data to OAM by DMA, the user program area (0x00-0x7FFF) should not be used as the starting address of the transfer. In some cases, data cannot be transferred from the user program area normally. CGB mode, however, does enable DMA transfers from the user program area.

2.4.11 Status Interrupts (Required)

Covers: DMG, SGB, and CGB
When using a status interrupt in DMG or in CGB in DMG mode, register IF should be set to 0 after the value of the STAT register is set. (In DMG, setting the STAT register value changes the value of the IF register, and an interrupt is generated at the same time as interrupts are enabled.)

2.4.12 Chattering (Recommended)

Covers: DMG, SGB, and CGB
To prevent buttons from inadvertently being pressed twice, an interval should be provided between key reads. (Although this varies with the software, keys are normally read approximately once per frame.)

3. PROGRAMMING CAUTIONS REGARDING MBCS

3.1 All MBCs

3.1.1 Protecting RAM Data (Recommended)

To protect RAM data, access to RAM should be disabled (RAMG←0x00) when it is not being accessed.

3.2 MBC3

3.2.1 Accessing the Clock Counters (Required)

If the clock counters themselves are counted up, accessing of the clock counters by the CPU is performed asynchronously. However, if these operations are performed simultaneously, the clock counters may fail. To prevent this, MBC3 provides an interface circuit for WR signals from the CPR. Use of this circuit necessitates a delay when accessing control register 3 and the clock counter registers (RTC_S, RTC_M, RTC_H, RTC_DL, and RTC_DH). Thus, whenever accessing these registers consecutively, interpose a delay of 4 cycles between accesses.

When reading clock counter data:

- Latch all clock counter data using control register 3.

4-cycle delay required

- Read the data in the clock counter registers.

When writing values to the clock counters:

- Set data in clock counter register RTC_S.

4-cycle delay required

- Set data in clock counter register RTC_M.

4-cycle delay required

- Set data in clock counter register RTC_H.

4-cycle delay required

- Set data in clock counter register RTC_DL.

4-cycle delay required

- Set data in clock counter register RTC_DH.

3.2.2 Condensation (Required)

MBC3 uses a crystal oscillator for its clock counter operation, and condensation on the oscillator may halt its oscillation, preventing the clocks from counting up. Once the condensation disappears, the clocks will resume counting up from where they stopped. However, please ensure that the counter stoppage does not result in a loss of program control.

3.2.3 Control Register Initialization (Required)

Although control registers 0-3 are initialized (see Section 3.2, *Description of Registers*) when the Game Boy power is turned on, they are not initialized by a hard reset of SNES when Super Game Boy is used. Therefore, please be sure to implement a software reset of these registers.

3.2.4 Clock Counter Registers (Required)

When commercial GB software that use MBC3 are shipped from the factory, the values of the clock counter registers are undefined. Therefore, please ensure that these registers are initialized.

3.3 MBC5

3.3.1 Memory Image (Required)

If a memory device is used that uses less than the maximum amount of memory available (ROM: 64 Mbits; RAM: 1 Mbit) , a memory image is generated for the empty bank area. Therefore, please do not develop software that uses an image, because it may cause failures.

3.3.2 Specifying External Sound Input (VIN) (Required)

Always use the sound control register (NR50) with bits 7 and 3 (VIN function OFF) set to 0. Because the VIN terminal is used in development flash ROM cartridges, using the register with VIN set to ON will produce sound abnormalities.

3.3.3 Disabling Vibration Using the SGB, SGB2, or 64GB Pak (Recommended)

When MBC5 with rumble feature is used by SGB, SGB2, or the 64GB Pak, vibration should be turned off by the program to prevent failures caused by a faulty connection. For methods of recognizing SGB and SGB2, see Chapter 6, section 4.2, Recognizing SGB. With the 64GB Pak, vibration is controlled by the N64 software. Therefore, N64 software programs that support MBC5 should not write data to bit 3 of the RAM bank register.

3.3.4 Disabling Vibrations for Resets and Pauses (Recommended)

Vibration should be halted during resets and pauses.
When power is turned on, the hardware should not be vibrated until some input is received from the controller.

3.3.5 Limiting the Period of Continuous Vibration (Recommended)

To prevent physical effects in the user such as numbness as a result of continuous vibration, limit the duration of continuous vibration as indicated below, regardless of the vibration strength.

- Limit the duration of continuous vibration to 1 minute.
- If the nature of the game makes longer periods of continuous vibration unavoidable, limit these periods to 3 minutes.

3.3.6 Rumble Feature Selection (Recommended)

The user should be allowed to set the rumble feature to ON or OFF or to select strong, mild, or OFF by means such as an initial-settings screen at the start of the game. In addition, the program should allow the user to easily change these settings even during a game if, for example, they are uncomfortable with the vibration. Such changes also should be allowed a pause.

3.3.7 Changes in Vibration Level with Battery Use (Recommended)

If the battery that powers the motor (size AAA alkaline battery) wears out, the perceived vibration level will be reduced even if the requested vibration level remains the same. Therefore, rumble operation should be checked both when the battery is new (1.6 V) and when it is at the end of its life (1.1 V).

4. SGB PROGRAMMING CAUTIONS

4.1 ROM Data (Required)

To use the functions of SGB (system commands), the following values must be stored in ROM at the locations indicated.
0x146 ← 0x03, 0x14B ← 0x33

4.2 Default Data (Required)

When writing programs that use the functions of SGB, use the initialization routine of the game program to send default data (see Chapter 6) to the register file.

4.3 SOU_TRN Default Data (Required)

When using the SOU_TRN system command, send the SOU_TRN default data (see Chapter 6) to the register file before SOU_TRN is used.

5. PROGRAMMING CAUTIONS REGARDING POCKET PRINTER

5.1 Transfer Time Intervals (Required)

Transfer time intervals vary depending on the manufacturer. The timings indicated in Chapter 9 should be used to avoid faulty operation with a printer from a particular manufacturer.

5.2 Printing Multiple Sheets Continuously (Recommended)

Between 2 and 255 sheets can be printed continuously by an application. However, because this may take a long time, the user should be given a means of halting a print job in progress.

5.3 Print Density (Recommended)

Because it is very inconvenient to adjust the density each time the program is started, the print density data should be backed up whenever possible.

5.4 Operation After the Motor is Stopped (Required)

If a print instruction packet is sent within 100 msec of when the motor is stopped, the print starting position may be incorrect. Therefore, print instruction packets should always be sent at least 100 msec after the motor is stopped.

5.5 Feeds (Required)

In setting the number of line feeds to be inserted before and after printing (byte 2 of the data portion of the print instruction packet), always specify a value of 1 or greater for the number of feeds before printing and 3 or greater for the number after printing. Otherwise, problems can arise, such as double printing twice on a single line or failure of the last line of print to reach the paper cutter.

5.6 Point of Caution During Debugging (Recommended)

There are two types printers, each made by a different manufacturer (Seiko Instruments and Hosiden). As part of final debugging, the program should be checked with at least one printer of each type.

5.7 Sample Program Provided by Nintendo (Recommended)

Modifying the program to suit the intended use is permitted. However, in creating the original program, values for timing and other parameters were calculated to allow normal operation. These parameters must therefore be carefully considered when modifying the program.

6. PROGRAMMING CAUTIONS FOR U.S. PROGRAMMERS

If you are unable to verify that the system is a Super Game Boy, and the Accumulator returns the same value if the game is inserted in the Super Game Boy or original Game Boy hardware, follow the instructions below.

If your game is Super Game Boy (SGB) enhanced, then you just need to use the MLT_REQ function. Otherwise, you must use the SGB libraries to verify if the game is in an SGB. (These libraries are located in the CGB files section of Wario World under SGBlib.zip.) You will need to call the SGBCHK function from these libraries right after the Soft Reset label. To use this function, you must set the ROM Registration area for SGB ($146h) to $03, which allows access to the SGB REgisters. (Don't forget to readjust the Complement Check.)

Also, on the Software Submission sheet, make sure you note that the game has a $03 in address $146, but in the remarks section, explain that the game doesn't use any of the SGB features.