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CHAPTER 8: GAME BOY MEMORY CONTROLLERS (MBC)

1. MBC1

1.1 Overview

MBC1 is a memory controller that enables the use of 512 Kbits (64 Kbytes) or more of ROM and 256 Kbits (32 Kbytes) of RAM. It can be used as follows.

- To control up to 4 Mbits of ROM
  When used to control up to 4 Mbits (512 Kbytes) of ROM, MBC1 can control up to 256 Kbits (32 Kbytes) of RAM.

- To control 8 Mbits or more of ROM
  When MBC1 is used to control up to 8 MBits (1 MB) or 16 MBits (2 MB) of ROM, the following conditions apply

  - When used to control 8 MBits of ROM
    MCB cannot use ROM addresses 0x080000-0x083FFF (Bank 0x20)

  - When used to control 16 MBits of ROM

    MBC1 cannot use ROM Addresses { 0x8000-0x083FFF (Bank 0x20), x100000-0x103FFF (Bank 0x40), 0x180000-0x183FFF (Bank 0x60) }

  RAM use by MBC1 is restricted to 64 Kbits (8 Kbytes).

1.2 Description of Registers

- Register 0: RAMCS gate data (serves as write-protection for RAM)
  Write addresses: 0x0000-0x1FFF Write data: 0x0A
  Writing 0x0A to 0x0-0x1FFF causes the $\overline{CS}$ to be output, allowing access to RAM.

- Register 1: ROM bank code
  Write addresses: 0x2000-0x3FFF Write data: 0x01-0x1F
  The ROM bank can be selected.

- Register 2: Upper ROM bank code when using 8 Mbits or more of ROM (and register 3 is 0)
  Write addresses: 0x4000-0x5FFF Write data: 0-3
  The upper ROM banks can be selected in 512-Kbyte increments.
  Write value of 0 selects banks 0x01-0x1F
  Write value of 1 selects banks 0x21-0x3F
  Write value of 2 selects banks 0x41-0x5F
  Write value of 3 selects banks 0x61-0x7F

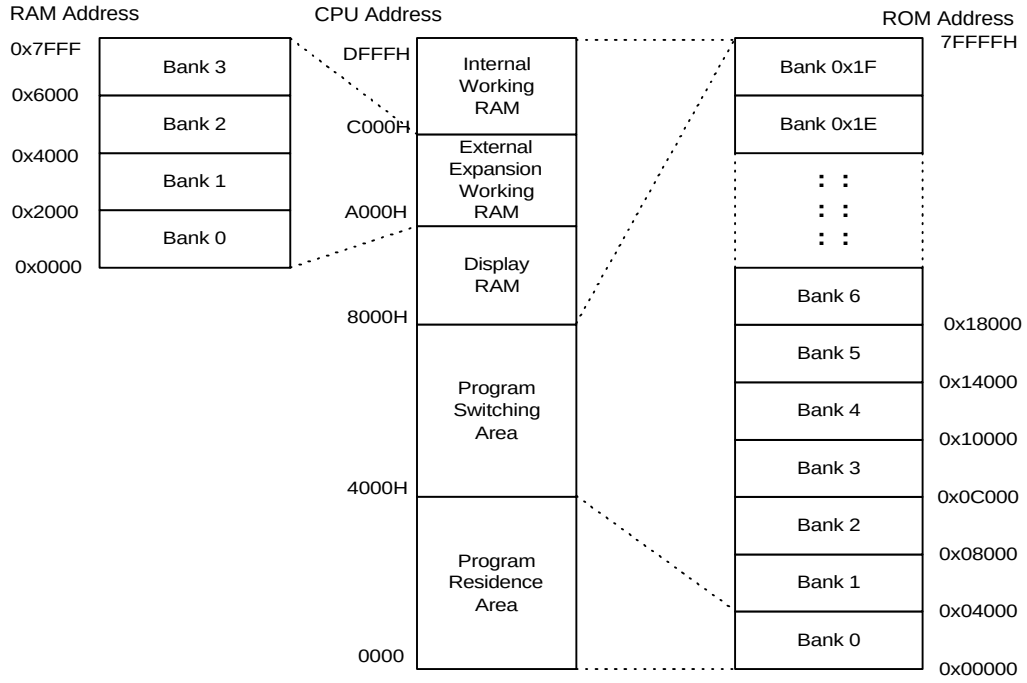
  : RAM bank code when using 256 Kbits of RAM (and register 3 is 1)

  Write addresses: 0x4000-0x5FFF Write data: 0-3
  The RAM bank can be selected in 8-Kbyte increments.

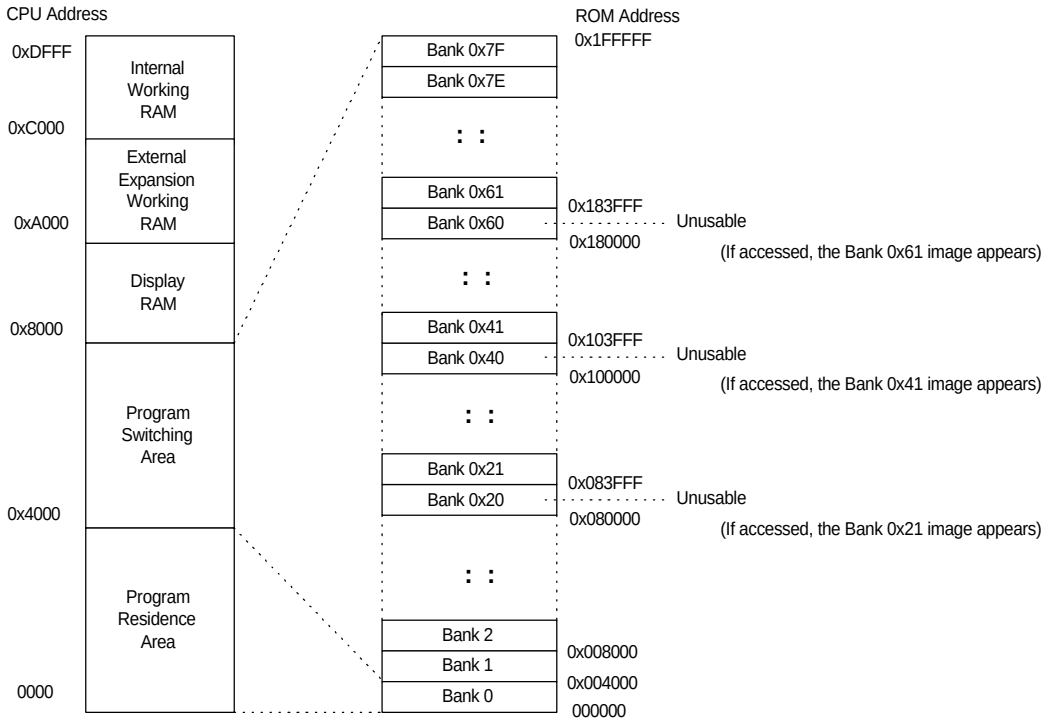
- Register 3: ROM/RAM change
  Write addresses: 0x6000-0x7FFF Write Data: 0-1
  Writing 0 causes the register 2 output to control switching of the higher ROM bank.
  Writing 1 causes the register 2 output to control switching of the RAM bank.

1.3 Memory Map

- When Used to Control up to 4 Mbits of ROM



- When Used to Control up to 8 Mbits of ROM



2. MBC2

2.1 Overview

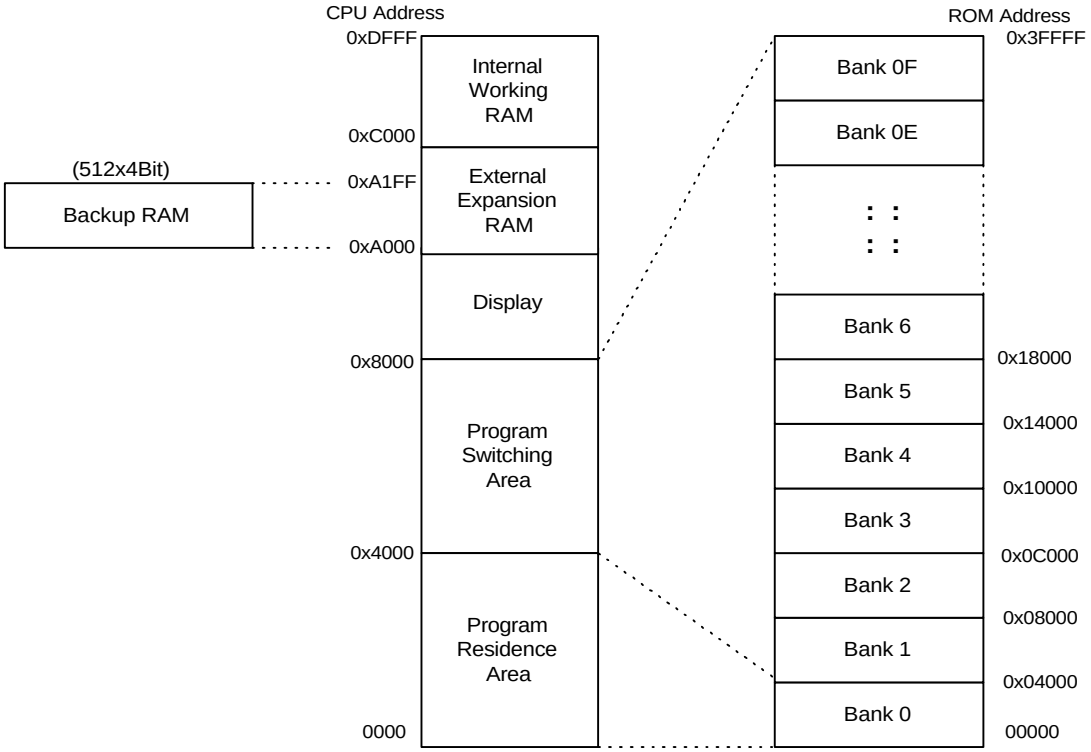
Controller for up to 2 Mbits (256 Kbytes) of ROM with built-in backup RAM (512 x 4 bits).

2.2 Description of Registers

- Register 0: RAMCS gate data (serves as write-protection for RAM)
  Write addresses: 0x000-0x0FFF Write data: 0x0A
  Writing 0x0A to 000-0x0FFF causes the CS to be output, allowing access to RAM.

- Register 1: ROM bank code
  Write addresses: 0x2100-0x21FF Write data: 0x01-0x0F
  The ROM bank can be selected.

2.3 Memory Map



2.4 Backup RAM

Allocated to the D0-D3 areas of CPU addresses 0xA000-0xA1FF
Backup RAM is write-protected by a power-on reset.
To protect backup data, avoid removing write protection unless necessary.

3. MBC3

3.1 Overview

MBC3 is the memory bank controller that allows use of between 512 Kbits (64 Kbytes) and 16 Mbits (2 MB) of ROM and 256 Kbits (32 Kbytes) of RAM.
Built into the controller are clock counters that operate by means of an external crystal oscillator (32.768 KHz). The clock counters are accessed by RAM bank switching.
RAM and clock counter data can be backed up by an external lithium battery.

3.2 Description of Registers

Settings for control registers 0-3 are specified by writing data to the ROM area.

- Register 0: Write protects RAM and the clock counters (default: 0)
  Write addresses: 0x0000-0x1FFF Write data: 0x0A
  Allows access to RAM and the clock counter registers.

- Register 1: ROM bank code (default: 0, selects ROM bank 1)
  Write addresses: 0x2000-0x3FFF Write data: 0x01-0x7F
  Allows the ROM bank to be selected in 16-Kbyte increments.

- Register 2: RAM bank code (default: 0, selects RAM bank 0)
  Write addresses: 0x4000-0x5FFF Write data: 0-3
  Allows the RAM bank to be selected in 8-Kbyte increments.

  Write addresses: 0x4000-0x5FFF Write data: 0x08-0x0C
  Allows a clock counter to be selected.

Data	Register	Range of Values	Function
0x08	RTC_S	0-59 (0-0x3B)	Seconds counter (6 bits)
0x09	RTC_M	0-59 (0-0x3B)	Minutes counter (6 bits)
0x0A	RTC_H	0-23 (0-0x17)	Hours counter (5 bits)
0x0B	RTC_DL	0-255 (0-0xFF)	Lower-order 8 bits of days counter
0x0C	RTC_DH	bit7 bit0 [ ] [ ] 0 0 0 0 0 [ ] Bit 0: Most significant bit of days counter Bit 6: HALT Bit 7: Carry bit of days counter	Higher-order bit and carry bit of days counter. HALT starts and stops the clock counters.

* The days counter consists of a 9-bit counter + a carry bit. Thus, it can count from 0 to 511 (0x000-0x1FF).
* Once the carry bit is set to 1, it remains 1 until 0 is written.
* The counters operate when HALT is 0 and stop when HALT is 1.
* Values outside the given counter ranges will not be correctly written.

- Register 3: Latches the data for all clock counters (default: 0)
  Write addresses: 0x6000-0x7FFF Write Data: 0 → 1
  Writing 0 → 1 causes all counter data to be latched. The latched contents are retained until 0 → 1 is written again.

3.3 Accessing the Clock Counters

The clock counter registers are assigned to the external expansion RAM area of the CPU address space. To access the clock counters, RAM bank switching must first be performed.

External expansion RAM Area (0xA000-0xBFFF) Bank Map

Bank	Device	Notes
0x00	RAM BANK 0	
0x01	RAM BANK 1	
0x02	RAM BANK 2	
0x03	RAM BANK 3	
		Not used
0x08	Seconds counter	
0x09	Minutes counter	
0x0A	Hours counter	
0x0B	Days counter (L)	
0x0C	Days counter (H)	
:		Not used

The following are examples of accessing the clock counters.

3.3.1 Reading

The clock counters are accessed by first writing 0x0A to register 0. This opens the gate used to access the counters. To read clock counter values, write 1 to register 3 to latch the values of all the registers. If the value of register 3 is already 1, first set it to 0 and then to 1. While this register is set to 1, the clock counters will operate but the latched values of all of the clock counters will not change. This allows the clock counters to be read.

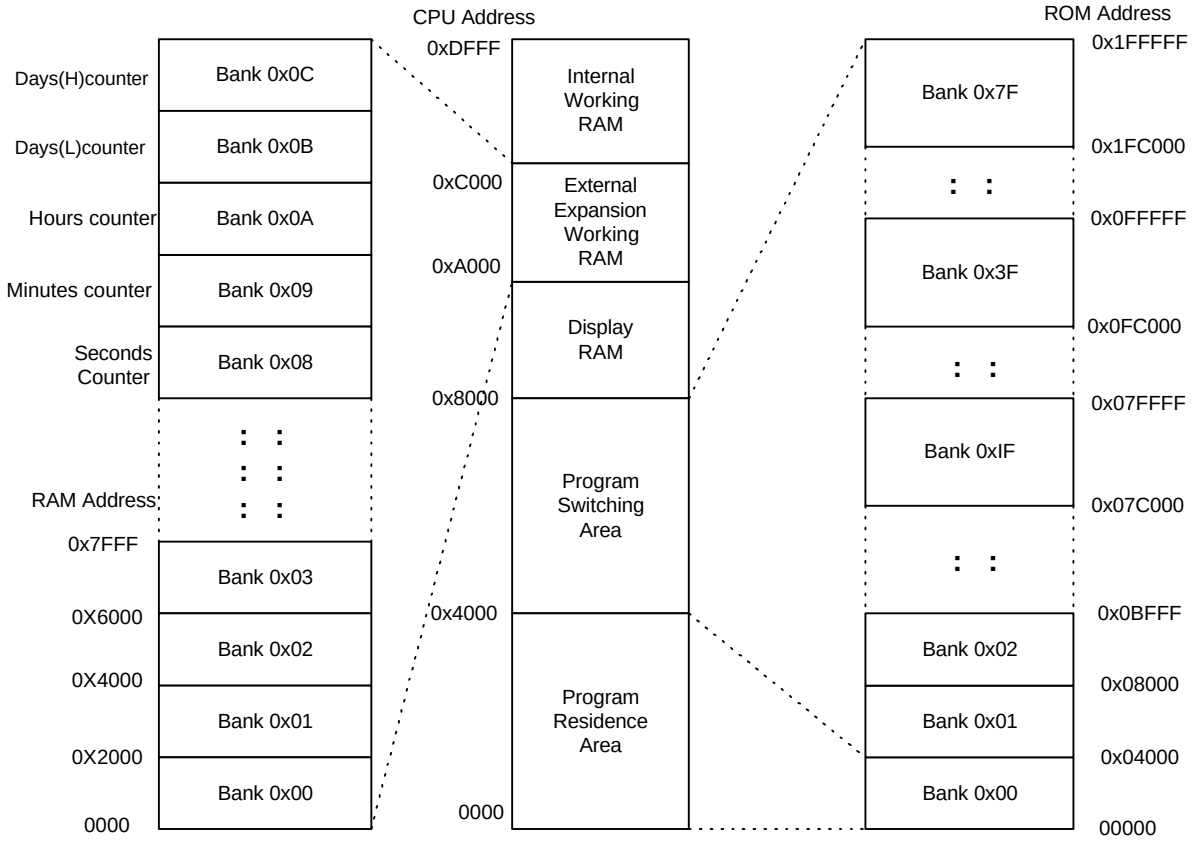
For example, the seconds counter register can be accessed and read by first setting the RAM bank to 8, then reading from any CPU address between 0xA000 and 0xBFFF.

3.3.2 Writing

Writing 0x0A to register 0 opens the access gate, allowing each clock counter register to be written to.

3.4 Memory Map

- ROM bank 0 is assigned to the program residence area (0x0000-0x3FFF) of the CPU memory space (unchangeable).
- One bank from among ROM banks 0x01-0x7F can be assigned to the program switching area (0x4000-0x7FFF) of the CPU memory space.
- One bank from among RAM banks 0-3 and the clock counter registers (RAM banks 0x08-0x0C) can be assigned to the external expansion working RAM area (0xA000-0xBFFF) of the CPU memory space.



3.5 Programming Cautions

3.5.1 Accessing the Clock Counters

Although counting up of the clock counters themselves and accessing the clock counters from the CPU are performed asynchronously, clock counter failure may result if both operations are performed at the same time. To prevent this, MBC3 provides an interface circuit for WR signals from the CPU. Use of this circuit necessitates a delay when accessing control register 3 and the clock counter registers (RTC_S, RTC_M, RTC_H, RTC_DL, and RTC_DH). Thus, whenever accessing these registers consecutively, interpose a delay of 4 cycles between accesses.

When reading clock counter data:

- Latch all clock counter data using control register 3.

4-cycle delay required

- Read the data in the clock counter registers.

When writing values to the clock counters:

- Set data in clock counter register RTC_S.

4-cycle delay required

- Set data in clock counter register RTC_M.

4-cycle delay required

- Set data in clock counter register RTC_H.

4-cycle delay required

- Set data in clock counter register RTC_DL.

4-cycle delay required

- Set data in clock counter register RTC_DH.

3.5.2 Condensation

MBC3 uses a crystal oscillator for its clock counter operation, and condensation on the oscillator may halt its oscillation, preventing the clocks from counting up. Once the condensation disappears, the clocks will resume counting up from where they stopped. However, please ensure that the counter stoppage does not result in a loss of program control.

3.5.3 Control Register Initialization

Although control registers 0-3 are initialized (see Section 3.2, *Description of Registers*) when Game Boy power is turned on, they are not initialized by a hard reset of SNES when Super Game Boy is used. Therefore, please be sure to implement a software reset of these registers.

3.5.4 Clock Counter Registers

When commercial Game Boy software that uses MBC3 is shipped from the factory, the values of the clock counter registers are undefined. Therefore, please ensure that these registers are initialized.

4. MBC5

4.1 Overview

Supports CGB double-speed mode.

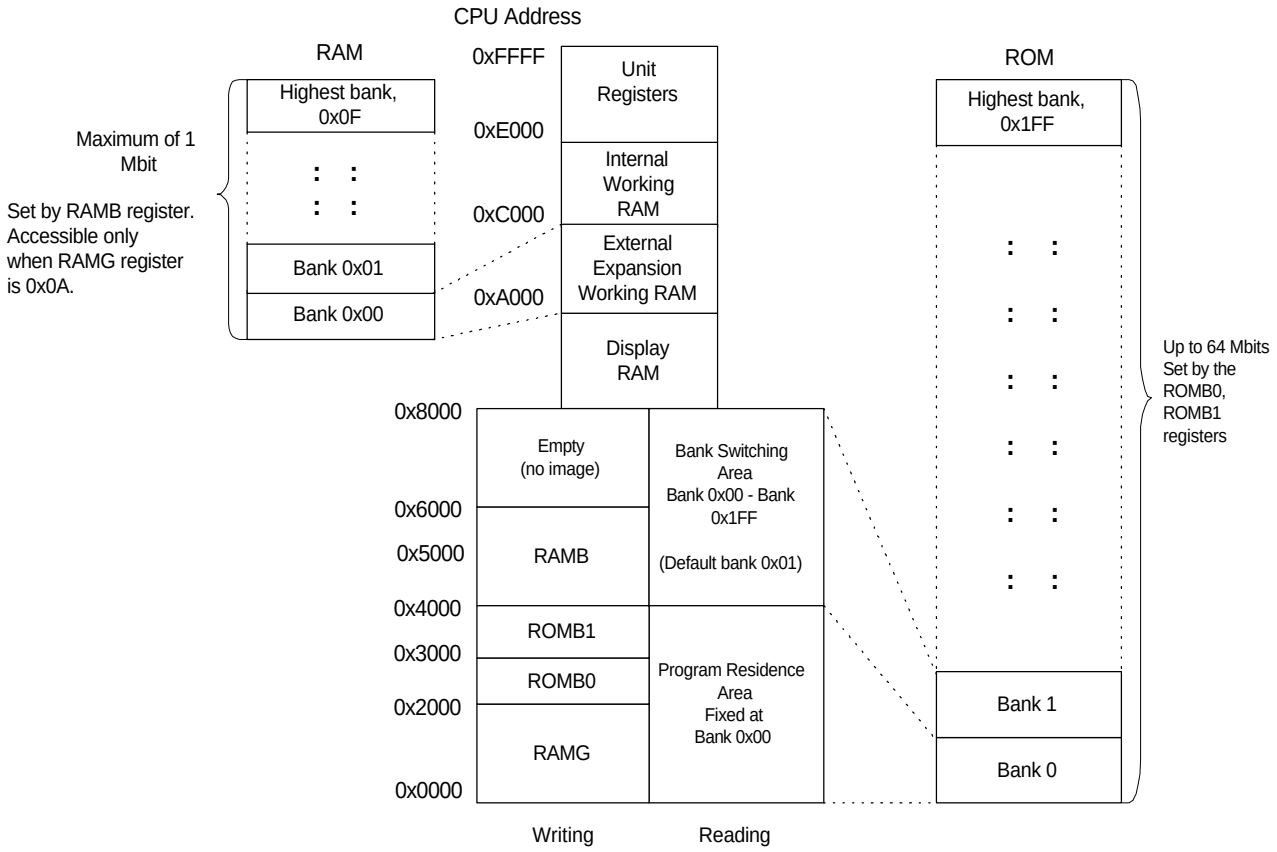
MBC5 can use up to 64 Mbits of ROM (512 banks of 128 bits each) and 1 Mbit of RAM (16 banks of 64 Kbits each).

Upwardly compatible with MBC1.

4.2 Registers

Name	Addresses (hex)
RAMG	0000-1FFF
ROMB 0	2000-2FFF
ROMB 1	3000-3FFF
RAMB	4000-5FFF

4.3 Memory Map

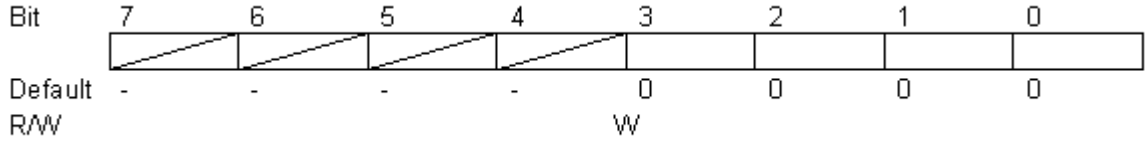


During a write, data is written to the bank control registers at CPU addresses 0x0000-0x7FFF. During a read, the contents of ROM are read from these addresses.

4.4 Description of Registers

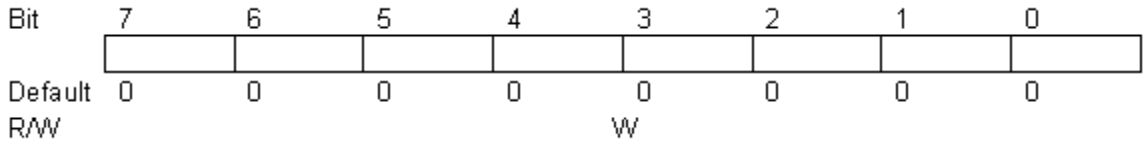
- Register for Specifying External Expansion Memory (RAMG)

  Specifies whether external expansion RAM is accessible. Access to this RAM is enabled by writing 0x0A to the RAMG register space, 0x0000-0x1FFF. Writing any other value to this register disables reading to and writing from RAM.



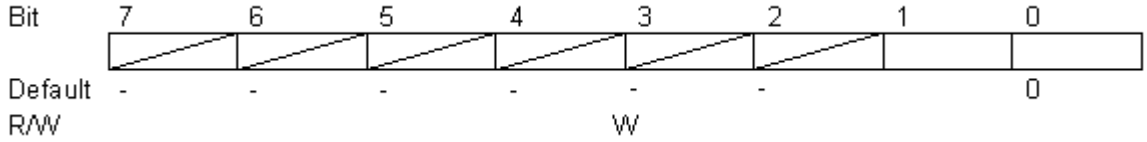
- Lower ROM Bank Register (ROMB0)

  Specifies the lower-order 8 bits of a 9-bit ROM bank.
  The ROM bank can be changed by writing the desired ROM bank number to the ROMB0 register area, 0x2000-0x2FFF.



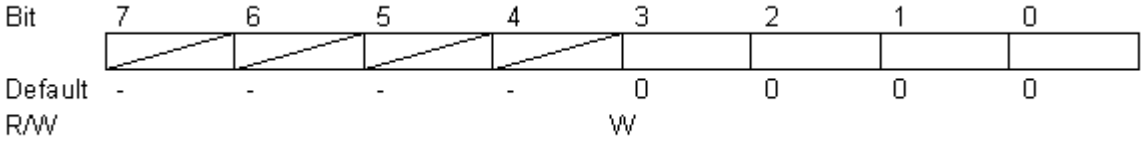
- Upper ROM Bank Register (ROMB1)

  Specifies the higher-order 1 bit of a 9-bit ROM bank.
  The ROM bank can be changed by writing the desired ROM bank number to the ROMB1 register area, 0x3000-0x3FFF.



- RAM Bank Register (RAMB)

  Specifies the RAM bank
  The RAM bank can be changed by writing the desired RAM bank number to the RAMB register area, 0x4000-0x5FFF.



Note	***Although the bits marked with ▨ are ignored by MBC5, they should be used after being set to 0. The default values are set automatically when power is turned on.***

4.5 Programming Cautions

4.5.1 When Migrating from MBC1 to MBC5

- Use of Register 1

  If an MBC1 program uses register 1 (ROM bank control register) addresses 0x3000-0x3FFF, the bank intended for selection by ROMB1 in MBC5 will not be selected.

  Addresses 0x2000-0x2FFF of register 1 should be used by programs that use MBC1.

- Use of Register 2

  Note that in MBC1, programs that use 8 Mbits or more use register 2 (ROM or RAM bank control register) for the high ROM bank. Consequently, in MBC5 the RAM bank is different while the ROM bank is unchanged.

- ROM Banks 0x20, 0x40, and 0x60

  ROM banks 0x20, 0x40, and 0x60 cannot be used in MBC1, but they can be used in MBC5.

- MBC1 Register 3 (ROM/RAM change)

  Because the addresses of ROM and RAM are independent of each other in MBC5, ROM/RAM switching is unnecessary.
  Any write instructions to register3 left in a program that uses MBC1 are ignored by MBC5 and have no effect.

4.5.2 General Notes

- Memory Image

  If a memory device is used that uses less than the maximum amount of memory available (ROM: 64 Mbits; RAM: 1 Mbit) , a memory image is generated for the empty bank area. Therefore, please do not develop software that uses an image, because it may cause failures.

- RAM Data Protection

  To protect RAM data, it is recommended that RAM access be disabled when RAM is not being accessed (RAMG ← 0x00) .

- Specifying External Sound Input (VIN)

  Always use the sound control register (NR50) with bits 7 and 3 (VIN function OFF) set to 0. Because the VIN terminal is used in development flash ROM cartridges, using the register with VIN set to ON will produce sound abnormalities.

4.6 Examples of MBC5 programs on DMG and CGB

- Set the bank switching area (0x4000-0x7FFF) to 0x1FF.

```
LD A,$FF
LD ($2000),A    ;ROMB0 setting
LD A,$01
LD ($3000),A    ;ROMB1 setting
|
|
|
```

- Set the external expansion memory area (0xA000-0xBFFF) to 0x0F.

```
LD A,$0F
LD ($4000),A      ; RAMB setting
LD A,$0A
LD ($0000),A      ; Enable access to RAM
|
|                 } RAM Access Processing
|
LD A,$00
LD ($0000), A     ; Disable access to RAM
```

5. MBC5 (WITH RUMBLE FEATURE)

5.1 Overview

This cartridge is the same as the previous MBC5 cartridge but also includes a rumble motor and size AAA battery to power the motor. The motor is controlled by the program using the MBC5 RAM bank register (RAMB, bit 3).

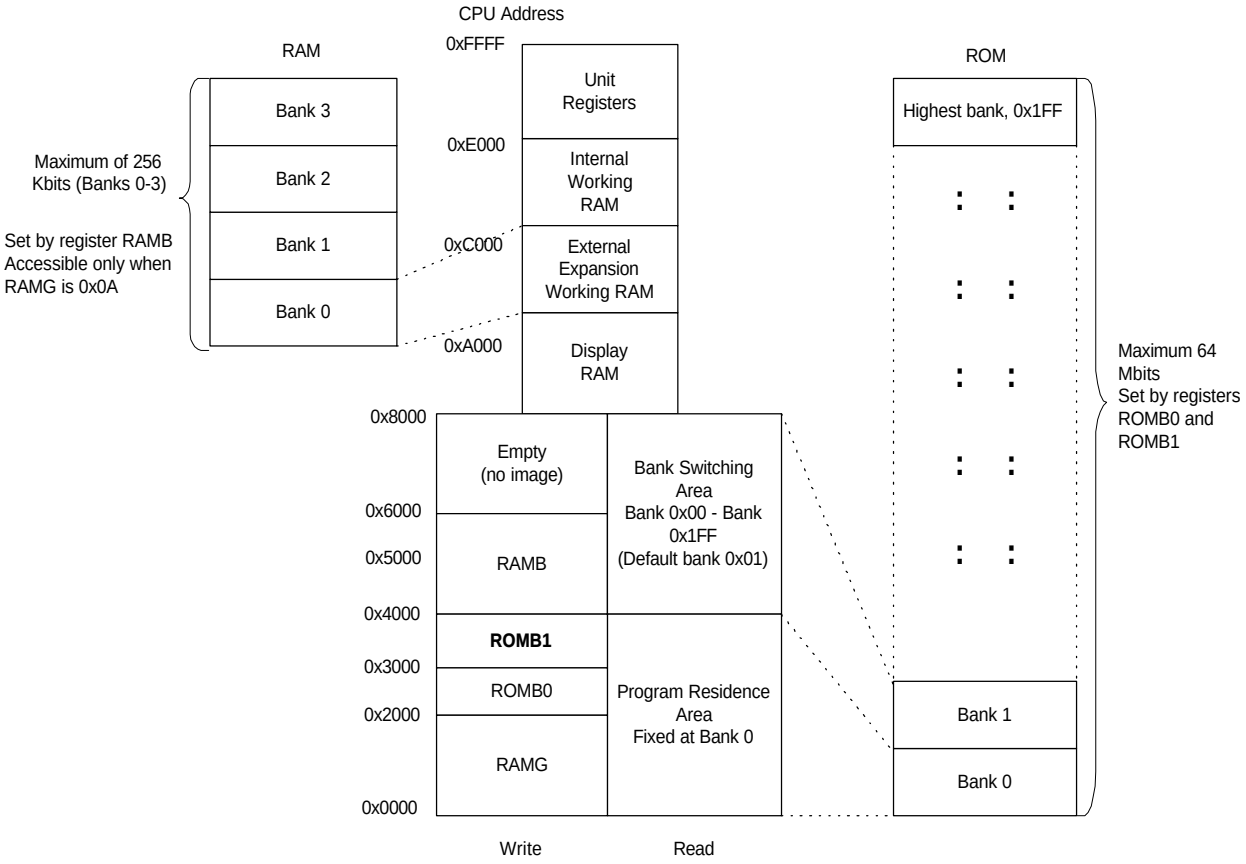
MBC5 supports CGB normal- and double-speed modes.

Up to 64 Mbits (512 banks of 128 Kbits each) of ROM and 256 Kbits of RAM (4 banks of 64 Kbits each) can be used.

5.2 Registers

Name	Addresses (hex)	Notes
RAMG	0000-1FFF	Each register executes its control using any one of the address spaces at left.
ROMB 0	2000-2FFF	
ROMB 1	3000-3FFF	
RAMB	4000-5FFF	

5.3 Memory Map

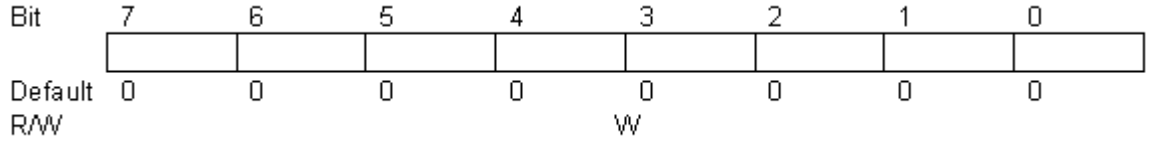


* During a write, data is written to the bank control registers at CPU addresses 0x0000-0x7FFF. During a read, the contents of ROM are read from these addresses.

5.4 Description of Registers

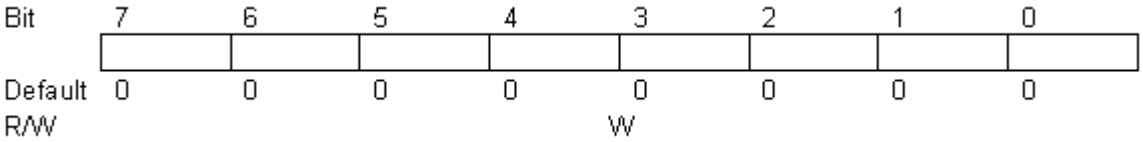
- Register for Specifying External Expansion Memory (RAMG)

  Specifies whether external expansion RAM is accessible. Access to this RAM is enabled by writing 0x0A to the RAMG register (any single address in 0x0000-0x1FFF). Writing any other value to this register disables reading to and writing from RAM.



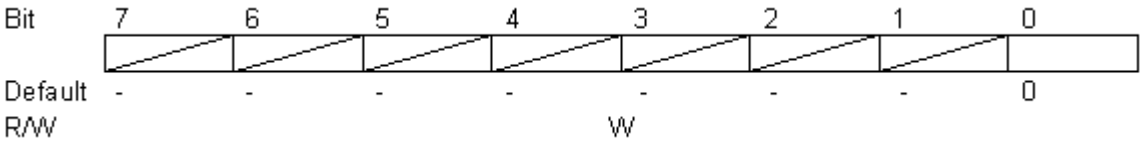
- Lower ROM Bank Register (ROMB0)

  Specifies the lower-order 8 bits of a 9-bit ROM bank.
  The ROM bank can be changed by writing the desired ROM bank number to the ROMB0 register (any single address in 0x2000-0x2FFF).



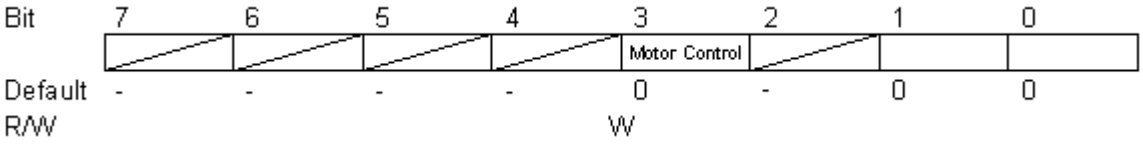
- Upper ROM Bank Register (ROMB1)

  Specifies the higher-order 1 bit of a 9-bit ROM bank.
  The ROM bank can be changed by writing the desired ROM bank number to the ROMB1 register (any single address in 0x3000-0x3FFF).

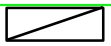


- RAM Bank Register (RAMB)

  Specifies the RAM bank.
  The RAM bank can be changed by writing the desired RAM bank number to the RAMB register (any single address in 0x4000-0x5FFF).



Bits 0-1: Register for RAM bank setting
Bit 3: Motor control register (1: motor ON; 0: motor OFF)

Note	***Be sure to set the bits marked with  to 0 before using them. The default values are set automatically when power is turned on.***

5.5 Motor Control

5.5.1 Vibration Level

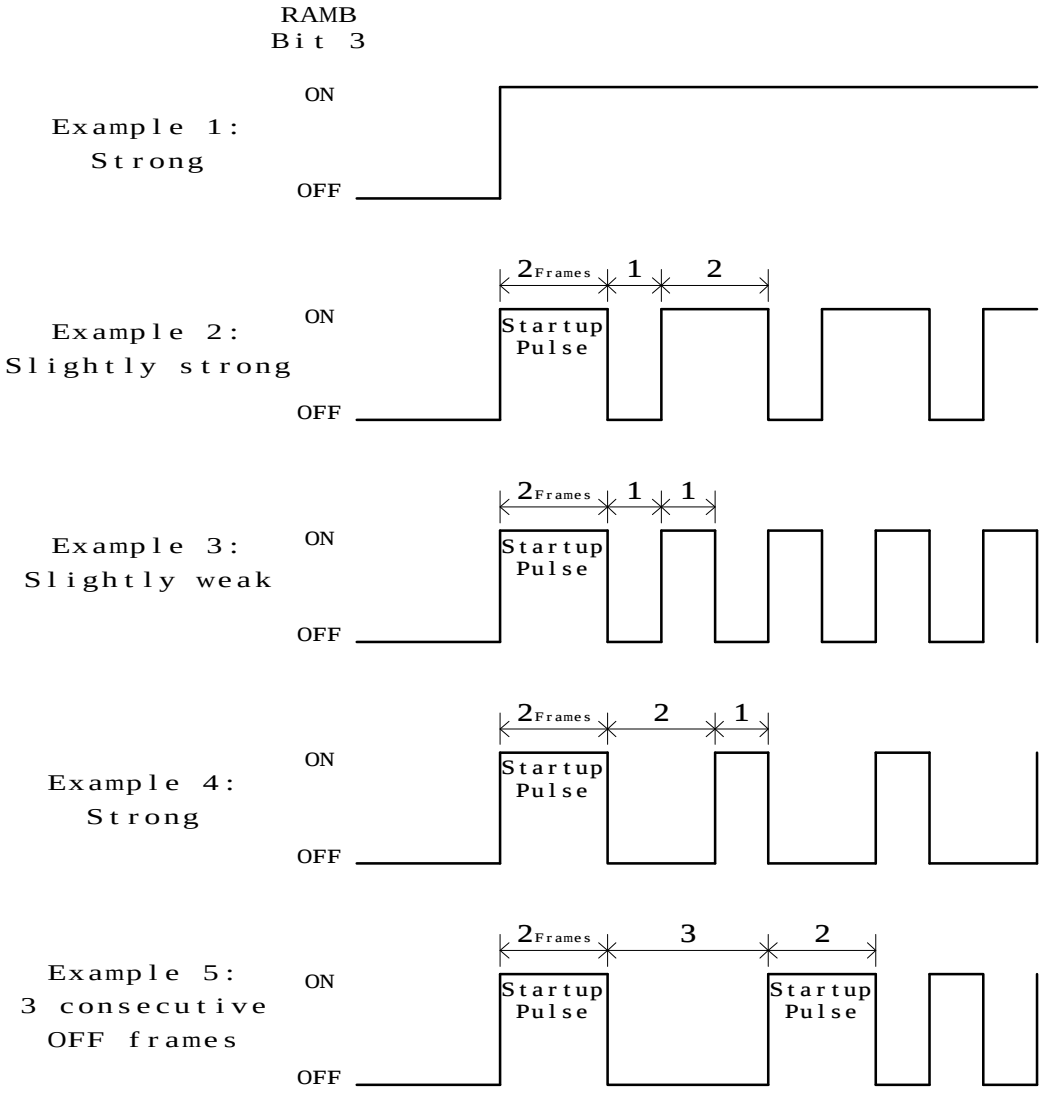
Control of the rumble motor consists of setting it to ON or OFF.
The vibration level can be controlled by sending pulses of combined ON/OFF instructions in short cycles. Please comply with the following points when implementing vibration control.

(1) Set the frame rate to 1 frame per 1/60 second and control vibration frame by frame.

(2) At the start of vibration control, send a startup pulse (at least 2 ON frames).
A startup pulse also should be sent if the width of an OFF pulse is 3 or more consecutive frames. This is necessary because startup from a complete stop requires a certain amount of time.

(see Ex. 5)

5.5.2 Vibration Pulse Examples



5.6 Programming Cautions

IMPORTANT

5.6.1 Memory Image

If a memory device is used that uses less than the maximum amount of memory available (ROM: 64 Mbits; RAM: 256 Kbits) , an empty bank area (memory image) results. Please do not access this empty bank area. Doing so may result in faulty operation.

5.6.2 RAM Data Protection

To protect RAM data, it is recommended that RAM access be disabled (RAMG 0x00) when RAM is not being accessed.

5.6.3 Specifying External Sound Input (VIN)

Always use the sound control register (NR50) with bits 7 and 3 set to 0 (VIN function OFF). Because the VIN terminal is used in development flash ROM cartridges, using the register with VIN set to ON will produce sound abnormalities.

5.6.4 Disabling Vibration Using the SGB, SGB2, or 64GB Pak

When MBC5 is used by SGB, SGB2, or the 64GB Pak, vibration should be turned off by the program to prevent failures caused by a faulty connection. For methods of recognizing SGB and SGB2, see the description of the MLT_REQ command in Chapter 6, Section 3.2, *System Command Details*. With the 64GB Pak, vibration is controlled by the N64 software. Therefore, N64 software programs that support MBC5 should not write data to bit 3 of the RAM bank register.

5.6.5 Limiting the Period of Continuous Vibration

To prevent physical effects in the user such as numbness as a result of continuous vibration, limit the duration of continuous vibration as indicated below, regardless of the vibration strength (see Section 5.5.2, *Vibration Pulse Examples*).

- The duration of continuous vibration should generally be limited to a maximum of 1 minute.
- The period of no vibration between the finish of one period of vibration and the start of the next period generally must be at least as long as the vibration time.

The above points are guidelines that should be followed in most cases. However, if adhering to these guidelines is made difficult by factors such as the game content, take appropriate measures while keeping in mind the points noted in Section 6.7, *Effects of Vibration on the Body*.

5.6.6 Disabling Vibration for Resets and Pauses

Vibration should be halted during resets and pauses.
When power is turned on, the unit should not be vibrated until some input is received from the controller.

5.6.7 Rumble Feature Selection

The user should be allowed to set the rumble feature to ON or OFF or to select strong, mild, or OFF by means such as an initial-settings screen at the start of the game. In addition, the program should allow the user to easily change these settings even during a game if, for example, they are uncomfortable with the vibration. Such changes also should be allowed a pause.

5.6.8 Changes in Vibration Level with Battery Use

If the battery that powers the motor (Size AAA alkaline battery) wears out, the perceived vibration level will be reduced even if the requested vibration level remains the same. Therefore, rumble operation should be checked both when the battery is new (1.6 V) and when it is at the end of its life (1.1 V).

5.7 Physical Effects of Vibration on the Body

Users have occasionally experienced numbness for some time after continuous vibration lasting several tens of seconds to several minutes. This may occur regardless of the strength of the vibration (see Section 5.5.2, *Vibration Pulse Examples*).

Unfortunately, the effects of continuous vibration on the body are not yet clear. Thus, the guidelines presented in Section 5.6.5, *Limiting the Period of Continuous Vibration*, are intended to give priority to user safety. However, software development requires free thinking and original ideas, and there may well be cases in which the use of continuous vibration in a game is desirable.

Because each game is different, the limitations presented in Section 5.6.5 are by their nature not restrictions that should be enforced digitally. It is instead preferable for the developer to adequately consider user safety when determining the game's content.

For example, even supposing that continuous vibration does last for more than 1 minute, it may not pose a safety problem if it is used infrequently, such as only when special events occur. Conversely, if vibrations lasting several seconds to several tens of seconds are repeated at short intervals, the effects on the user may be the same as with continuous, long-term vibration.

Thus, the guidelines presented in Section 5.6.5 are not absolute restrictions. However, even if a program varies from these guidelines, the following points should be considered minimum requirements and strictly observed.

- Continuous vibration should not exceed 3 minutes for any reason.
- Because the effects of continous vibration vary from person to person, the strength of these effects on the user should not be determined independently by the developer. Rather, this determination should be arrived at after considering the opinions of many others during debugging and other phases of development.