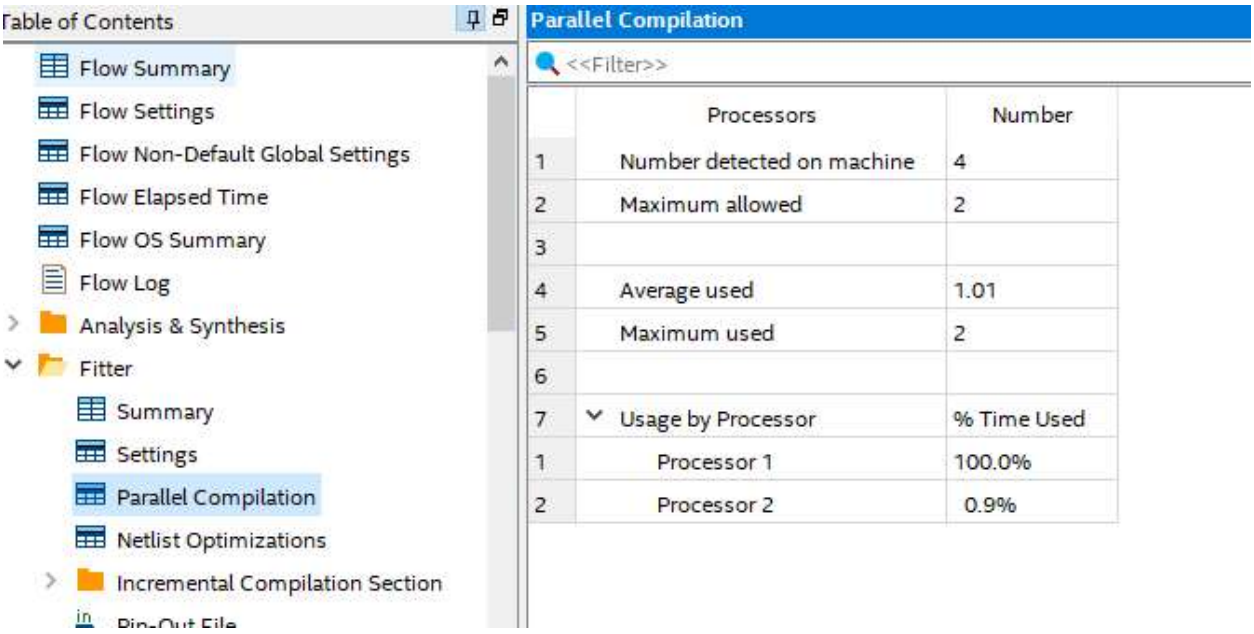
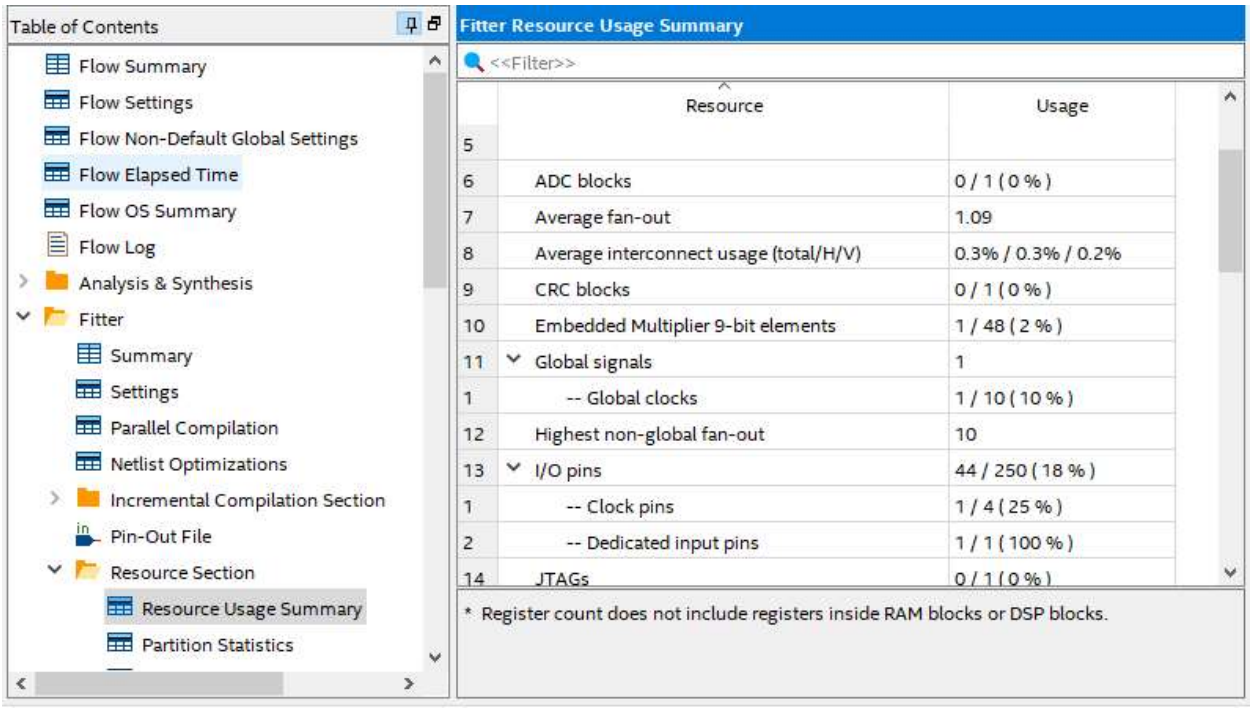
Compilation Report at the end(% utilization) Adolf D'costa

Fitter Status	Successful - Wed Jul 24 03:48:47 2019
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	pipemult2
Top-level Entity Name	pipemult
Family	MAX 10
Device	10M08DAF484C8GES
Timing Models	Preliminary
Total logic elements	6 / 8,064 (< 1 %)
Total registers	21
Total pins	44 / 250 (18 %)
Total virtual pins	0
Total memory bits	512 / 387,072 (< 1 %)
Embedded Multiplier 9-bit elements	1 / 48 (2 %)
Total PLLs	0 / 2 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 1 (0 %)



	Processors	Number
1	Number detected on machine	4
2	Maximum allowed	2
3		
4	Average used	1.01
5	Maximum used	2
6		
7	Usage by Processor	% Time Used
1	Processor 1	100.0%
2	Processor 2	0.9%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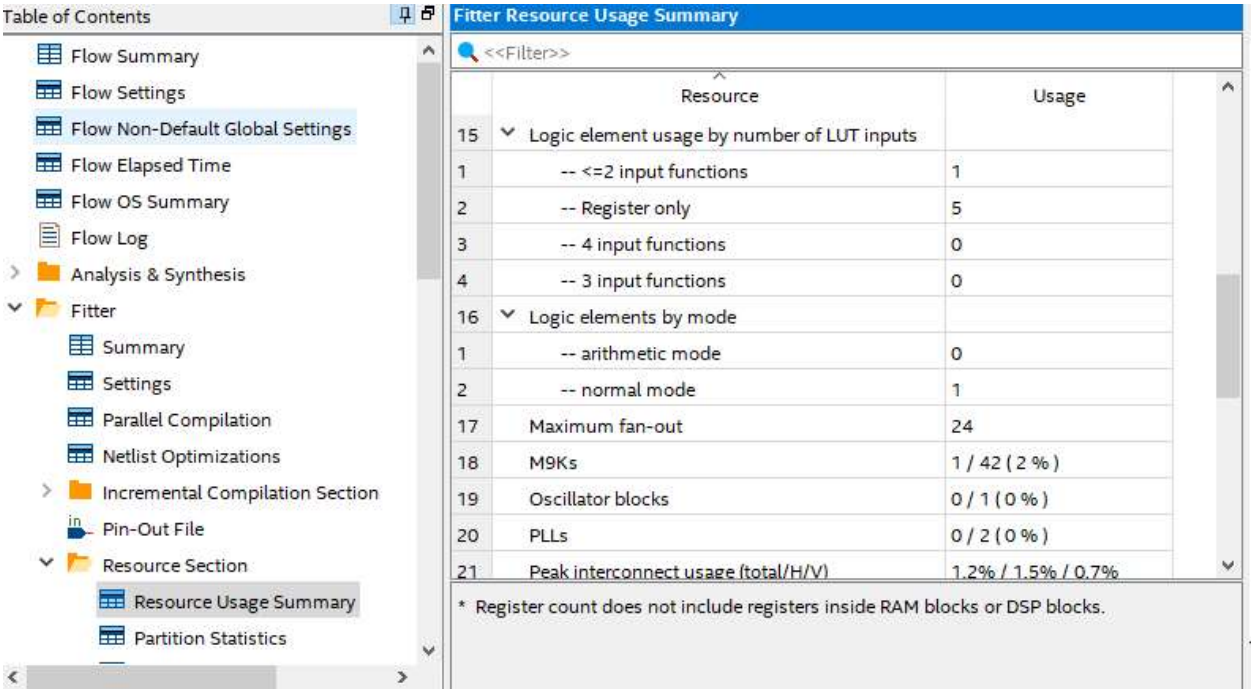
5
6 ADC blocks 0 / 1 (0 %)
7 Average fan-out 1.09
8 Average interconnect usage (total/H/V) 0.3% / 0.3% / 0.2%
9 CRC blocks 0 / 1 (0 %)
10 Embedded Multiplier 9-bit elements 1 / 48 (2 %)
11 Global signals 1
1 -- Global clocks 1 / 10 (10 %)
12 Highest non-global fan-out 10
13 I/O pins 44 / 250 (18 %)
1 -- Clock pins 1 / 4 (25 %)
2 -- Dedicated input pins 1 / 1 (100 %)
14 JTAGs 0 / 1 (0 %)
* Register count does not include registers inside RAM blocks or DSP blocks.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Usage
15 Logic element usage by number of LUT inputs
1 -- <=2 input functions 1
2 -- Register only 5
3 -- 4 input functions 0
4 -- 3 input functions 0
16 Logic elements by mode
1 -- arithmetic mode 0
2 -- normal mode 1
17 Maximum fan-out 24
18 M9Ks 1 / 42 (2 %)
19 Oscillator blocks 0 / 1 (0 %)
20 PLLs 0 / 2 (0 %)
21 Peak interconnect usage (total/H/V) 1.2% / 1.5% / 0.7%
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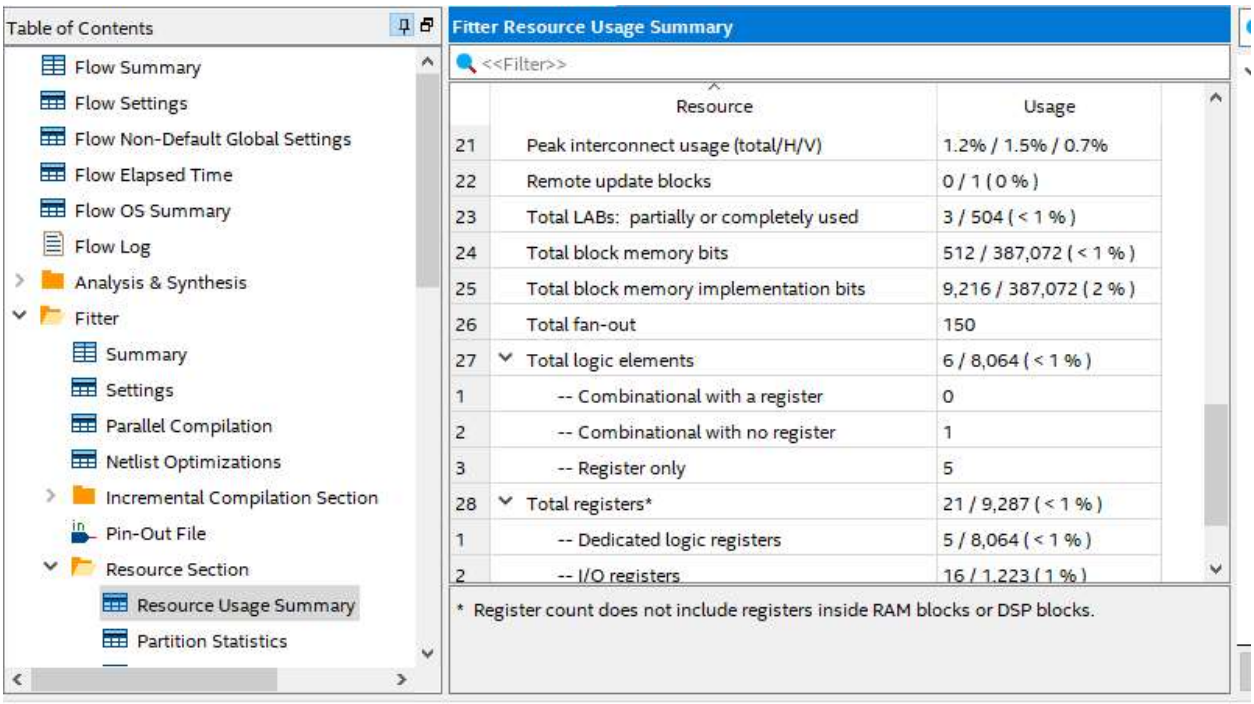
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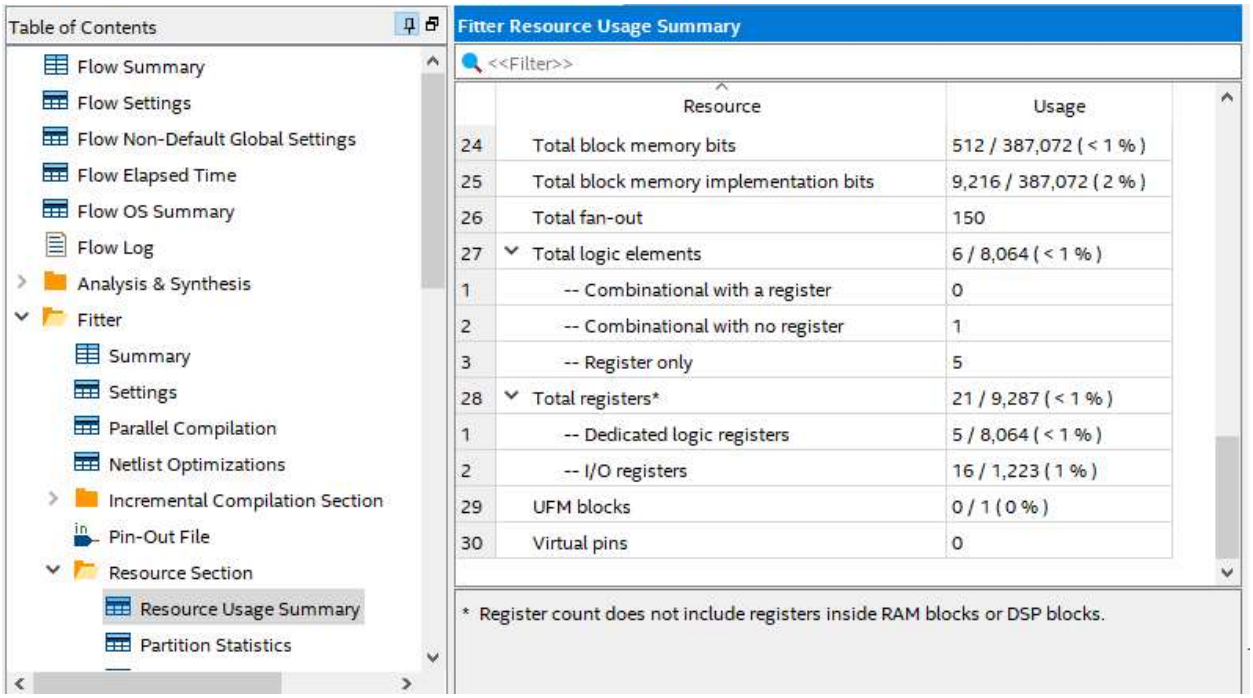
Usage
21 Peak interconnect usage (total/H/V) 1.2% / 1.5% / 0.7%
22 Remote update blocks 0 / 1 (0 %)
23 Total LABs: partially or completely used 3 / 504 (< 1 %)
24 Total block memory bits 512 / 387,072 (< 1 %)
25 Total block memory implementation bits 9,216 / 387,072 (2 %)
26 Total fan-out 150
27 Total logic elements 6 / 8,064 (< 1 %)
1 -- Combinational with a register 0
2 -- Combinational with no register 1
3 -- Register only 5
28 Total registers* 21 / 9,287 (< 1 %)
1 -- Dedicated logic registers 5 / 8,064 (< 1 %)
2 -- I/O registers 16 / 1,223 (1 %)
* Register count does not include registers inside RAM blocks or DSP blocks.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3 -- Register only 5
28 Total registers* 21 / 9,287 (< 1 %)
1 -- Dedicated logic registers 5 / 8,064 (< 1 %)
2 -- I/O registers 16 / 1,223 (1 %)
29 UFM blocks 0 / 1 (0 %)
30 Virtual pins 0
* Register count does not include registers inside RAM blocks or DSP blocks.