

## Compilation Report at the end (Fmax)

Adolf D'costa

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Slow 1200mV 85C Model Fmax Summary

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	Fmax	Restricted Fmax	Clock Name	Note
1	128.21 MHz	128.21 MHz	clk1	

This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of

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Slow 1200mV 85C Model Setup Summary

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	Clock	Slack	End Point TNS
1	clk1	0.200	0.000

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	Clock	Slack	End Point TNS
1	clk1	0.472	0.000