Espelhos de corrente (Current Mirrors)

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Espelho de corrente

- Apresentam diversas vantagens em relação a amplificadores de um ramo:

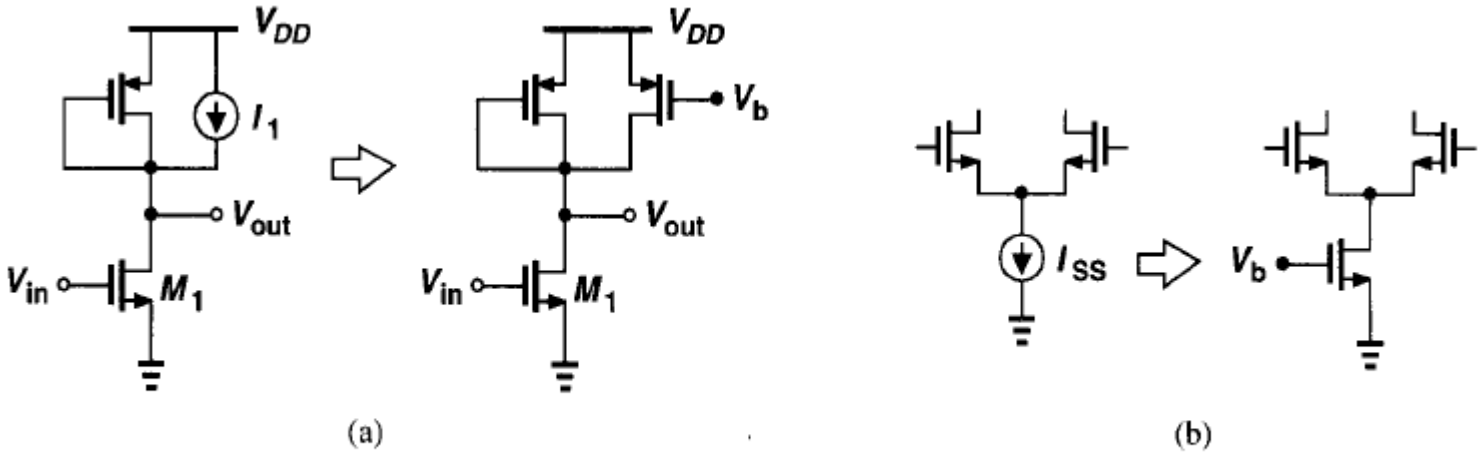


Figure 5.1 Applications of current sources.

Espelho de corrente

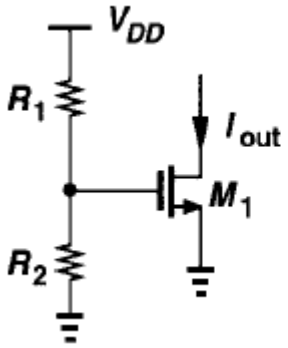


Figure 5.2 Definition of current by resistive divider.

Espelho de corrente

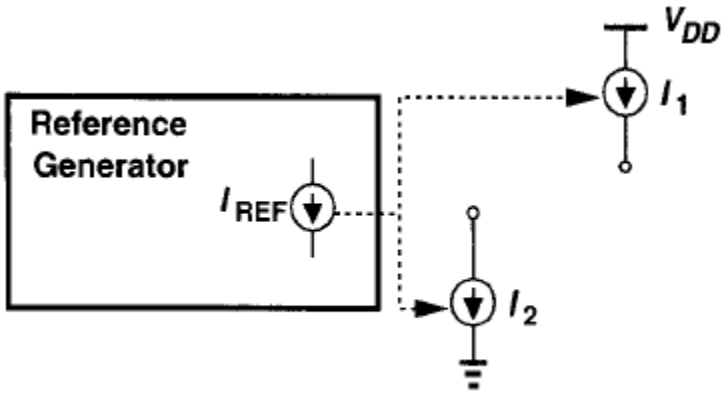


Figure 5.3 Use of a reference to generate various currents.

Espelho de corrente

$$I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2$$

$$I_{out} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2,$$

$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF}.$$

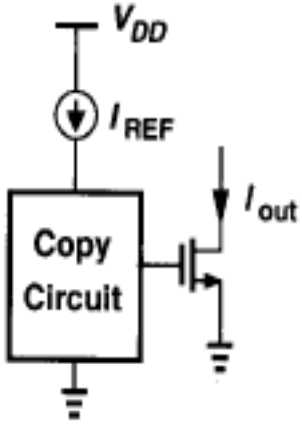
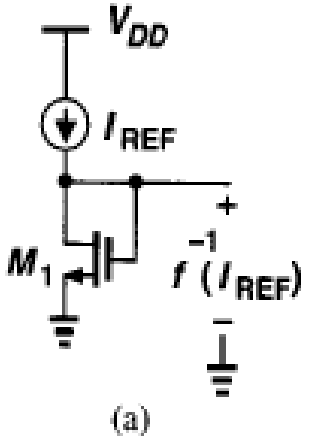


Figure 5.4 Conceptual means of copying currents.



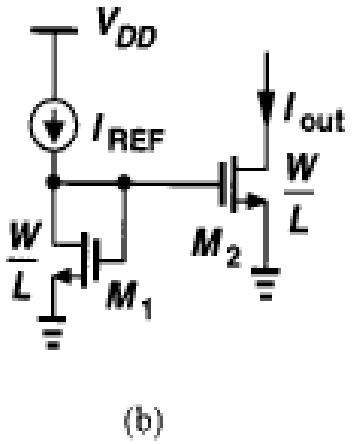


Figure 5.5 (a) Diode-connected device providing inverse function, (b) basic current mirror.

Espelho de corrente

Example 5.1

In Fig. 5.6, find the drain current of M_4 if all of the transistors are in saturation.

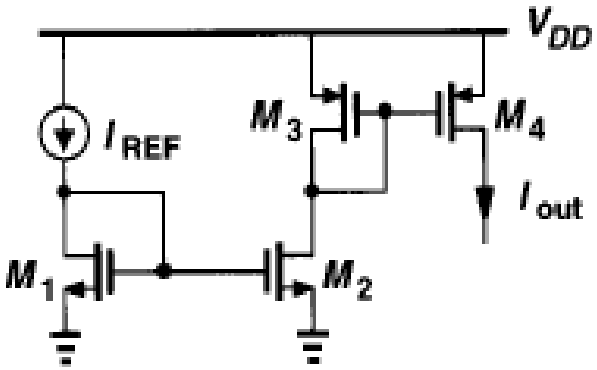


Figure 5.6

Solution

We have $I_{D2} = I_{REF}[(W/L)_2/(W/L)_1]$. Also, $|I_{D3}| = |I_{D2}|$ and $I_{D4} = I_{D3}[(W/L)_4/(W/L)_3]$. Thus, $|I_{D4}| = \alpha\beta I_{REF}$, where $\alpha = (W/L)_2/(W/L)_1$ and $\beta = (W/L)_4/(W/L)_3$. Proper choice of α and β can establish large or small ratios between I_{D4} and I_{REF}. For example, $\alpha = \beta = 5$ yields a magnification factor of 25. Similarly, $\alpha = \beta = 0.2$ can be utilized to generate a small, well-defined current.

Espelho de corrente

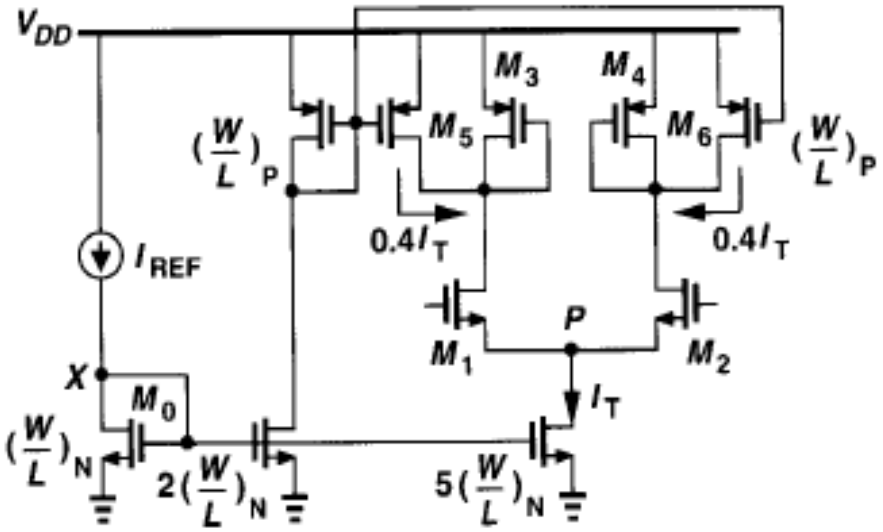


Figure 5.7 Current mirrors used to bias a differential amplifier.

Espelho de corrente

Example 5.2

Calculate the small-signal voltage gain of the circuit shown in Fig. 5.8.

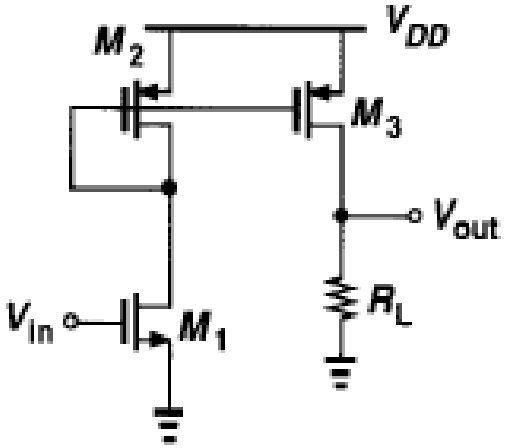


Figure 5.8

Solution

The small-signal drain current of M_1 is equal to $g_{m1}V_{in}$. Since $I_{D2} = I_{D1}$ and $I_{D3} = I_{D2}(W/L)_3/(W/L)_2$, the small-signal drain current of M_3 is equal to $g_{m1}V_{in}(W/L)_3/(W/L)_2$, yielding a voltage gain of $g_{m1}R_L(W/L)_3/(W/L)_2$.

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$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2(1 + \lambda V_{DS1})$$

$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2(1 + \lambda V_{DS2}),$$

$$\frac{I_{D2}}{I_{D1}} = \frac{(W/L)_2}{(W/L)_1} \cdot \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}.$$

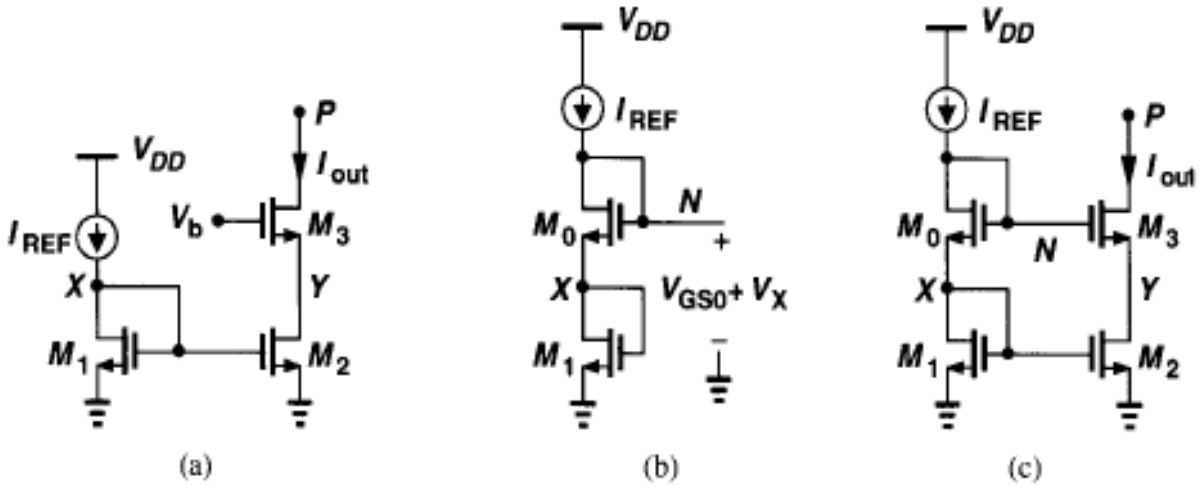

Figure 5.9 (a) Cascode current source, (b) modification of mirror circuit to generate the cascode bias voltage, (c) cascode current mirror.

Cascode Current-mirrors

Example 5.3

In Fig. 5.10, sketch V_X and V_Y as a function of I_{REF}. If I_{REF} requires 0.5 V to operate as a current source, what is its maximum value?

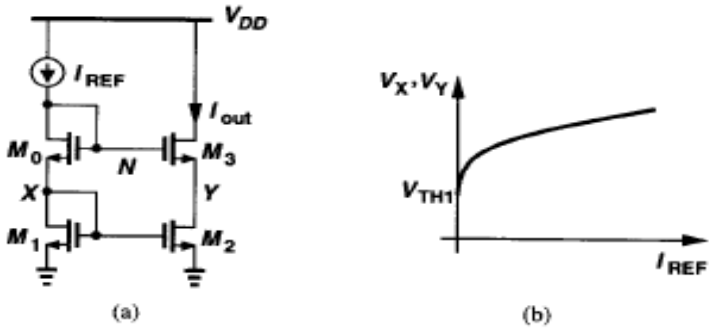

Figure 5.10

Solution

Since M_2 and M_3 are properly ratioed with respect to M_1 and M_0, we have $V_Y = V_X \approx \sqrt{2I_{REF}/[\mu_n C_{ox}(W/L)_1]} + V_{TH1}$. The behavior is plotted in Fig. 5.10(b).

To find the maximum value of I_{REF}, we note that

$$V_N = V_{GS0} + V_{GS1} \tag{5.8}$$

$$= \sqrt{\frac{2I_{REF}}{\mu_n C_{ox}}}\left[\sqrt{\left(\frac{L}{W}\right)_0} + \sqrt{\left(\frac{L}{W}\right)_1}\right] + V_{TH0} + V_{TH1}. \tag{5.9}$$

Thus,

$$V_{DD} - \sqrt{\frac{2I_{REF}}{\mu_n C_{ox}}}\left[\sqrt{\left(\frac{L}{W}\right)_0} + \sqrt{\left(\frac{L}{W}\right)_1}\right] - V_{TH0} - V_{TH1} = 0.5\ \text{V}. \tag{5.10}$$

and hence

$$I_{REF,max} = \frac{\mu_n C_{ox}}{2}\frac{(V_{DD} - 0.5\ \text{V} - V_{TH0} - V_{TH1})^2}{(\sqrt{(L/W)_0} + \sqrt{(L/W)_1})^2}. \tag{5.11}$$

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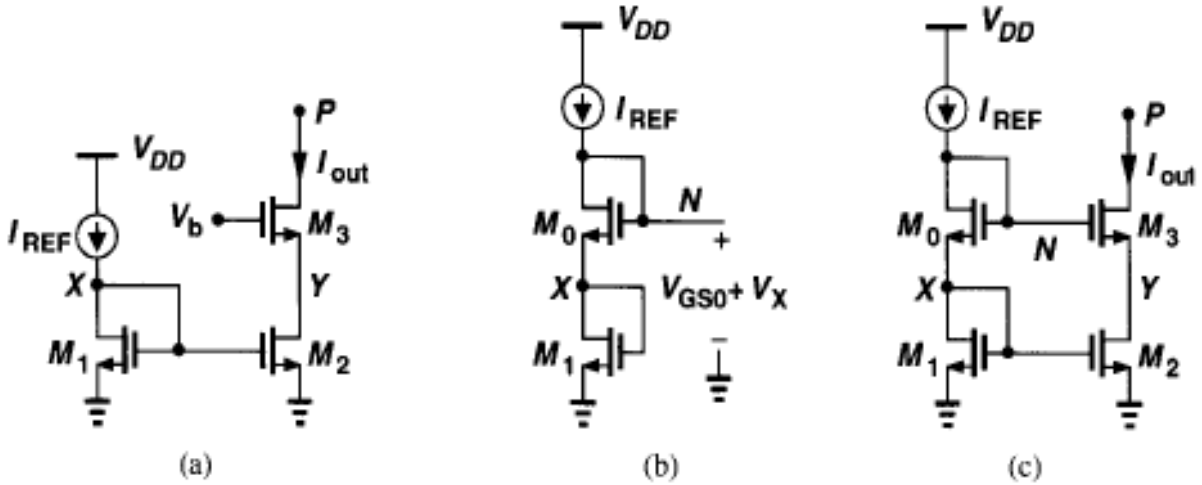

Figure 5.9 (a) Cascode current source, (b) modification of mirror circuit to generate the cascode bias voltage, (c) cascode current mirror.

minimum allowable voltage at node P is equal to

$$V_N - V_{TH} = V_{GS0} + V_{GS1} - V_{TH} \tag{5.12}$$

$$= (V_{GS0} - V_{TH}) + (V_{GS1} - V_{TH}) + V_{TH}. \tag{5.13}$$

i.e., two overdrive voltages plus one threshold voltage. How does this value compare with that in Fig. 5.9(a) if V_b could be chosen more arbitrarily? As shown in Fig. 3.51, V_b could be so low that the minimum allowable voltage at P is merely two overdrive voltages. Thus, the cascode mirror of Fig. 5.9(c) "wastes" one threshold voltage in the headroom. This is because $V_{DS2} = V_{GS2}$, whereas V_{DS2} could be as low as $V_{GS2} - V_{TH}$ while maintaining M_2 in saturation.

Cascode Current-mirrors

Fig. 5.11 summarizes our discussion. In Fig. 5.11(a), V_b is chosen to allow the lowest possible value of V_P but the output current does not accurately track I_{REF} because M_1 and M_2 sustain unequal drain-source voltages. In Fig. 5.11(b), higher accuracy is achieved but the minimum level at P is higher by one threshold voltage.

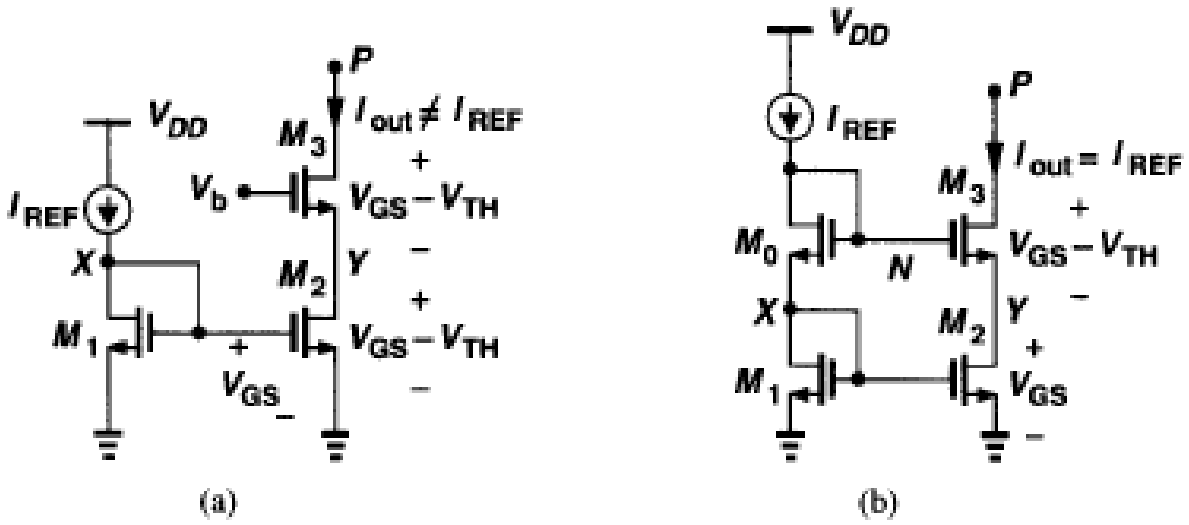

Figure 5.11 (a) Cascode current source with minimum headroom voltage, (b) headroom consumed by a cascode mirror.

Before resolving this issue, it is instructive to examine the large-signal behavior of a cascode current source.

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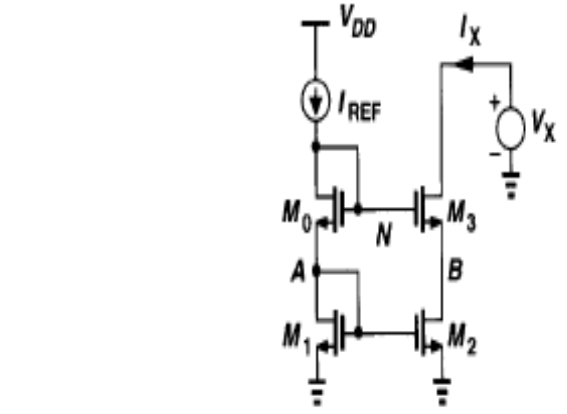
Example 5.4

In Fig. 5.12(a), assuming all of the transistors are identical, sketch I_X and V_B as V_X drops from a large positive value.

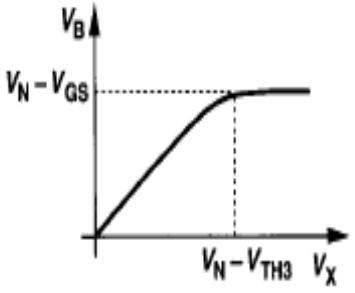
Solution

For $V_X \geq V_N - V_{TH}$, both M_2 and M_3 are in saturation, $I_X = I_{REF}$ and $V_B = V_A$. As V_X drops, which transistor enters the triode region first, M_3 or M_2? Suppose M_2 enters the triode region before M_3 does. For this to occur, V_{DS2} must drop and, since V_{GS2} is constant, so must I_{D2}. This means V_{GS3} increases while I_{D3} decreases, which is not possible if M_3 is still in saturation. Thus, M_3 enters the triode region first.

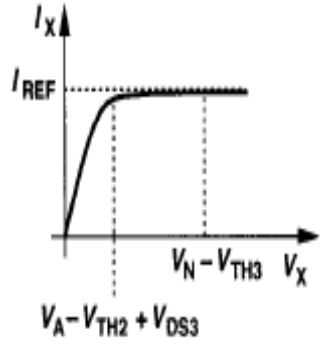
As V_X falls below $V_N - V_{TH}$, M_3 enters the triode region, requiring a greater gate-source overdrive to carry the same current. Thus, as shown in Fig. 5.12(b), V_B begins to drop, causing I_{D2} and hence I_X to decrease slightly. As V_X and V_B decrease further, eventually we have $V_B < V_A - V_{TH}$, and M_2 enters the triode region. At this point, I_{D2} begins to drop sharply. For $V_X = 0$, $I_X = 0$, and M_2 and M_3 operate in deep triode region. Note that as V_X drops below $V_N - V_{TH3}$, the output impedance of the cascode falls rapidly because g_{m3} degrades in the triode region.



(a)



(b)



(c)

Figure 5.12

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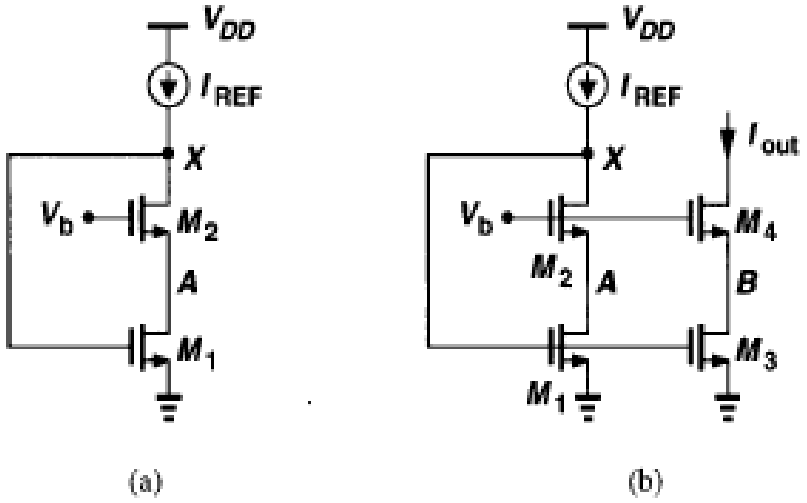

Figure 5.13 Modification of cascode mirror for low-voltage operation.

In order to eliminate the accuracy-headroom trade-off described above, we first study the modification depicted in Fig. 5.13(a). Note that this circuit is in fact a cascode topology with its output shorted to its input. How can we choose V_b so that both M_1 and M_2 are in saturation? We must have $V_b - V_{TH2} \leq V_X (= V_{GS1})$ for M_2 to be saturated and $V_{GS1} - V_{TH1} \leq V_A (= V_b - V_{GS2})$ for M_1 to be saturated. Thus,

$$V_{GS2} + (V_{GS1} - V_{TH1}) \leq V_b \leq V_{GS1} + V_{TH2}. \tag{5.14}$$

A solution exists if $V_{GS2} + (V_{GS1} - V_{TH1}) \leq V_{GS1} + V_{TH2}$, i.e., if $V_{GS2} - V_{TH2} \leq V_{TH1}$. We must therefore size M_2 such that its overdrive voltage remains less than one threshold voltage.

Cascode Current-mirrors

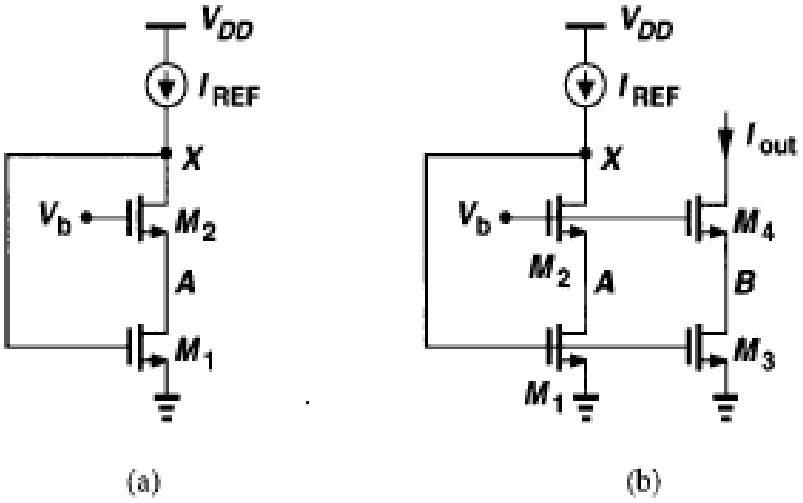

Figure 5.13 Modification of cascode mirror for low-voltage operation.

Now consider the circuit shown in Fig. 5.13(b), where all of the transistors are in saturation and proper ratioing ensures that $V_{GS2} = V_{GS4}$. If $V_b = V_{GS2} + (V_{GS1} - V_{TH1}) = V_{GS4} + (V_{GS3} - V_{TH3})$, then the cascode current source M_3-M_4 consumes minimum headroom (the overdrive of M_3 plus that of M_4) while M_1 and M_3 sustain equal drain-source voltages, allowing accurate copying of I_{REF}. We call this a "low-voltage cascode."

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We must still generate V_b. For minimal voltage headroom consumption, $V_A = V_{GS1} - V_{TH1}$ and hence V_b must be equal to (or slightly greater than) $V_{GS2} + (V_{GS1} - V_{TH1})$. Fig. 5.14(a) depicts an example, where M_5 generates $V_{GS5} \approx V_{GS2}$ and M_6 together with R_b produces $V_{DS6} = V_{GS6} - R_b I_1 \approx V_{GS1} - V_{TH1}$. Some inaccuracy nevertheless arises because M_5 does not suffer from body effect whereas M_2 does. Also, the magnitude of $R_b I_1$ is not well-controlled.

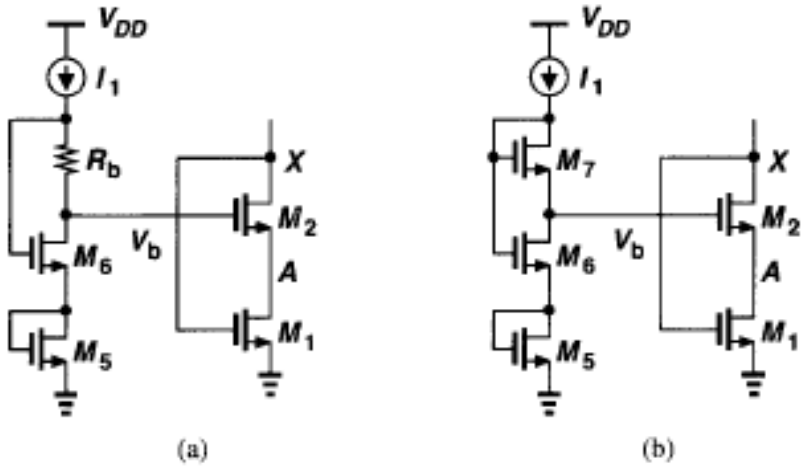

Figure 5.14 Generation of gate voltage V_b for cascode mirrors.

An alternative circuit is shown in Fig. 5.14(b), where the diode-connected transistor M_7 has a large W/L so that $V_{GS7} \approx V_{TH7}$. That is, $V_{DS6} \approx V_{GS6} - V_{TH7}$ and hence $V_b = V_{GS5} + V_{GS6} - V_{TH7}$. While requiring no resistors, this circuit nonetheless suffers from similar errors due to body effect. Some margin is therefore necessary to ensure M_1 and M_2 remain in saturation.

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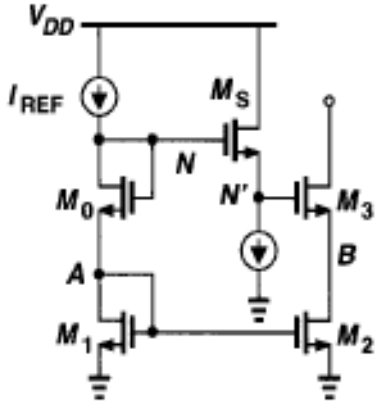


Figure 5.15 Low-voltage cascode using a source follower level shifter.

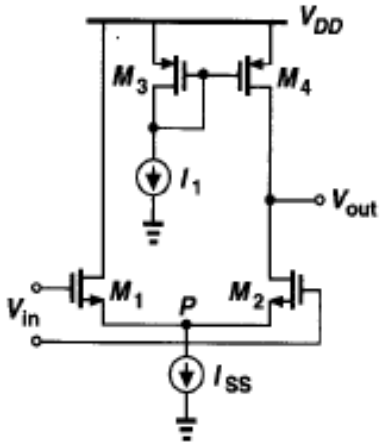
We should mention that low-voltage cascodes can also be biased using source followers. Shown in Fig. 5.15, the idea is to shift the gate voltage of M_3 down with respect to V_N by interposing a source follower. If M_S is biased at a very low current density, $I_D/(W/L)$, then its gate-source voltage is approximately equal to V_{TH3}, i.e., $V_{N'} \approx V_N - V_{TH3}$, and

$$V_B = V_{GS1} + V_{GS0} - V_{TH3} - V_{GS3} \tag{5.15}$$

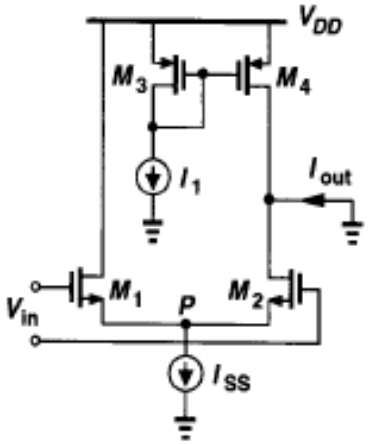
$$= V_{GS1} - V_{TH3}, \tag{5.16}$$

implying that M_2 is at the edge of the triode region. In this topology, however, $V_{DS2} \neq V_{DS1}$, introducing substantial mismatch. Also, if the body effect is considered for M_0, M_S, and M_3, it is difficult to guarantee that M_2 operates in saturation. We should mention that, in addition to reducing the systematic mismatch due to channel-length modulation, the cascode structure also provides a high output impedance.

Active Current-mirrors



(a)



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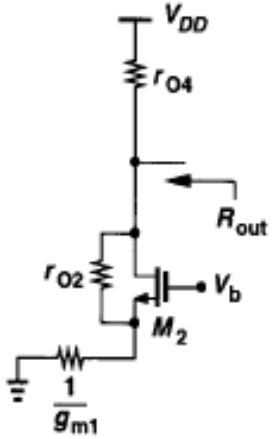


(c)

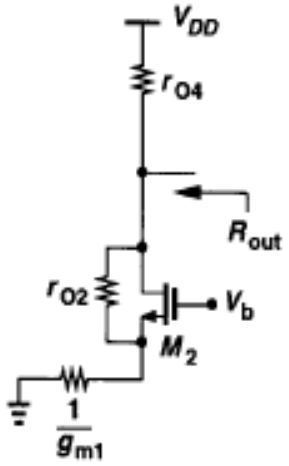
Figure 5.17 (a) Differential pair with current-source load, (b) circuit for calculation of G_m, (c) circuit for calculation of R_{out}.

Active Current-mirrors

Writing $|A_v| = G_m R_{out}$ and recognizing from Fig. 5.17(b) that $G_m = I_{out}/V_{in} = (g_{m1}V_{in}/2)/V_{in} = g_{m1}/2$, we simply need to compute R_{out}. As illustrated in Fig. 5.17(c), for this calculation, M_2 is degenerated by the source output impedance, $1/g_{m1}$, of M_1, thereby exhibiting an output impedance equal to $(1 + g_{m2}r_{O2})(1/g_{m1,2}) + r_{O2} = 2r_{O2} + 1/g_{m1} \approx 2r_{O2}$. Thus, $R_{out} \approx (2r_{O2})\|r_{O4}$, and

$$|A_v| \approx \frac{g_{m1}}{2}[(2r_{O2})\|r_{O4}]. \tag{5.17}$$

Interestingly, if $r_{O4} \to \infty$, then $A_v \to g_{m1}r_{O2}$. This can be explained by the second approach.



(c)

Active Current-mirrors

Interestingly, if $r_{O4} \to \infty$, then $A_v \to g_{m1} r_{O2}$. This can be explained by the second approach.

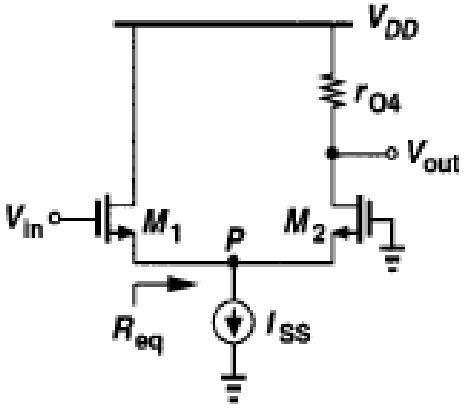


Figure 5.18 Circuit for calculation of V_P/V_{in}.

$$R_{eq} \approx \frac{1}{g_{m2}} + \frac{r_{O4}}{g_{m2} r_{O2}}$$

$$= \frac{1}{g_{m2}} \left(1 + \frac{r_{O4}}{r_{O2}}\right).$$

In our second approach, we calculate V_P/V_{in} and V_{out}/V_P and multiply the results to obtain V_{out}/V_{in}. With the aid of Fig. 5.18,

$$\frac{V_P}{V_{in}} = \frac{R_{eq}}{R_{eq} + \frac{1}{g_{m1}}}, \qquad (5.18)$$

where R_{eq} denotes the resistance seen looking into the source of M_2. Since the drain of M_2 is terminated by a relatively large resistance, r_{O4}, the value of R_{eq} must be obtained from Eq. (3.110):

$$\frac{V_P}{V_{in}} = \frac{1 + \frac{r_{O4}}{r_{O2}}}{2 + \frac{r_{O4}}{r_{O2}}}.$$

Note that if $r_{O4} \to 0$, $V_P/V_{in} \to 1/2$ and if $r_{O4} \to \infty$, then $V_P/V_{in} \to 1$.

Active Current-mirrors

We now calculate V_{out}/V_P while taking r_{O2} into account. From Fig. 5.19,

$$\frac{V_{out}}{V_P} = \frac{1 + g_{m2}r_{O2}}{1 + \frac{r_{O2}}{r_{O4}}}$$

$$\approx \frac{g_{m2}r_{O2}}{1 + \frac{r_{O2}}{r_{O4}}}.$$

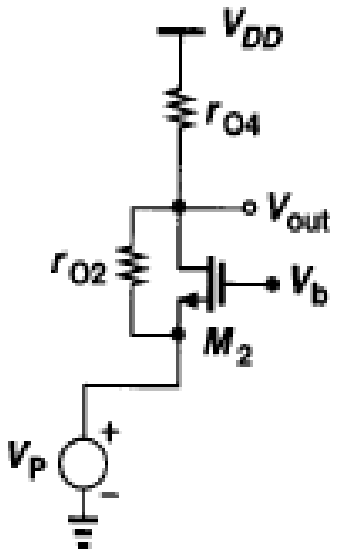


Figure 5.19 Circuit for calculation of V_{out}/V_P.

have

$$\frac{V_{out}}{V_{in}} = \frac{1 + \frac{r_{O4}}{r_{O2}}}{2 + \frac{r_{O4}}{r_{O2}}} \cdot \frac{g_{m2}r_{O2}}{1 + \frac{r_{O2}}{r_{O4}}}$$

$$= \frac{g_{m2}r_{O2}r_{O4}}{2r_{O2} + r_{O4}}$$

$$= \frac{g_{m2}}{2}[(2r_{O2}) \| r_{O4}].$$

Active Current-mirrors

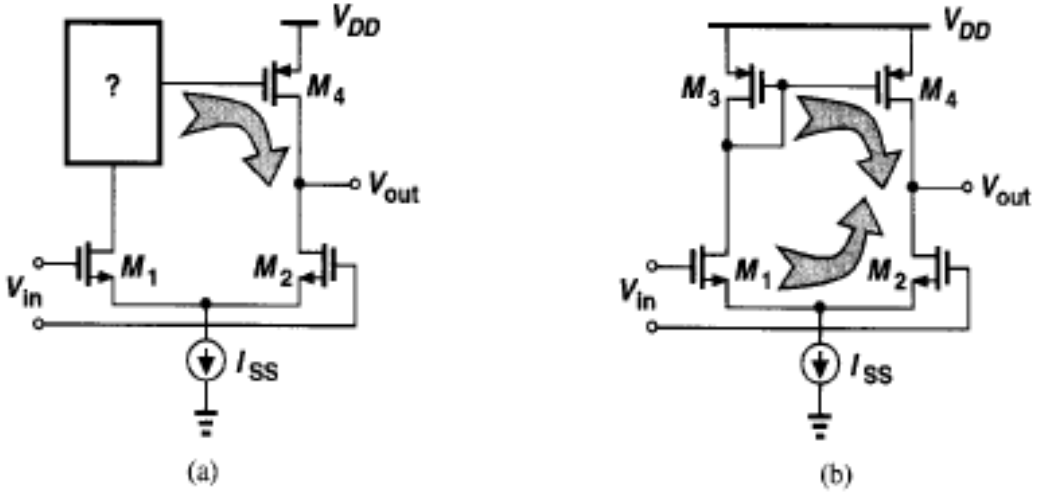


Figure 5.20 (a) Concept of combining the drain currents of M_1 and M_2, (b) realization of (a).

In the circuit of Fig. 5.17, the small-signal drain current of M_1 is "wasted." As conceptually shown in Fig. 5.20(a), it is desirable to utilize this current with proper polarity at the output. This can be accomplished as depicted in Fig. 5.20(b), where M_3 and M_4 are identical. To see how M_3 enhances the gain, suppose the gate voltage of M_1 increases by a small amount, increasing I_{D1} by ΔI and decreasing I_{D2} by ΔI. Since $|I_{D3}|$ and hence $|I_{D4}|$ also increase by ΔI, we observe that the output voltage tends to increase through two mechanisms: the drain current of M_2 drops *and* the drain current of M_4 rises.[3] In contrast to the circuit of Fig. 5.17, here M_4 assists M_2 with the voltage change at the output. This configuration is called a differential pair with active current mirror.[4] An important property of this circuit is that it converts a differential input to a single-ended output.

Active Current-mirrors – Large Signal

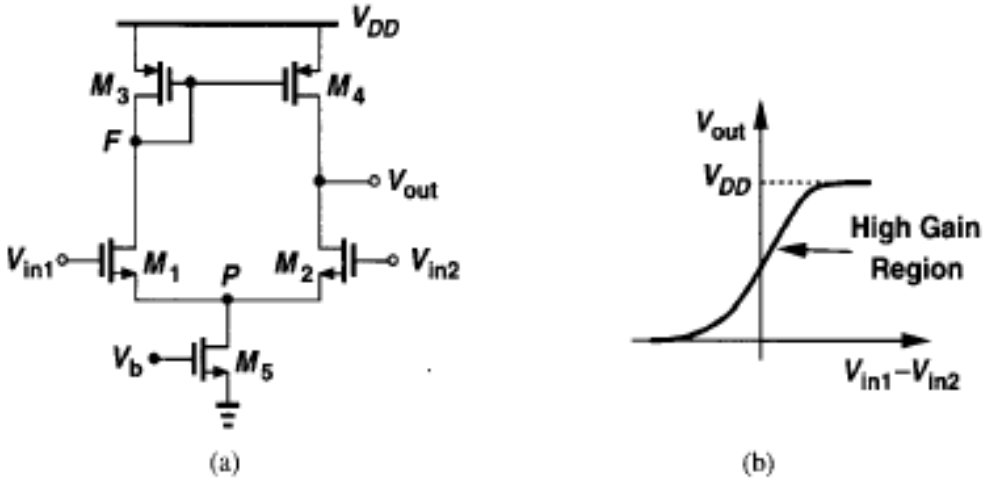


Figure 5.21 (a) Differential pair with active current mirror and realistic current source, (b) large-signal input-output characteristic.

Let us study the large-signal behavior of the circuit. To this end, we replace the ideal tail current source by a MOSFET as shown in Fig. 5.21(a). If V_{in1} is much more negative than V_{in2}, M_1 is off and so are M_3 and M_4. Since no current can flow from V_{DD}, both M_2 and M_5 operate in deep triode region, carrying zero current. Thus, $V_{out} = 0$.[5] As V_{in1} approaches V_{in2}, M_1 turns on, drawing part of I_{D5} from M_3 and turning M_4 on. The output voltage then depends on the difference between I_{D4} and I_{D2}. For a small difference between V_{in1} and V_{in2}, both M_2 and M_4 are saturated, providing a high gain [Fig. 5.21(b)]. As V_{in1} becomes more positive than V_{in2}, I_{D1}, $|I_{D3}|$, and $|I_{D4}|$ increase and I_{D2} decreases, eventually driving M_4 into the triode region. If $V_{in1} - V_{in2}$ is sufficiently large, M_2 turns off, M_4 operates in deep triode region with zero current, and $V_{out} = V_{DD}$. Note that if $V_{in1} > V_F + V_{TH}$, then M_1 enters the triode region.

Active Current-mirrors – Large Signal

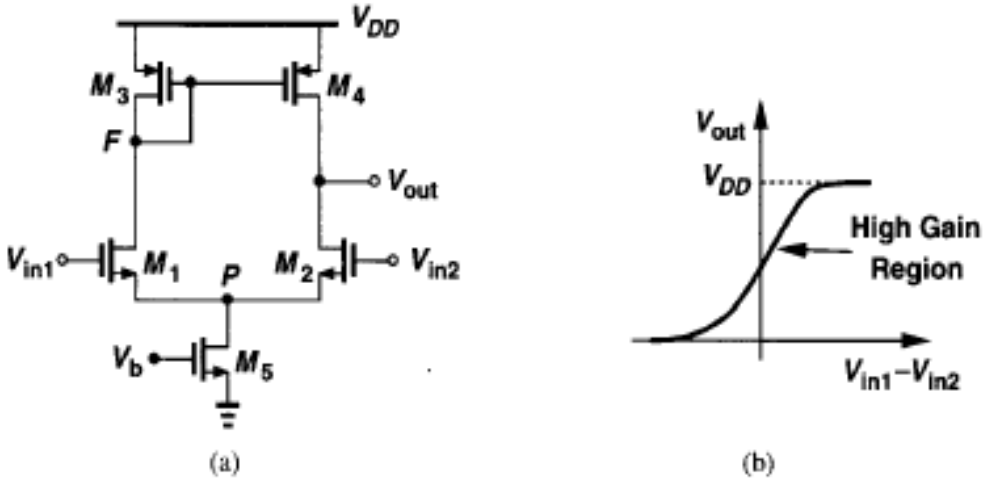


Figure 5.21 (a) Differential pair with active current mirror and realistic current source, (b) large-signal input-output characteristic.

The choice of the input common-mode voltage of the circuit is also important. For M_2 to be saturated, the output voltage cannot be less than $V_{in,CM} - V_{TH}$. Thus, to allow maximum output swings, the input CM level must be as low as possible, with the minimum given by $V_{GS1,2} + V_{DSS,min}$. The direct relationship between the input CM level and the output swing in this circuit is a critical drawback.

Active Current-mirrors – Large Signal

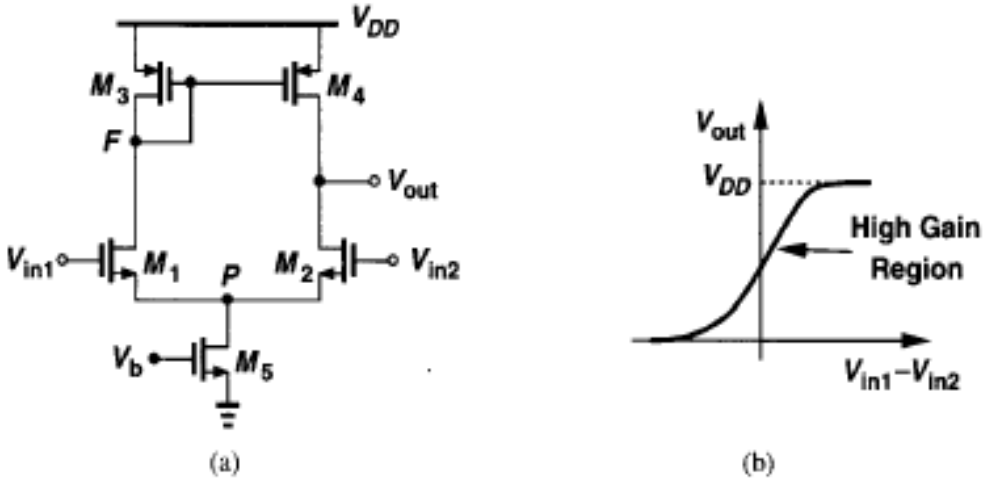


Figure 5.21 (a) Differential pair with active current mirror and realistic current source, (b) large-signal input-output characteristic.

What is the output voltage of the circuit when $V_{in1} = V_{in2}$? With perfect symmetry, $V_{out} = V_F = V_{DD} - |V_{GS3}|$. This can be proved by contradiction as well. Suppose, for example, that $V_{out} < V_F$. Then, due to channel-length modulation, M_1 must carry a greater current than M_2 (and M_4 a greater current than M_3). In other words, the total current through M_1 is greater than half of I_{SS}. But this means that the total current through M_3 also exceeds $I_{SS}/2$, violating the assumption that M_4 carries more current than M_3. In reality, however, asymmetries in the circuit may result in a large deviation in V_{out}, possibly driving M_2 or M_4 into the triode region. For example, if the threshold voltage of M_2 is slightly smaller than that of M_1, the former carries a greater current than the latter even with $V_{in1} = V_{in2}$, causing V_{out} to drop significantly. For this reason, the circuit is rarely used in an open-loop configuration to amplify small signals.

Active Current-mirrors – Large Signal

Example 5.5

Assuming perfect symmetry, sketch the output voltage of the circuit in Fig. 5.22(a) as V_{DD} varies from 3 V to zero. Assume that for $V_{DD} = 3$ V all of the devices are saturated.

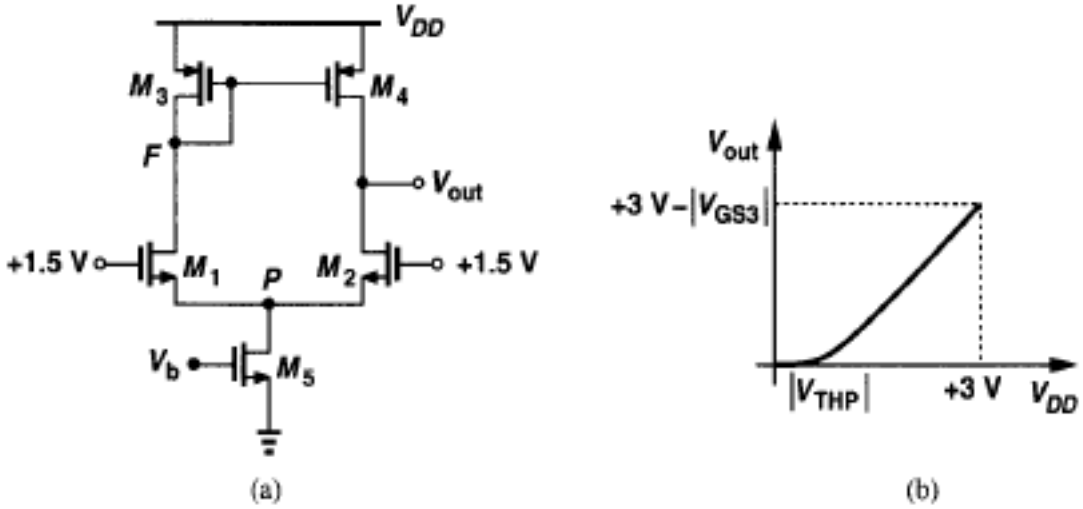


Figure 5.22

Solution

For $V_{DD} = 3$ V, symmetry requires that $V_{out} = V_F$. As V_{DD} drops, so do V_F and V_{out} with a slope close to unity [Fig. 5.22(b)]. As V_F and V_{out} fall below $+1.5\text{ V} - V_{THN}$, M_1 and M_2 enter the triode region, but their drain currents are constant if M_5 is saturated. Further decrease in V_{DD} and hence V_F and V_{out} causes V_{GS1} and V_{GS2} to increase, eventually driving M_5 into the triode region.

Thereafter, the bias current of all of the transistors drops, lowering the rate at which V_{out} decreases. For $V_{DD} < |V_{THP}|$, we have $V_{out} = 0$.

Active Current-mirrors – Small-signal

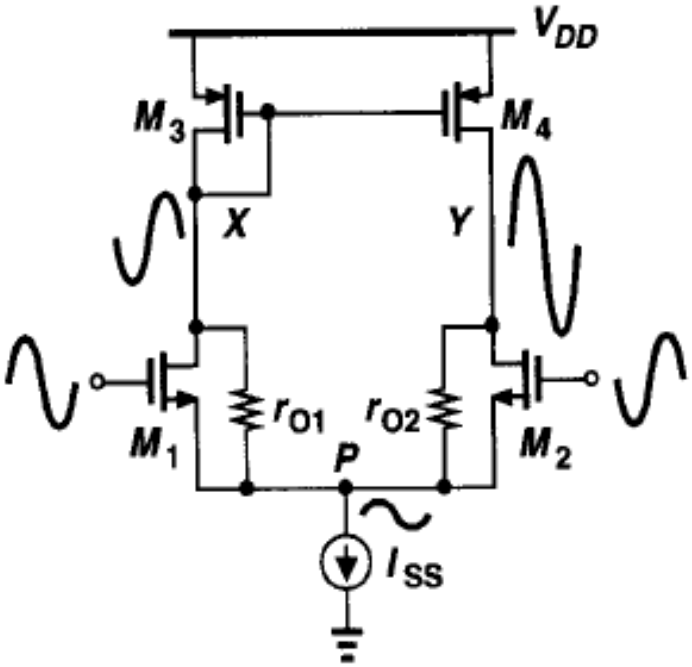


Figure 5.23 Asymmetric swings in a differential pair with active current mirror.

X and Y are vastly different. This is because the diode-connected device M_3 yields a much lower voltage gain from the input to node X than that from the input to node Y. As a result, the effects of V_X and V_Y at node P (through r_{O1} and r_{O2}, respectively) do not cancel each other and this node cannot necessarily be considered a virtual ground. We compute the gain using two different approaches.

Active Current-mirrors – Small-signal

In the first approach, we write $|A_v| = G_m R_{out}$ and obtain G_m and R_{out} separately. For the calculation of G_m, consider Fig. 5.24(a). The circuit is not quite symmetric but

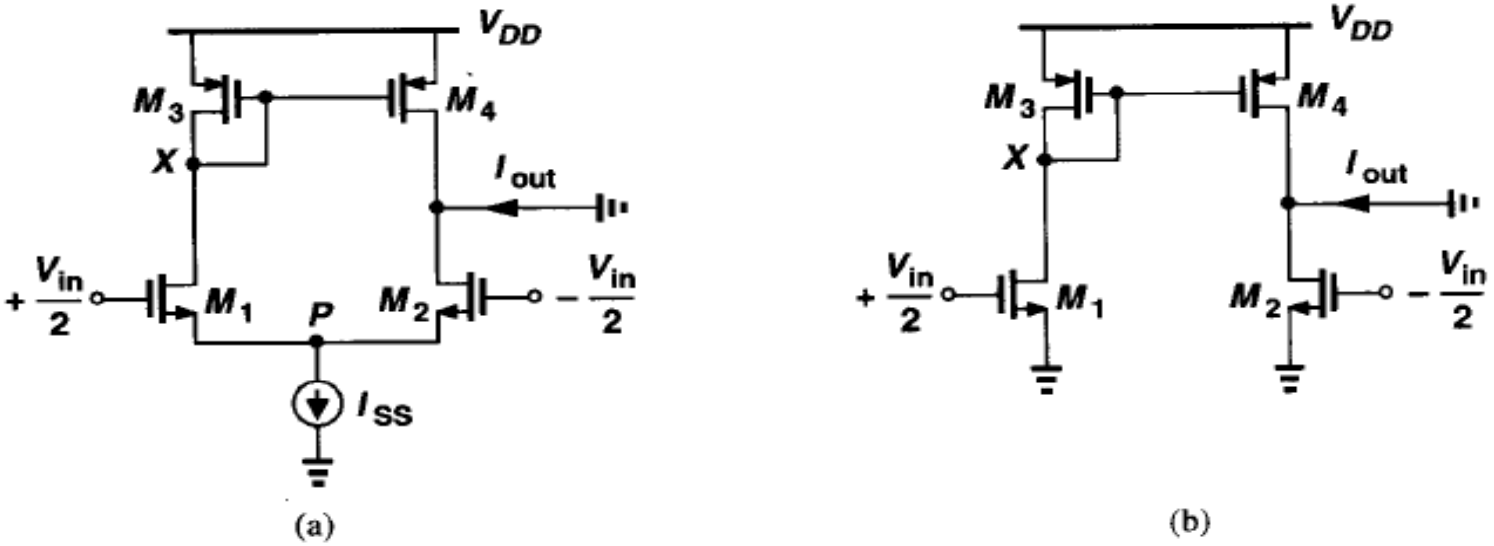


Figure 5.24 (a) Circuit for calculation of G_m, (b) circuit of (a) with node P grounded.

because the impedance seen at node X is relatively low and the swing at this node small, the current returning from X to P through r_{O1} is negligible and node P can be viewed as a virtual ground [Fig. 5.24(b)]. Thus, $I_{D1} = |I_{D3}| = |I_{D4}| = g_{m1,2}V_{in}/2$ and $I_{D2} = -g_{m1,2}V_{in}/2$, yielding $I_{out} = -g_{m1,2}V_{in}$ and hence $|G_m| = g_{m1,2}$. Note that, by virtue of active current mirror operation, this value is twice the transconductance of the circuit of Fig. 5.17(b).

Active Current-mirrors – Small-signal

Calculation of R_{out} is less straightforward. We may surmise that the output resistance of this circuit is equal to that of the circuit in Fig. 5.17(c), namely, $(2r_{O2})\|r_{O4}$. In reality, however, the active mirror operation yields a different value because when a voltage is applied to the output to measure R_{out}, the gate voltage of M_4 does not remain constant. Rather than draw the entire equivalent circuit, we observe that, for small signals, I_{SS} is open [Fig. 5.25(a)], any current flowing into M_1 must flow out of M_2, and the role of the two transistors can be

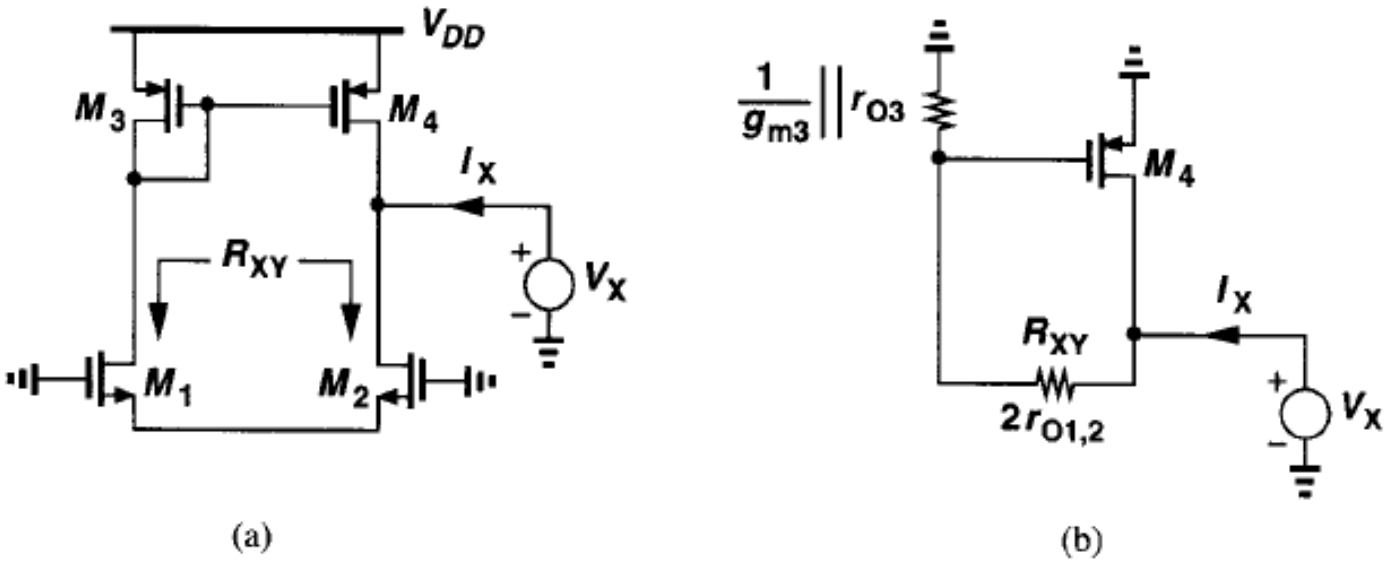


Figure 5.25 (a) Circuit for calculating R_{out}, (b) substitution of M_1 and M_2 by a resistor.

Active Current-mirrors – Small-signal

represented by a resistor $R_{XY} = 2r_{O1,2}$ [Fig. 5.25(b)]. As a consequence, the current drawn from V_X by R_{XY} is mirrored by M_3 into M_4 with unity gain. We can therefore write:

$$I_X = 2\frac{V_X}{2r_{O1,2} + \frac{1}{g_{m3}} \Big\| r_{O3}} + \frac{V_X}{r_{O4}}, \tag{5.27}$$

where the factor 2 accounts for current copying action of M_3 and M_4. For $2r_{O1,2} \gg (1/g_{m3}) \| r_{O3}$, we have

$$R_{out} \approx r_{O2} \| r_{O4}. \tag{5.28}$$

The overall voltage gain is thus equal to $|A_v| = G_m R_{out} = g_{m1,2}(r_{O2} \| r_{O4})$, somewhat higher than that of the circuit in Fig. 5.17(a).

Active Current-mirrors – Small-signal

The second approach to calculating the voltage gain of the circuit is illustrated in Fig. 5.26, providing more insight into the operation. We substitute the input source and M_1 and M_2 by a Thevenin equivalent. As illustrated in Fig. 5.27(a), for the Thevenin voltage calculation, node P is a virtual ground because of symmetry, and a half-circuit equivalent yields $V_{eq} = g_{m1,2} r_{O1,2} V_{in}$. Moreover, the output resistance is $R_{eq} = 2r_{O1,2}$. From Fig. 5.27(b),

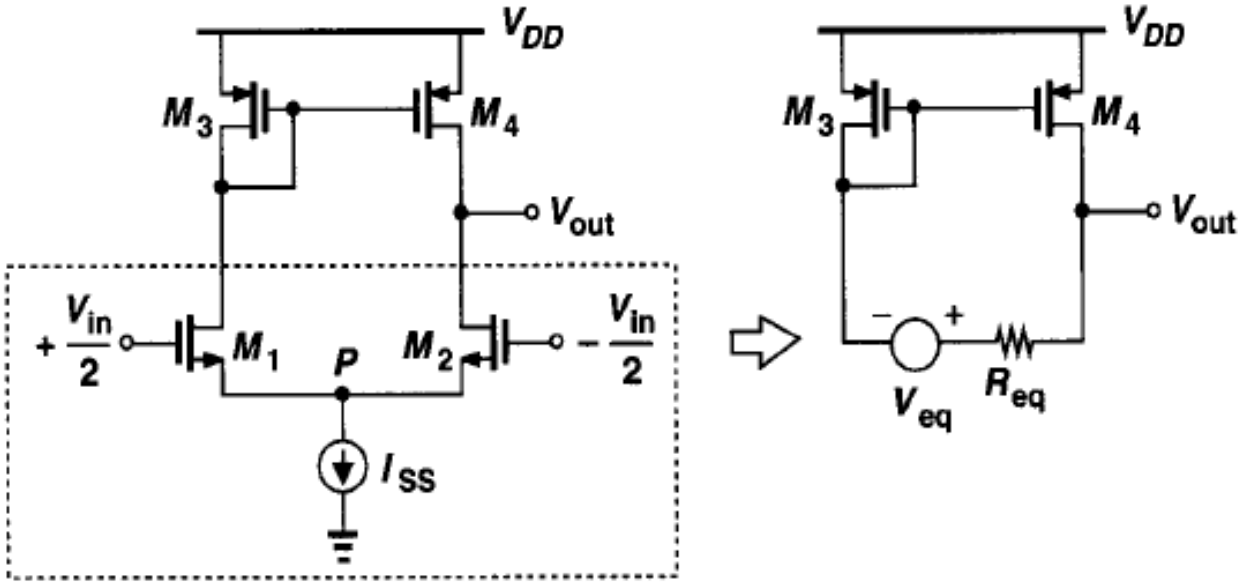


Figure 5.26 Substitution of the input differential pair by a Thevenin equivalent.

Active Current-mirrors – Small-signal

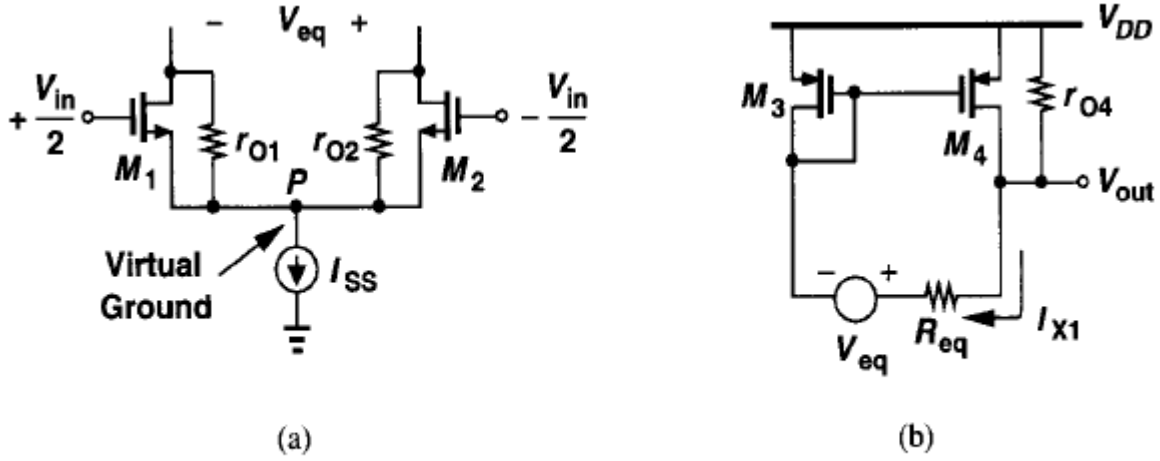


Figure 5.27 (a) Calculation of the Thevenin equivalent voltage, (b) simplified circuit.

we note that the current through R_{eq} is

$$I_{X1} = \frac{V_{out} - g_{m1,2}r_{O1,2}V_{in}}{2r_{O1,2} + \dfrac{1}{g_{m3}} \| r_{O3}}. \tag{5.29}$$

The fraction of this current that flows through $1/g_{m3}$ is mirrored into M_4 with unity gain. That is,

$$2\frac{V_{out} - g_{m1,2}r_{O1,2}V_{in}}{2r_{O1,2} + \dfrac{1}{g_{m3}} \| r_{O3}} \cdot \frac{r_{O3}}{r_{O3} + 1/g_{m3}} = -\frac{V_{out}}{r_{O4}}. \tag{5.30}$$

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1,2}r_{O3,4}r_{O1,2}}{r_{O1,2} + r_{O3,4}} = g_{m1,2}(r_{O1,2} \| r_{O3,4}).$$

Assuming $2r_{O1,2} \gg (1/g_{m3,4}) \| r_{O3,4}$, we obtain

Active Current-mirrors – Small-signal

Example 5.6

Calculate the small-signal voltage gain of the circuit shown in Fig. 5.28. How does the performance of this circuit compare with that of a differential pair with active mirror?

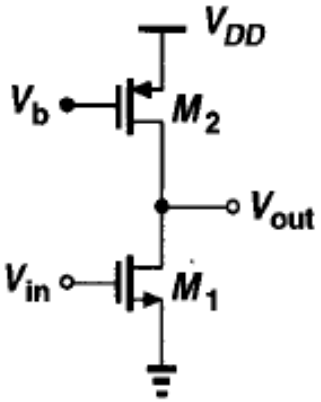


Figure 5.28

Solution

We have $A_v = g_{m1}(r_{O1} \| r_{O2})$, similar to the value derived above. For given device dimensions, this circuit requires half of the bias current to achieve the same gain as a differential pair. However, advantages of differential operation often outweigh the power penalty.

Active Current-mirrors – Common-mode

Let us now study the common-mode properties of the differential pair with active current mirror. We assume $\gamma = 0$ for simplicity and leave a more general analysis including body effect for the reader. Our objective is to predict the consequences of a finite output impedance in the tail current source. As depicted in Fig. 5.29, a change in the input CM level leads to

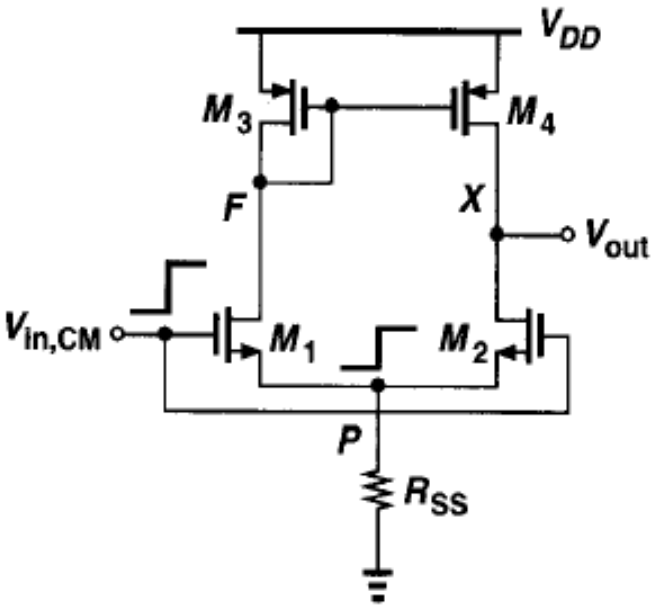


Figure 5.29 Differential pair with active current mirror sensing a common-mode change.

a change in the bias current of all of the transistors. How do we define the common-mode gain here? Recall from Chapter 4 that the CM gain represents the *corruption* of the output

Active Current-mirrors – Common-mode

signal of interest due to variations of the input CM level. In the circuits of Chapter 3, the output signal was sensed differentially and hence the CM gain was defined in terms of the output differential component generated by the input CM change. In the circuit of Fig. 5.29, on the other hand, the output signal of interest is sensed with respect to ground. Thus, we define the CM gain in terms of the single-ended output component produced by the input CM change:

$$A_{CM} = \frac{\Delta V_{out}}{\Delta V_{in,CM}}. \tag{5.33}$$

To determine A_{CM}, we observe that if the circuit is symmetric, $V_{out} = V_F$ for any input CM level. For example, as $V_{in,CM}$ increases, V_F drops and so does V_{out}. In other words, nodes F and X can be shorted [Fig. 5.30(a)], resulting in the equivalent circuit shown

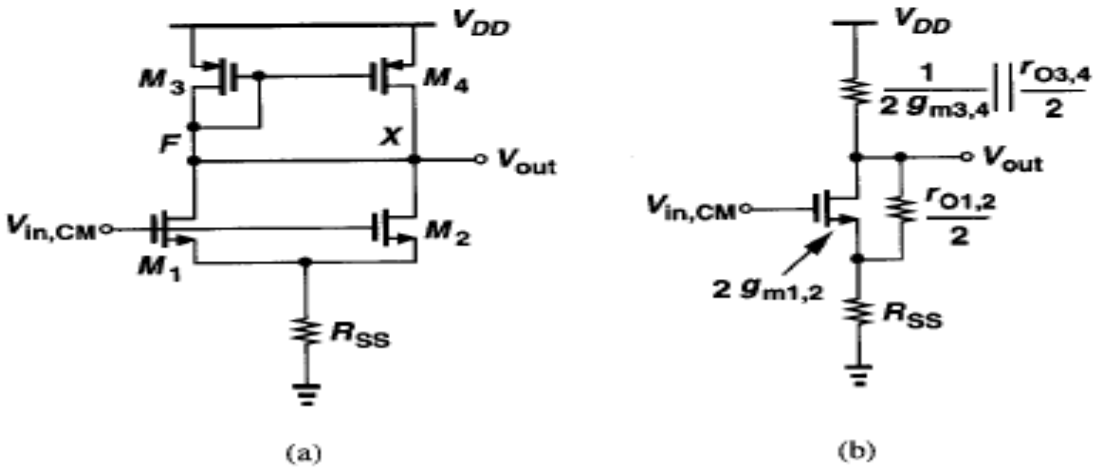


Figure 5.30 (a) Simplified circuit of Fig. 5.29, (b) equivalent circuit of (a).

Active Current-mirrors – Common-mode

in Fig. 5.30(b). Here, M_1 and M_2 appear in parallel and so do M_3 and M_4. It follows that

$$A_{CM} \approx \frac{-\frac{1}{2g_{m3,4}} \| \frac{r_{O3,4}}{2}}{\frac{1}{2g_{m1,2}} + R_{SS}} \tag{5.34}$$

$$= \frac{-1}{1 + 2g_{m1,2}R_{SS}} \frac{g_{m1,2}}{g_{m3,4}}, \tag{5.35}$$

where we have assumed $1/(2g_{m3,4}) \ll r_{O3,4}$ and neglected the effect of $r_{O1,2}/2$. The CMRR is then given by

$$CMRR = \left| \frac{A_{DM}}{A_{CM}} \right| \tag{5.36}$$

$$= g_{m1,2}(r_{O1,2} \| r_{O3,4}) \frac{g_{m3,4}(1 + 2g_{m1,2}R_{SS})}{g_{m1,2}} \tag{5.37}$$

$$= (1 + 2g_{m1,2}R_{SS}) g_{m3,4}(r_{O1,2} \| r_{O3,4}). \tag{5.38}$$

Equation (5.35) indicates that, even with perfect symmetry, the output signal is corrupted by input CM variations, a drawback that does not exist in the fully differential circuits of Chapter 3. High-frequency common-mode noise therefore degrades the performance considerably as the capacitance shunting the tail current source exhibits a lower impedance.

Active Current-mirrors – Common-mode

Example 5.7

The CM gain of the circuit of Fig. 5.29 can be shown to be *zero* by a (flawed) argument. As shown in Fig. 5.31(a), if $V_{in,CM}$ introduces a change of ΔI in the drain current of each input transistor, then

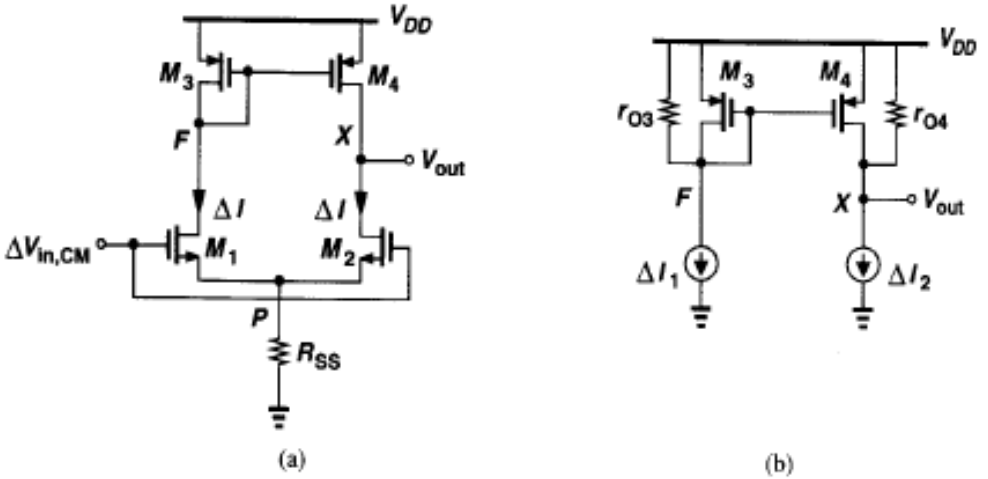


Figure 5.31

I_{D3} also experiences the same change and so does I_{D4}. Thus, M_4 seemingly provides the additional current required by M_2, and the output voltage need not change, i.e., $A_{CM} = 0$. Explain the flaw in this proof.

Solution

The assumption that ΔI_{D4} completely cancels the effect of ΔI_{D2} is incorrect. Consider the equivalent circuit shown in Fig. 5.31(b). Since

$$\Delta V_F = \Delta I_1 \left(\frac{1}{g_{m3}} \Big\| r_{O3} \right), \tag{5.39}$$

we have

$$|\Delta I_{D4}| = g_{m4} \Delta V_F$$

$$= g_{m4} \Delta I_1 \frac{r_{O3}}{1 + g_{m3} r_{O3}}.$$

This current and ΔI_2 ($= \Delta I_1 = \Delta I$) give a net voltage change equal to

$$\Delta V_{out} = (\Delta I_1 g_{m4} \frac{r_{O3}}{1 + g_{m3} r_{O3}} - \Delta I_2) r_{O4}$$

$$= -\Delta I \frac{1}{g_{m3} r_{O3} + 1} r_{O4},$$

which is equal to the voltage change at node F.

Active Current-mirrors – Common-mode

It is also instructive to calculate the common-mode gain in the presence of mismatches. As an example, we consider the case where the input transistors exhibit slightly different transconductances [Fig. 5.32(a)]. How does V_{out} depend on $V_{in,CM}$? Since the change at

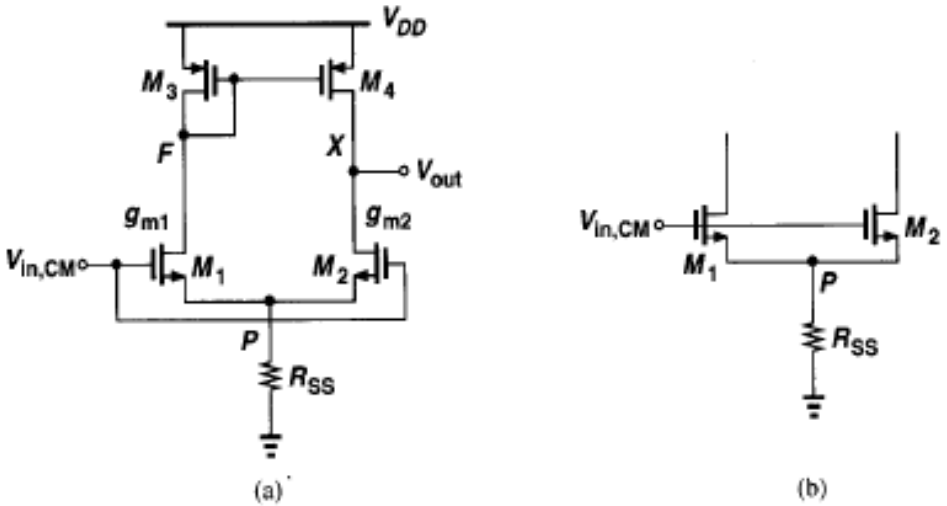


Figure 5.32 Differential pair with g_m mismatch.

nodes F and X is relatively small, we can compute the change in I_{D1} and I_{D2} while neglecting the effect of r_{O1} and r_{O2}. As shown in Fig. 5.32(b), the voltage change at P can be obtained by considering M_1 and M_2 as a single transistor (in a source follower configuration) with a transconductance equal to $g_{m1} + g_{m2}$, i.e.,

$$\Delta V_P = \Delta V_{in,CM} \frac{R_{SS}}{R_{SS} + \dfrac{1}{g_{m1} + g_{m2}}}, \tag{5.44}$$

Active Current-mirrors – Common-mode

where body effect is neglected. The changes in the drain currents of M_1 and M_2 are therefore given by

$$\Delta I_{D1} = g_{m1}(\Delta V_{in,CM} - \Delta V_P) \tag{5.45}$$

$$= \frac{\Delta V_{in,CM}}{R_{SS} + \dfrac{1}{g_{m1} + g_{m2}}} \frac{g_{m1}}{g_{m1} + g_{m2}} \tag{5.46}$$

$$\Delta I_{D2} = g_{m2}(\Delta V_{in,CM} - \Delta V_P) \tag{5.47}$$

$$= \frac{\Delta V_{in,CM}}{R_{SS} + \dfrac{1}{g_{m1} + g_{m2}}} \frac{g_{m2}}{g_{m1} + g_{m2}}. \tag{5.48}$$

The change ΔI_{D1} multiplied by $(1/g_{m3})\|r_{O3}$ yields $|\Delta I_{D4}| = g_{m4}[(1/g_{m3})\|r_{O3}]\Delta I_{D1}$. The difference between this current and ΔI_{D2} flows through the output impedance of the circuit, which is equal to r_{O4} because we have neglected the effect of r_{O1} and r_{O2}:

$$\Delta V_{out} = \left[\frac{g_{m1}\Delta V_{in,CM}}{1 + (g_{m1} + g_{m2})R_{SS}} \frac{r_{O3}}{r_{O3} + \dfrac{1}{g_{m3}}} - \frac{g_{m2}\Delta V_{in,CM}}{1 + (g_{m1} + g_{m2})R_{SS}} \right] r_{O4} \tag{5.49}$$

$$= \frac{\Delta V_{in,CM}}{1 + (g_{m1} + g_{m2})R_{SS}} \frac{(g_{m1} - g_{m2})r_{O3} - g_{m2}/g_{m3}}{r_{O3} + \dfrac{1}{g_{m3}}} r_{O4}. \tag{5.50}$$

If $r_{O3} \gg 1/g_{m3}$, we have

$$\frac{\Delta V_{out}}{\Delta V_{in,CM}} \approx \frac{(g_{m1} - g_{m2})r_{O3} - g_{m2}/g_{m3}}{1 + (g_{m1} + g_{m2})R_{SS}}. \tag{5.51}$$

Compared to Eq. (5.35), this result contains the additional term $(g_{m1} - g_{m2})r_{O3}$ in the numerator, revealing the effect of transconductance mismatch on the common-mode gain.