Universidade de Brasília

Faculdade UnB Gama

Projeto de Circuitos Eletrônicos Integrados 2

Projeto de Amplificadores de 2 Estágios (Revisão)

Professor: Wellington Amaral (waamaral@unb.br)

Amp. Op. de 2 Estágios

Considerações

$$R_1 \approx \frac{1}{g_{m3}} \| r_{ds3} \| r_{ds1} \approx \frac{1}{g_{m3}}$$

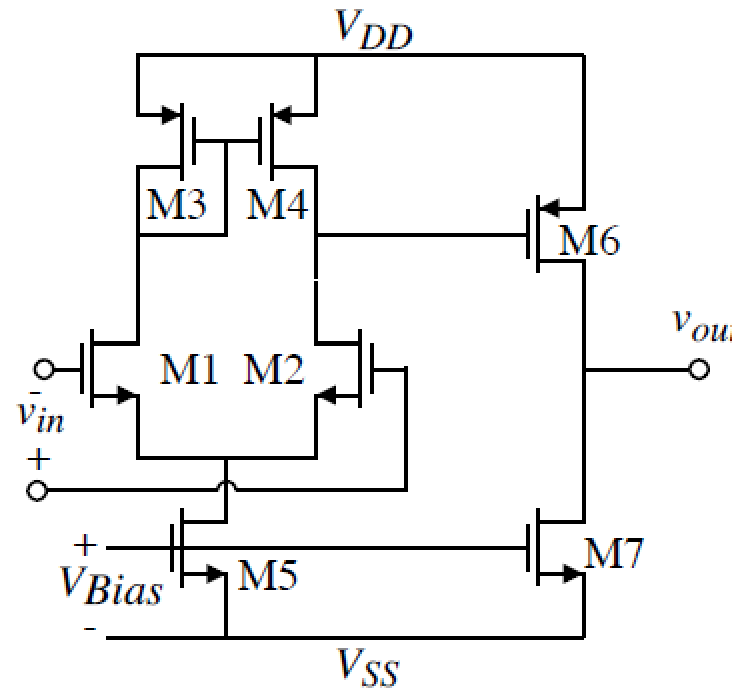
$$C_1 = C_{gs3} + C_{gs4} + C_{bd1} + C_{bd3}$$

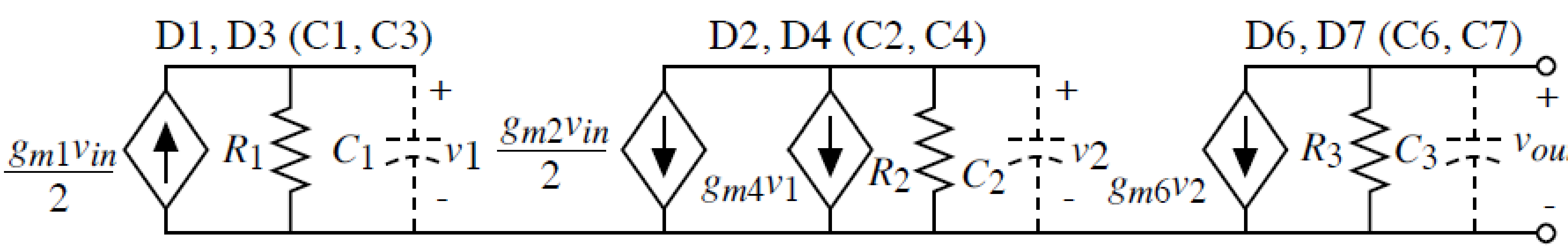
$$R_2 = r_{ds2} \| \, r_{ds4}$$

$$C_2 = C_{gs6} + C_{bd2} + C_{bd4}$$

$$R_3 = r_{ds6} \| \, r_{ds7}$$

$$C_3 = C_L + C_{bd6} + C_{bd7}$$





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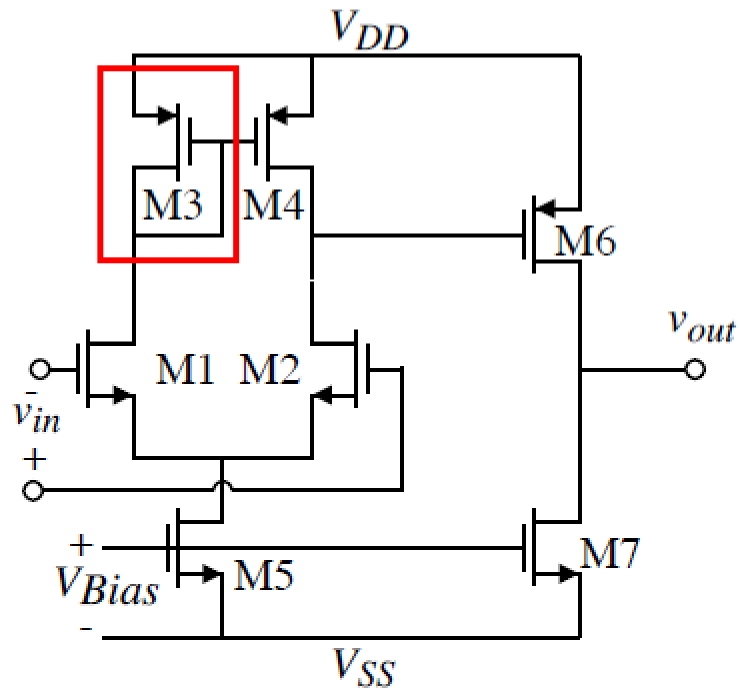

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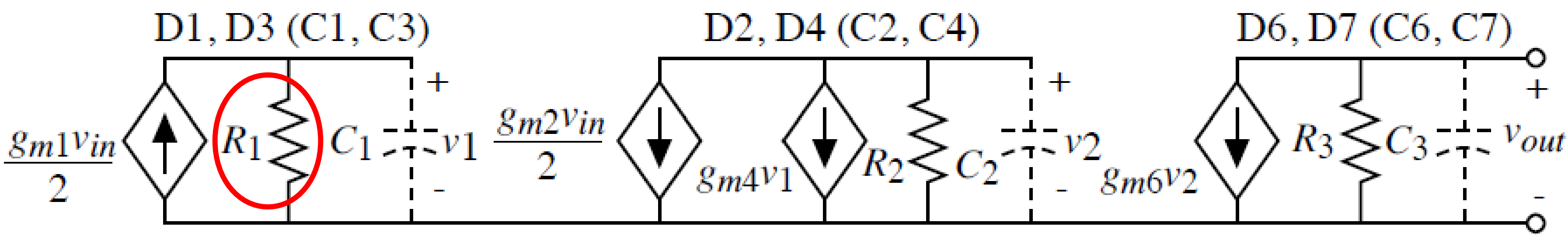

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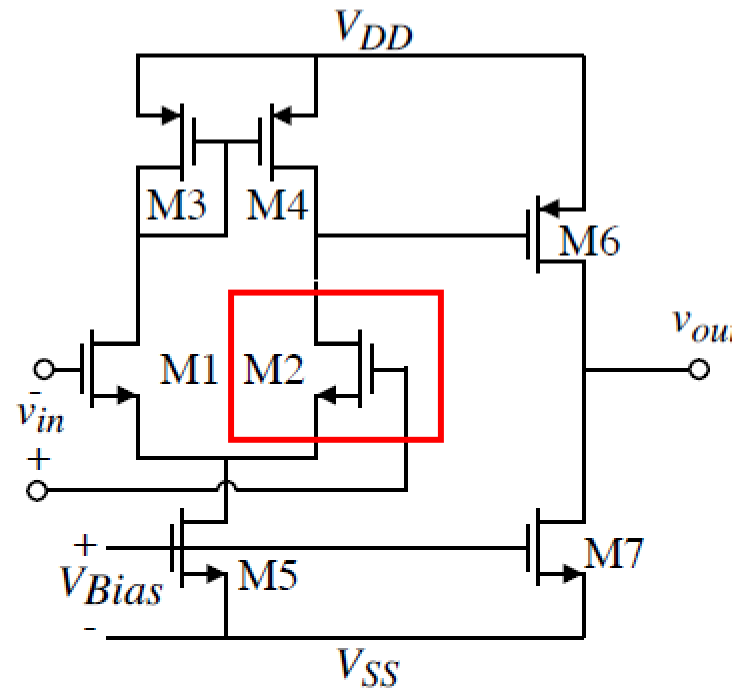

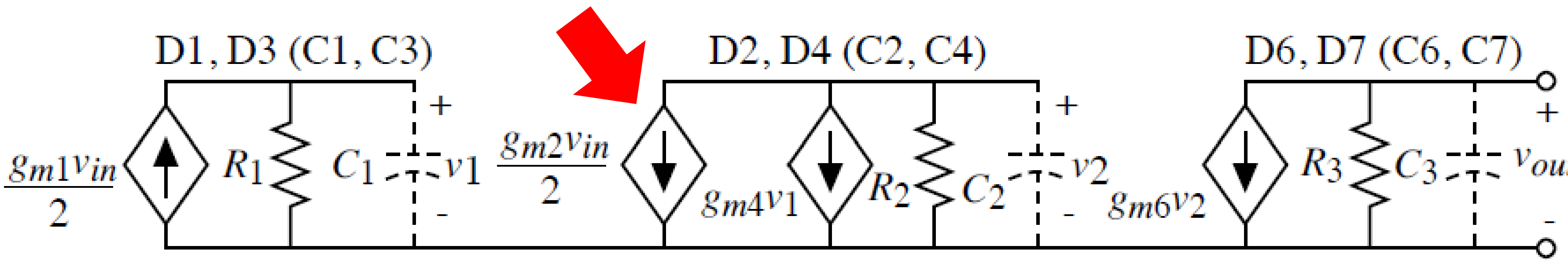

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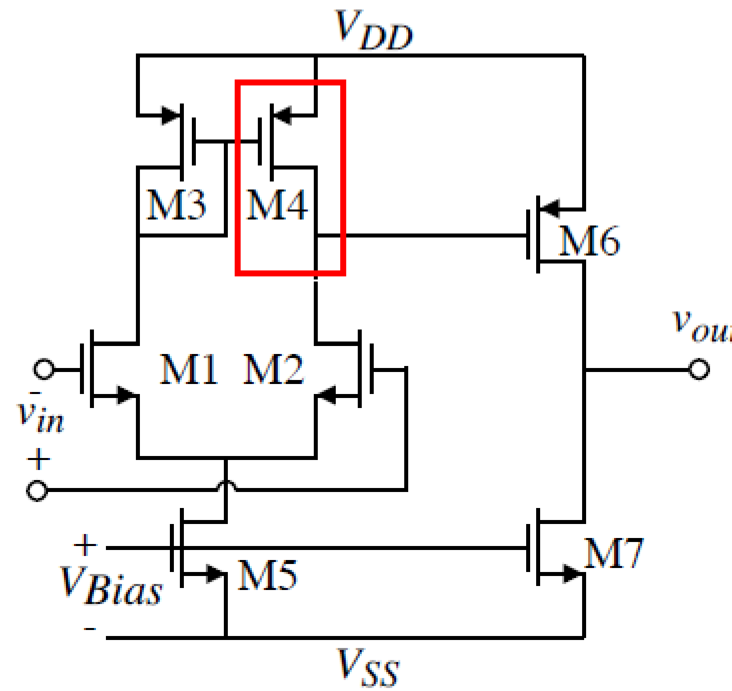
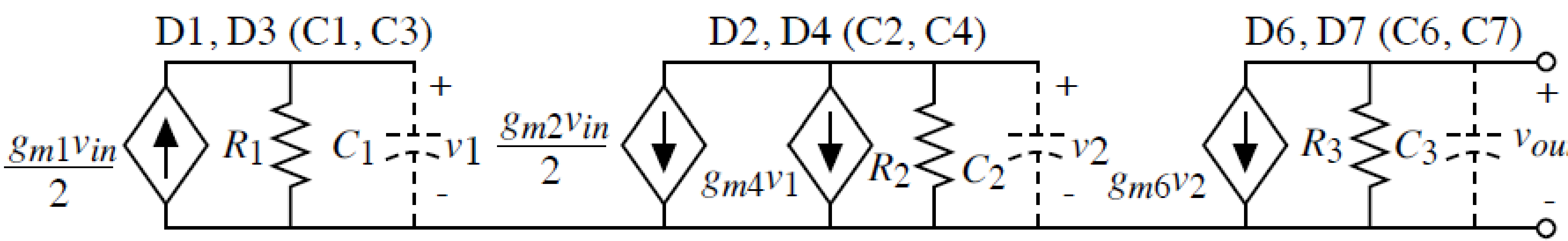
Tensão V1 no *gate* de M3/M4 é dada por ($gm1*V_{in}/2$)*R1





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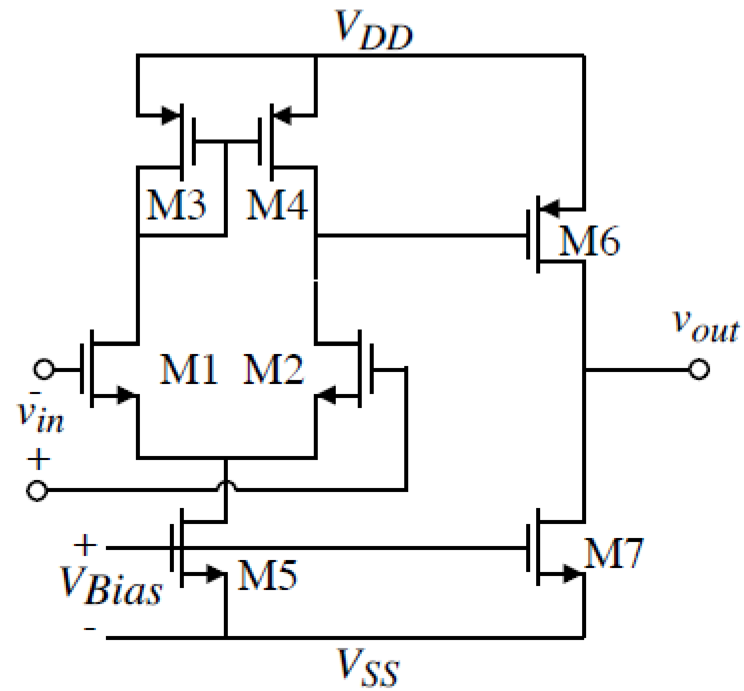

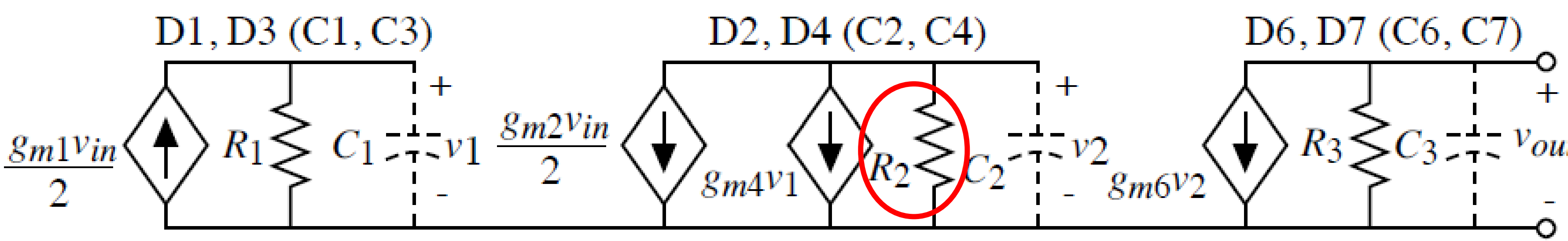

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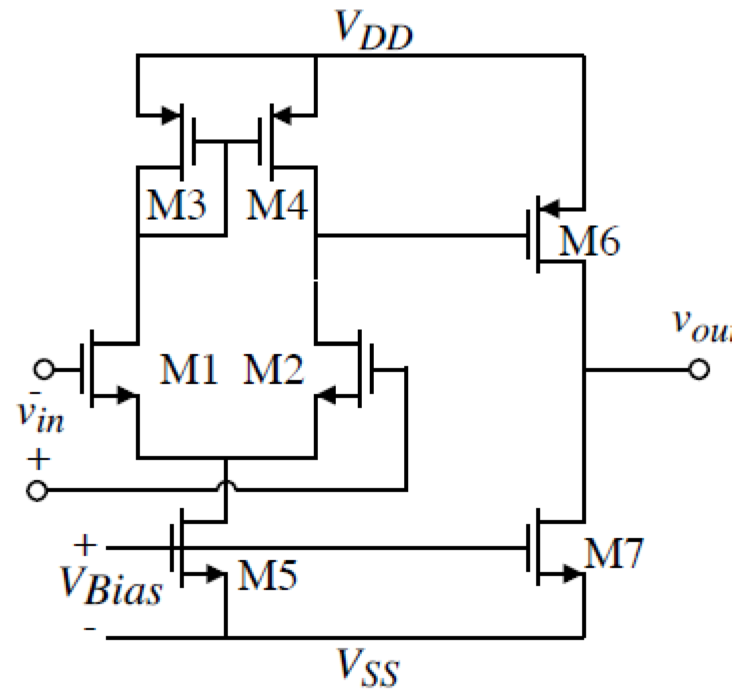
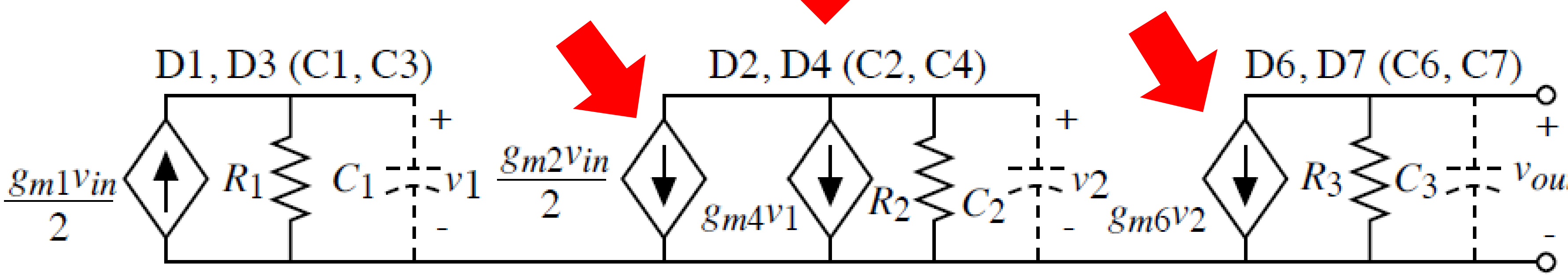


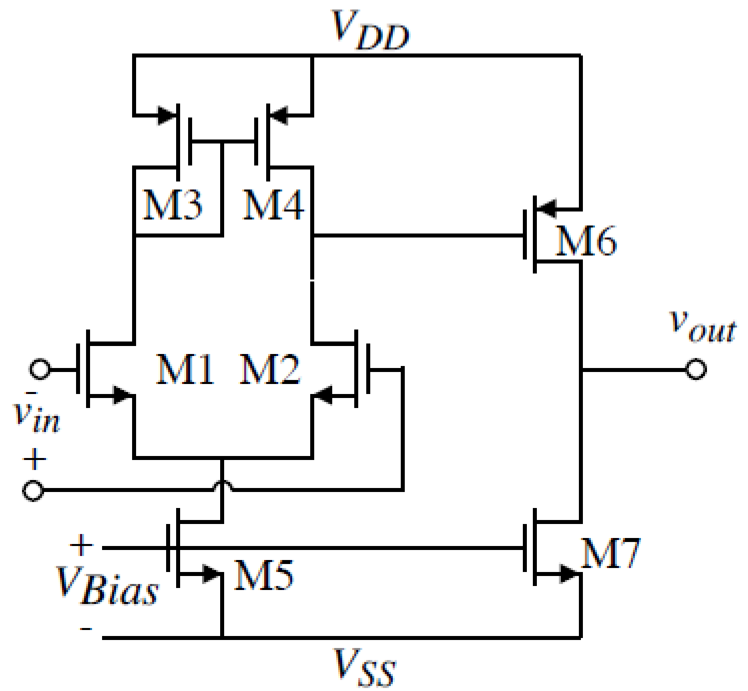
Tensão V2 é dada pelo somatório das duas fontes de corrente vezes R2

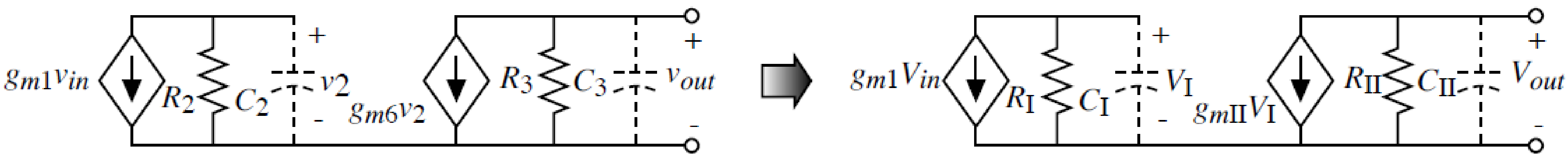


Amp. Op. de 2 Estágios

Considerações

➢ Considerando que R1 é pequeno.





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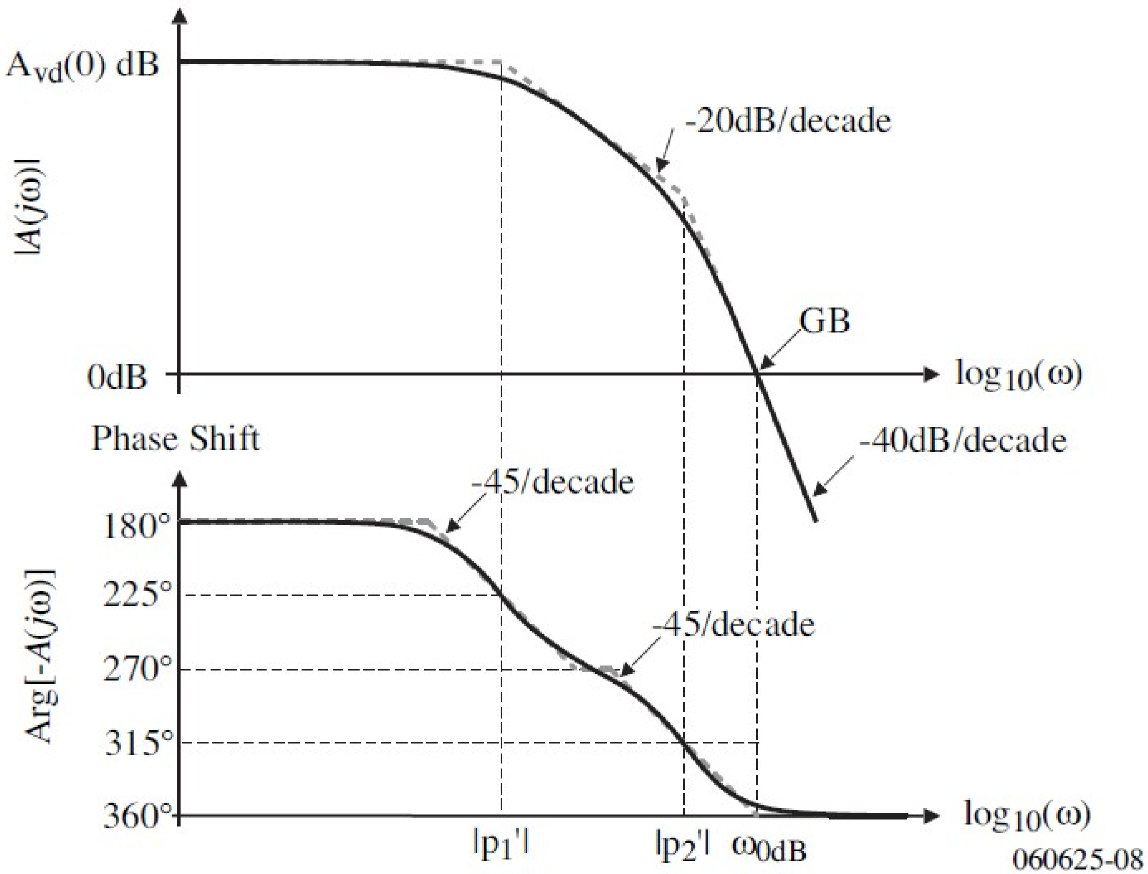
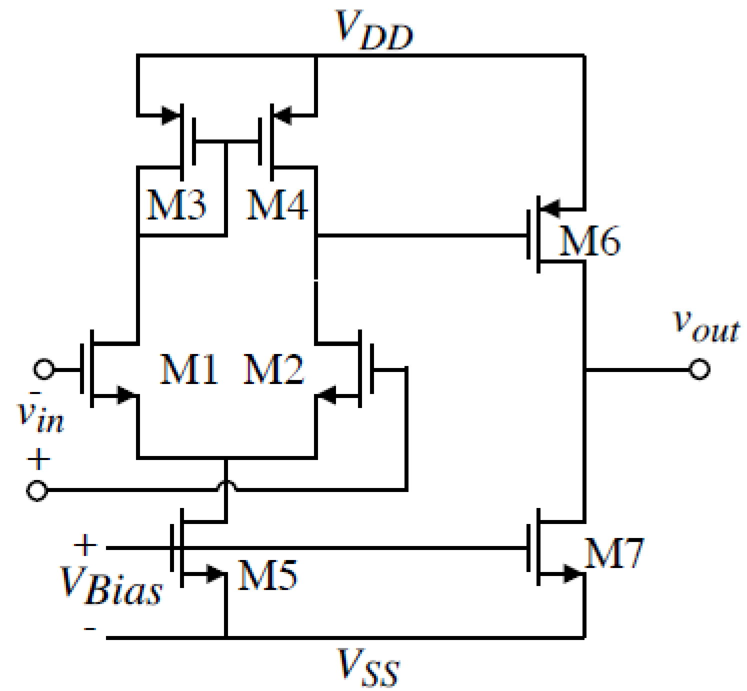




Margem de fase menor que 45°!!

Amp. Op. de 2 Estágios

Considerações

Compensação Miller

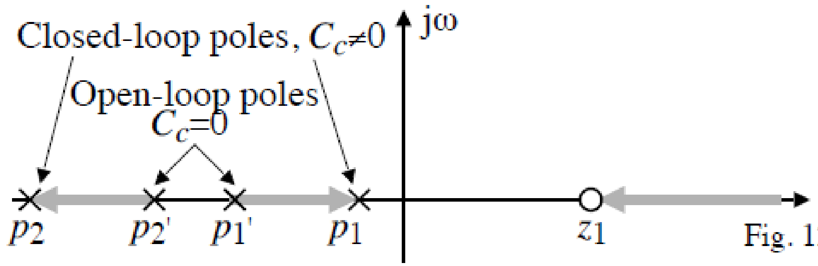
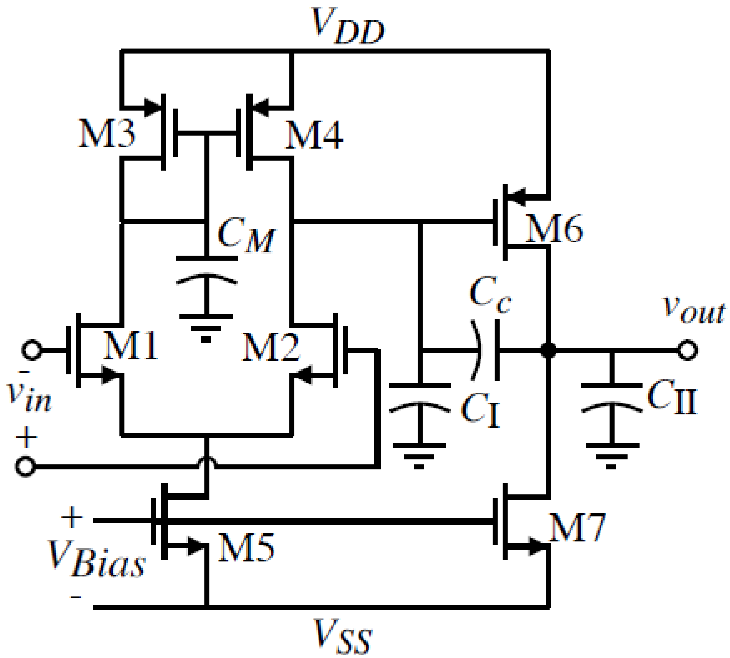


Fig. 120-11



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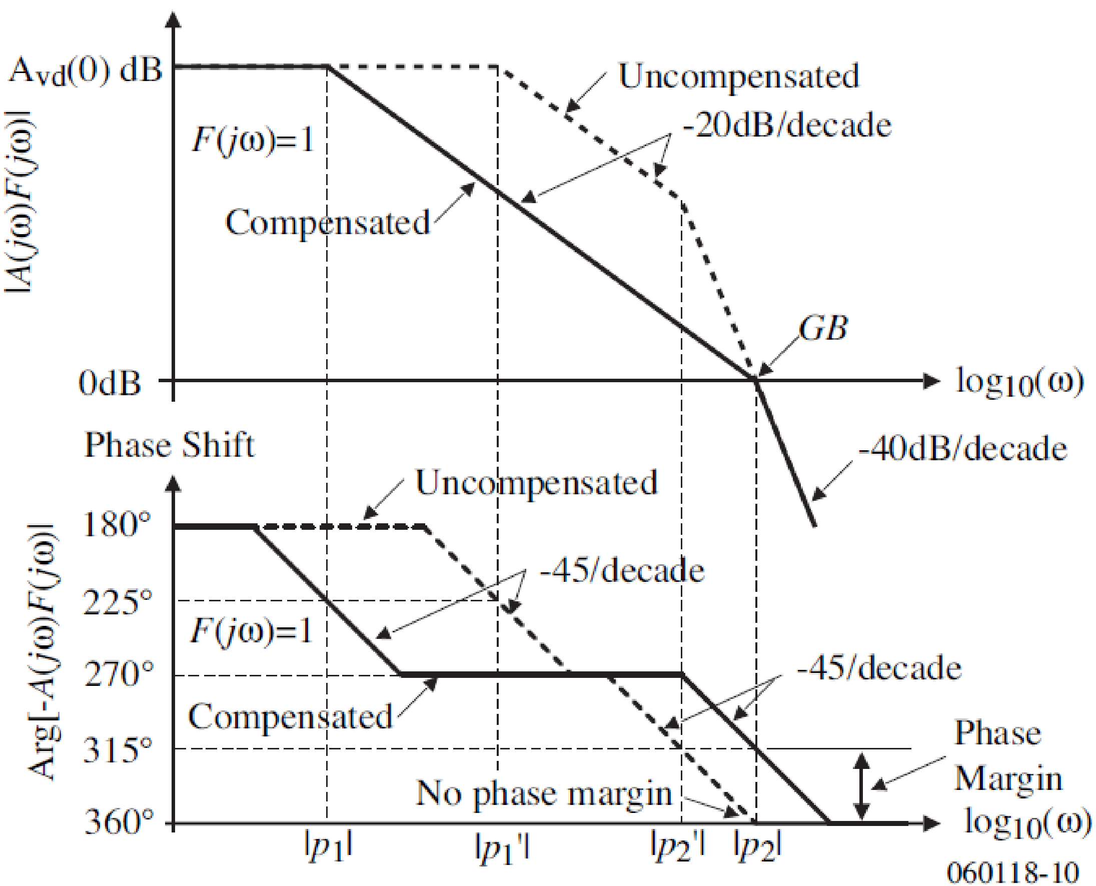
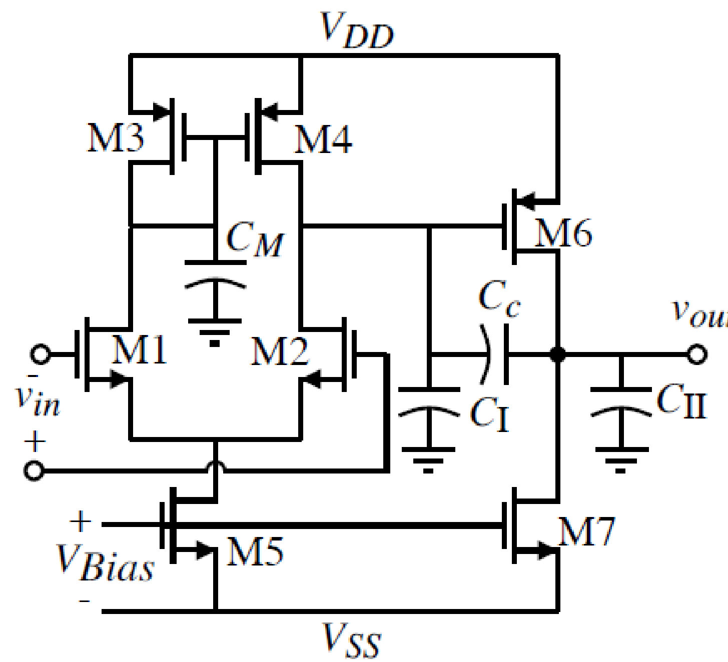
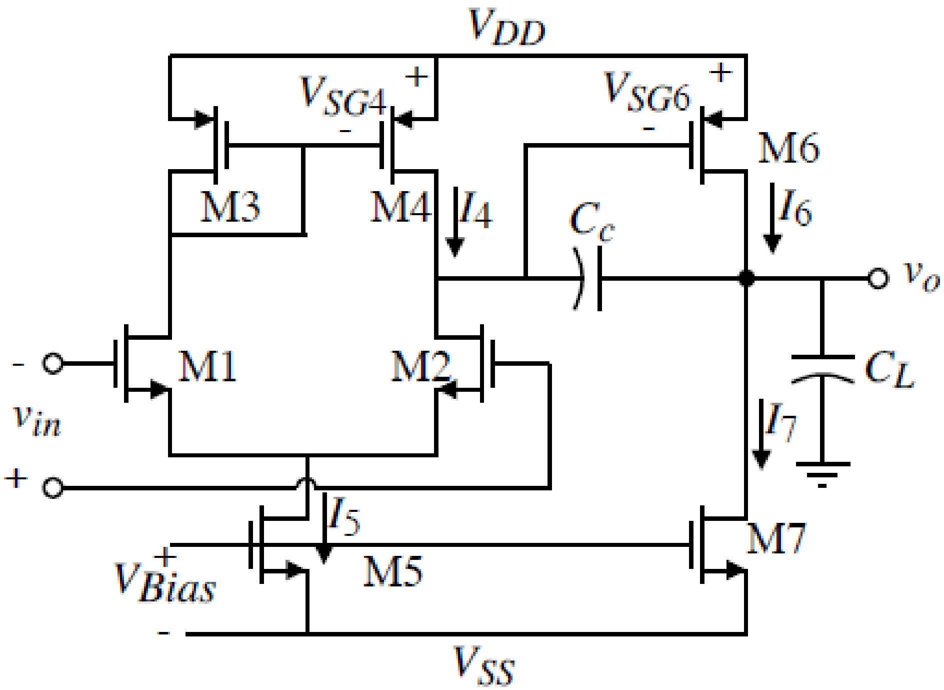




Amp. Op. de 2 Estágios

Especificações Necessárias

1. Gain at dc, $A_v(0)$
2. Gain-bandwidth, GB
3. Phase margin (or settling time)
4. Input common-mode range, ICMR
5. Load Capacitance, C_L
6. Slew-rate, SR
7. Output voltage swing
8. Power dissipation, P_{diss}



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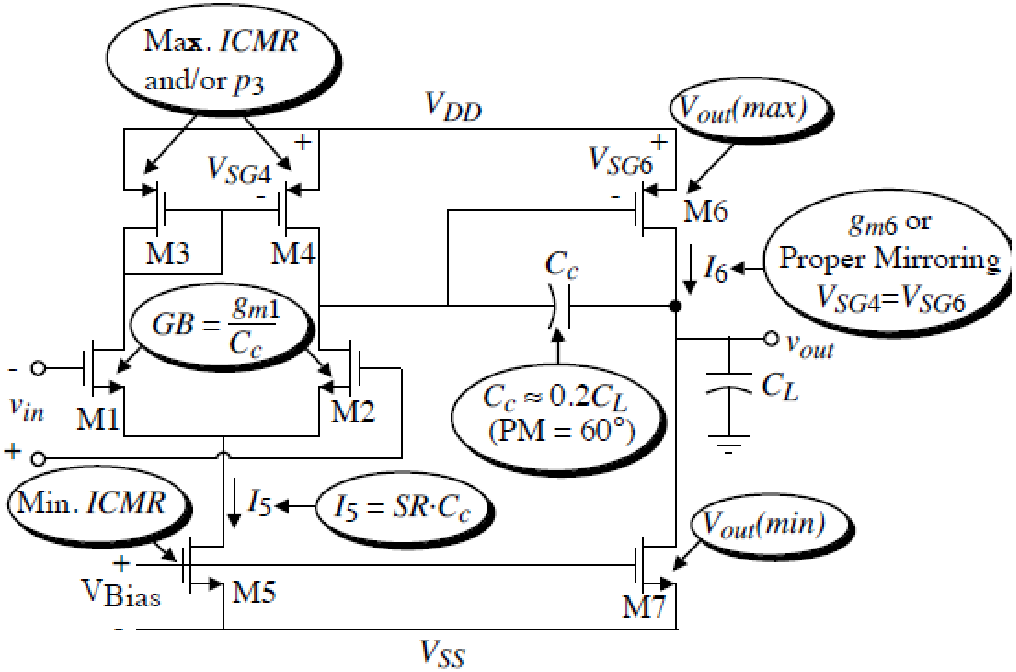
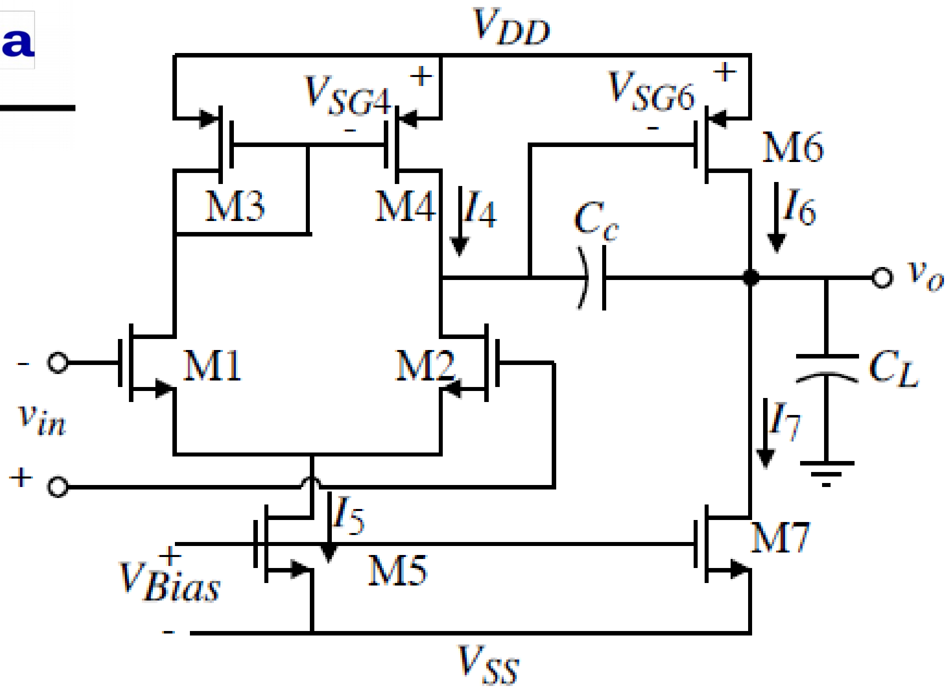


Equações de Projeto (Considerações)



1- $V_{SG4} = V_{SG6}$ (1)

2- Se $V_{SG4} = V_{SG6} \Rightarrow I_6 = \left(\frac{S_6}{S_4}\right) I_4$ (2)

3- O projeto deve satisfazer a "Condição de Balanceamento/Casamento": I6 = I7 (3)

Além disto: $I_7 = \left(\frac{S_7}{S_5}\right) I_5 = \left(\frac{S_7}{S_5}\right)(2I_4)$ (4)

4- Logo, $\boxed{\frac{S_6}{S_4} = \frac{2S_7}{S_5}}$ (5)

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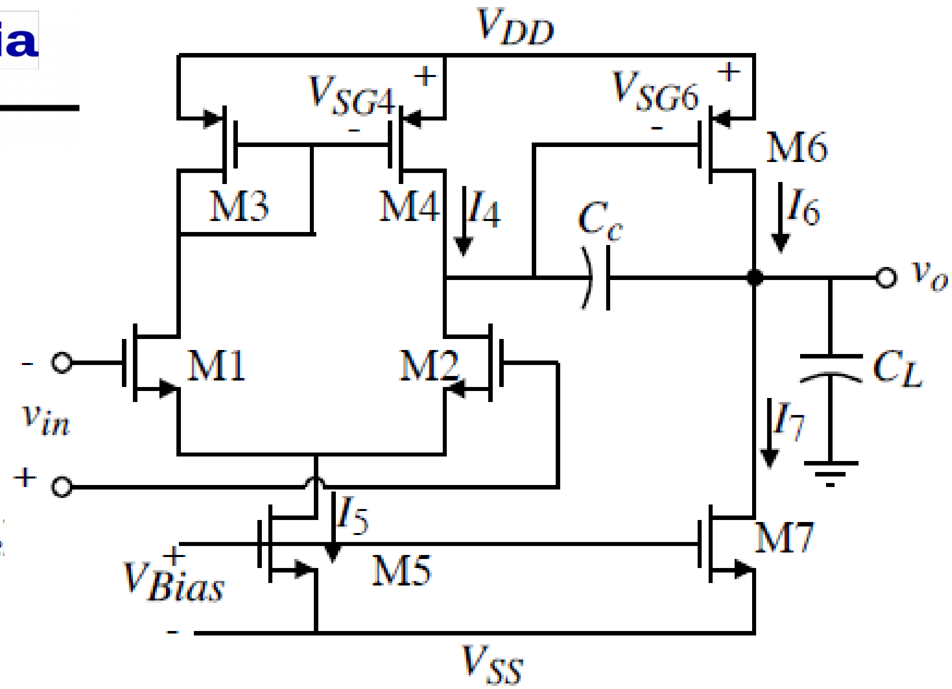
Equações de Projeto (Considerações)



Slew rate $SR = \frac{I_5}{C_c}$(Assuming $I_7 >> I_5$ and $C_L > C_c$

First-stage gain $A_{v1} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} = \frac{2g_{m1}}{I_5(l_2 + l_4)}$

Second-stage gain $A_{v2} = \frac{g_{m6}}{g_{ds6} + g_{ds7}} = \frac{g_{m6}}{I_6(l_6 + l_7)}$

Gain-bandwidth $GB = \frac{g_{m1}}{C_c}$

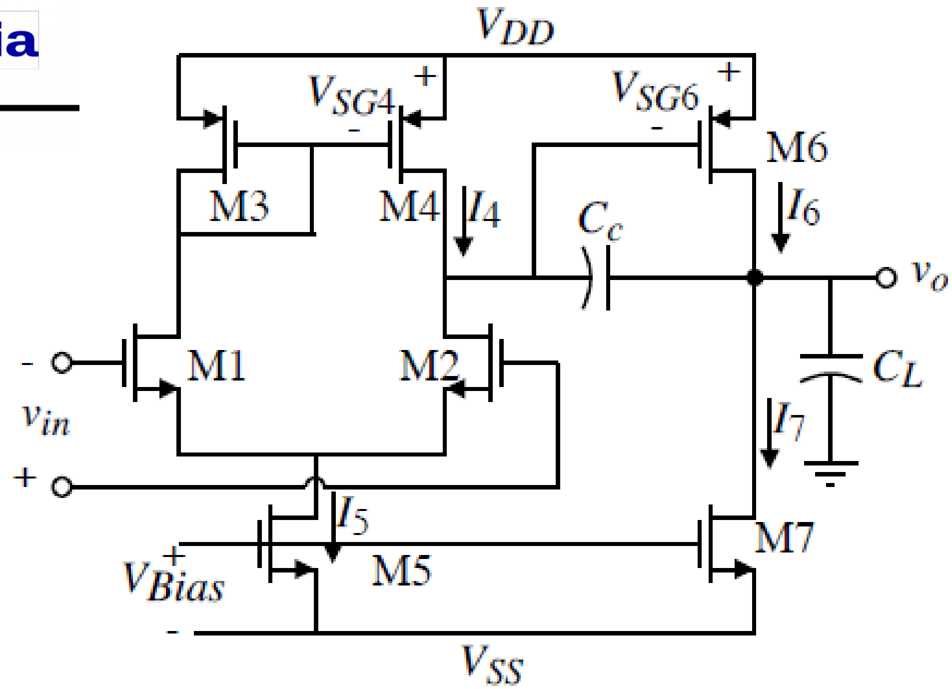
Output pole $p_2 = \frac{-g_{m6}}{C_L}$

RHP zero $z_1 = \frac{g_{m6}}{C_c}$

60° phase margin requires that $g_{m6} = 2.2g_{m2}(C_L/C_c)$ if all other roots are ≥ $10GB$.

Positive ICMR $V_{in(max)} = V_{DD} - \sqrt{\frac{I_5}{b_3}} - |V_{T03}|_{(max)} + V_{T1(min)})$

Negative ICMR $V_{in(min)} = V_{SS} + \sqrt{\frac{I_5}{b_1}} + V_{T1(max)} + V_{DS5}(\text{sat})$



Etapas de Projeto

1 - $C_c > 0.22 C_L$

2 - $I_5 = SR \cdot C_c$

3 - $S_3 = \dfrac{I_5}{K'_3[V_{DD} - V_{in}(\max) - |V_{T03}|(\max) + V_{T1}(\min)]^2}$

4 - $g_{m1} = GB \cdot 2\pi \cdot C_c \rightarrow S_2 = \dfrac{g_{m1}^2}{K'_1 I_5}$

5 - $V_{DS5}(\mathrm{sat}) = V_{in}(\min) - V_{SS} - \sqrt{\dfrac{I_5}{\beta_1}} - V_{T1}(\max) \geq 100\ \mathrm{mV}$

$\beta = K.S$

6 - $S_5 = \dfrac{2I_5}{K'_5[V_{DS5}(\mathrm{sat})]^2}$

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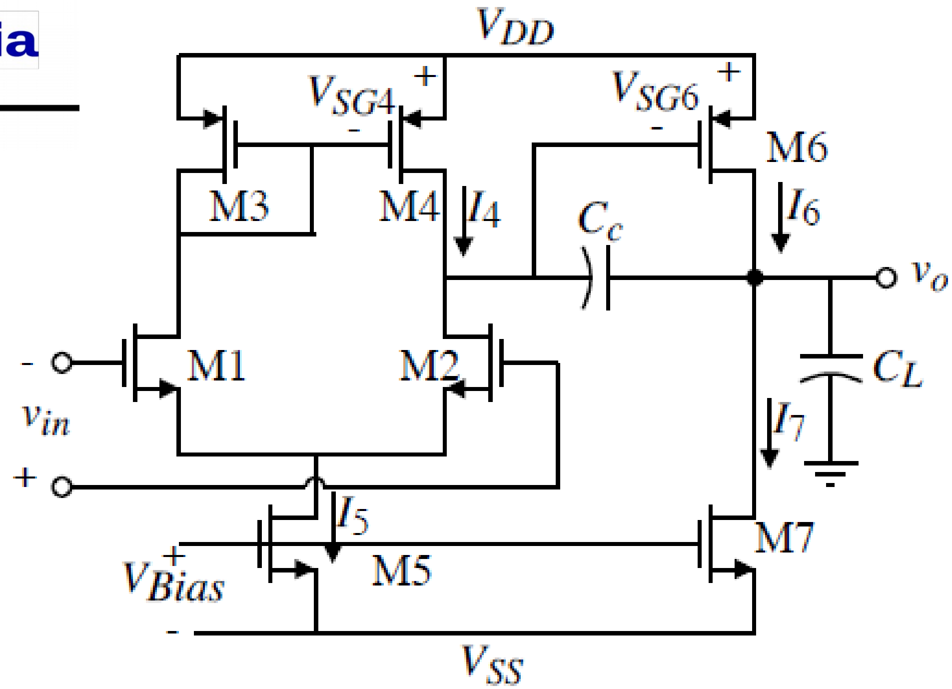

Etapas de Projeto

7 - $g_{m6} \geq 10 g_{m1}$

$g_{m4} = \sqrt{2K_P' S_4 I_4}$

8 - $S_6 = \frac{g_{m6}}{g_{m4}} S_4$

9 - $I_6 = \frac{g_{m6}^2}{2K'_6 S_6}$

10 - $S_7 = (I_6/I_5) S_5$

11 - $P_{diss} = (I_5 + I_6)(V_{DD} + |V_{SS}|)$

12 - $A_v = \frac{2 g_{m2} g_{m6}}{I_5(l_2 + l_4) I_6(l_6 + l_7)}$

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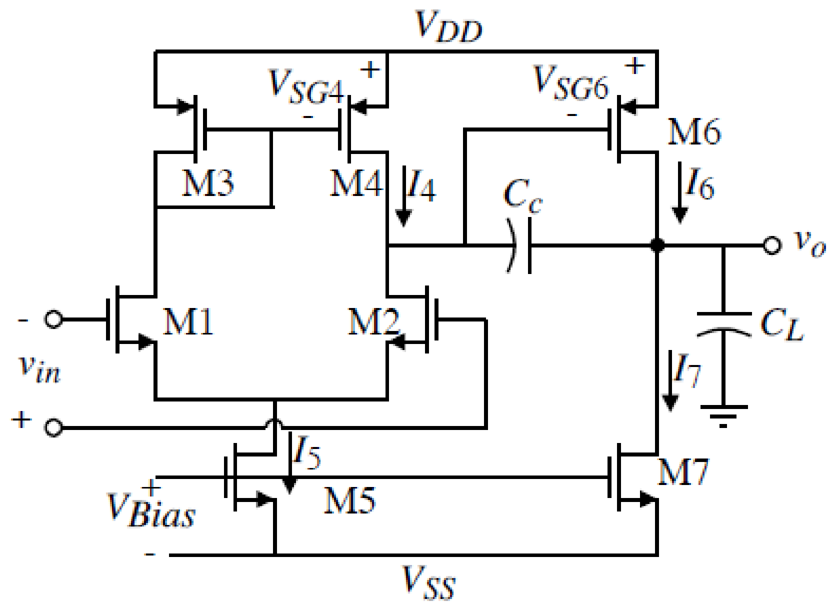
Amp. Op. de 2 Estágios

Exercício



➢ Projete um Amp. Op de 2 Estágios com as seguintes especificações:

Av > 3000 V/V	VDD = 1,8v
Margem de fase 60°	0,5>Vout range>1,3V
GB = 5MHz	SR > 4V/us
ICMR = 0,9V a 1,3V	Pdiss $\leq$ 2mW

➢ Dados da tecnologia:

Vtn = 0,397V	$\lambda_N = 0{,}06V^{-1}$
Vtp = 0,457V	$\lambda_P = 0{,}08V^{-1}$
Kn = 593uA/V^2	Cox = 8,82E-15 F/um2
Kp = 216uA/V^2	

➢ Demais dados de projeto:

C_L = 2pF
Lmin e Wmin = 0,5um

Referências

➢ Phillip Allen, Douglas Holberg, " CMOS Analog Circuit Design", **Capítulo 6** Oxford, 2a ed., 2002.