a ranked alphabet

arity 2

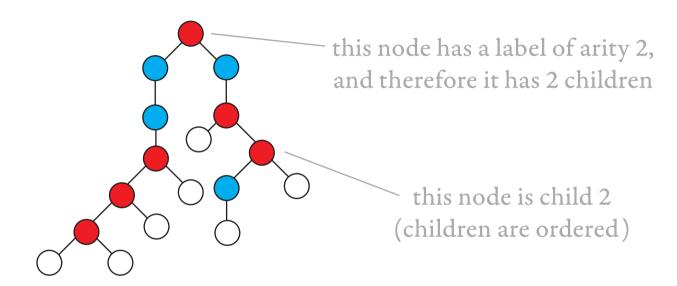


arity 1



arity 0

a tree







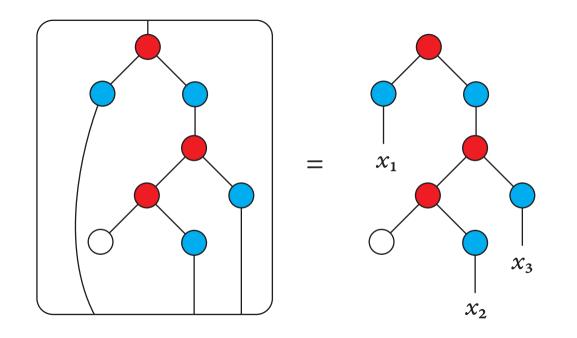


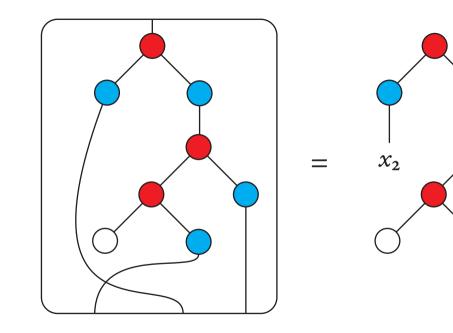


substitute(t)

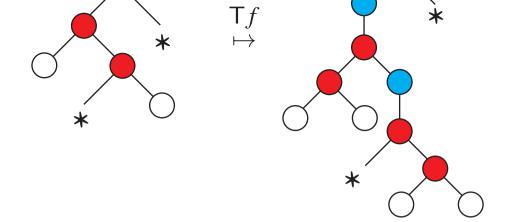


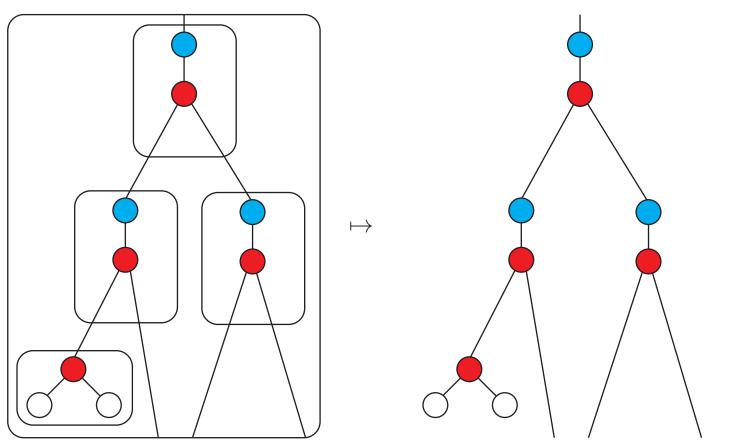






 x_1











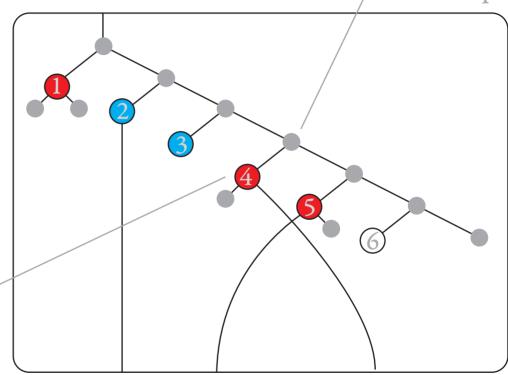
input

3 6

number the non-port nodes in the input term according to their appearance in the pre-order traversal

use a copy of the corresponding node, with edges to the ports inherited, and other edges plugged by •

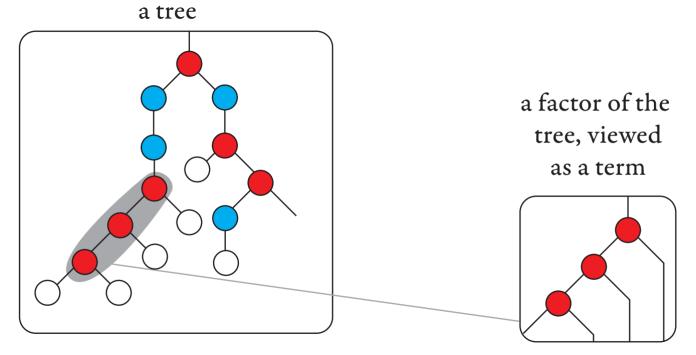
create a binary node for each non-port node in / the input term



output

a factorisation equivalence



















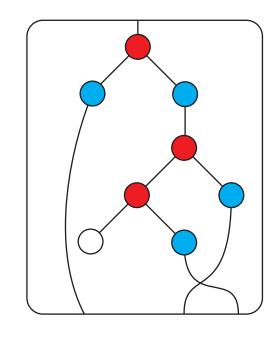




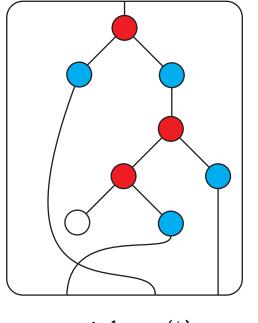








If the root has arity n, and $1 \le i < j \le n$, then all ports of the *j*-th subterm of the root are after all ports of the *i*-th subterm of the root

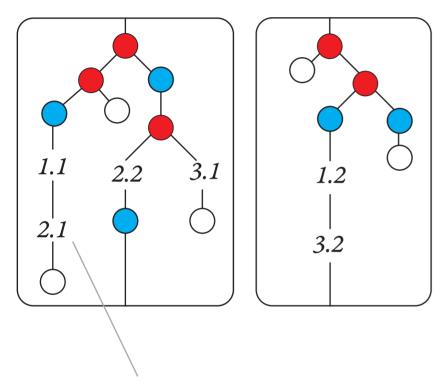


satisfies (*)

violates (*)

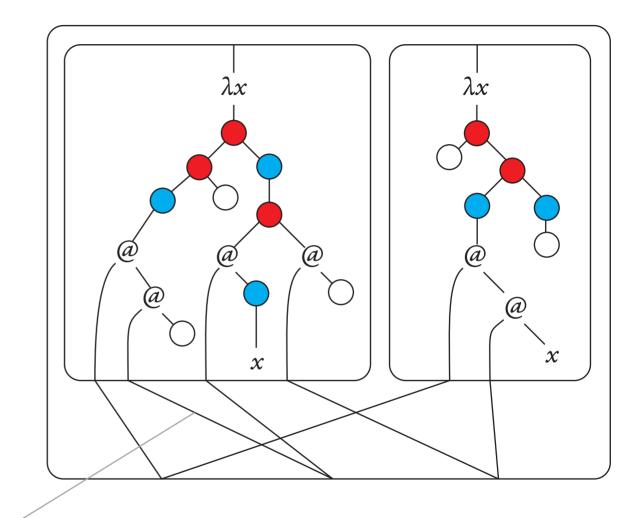
a register update

its dual

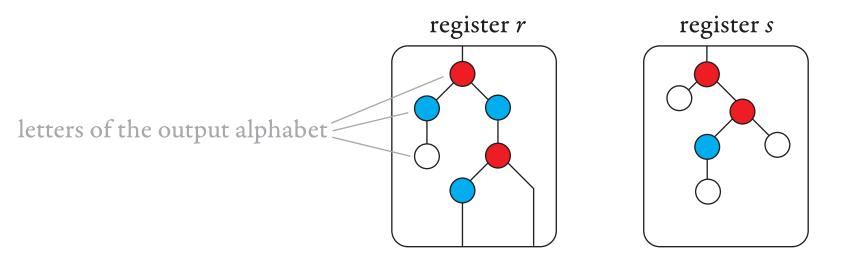


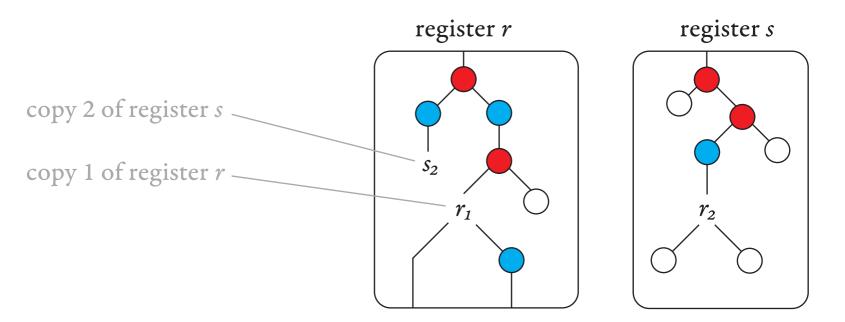
Variable *i.j* represents register *i* in the *j*-th argument of the reigster update.

In the dual, this variable is mapped to the *i*-th edge which enters the *j*-th port of the reducer.

















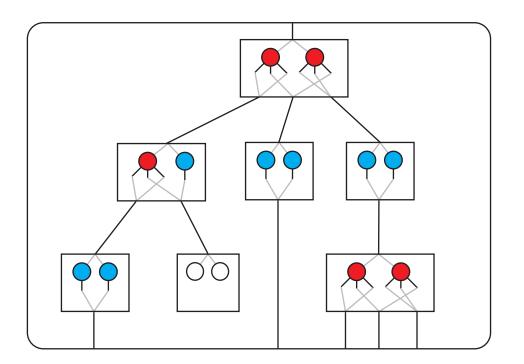


factors with branching nodes

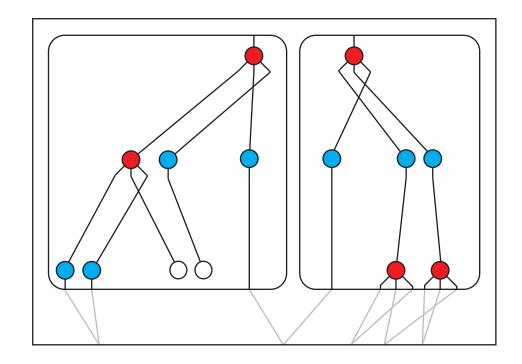


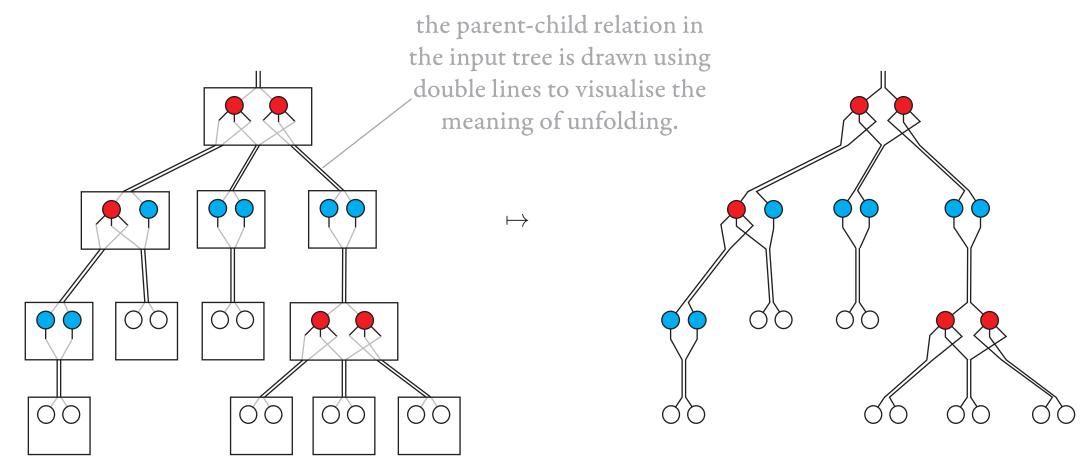


input



output















λ-term of type *o*



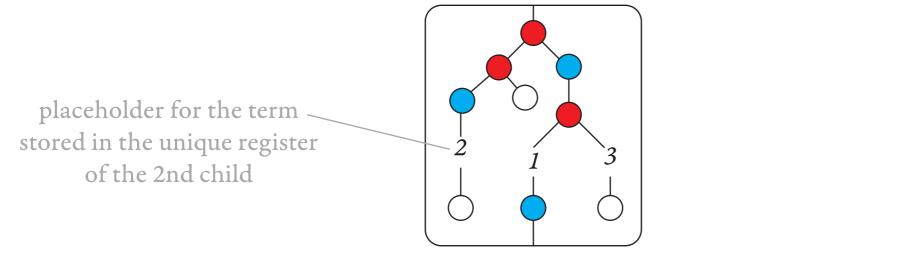




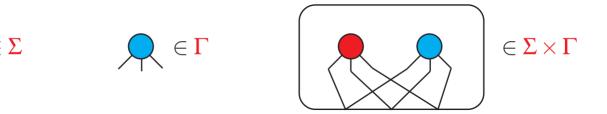
 λx .



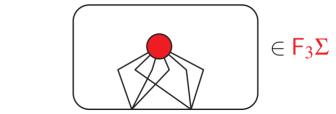












 $\in {\color{red}\Sigma}$

