Design of a Planar Transformer

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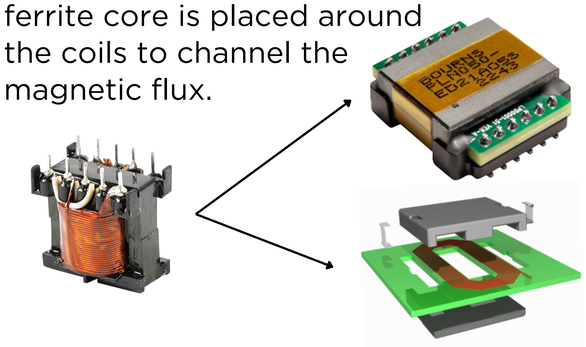
What is it?

Instead of the typical copper wire wound transformers that we have been using this semester, planar transformers utilize flat windings that are printed on a single circuit board. The copper traces are are routed circularly on each layer of the PCB to form the transformer coils, while a ferrite core is placed around the coils to channel the magnetic flux.

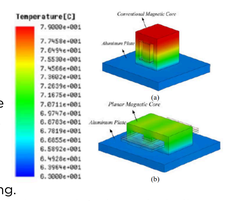


Traditional vs. Planar

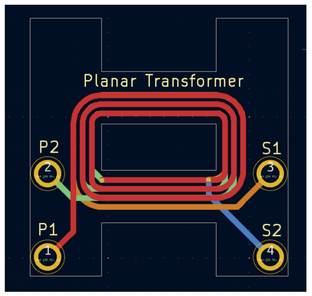
Wire Wound	
Advantages	Disadvantages
• Lower parasitic capacitance • Easier prototyping/testing • More research/knowledge available	• Tall height • Higher resistance and poorer thermal management • Higher leakage inductance • Potential inaccuracies in repeatability

Planar	
Advantages	Disadvantages
• **Greater efficiency** [1] • Low profile; small volume [2] • Improved thermal management • Repeatability [3] • Low leakage inductance [4] • Higher power density • Lower EMI; less noise [5]	• Larger footprint/surface area • Higher parasitic capacitance [6] • Low copper fill factor [7] • Difficulty prototyping

1. Given their larger surface-to-volume ratio, planars tend to have greater efficiency and higher power density because there is less space for heat to build up, resulting in lower overall energy losses.
2. Given the smaller footprint compared to traditional transformers, planars are space saving, freeing up space for more components or condensing the design overall.
3. Thanks to the planar being embedded into a PCB, it is quite simple to have a practically identical planar manufactured, whereas there is more error introduced into the system via traditional transformer manufacturing.
4. Given the nature of the planar PCB, it is much easier to achieve an interleaved winding, providing for a lower leakage inductance and improved efficiency.
5. With the thinner and wider copper windings, the skin and proximity effects due to high frequencies are reduced, in addition to EMI and noise.
6. This decreases the number of turns possible. We can increase the number of turns/layers by decreasing the width, but the tradeoff is more winding loss.
7. Since the wider conductors are stacked closer together, there is more surface area touching between two given conductors, leading to higher winding capacitances.

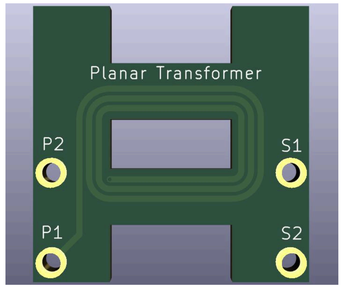


KiCad Layout



Transformer layout in KiCad

We laid out our planar transformer design in KiCad. Our final design consists of a 4-layer board, with the primary winding turns routed on the first and second layers, the secondary winding routed on the third layer, and the fourth used for pinout routing.



3D render of PCB

Design Calculations

We chose to use a Planar E E18 core, as it has a low profile and fits well in our lab hardware footprint. We decided on a track spacing of 0.3mm. We then maximized the width of our traces to fit on a 4 layer board and used 2oz copper to reduce temperature rise, resulting in a track width of 0.53mm. Calculations for individual transformer parameters can be seen to the right.

Primary Turns

$$N_1 = \frac{V_{in} D}{2 f_s B_{max} A_e} = 5$$

Secondary Turns

$$N_2 = \frac{N_1 V_{out}}{V_{in}} = 3$$

Magnetizing Inductance

$$L_{primary} = \frac{V_{in} D^2}{2 P_{out} F_s} = 18uH$$

Air Gap

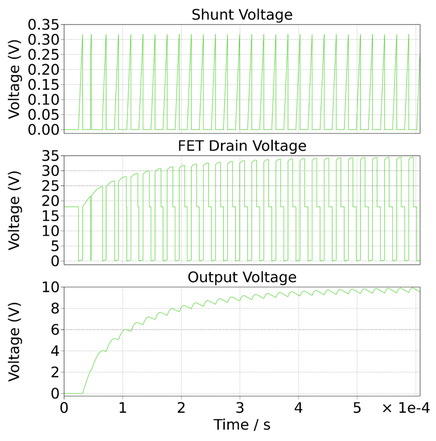
$$L_e = \frac{\mu_0 N_1^2 A_e}{L_{primary}} = 2.46thou$$

Vin = input voltage, 18V
D = duty cycle, 0.35
fs = switching frequency, 50kHz
$Bmax$ = maximum flux density, 0.3T
Ae = effective cross-sectional area, 39.5mm^2
$Vout$ = output voltage, 10V
$Pout$ = output power, 20W
uo = permeability of free space, 4πe-7 N/A^2

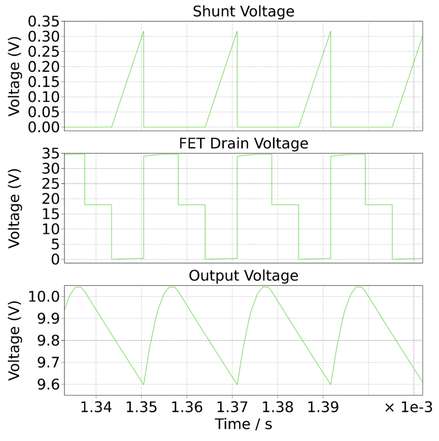
Planar E E/18 Core

PLECS Simulation

To verify our design, we simulated our planar transformer design using a PLECS model of our lab hardware. Our initial simulation results show waveforms similar to our wire wound transformer, verifying our parameters. A next step for our simulation would include modelling the parasitic capacitance and leakage inductance of the transformer to more accurately model the hardware.



Simulated waveforms at startup



Waveforms at steady-state

Additional Calculations

Parasitic Capacitance

Parasitic capacitance calculations are considerably difficult to do accurately. These are approximate calculations.

$$C_0 = \varepsilon_0 \varepsilon_r \frac{A}{d}$$

$$C_d = \frac{(n+1)(2n+1)}{12n} C_0$$

$$C_w = \frac{4(m-1)}{m^2} C_d$$

ε_0 = permittivity of free space, 8.854e-12 F/m
ε_r = relative permittivity of material between two conductors (FR4 = 4.8)
A = overlapping area
d = separated distance

C_0 = capacitance of two PCB traces with overlapping areas
C_d = capacitance between two layers with n turns
C_w = capacitance with m layers in series for the same winding

The parasitic capacitance that we calculated was 0.0198 pF, which seems reasonable.

Leakage Inductance

$$H = \frac{F}{b_w} = \frac{NI}{b_w}$$

$$E/v = \frac{1}{2} BH = \frac{1}{2} \mu_0 H^2$$

$$E = \frac{1}{2} L I^2 \therefore L_L = 2E/I^2$$

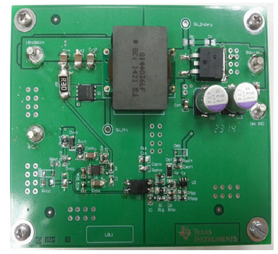
b_w = winding breadth
B = flux density
μ_0 = permeability of free space
N = number of primary turns
I = RMS output current
H = field intensity
E/v = energy density
E = total energy

We calculated a leakage inductance of 2.2e-15 H, which is much smaller than that of our copper wire transformer, which was 8.9e-7 H. We would expect a very small leakage inductance due to the planar windings, but we are unsure if the calculated should be this negligible.

All calculations can be found in our GitHub.

Applications of Planars

Planar transformers are useful for low power, high power density applications. They are often used in flyback converters for their low leakage inductances, strong thermal performance, and low profile.



Flyback converter using a planar transformer

Sources & Design Files

Sources

GitHub