MADVLSI: Final Project Report

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In this project, we made a Harmonic-Cancelling Sine Wave Generator. The circuit contains three main components: a 16-bit shift register to generate offset square wave signals, a irrationally weighted DAC known as a harmonic-cancelling DAC (HC-DAC) to scale and sum these square wave signals to form an approximate sine wave signal, and an output filtering stage to remove remaining higher order harmonics in the sine wave signal to create a sine wave with high spectral purity. This report includes five main sections: an overview of the overall architecture of the circuit, schematic capture and simulation that shows the schematic diagram in xschem and transient simulation results, layout design in Skywater technology, a layout versus schematic (LVS) that compared the schematic and layout designs, and a link to the design files in the end.

1 Architecture Overview

Our circuit architecture creates a sine wave signal by first generating a set of phase shifted square wave signals. These square wave signals are then scaled by a set of irrational weights and are then summed to create an step-wise approximated sine wave signal. This method of creating an approximated sine wave signals does not include lower order harmonics, so only higher order harmonics need to be filtered out in the output stage. To remove these harmonics and improve the spectral purity of the signal, the approximated signal is put through an output low-pass filtering stage, smoothing out the waveform and removing higher order harmonics from the signal, leaving a high fidelity sine wave as the output of our circuit.

2 Implementation

2.1 High Level Schematic and Layout Design

The schematic diagram and the layout in Magic of the overall hardware architecture are shown in Figure 1 and Figure 2 respectively.

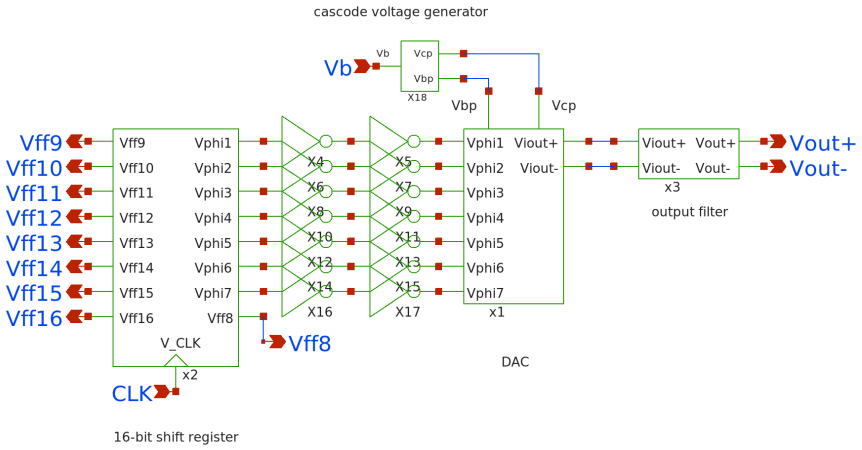


Figure 1: Complete schematic of the sine wave generator in Magic.

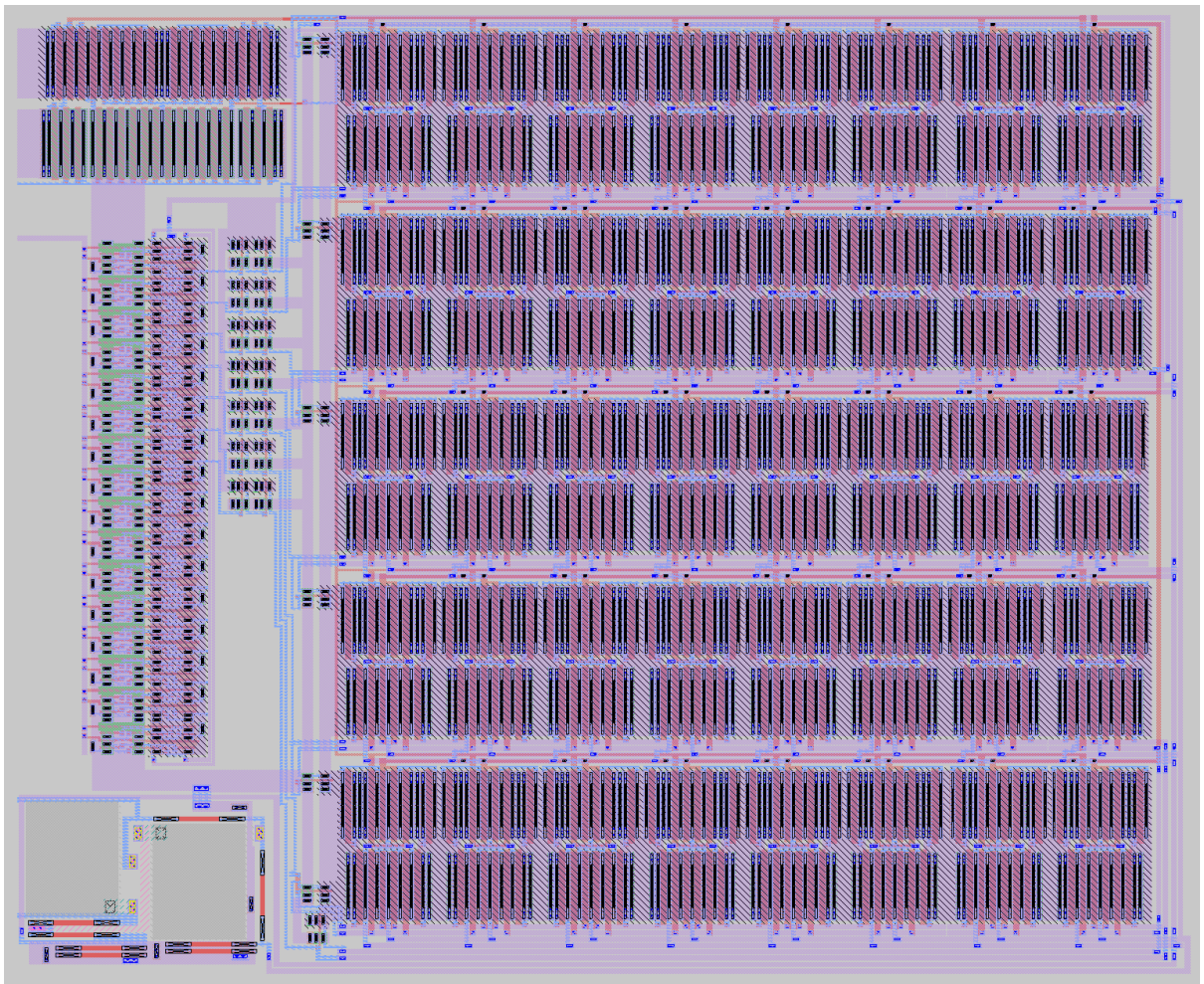
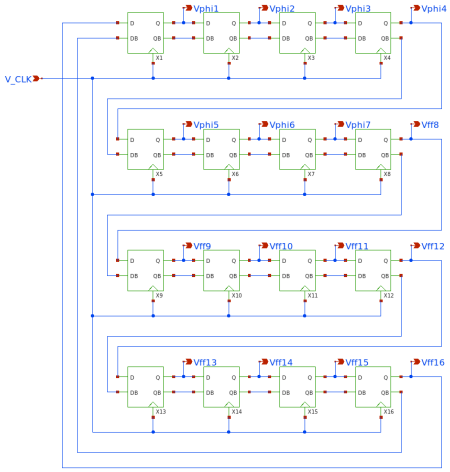


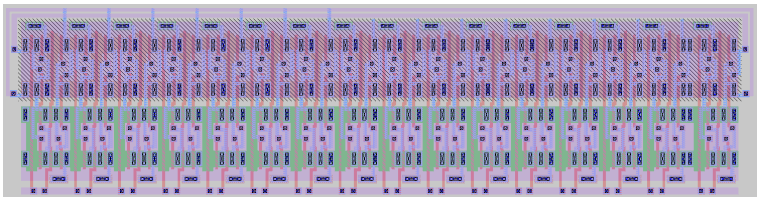
Figure 2: Complete layout of the sine wave generator in Magic.

2.2 Shift Register

Several different circuit elements were designed to implement each stage of this architecture. To create the phase shifted square wave signals, a 16-bit shift register was implemented. Half of these registers are initially set high to create a 16 stage square wave signal, and 7 consecutive register signals are sampled to generate 7 square signals, each phase shifted by one stage. These signals are then passed through a double-inverter buffer to remove signal artifacts. Figure 3 shows the schematic of the 16-bit shift register. Each flip-flop in the shift register utilizes the CSRL logic identical to the flip-flops designed in Mini Project 2.



(a) The schematic of the 16-bit shift register. Half of the flip-flops in the register are initially set high to generate phase offset square wave signals.



(b) Complete layout of the shift register.

Figure 3: Shift register implementation in (a) schematic and (b) layout.

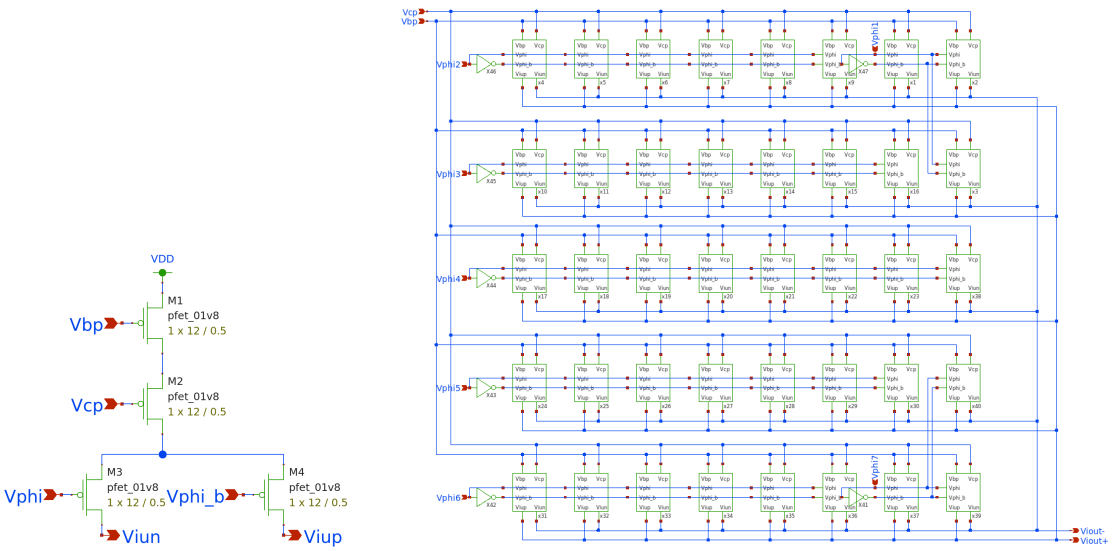
2.3 DAC

To scale and sum these signals, a 7-bit DAC with non-binary weighting was implemented. Instead of binary weights, the HC-DAC utilizes irrational weights for each signal selected to best approximate a sine wave shape when summed. The HC-DAC takes in the phase-shifted square wave signals, and scales and sums them to create an approximated sine wave signal.

The implemented DAC utilizes a current-steering architecture, which contains "unit-current" cells that control how the inputted signal is scaled. The more of these unit-current cells that are summed for a given signal, the larger the amplitude of the scaled signal will be. Figure 4 shows the schematics for the DAC.

2.4 Cascode Voltage Generator

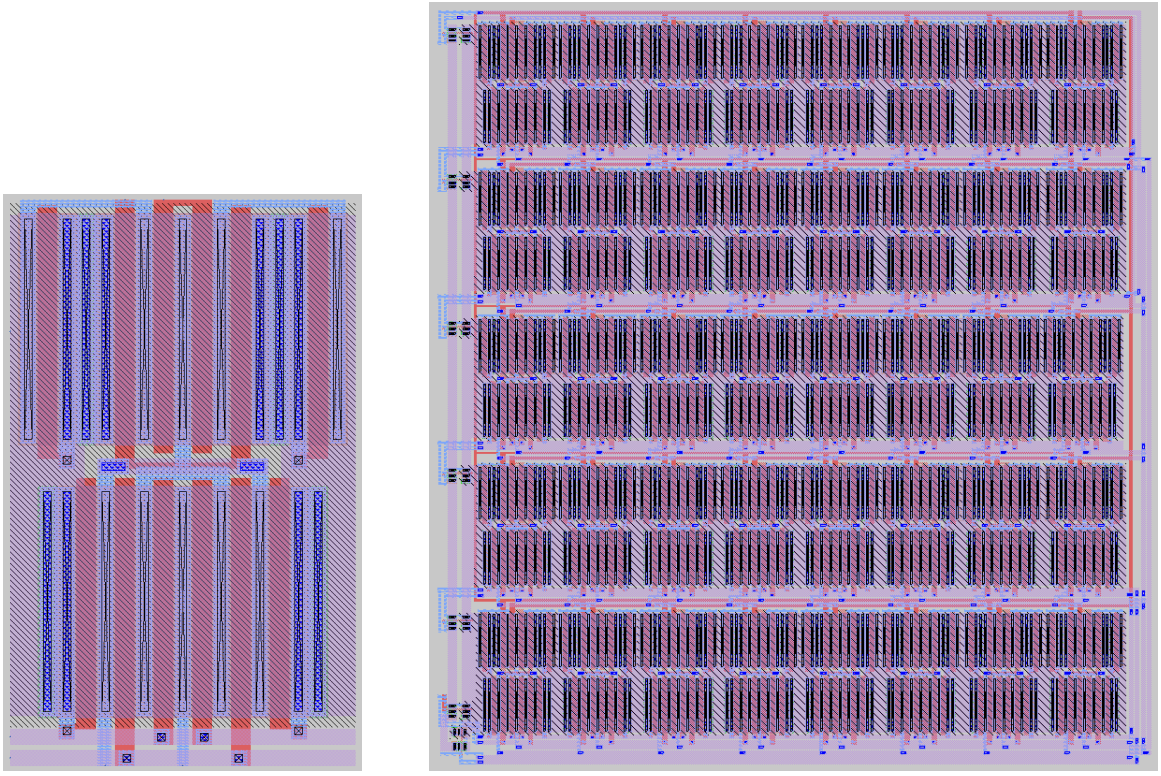
According to the unit current cells in the DAC in Figure 4, we need to fix the common node of the drains of M3 and M4 for the cells to function properly. Therefore, we attached a cascode voltage generator shown in Figure 6 to generate V_{bp} and V_{cp} from an input current source I_b.



(a) Transistor level schematic of a "unit-current" cell in the DAC.

(b) Schematic of the complete DAC. Each symbol represents a unit-current cell. The number of unit-current cells summed for each phi signal determines the amplitude of the scaled signal to be summed.

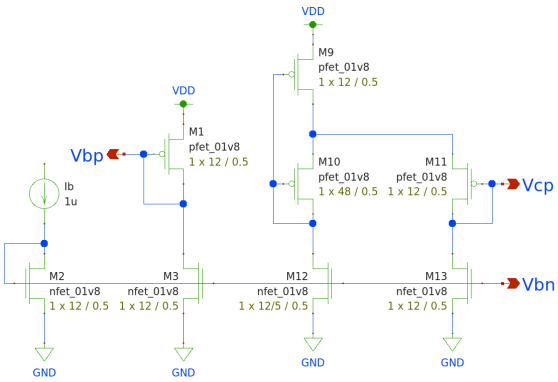
Figure 4: (a) Unit cell and (b) overall DAC implementation in xschem schematic.



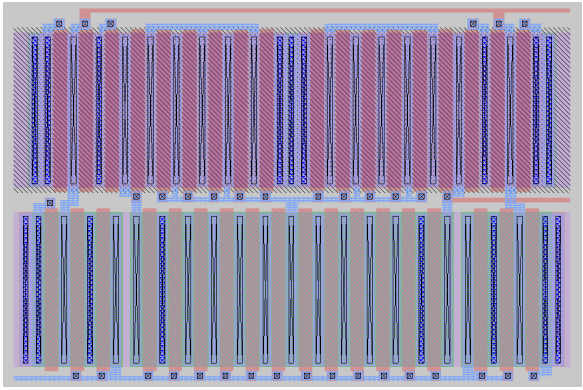
(a) Layout of a unit current cell in the DAC.

(b) Complete layout of the DAC.

Figure 5: Schematic capture and layout of the complete DAC.



(a) The schematic for the bias generator circuit, generating V_{bp} and V_{cp} for the HC-DAC.



(b) Layout of cascoded voltage generator.

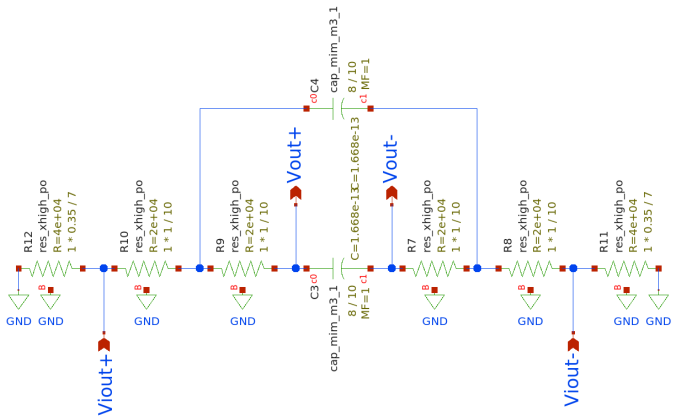
Figure 6: (a) Schematic and (b) layout of the cascode voltage generator

2.5 Output Filter

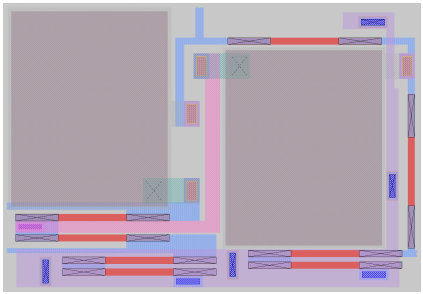
To remove higher order harmonics from this sine wave signal, the signal is then put through an output low-pass filtering stage, as shown in Figure 7. In the original design of the circuit, the first order RC filter values were primarily determined by the equation which defines the corner 3dB frequency:

$$3dB = \frac{1}{4\pi(R_{10} + R_{12})C} Hz.$$

In our system, we added a secondary RC low-pass filter in addition to this approach, and that gave us a decent quality of our output sine waves.



(a) Schematic capture of the second order output filter, which takes two input currents V_{iout+} and V_{iout-} to obtain a voltage difference for the capacitor $C4$. The final output sine wave voltage is the result of the difference across $C4$.



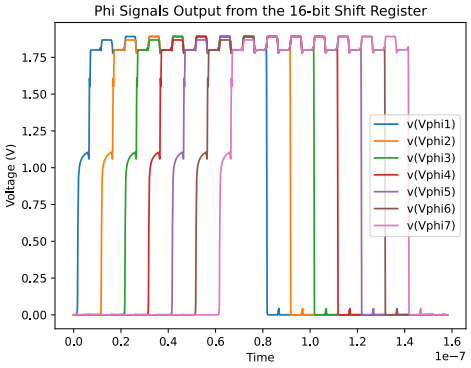
(b) Layout of the second order output filter.

Figure 7: Schematic capture and layout of the output filter.

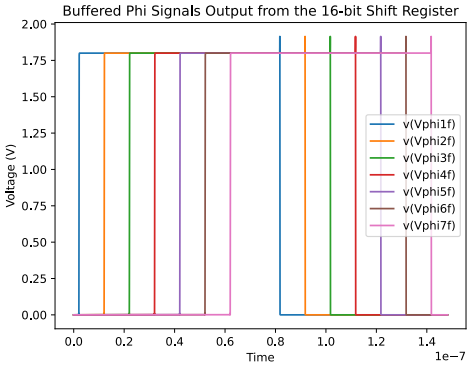
3 Simulation Results

3.1 Intermediate Testing Results

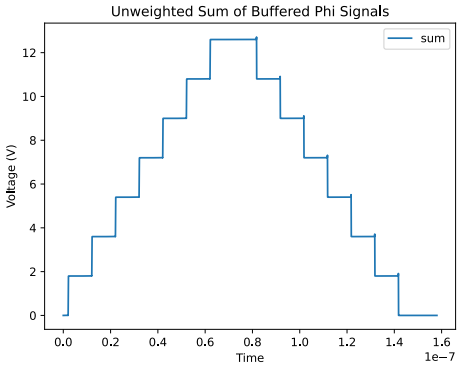
The labelled phi signals were then sampled over a transient simulation, resulting in the waveform shown in Figure 11a. To remove the "high" state signal artifacts from the phi signals, each signal was passed through a double-inverter buffer, resulting in the waveform shown in Figure 11b.



(a) Initial simulation results of the 16-bit shift register. Some signal artifacts are visible in the "high" state of these waveform due to the implemented CSRL logic.



(b) Buffered simulation results of the 16-bit shift register. The shown phi waveform now have a "high" state without artifacts.

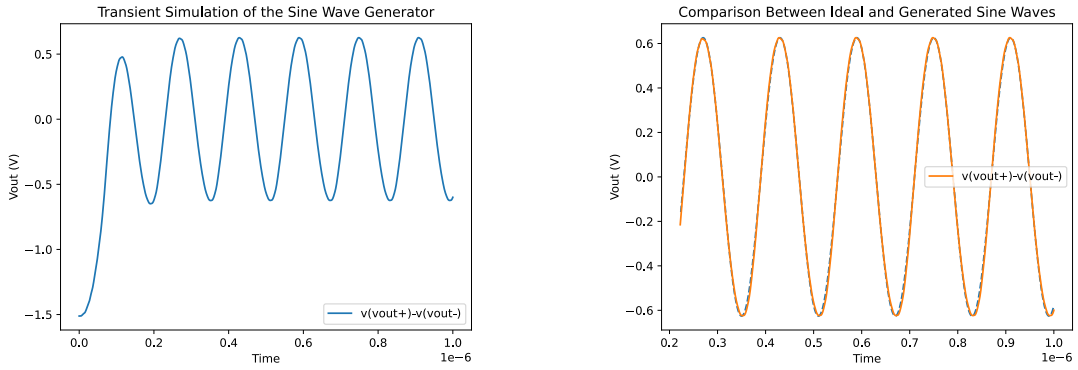


(c) Unweighted sum of the first 7 Vphi signals that makes up a triangular wave.

Figure 8: (a) Raw Vphi signals coming from the 16-bit shift register, (b) buffered Vphi signals, and (c) the sum of all seven Vphi signals coming out of the buffers.

3.2 Transient and Monte Carlo Simulations on the Circuit Schematic in Xschem

The transient and Monte Carlo simulation results are shown in Figure 9 and Figure 10.



(a) Transient simulation results of the sine wave generator.

(b) Comparison between ideal and cleaned generated sine waves.

Figure 9: Transient simulation results.

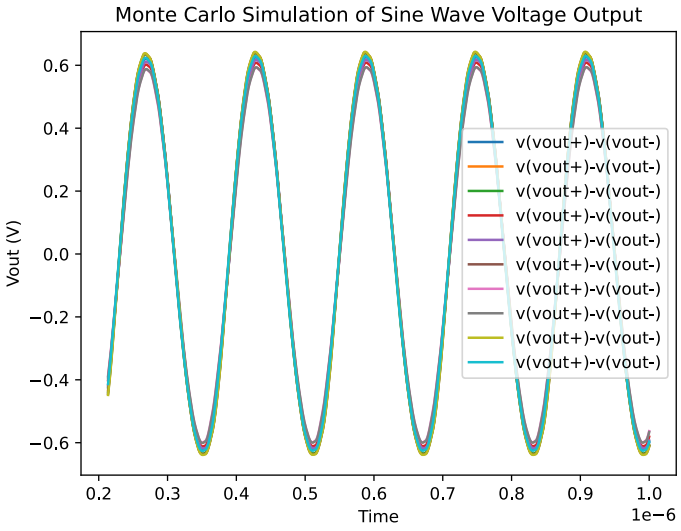
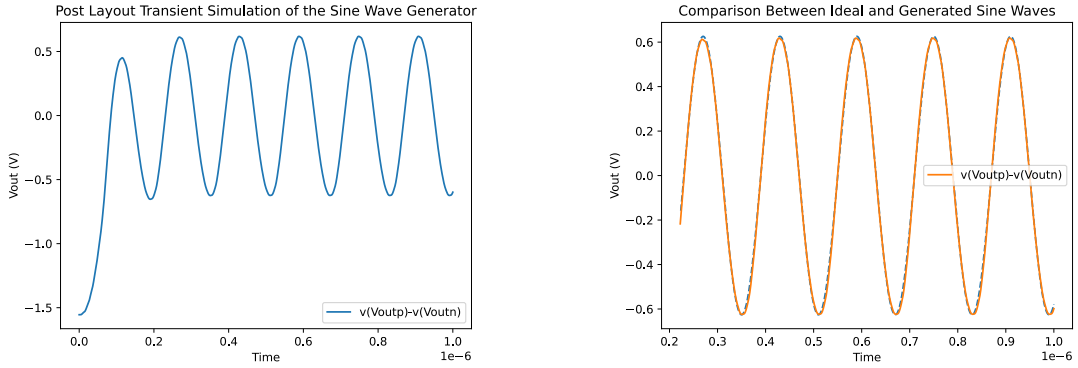


Figure 10: Cleaned Monte Carlo simulation results from the xschem schematic. This graph shows some inconsistencies especially at the maximum and minimum values over a period of the sine wave.

3.3 Post Layout Simulations

Figure 11 and Figure 12 showed our test-harness results from the post-layout simulations. The results did not show significant differences compared to the schematic simulations.



(a) Transient simulation results of the sine wave generator made in Magic layout.

(b) Comparison between ideal and cleaned generated sine waves.

Figure 11: Post-layout transient simulation results.

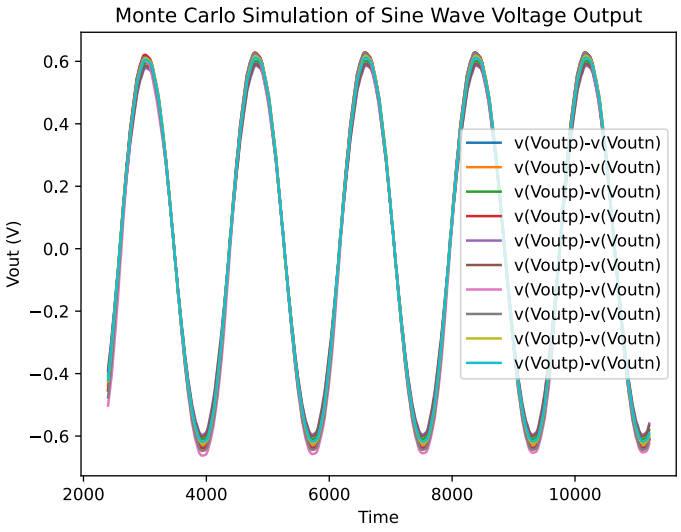


Figure 12: Post-layout Monte Carlo simulation results.

4 Potential Future Steps

Given the limited duration of time to spend on this project, we have not performed profound and quantitative analysis regarding the output signal quality of the sine wave generator. Some potential future steps on this project involve sweeping the circuit at different input clock frequencies and test its performances, as well as analyzing the harmonic distortion coefficients that we extracted from the generated sine waves.

5 Layout Versus Schematic

The layout versus schematic (LVS) output can be accessed here. The results showed that the netlists matched uniquely. The property errors are caused by the device model information regarding the P-Poly Precision resistors.

6 Design files

All the design files of this project can be accessed here.