MINISTRY OF EDUCATION AND RESEARCH
OF THE REPUBLIC OF MOLDOVA
Technical University of Moldova
Faculty of Computers, Informatics and Microelectronics
Department of Software and Automation Engineering

Report
Computer Architecture

Laboratory work no. 1

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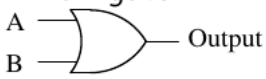
DISA, FCIM, UTM

Chișinău – 2023

Solutions:

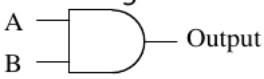
1.

OR gate

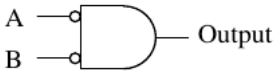


A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1

AND gate

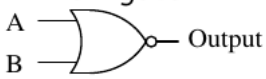


A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1



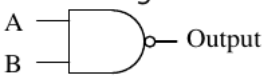
A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

NOR gate

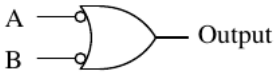


A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

NAND gate

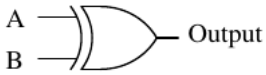


A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

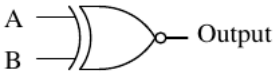


A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

EX-OR

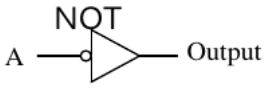


A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0



A	B	Output
0	0	1
0	1	0
1	0	0
1	1	1

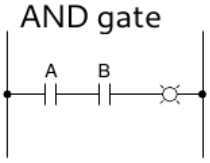
NOT



A	Output
0	1
1	0

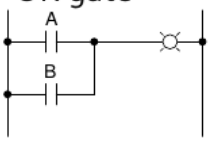
2.

AND gate



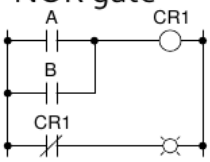
A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1

OR gate



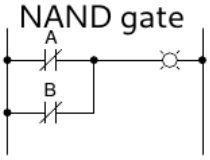
A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1

NOR gate



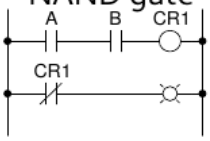
A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

NAND gate



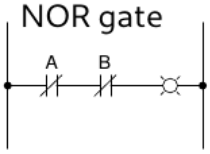
A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

NAND gate

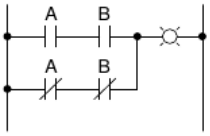


A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

NOR gate

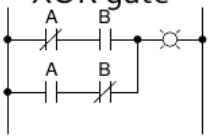


A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0



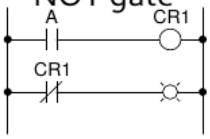
A	B	Output
0	0	1
0	1	0
1	0	0
1	1	1

XOR gate



A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

NOT gate



A	Output
0	1
1	0

3.

AB \ C	0	1
00	1	1
01	0	1
11	0	0
10	0	1

4.

AB \ CD	00	01	11	10
00	0	1	0	0
01	0	1	0	0
11	0	1	1	0
10	0	1	1	1

5. Only A and C change. B and D remain constant.

6. I noticed that this Karnaugh Map depends only on A and B. C and D can be any value, and the resulting expression will not be influenced.
(ABC'D' + ABC'D) + (ABCD + ABCD')=
(ABC') + (ABC) =
AB

7.

AB \ CD	00	01	10	11
00	0	0	0	0
01	0	1	0	1
10	0	0	0	0
11	0	1	0	1

In this notation it is very hard to spot clusters of bits and group them together to define an expression. The Gray notation is more useful for this. Here I can say that B and D remain the same in all conditions.

8.

AB \ CD	00	01	11	10	00	01	11	10
00	1	0	0	1	1	0	0	1
01	0	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0	0
10	1	0	0	1	1	0	0	1
00	1	0	0	1	1	0	0	1
01	0	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0	0
10	1	0	0	1	1	0	0	1

Yes, it becomes apparent.
We can group the expressions together, resulting in: **D'B'**

9. The mistake was made by not seeing the case when A'B'C, therefore making a huge mistake. A proper grouping should look like this by the following scenario. Group two elements and then one: **AC + A'BC**

10.

- select only 1s
- groups may be only in horizontal or vertical
- groups must be selected in a number of 2^n
- groups may overlap
- groups may wrap around the table (like a sheet of paper)

11. BD' + DC'B' + D'C'A' + D'CA

12. It is possible. The appropriate POS expression is:
(A' + B')
The difference between SOP and POS, is that in POS we group up zeroes, not ones. This is being achieved by selecting a group, getting the complement of this expression, and use OR instead of AND, and AND instead of OR.

13. The SOP expression is BC’

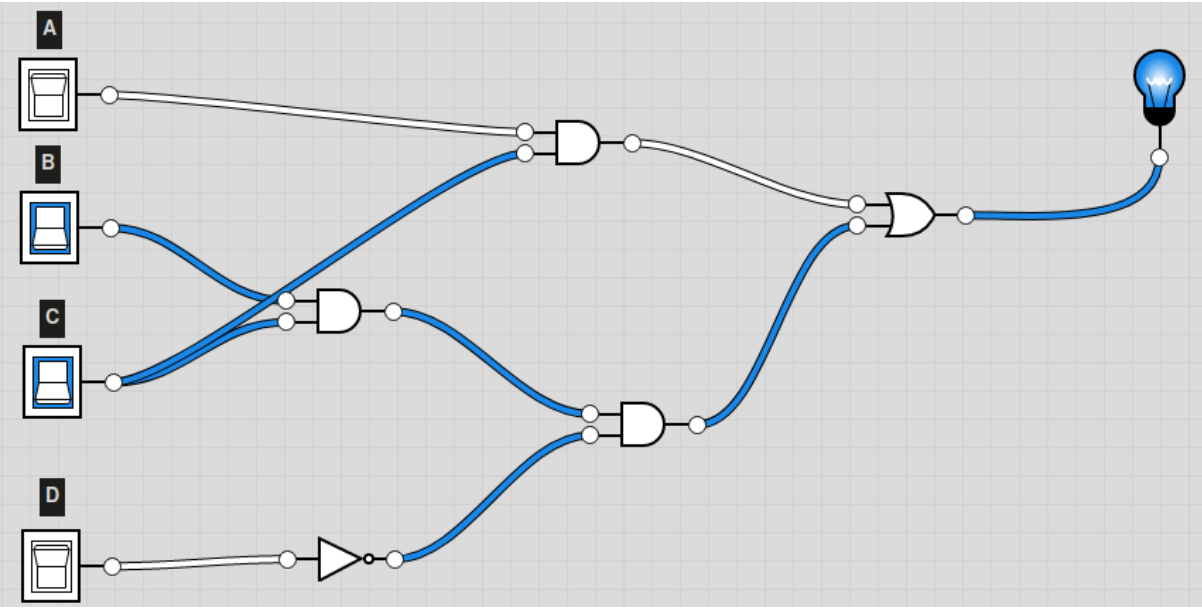
y_0		AB			
		00	01	11	10
C	0	0	1	1	0
	1	0	0	0	0

14. The Karnaugh map:

y_0		AB			
		00	01	11	10
CD	00	0	0	0	0
	01	0	0	0	0
	11	0	0	1	1
	10	0	1	1	1

The simple Boolean expression is: **BCD’ + AC**

Gate Circuit equivalent:

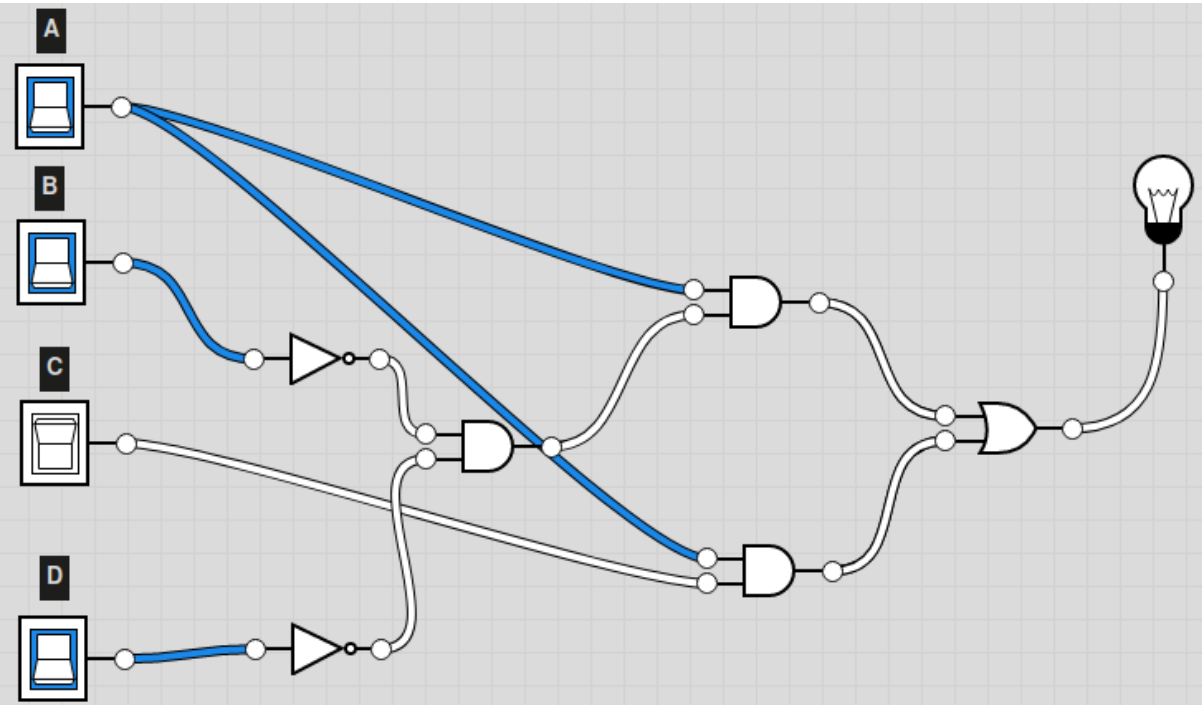


15. The Karnaugh map:

y_0		AB			
		00	01	11	10
CD	00	0	0	0	1
	01	0	0	0	0
	11	0	0	1	1
	10	0	0	1	1

The simple Boolean expression is: **AB’D’ + AC**

Gate Circuit Equivalent:

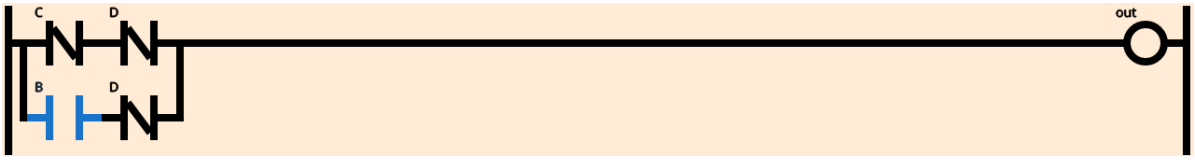


16. The Karnaugh map:

y_0		AB			
		00	01	11	10
CD	00	1	1	1	1
	01	0	0	0	0
	11	0	0	0	0
	10	0	1	1	0

The simple Boolean expression is: **C'D' + BD'**

Relay Circuit Equivalent:

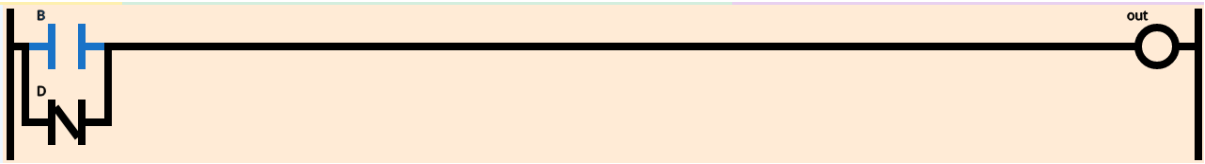


17. The Karnaugh map:

y_0		AB			
		00	01	11	10
CD	00	1	1	1	1
	01	0	1	1	0
	11	0	1	1	0
	10	1	1	1	1

The simple Boolean expression is: **D' + B**

Relay Circuit Equivalent:



Conclusion

In conclusion, the laboratory work was a valuable experience that allowed us to gain a deeper understanding of various important concepts in digital electronics. We explored the Karnaugh map, logic gates, relay logic functions, truth tables, Boolean algebra, and gate circuits, and saw how these elements can be used to build complex systems. The hands-on approach of the laboratory work made the learning process enjoyable and gave us a practical perspective on these abstract concepts. This work has equipped us with the tools and knowledge we need to tackle more advanced topics in digital electronics in the future. Overall, the laboratory work was a great way to solidify our understanding of these important concepts and prepare us for the challenges ahead.