dan.luu@gmail.com

SUMMARY

Background in hardware, software, and math. Experience in tools, prototyping, and hardware/software co-design.

EXPERIENCE

Microsoft, Engineer; Seattle, WA **2015 – Present**

- ◇ BitFunnel search engine. Near order of magnitude throughput/cost improvement *C++*
  - ○ Replaced largest and most complicated part of the system with 30LOC; 2x perf improvement
  - ○ Replaced poorly-understood ML configuration system with optimal mathematical formula
- ◇ Networking; multiple order of magnitude tail latency improvement *SystemVerilog*
  - ○ Half the latency of Amazon "enhanced networking"

Google, Engineer; Madison, WI **2013 – 2014**

- ◇ TPU (deep learning hardware accelerator); order of magnitude perf improvement over GPUs *SystemVerilog*
  - ○ Took project from requirements gathering stage (2 people) to full implementation stage (~20 people)

Recurse, Sabbatical; New York, NY **Spring 2013**

- ◇ Projects include channels and coroutines in C and a BitTorrent client in Scala.
- ◇ See https://github.com/danluu/ and http://danluu.com for more.

Centaur Technology (acquired by VIA), Member of Technical Staff; Austin, TX **2005 – 2013**

- ◇ x86 and ARM chip design and verification *Verilog / scripting languages*
- ◇ Other projects included formal verification, adding fault tolerance to a distributed system, post-silicon debug, test tooling, etc.

Ultrafast Optics and Fiber Communications Lab, Research Assistant; Lafayette, IN **2003 – 2005**

- ◇ Lab work, included speeding up parallel (256 wavelength) polarimeter by 40x *MATLAB and C*

IBM, Intern; Austin, TX **Summer 2003**

- ◇ Semi-formal / constrained random POWER6 completion unit functional verification *VHDL*

Micron Technology, Intern; Boise, ID **Summer 2002**

- ◇ Flash product engineering / characterization. Automated previously manual tasks. *Perl*

Spatial Systems Research Laboratory, Research Assistant; Madison, WI **2001**

- ◇ Studied tilings and related combinatorial models, e.g., alternating sign matricies and square ice

EDUCATION

BS Math & CMPE (Wisconsin, '00-'03), MS EE (Purdue, '03-'05)

NON-WORK PROJECTS

- ◇ Sega system on FPGA *https://github.com/danluu/sega-system-for-fpga*
- ◇ Randomized algorithms can beat LRU/psuedo-LRU caches: *http://danluu.com/2choices-eviction/*
- ◇ A fuzzer written in an hour that found ~20 bugs in Julia *https://github.com/danluu/Fuzz.jl*
- ◇ Web performance benchmarks for slow/flaky connections *http://danluu.com/web-bloat/*
- ◇ Formal verification of a secure hypervisor model *https://github.com/danluu/secvisor-formal-verification*
- ◇ See *https://github.com/danluu/* and *http://danluu.com* for more!

MISCELLANEOUS

- ◇ Work Authorization: U.S. Citizen