dan.luu@gmail.com

## SUMMARY

Background in hardware, software, and math. Experience in tools, prototyping, and hardware/software co-design.

## EXPERIENCE

**Microsoft, Engineer; Seattle, WA** **2015 – Present**

- ◇ Networking; mutiple order of magnitude tail latency improvement *SystemVerilog*
  - ○ Half the latency of Amazon "enhanced networking"
- ◇ BitFunnel search engine. Near order of magnitude throughput/cost improvement *C++*

**Google, Engineer; Madison, WI** **2013 – 2014**

- ◇ TPU (deep learning hardware accelerator); order of magnitude perf improvement over GPUs *SystemVerilog*
  - ○ Took project from requirements gathering stage (2 people) to full implementation stage (~20 people)

**Recurse, Sabbatical; New York, NY** **Spring 2013**

- ◇ Projects include channels and coroutines in C and a BitTorrent client in Scala.
- ◇ See https://github.com/danluu/ and http://danluu.com for more.

**Centaur Technology (acquired by VIA), Member of Technical Staff; Austin, TX** **2005 – 2013**

- ◇ Here's one particular six-month project (adding an ARM front-end to our x86):
  - ○ Helped reverse engineer the ARMv7 ISA (this was pre-AArch64)
  - ○ Created architectural simulator and got Android running on it *C*
  - ○ Implemented 1/2 of the translator, and wrote associated microcode *Verilog / Templating language*
  - ○ Created test generator that found 90% of the first 1000 bugs on the project *F#*
- ◇ Other roles (often brief) included formal verification, adding fault tolerance to a distributed system, post-silicon debug, test tooling, etc.

**Ultrafast Optics and Fiber Communications Lab, Research Assistant; Lafayette, IN** **2003 – 2005**

- ◇ Lab work, included speeding up parallel (256 wavelength) polarimeter by 40x *MATLAB and C*

**IBM, Intern; Austin, TX** **Summer 2003**

- ◇ Semi-formal / constrained random POWER6 completion unit functional verification *VHDL*

**Micron Technology, Intern; Boise, ID** **Summer 2002**

- ◇ Flash product engineering / characterization. Automated previously manual tasks. *Perl*

**Spatial Systems Research Laboratory, Research Assistant; Madison, WI** **2001**

- ◇ Studied tilings and related combinatorial models, e.g., alternating sign matricies and square ice

## EDUCATION

**BS Math & CMPE (Wisconsin, '00-'03), MS EE (Purdue, '03-'05)**

## NON-WORK PROJECTS

- ◇ See https://github.com/danluu/ and http://danluu.com for an exhaustive list
  - ○ Sega system on Xilinx Vertex FPGA; translated Z80 instructions into RISC $\mu$ops *Verilog and VHDL*
  - ○ Experiments with a randomized algorithm as cache eviction policy *Dinero IV and SPEC*
  - ○ A fuzzer written in an hour that found ~20 bugs in the Julia compiler and base libraries *Julia*
  - ○ Misc. experiments in deep learning *MATLAB and Octave*
  - ○ Formal verification of a secure hypervisor model *ACL2*

## MISCELLANEOUS

- ◇ Languages: English mother tongue. Once-fluent Vietnamese. Once-functional (now moribund) Japanese and French. Willing (and eager) to learn any language
- ◇ Work Authorization: U.S. Citizen