

## EXPERIENCE

- Recurse, Sabbatical; New York, NY** **Summer 2017**
- Microsoft, Engineer; Seattle, WA** **2015 – 2017**
- ◊ BitFunnel search engine; near order of magnitude throughput/cost improvement *C++*
    - Found an algorithmic simplification, reducing largest and most complicated part of the system to 30LOC
    - Replaced poorly-understood ML config system with optimal mathematical formula; 2x perf improvement
  - ◊ SmartNIC; multiple order of magnitude tail latency improvement *SystemVerilog*
    - Half the latency of Amazon “enhanced networking”
- Google, Engineer; Madison, WI** **2013 – 2014**
- ◊ TPU (deep learning hardware accelerator); 2nd person on project
    - Order of magnitude performance improvement over GPUs
    - <https://www.google.com/patents/WO2016186801A1>
    - <https://www.google.com/patents/US20160342889>
- Recurse, Sabbatical; New York, NY** **Spring 2013**
- Centaur Technology (acquired by VIA), Member of Technical Staff; Austin, TX** **2005 – 2013**
- ◊ Here’s one sample six-month project (adding an ARM front-end to our x86):
    - Helped reverse engineer the ARMv7 ISA (this was pre-AArch64)
    - Created architectural simulator and got Android running on it *C*
    - Implemented 1/2 of the translator, and wrote associated microcode *Verilog / Templating language*
    - Created test generator that found 90% of the first 1000 bugs on the project *F#*
  - ◊ Other projects included adding fault tolerance to a distributed system, post-silicon debug, test tooling, etc.
    - Improved job scheduling system, improving machine utilization from 60% to 92%
- Ultrafast Optics and Fiber Communications Lab, Research Assistant; Lafayette, IN** **2003 – 2005**
- ◊ Lab work, included speeding up parallel (256 wavelength) polarimeter by 40x *MATLAB and C*
- IBM, Intern; Austin, TX** **Summer 2003**
- ◊ Semi-formal / constrained random POWER6 completion unit functional verification *VHDL*
- Micron Technology, Intern; Boise, ID** **Summer 2002**
- ◊ Flash product engineering / characterization. Automated previously manual tasks. *Perl*
- Spatial Systems Research Laboratory, Research Assistant; Madison, WI** **2001**
- ◊ Studied tilings and related combinatorial models, e.g., alternating sign matrices and square ice

## EDUCATION

**BS Math & CMPE (Wisconsin, '00-'03), MS EE (Purdue, '03-'05)**

## NON-WORK PROJECTS

- ◊ Randomized algorithms can beat LRU/pseudo-LRU caches: <https://danluu.com/2choices-eviction/>
- ◊ A fuzzer written in an hour that found ~20 bugs in Julia <https://github.com/danluu/Fuzz.jl>
- ◊ Web performance benchmarks for slow/flaky connections <https://danluu.com/web-bloat/>
- ◊ Formal verification of a secure hypervisor model <https://github.com/danluu/secvisor-formal-verification>
- ◊ Combining AFL and QuickCheck for directed fuzzing <https://danluu.com/testing/>
- ◊ Terminal latency <https://danluu.com/term-latency/>
- ◊ Sega system on FPGA <https://github.com/danluu/sega-system-for-fpga>
- ◊ Keyboard vs. mousing speed <https://danluu.com/keyboard-v-mouse/>
- ◊ See <https://github.com/danluu/> and <http://danluu.com> for more!

## MISCELLANEOUS

- ◊ Work Authorization: U.S. Citizen