

dan.luu@gmail.com

EXPERIENCE

- Senior Hardware/Software Engineer, Google; Madison, WI** **2013 – 2014**
◊ Exploratory hardware/software co-design; details confidential —
- Sabbatical, Hacker School; New York, NY** **Spring 2013**
◊ Projects include channels and coroutines in C and a BitTorrent client in Scala.
◊ See <https://github.com/danluu/> and <http://danluu.com> for more.
- Member of Technical Staff, Centaur Technology (acquired by VIA); Austin, TX** **2005 – 2013**
◊ Recent projects are confidential. Here's an older six-month project (adding an ARM front-end to our x86):
 - ◊ Helped reverse engineer the ARMv7 ISA (this was pre-AArch64)
 - ◊ Created architectural simulator and got Android running on it *C*
 - ◊ Implemented $\frac{1}{2}$ of the translator, and wrote associated microcode *Internal templating language*
 - ◊ Created test generator that found 90% of the first 1000 bugs on the project *F#*
 - ◊ Result was a circa 2010 ARMv7 processor with better performance than any current ARM processor
- ◊ Other roles included formal verification, adding fault tolerance to a distributed system, post-silicon debug, test tooling, etc.
- Research Assistant, Ultrafast Optics and Fiber Communications Lab; Lafayette, IN** **2003 – 2005**
◊ Sped up parallel (256 wavelength) polarimeter by 40x, from 50 Hz to 2 kHz *MATLAB and C*
◊ Designed and built Fourier transform spectroscopy interferometer *MATLAB and C*
- Intern, IBM; Austin, TX** **Summer 2003**
◊ Semi-formal / constrained random POWER6 completion unit functional verification *VHDL*
- Intern, Micron Technology; Boise, ID** **Summer 2002**
◊ Engineering hipster: worked on flash before it was cool *Perl*
- Research Assistant, Spatial Systems Research Laboratory; Madison, WI** **2001**
◊ Studied tilings and related combinatorial models, e.g., alternating sign matrices and square ice

EDUCATION

BS Math & CMPE (Wisconsin, '00-'03), MS EE (Purdue, '03-'05)

NON-WORK PROJECTS

- ◊ See <https://github.com/danluu/> and <http://danluu.com> for an exhaustive list
- ◊ Sega system on Xilinx Vertex FPGA; translated Z80 instructions into RISC μ ops *Verilog and VHDL*
 - ◊ Experiments with a randomized algorithm as cache eviction policy *Dinero IV and SPEC*
 - ◊ A fuzzer written in an hour that found 20 bugs in the Julia compiler and base libraries *Julia*
 - ◊ Formal verification of a secure hypervisor model *ACL2*

MISCELLANEOUS

- ◊ Languages: English mother tongue. Once-fluent Vietnamese. Once-functional (now moribund) Japanese and French. Willing (and eager) to learn any language
- ◊ Work Authorization: U.S. Citizen