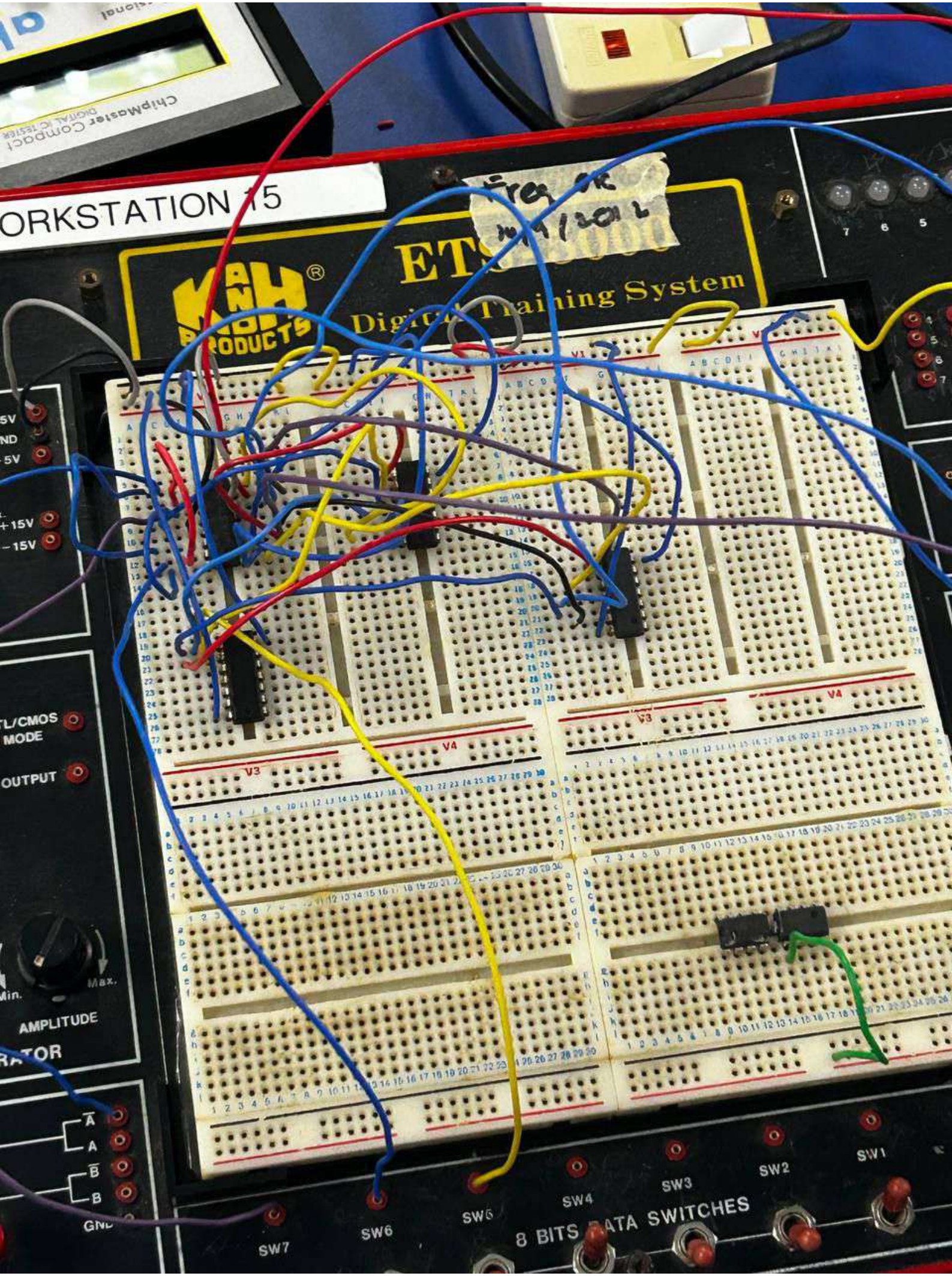

ORKSTATION 15
Digital Training System
+15V
-15V
OUTPUT
AMPLITUDE
SW7
SW6
SW5
SW4
SW3
SW2
SW1
8 BITS DATA SWITCHES

The symbol for a flip-flop often shows the asynchronous inputs as indicated below in Figure 3.

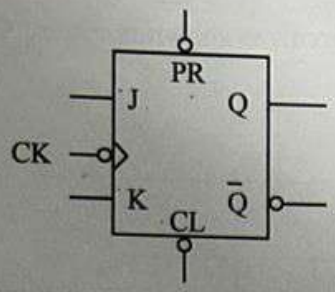


Figure 3: JK Flip-flops with asynchronous PRESET and CLEAR inpu

E. Preliminary Works

1) Using 7476 IC, connect the synchronous input (J, K) of a JK flip-flop to switches and its output (Q) to an LED. Connect the CLK input to a pulser switch, $\bar{A}$. Determine the logic level for each input combinations in Table 1 so that the desired result can be realized.

Table 1

Desired Result	$\overline{PRE}$	$\overline{CLR}$	J	K	CLK	Q
Set initial value Q = 1			X	X	--	
Output Q stays the same	1	1	0	0	⇓	0
Output Q become 0, no change in asynchronous input					⇓	
Output Q is not the previous Q	1	1			⇓	
RESET Q	1	1			⇓	
SET Q	1	1			⇓	

2) Answer all questions.

a) Which state that JK flip-flop has, but not on SR flip-flop.

Toggle

b) Identify whether the JK flip flop in 7476, is a positive-edge triggered or negative-edge triggered flip flop.

negative - edge triggered flip flop

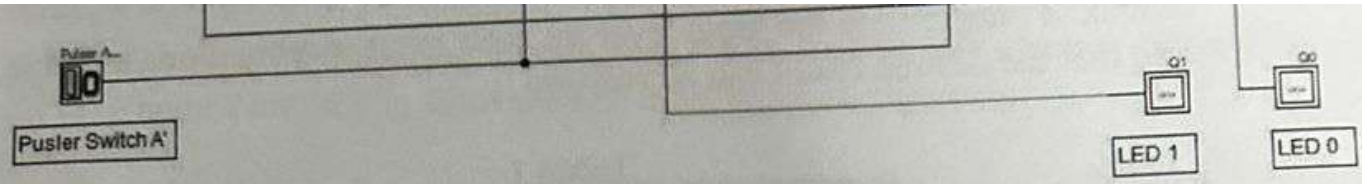


Figure 4: A Synchronous Counter Circuit

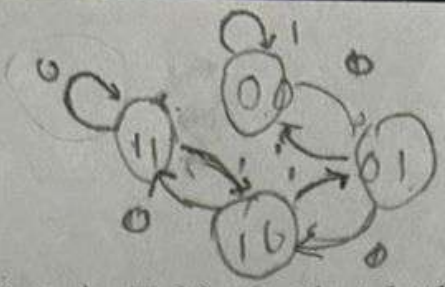
2) By using all materials and equipment's listed in section C, construct the physical circuit of Figure 4. (Make sure all ICs are connected to Vcc and GND).

3) Investigate the behavior of the counter by observing the next state of the counter for all combination of *Present State* and *X* values. Complete the *Next-State* table of the counter in Table 2. Ensure the Switch 0 is in HIGH state. (0=LOW, 1=HIGH)

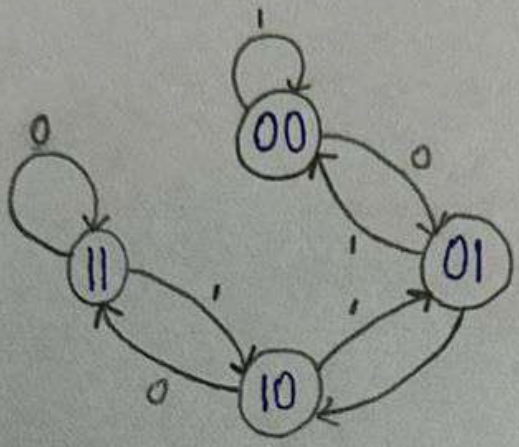
Table 2

Switch 7	Present State		Next State	
X (Input)	Q1 LED 1	Q0 LED 0	Q1 LED 1	Q0 LED 0
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	1	1
1	0	0	0	0
1	0	1	0	0
1	1	0	0	1
1	1	1	1	0

Fully Completed ☐ *Partially Completed* ☐ *Checked by:* _____



4) By referring to the *Next-State* in Table 2, sketch the state diagram of the counter.



5) By referring to the *Next-State* in Table 2 and the state diagram in (4), answer all questions.

a) What is the main indicator to decide that the counter is a synchronous counter?

the inputs transferred on the triggering edge of the clock.

b) How many states are available for the counter and what are they?

States available for the counter are 4 which are

00, 01, 10, 11.

c) What is the function of Switch 7 (X) in the circuit?

as input.

b) How many states are available for the counter and what are they?

States available for the counter are 4 which are

00, 01, 10, 11.

c) What is the function of Switch 7 (X) in the circuit?

as input.

d) What is the function of Switch 0 and Switch 1 in the circuit?

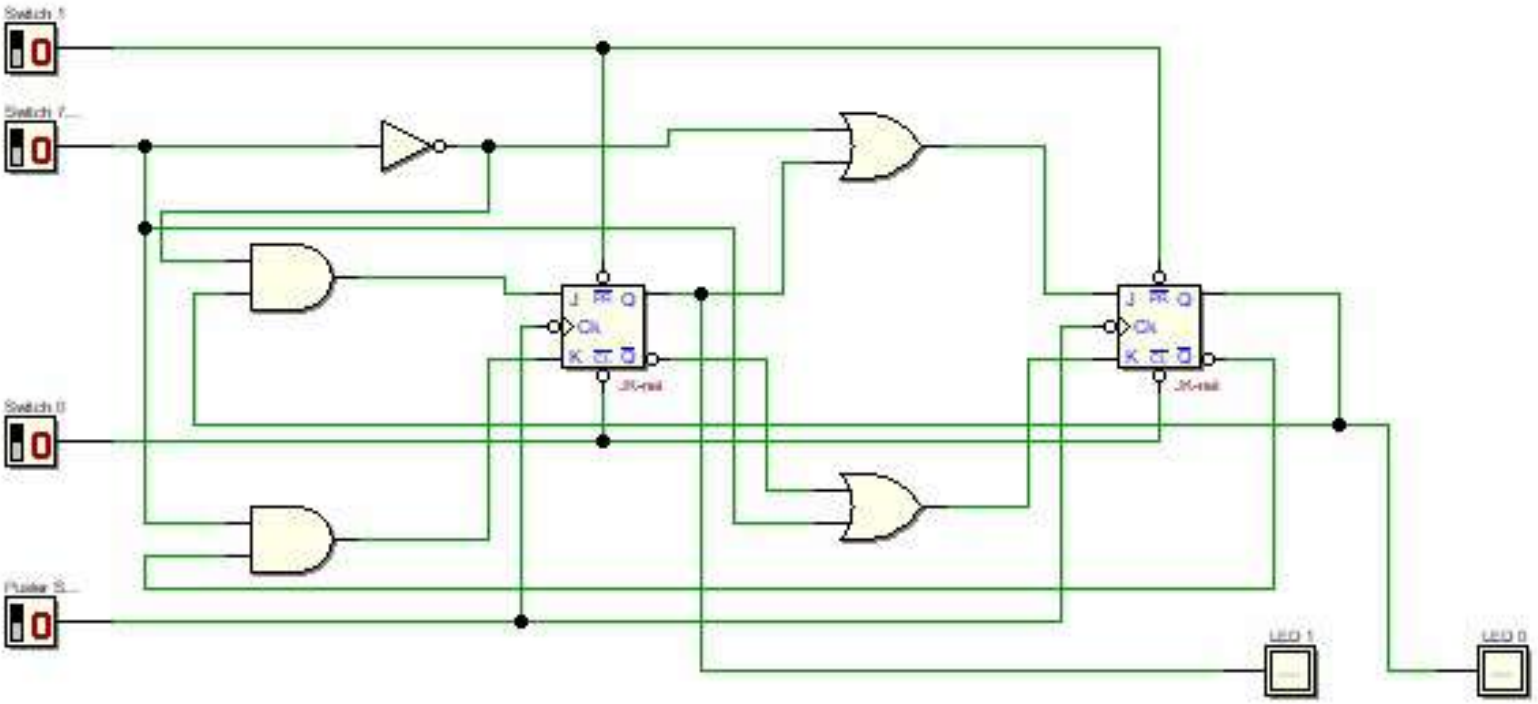
if switch 1, the counter will count down.

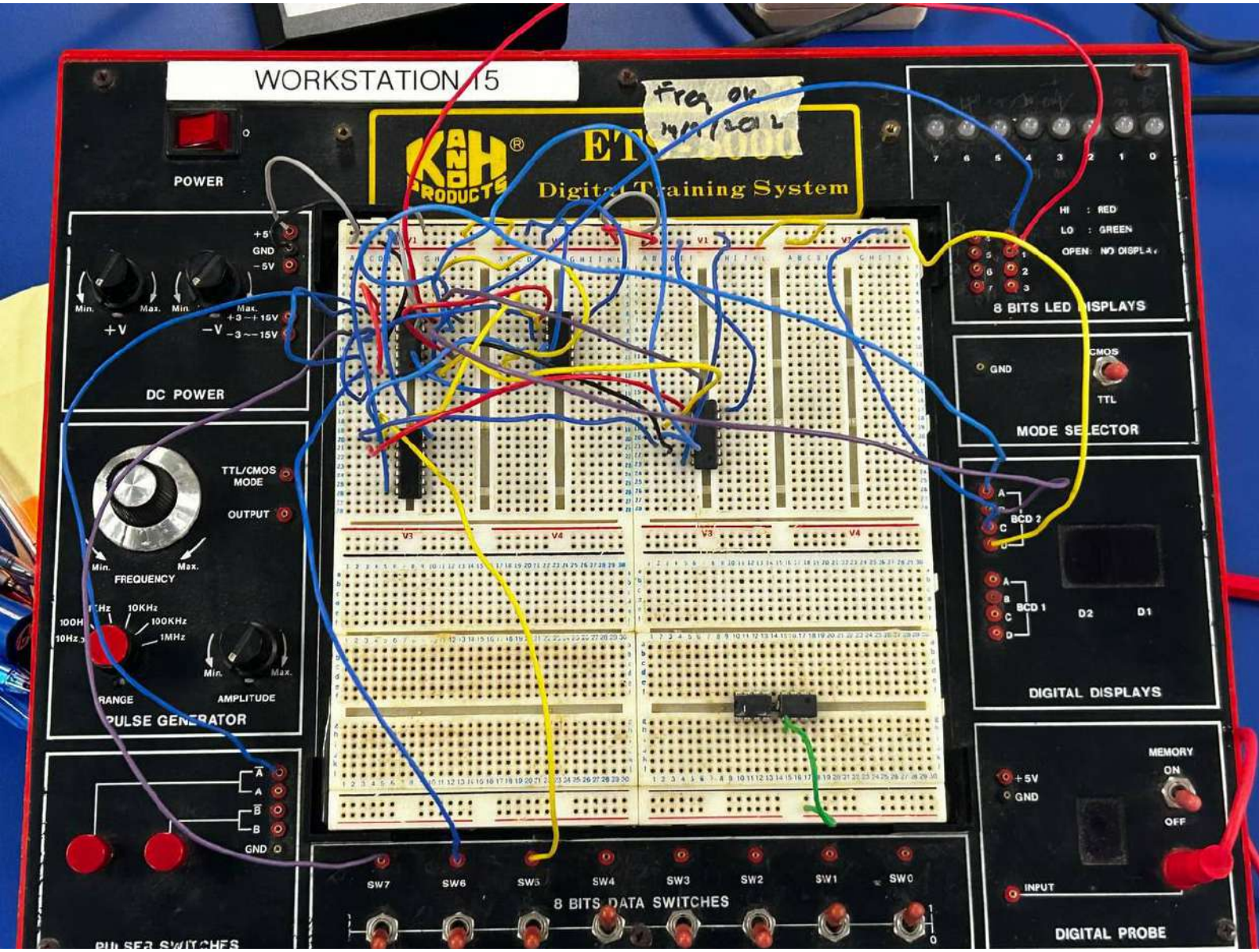
if switch 0, the counter will count up.

e) Is the counter a saturated counter or recycle counter?

a saturated counter

Fully Completed ☐ *Partially Completed* ☐ *Checked by:* _____


Switch 1
Switch 0
LED 1
LED 0


WORKSTATION 15
Freq OK
14/9/2021
POWER
Digital Training System
DC POWER
+5
GND
−5V
Min.
Max.
+V
−V
+3 ~ +15V
−3 ~ −15V
8 BITS LED DISPLAYS
HI : RED
LO : GREEN
OPEN: NO DISPLAY
MODE SELECTOR
CMOS
TTL
GND
TTL/CMOS MODE
OUTPUT
FREQUENCY
RANGE
AMPLITUDE
PULSE GENERATOR
100Hz
1KHz
10KHz
100KHz
1MHz
BCD 2
BCD 1
D2
D1
DIGITAL DISPLAYS
MEMORY
ON
OFF
INPUT
DIGITAL PROBE
GND
8 BITS DATA SWITCHES
SW7
SW6
SW5
SW4
SW3
SW2
SW1
SW0