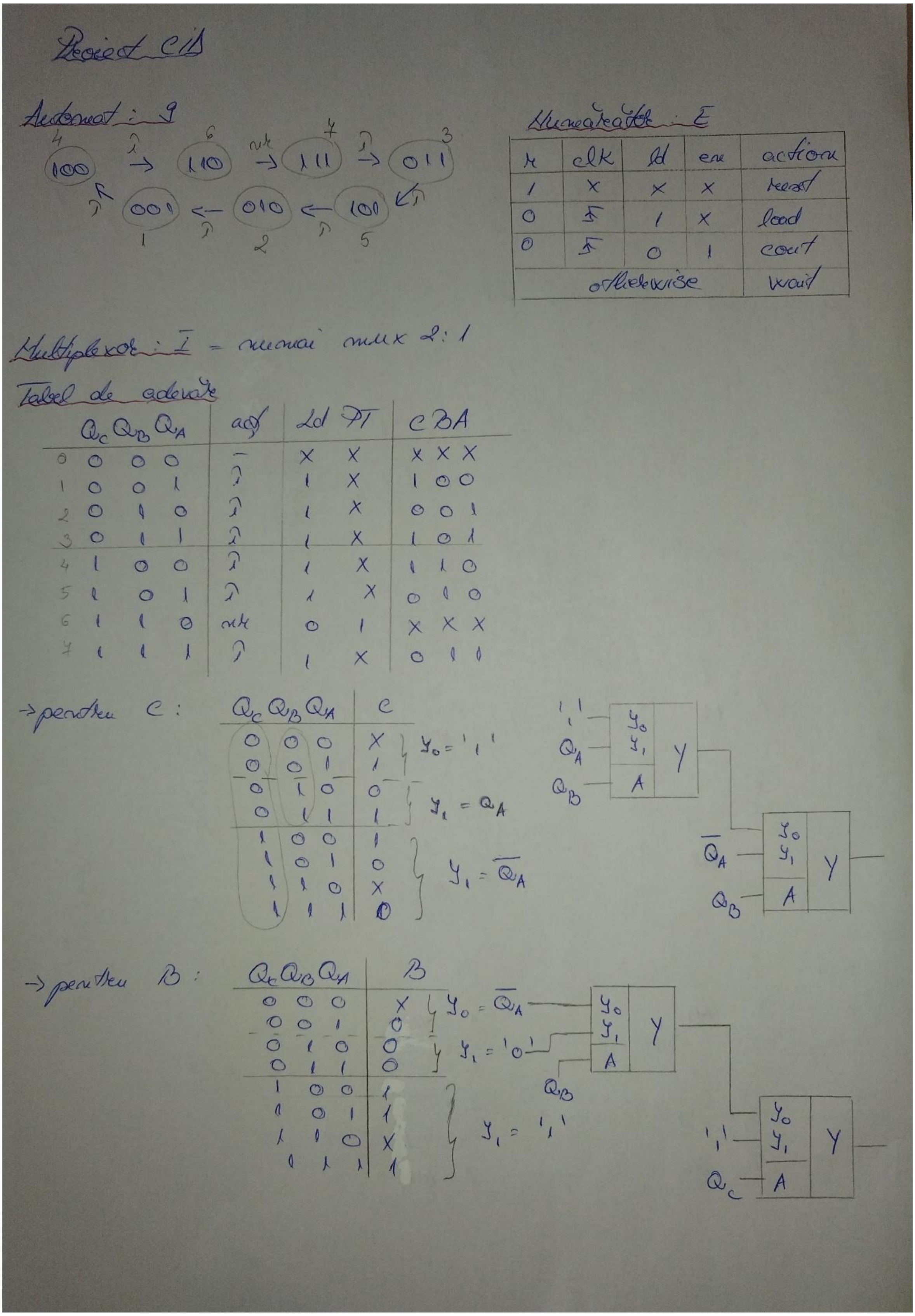
Proiect CID



Proiect CID

Automat : 9

4
100
î
6
110
nr
7
111
î
3
011
î
101
5
î
010
2
î
001
1
î

Numarator : E

r	clk	ld	en	action
1	x	x	x	reset
0	⎍	1	x	load
0	⎍	0	1	count
otherwise				wait

Multiplexor : I = numai mux 2:1

Tabel de adevăr

	Q_C	Q_B	Q_A	acț	Ld	PT	C	B	A
0	0	0	0	–	X	X	X	X	X
1	0	0	1	î	1	X	1	0	0
2	0	1	0	î	1	X	0	0	1
3	0	1	1	î	1	X	1	0	1
4	1	0	0	î	1	X	1	1	0
5	1	0	1	î	1	X	0	1	0
6	1	1	0	nr	0	1	X	X	X
7	1	1	1	î	1	X	0	1	1

→ pentru C :

Q_C	Q_B	Q_A	C
0	0	0	X
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	X
1	1	1	0

$Y_0 = '1'$

$Y_1 = Q_A$

$Y_1 = \overline{Q_A}$

'1'
Q_A
Q_B
Y_0
Y_1
A
Y
$\overline{Q_A}$
Q_B
Y_0
Y_1
A
Y

→ pentru B :

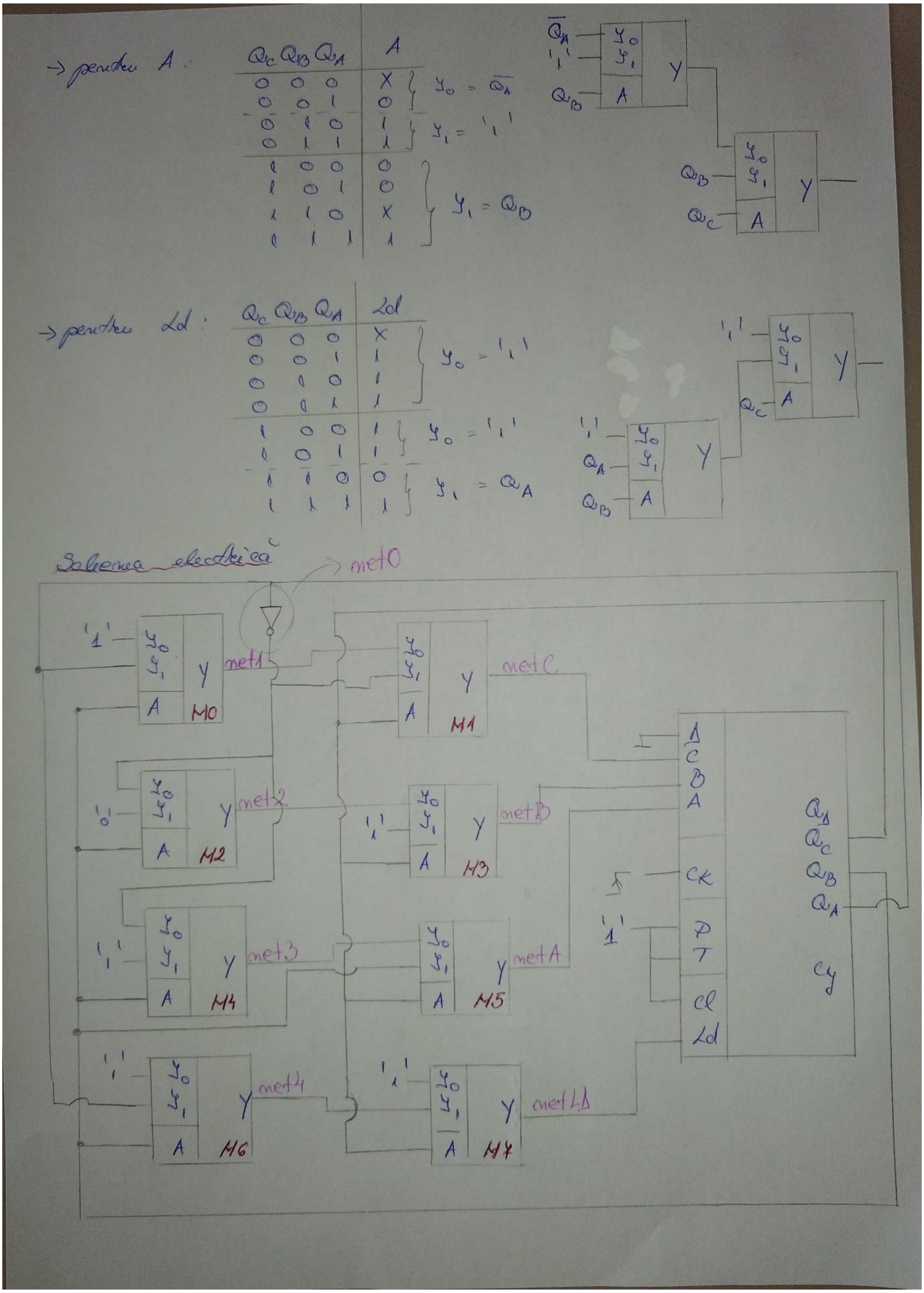
Q_C	Q_B	Q_A	B
0	0	0	X
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	1

$Y_0 = \overline{Q_A}$

$Y_1 = '0'$

$Y_1 = '1'$

Petruți Adriana
Grupa 2123, sg 2
PROIECT CID



→ pentru A:

Q_C	Q_B	Q_A	A	
0	0	0	X	$y_0 = \overline{Q_A}$
0	0	1	0	
0	1	0	1	$y_1 = '1'$
0	1	1	1	
1	0	0	0	$y_1 = Q_B$
1	0	1	0	
1	1	0	X	
1	1	1	1	

$\overline{Q_A}$
'1'
Q_B
y_0
y_1
A
Y
Q_B
Q_C
y_0
y_1
A
Y

→ pentru Ld:

Q_C	Q_B	Q_A	Ld	
0	0	0	X	$y_0 = '1'$
0	0	1	1	
0	1	0	1	
0	1	1	1	
1	0	0	1	$y_0 = '1'$
1	0	1	1	
1	1	0	0	$y_1 = Q_A$
1	1	1	1	

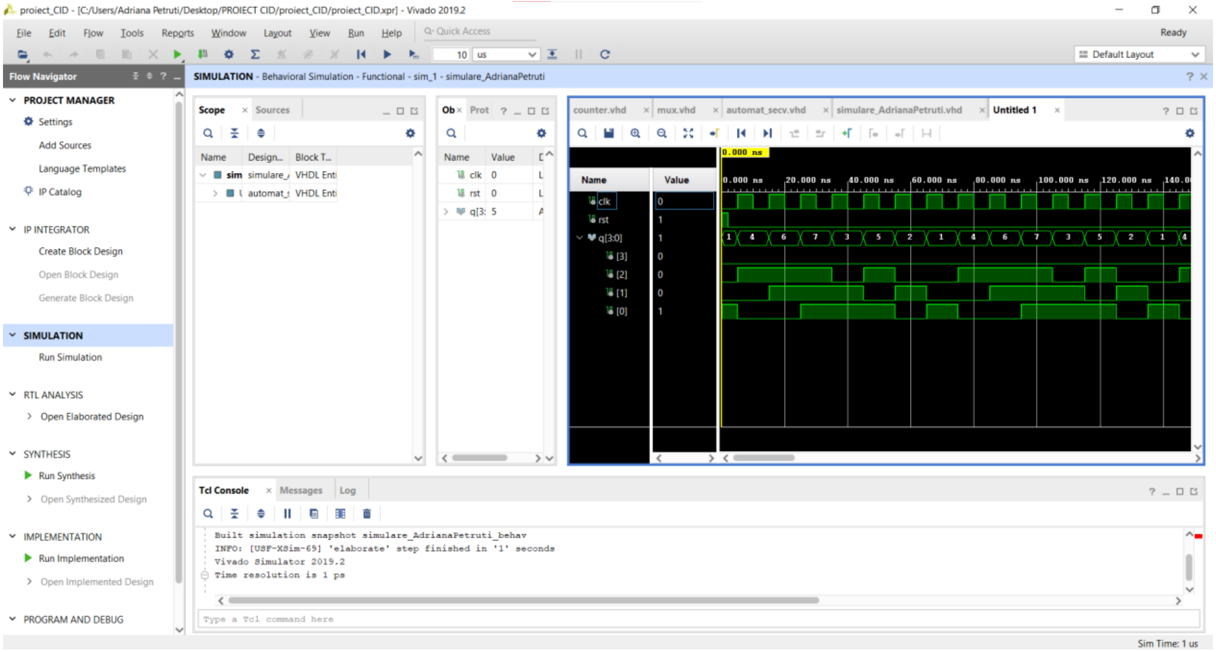
'1'
y_0
y_1
A
Y
Q_C
'1'
Q_A
Q_B
y_0
y_1
A
Y

Schema electrică

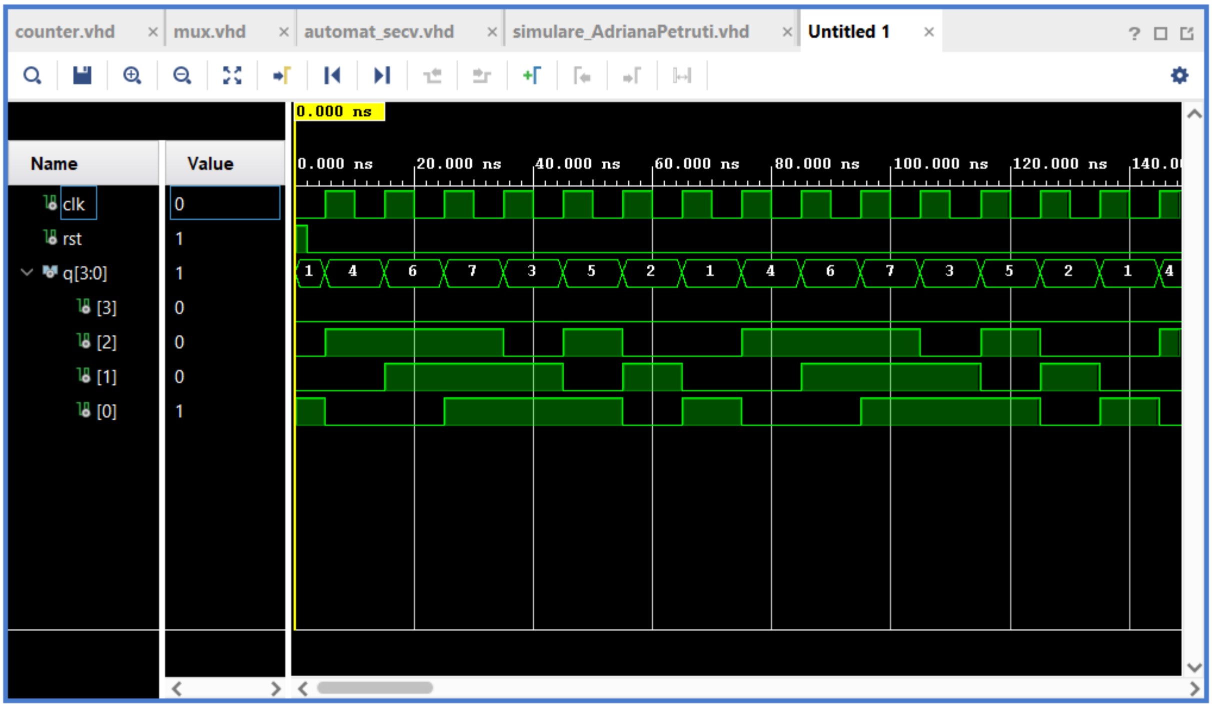
net0
'1'
y_0
y_1
Y
A
M0
net1
y_0
y_1
Y
A
M1
netC
'0'
y_0
y_1
Y
A
M2
net2
'1'
y_0
y_1
Y
A
M3
netB
'1'
y_0
y_1
Y
A
M4
net3
y_0
y_1
Y
A
M5
netA
'1'
y_0
y_1
Y
A
M6
net4
'1'
y_0
y_1
Y
A
M7
netLD
D
C
B
A
CK
'1'
P
T
Cl
Ld
Q_D
Q_C
Q_B
Q_A
Cy

Petruți Adriana
Grupa 2123, sg 2
PROIECT CID

- Simularea:



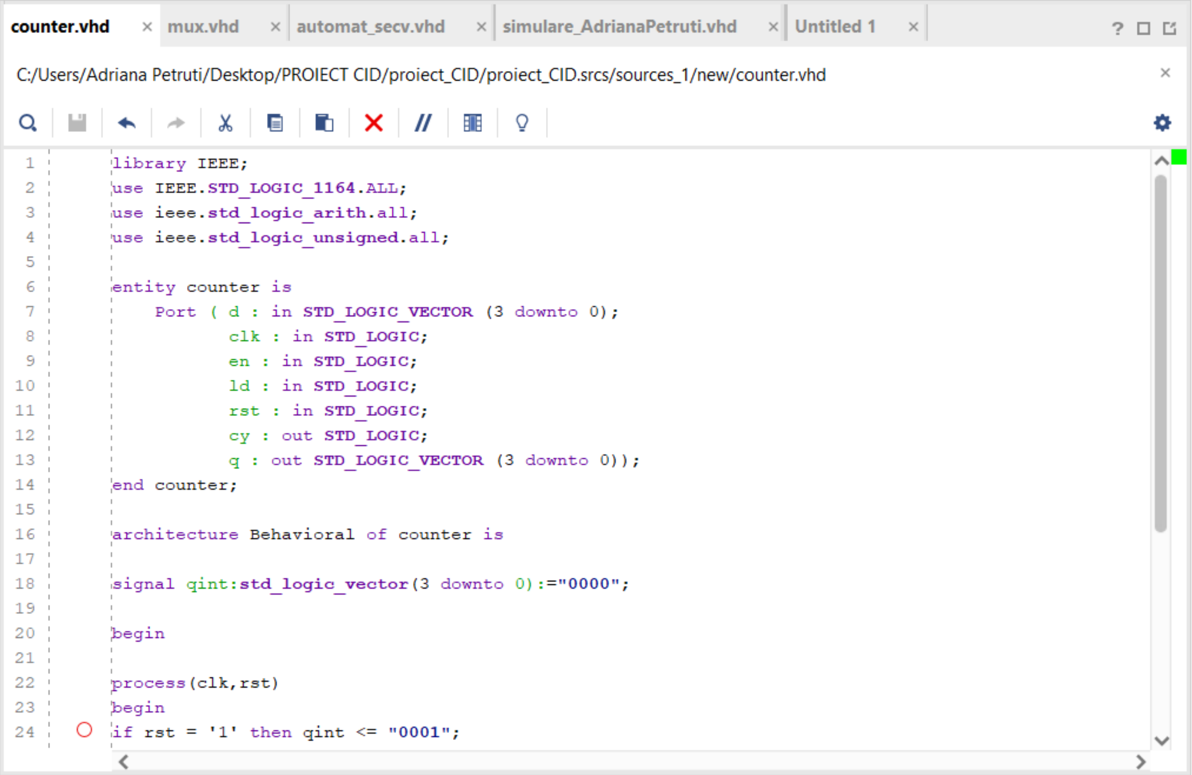
```
Built simulation snapshot simulare_AdrianaPetruti_behav
INFO: [USF-XSim-69] 'elaborate' step finished in '1' seconds
Vivado Simulator 2019.2
Time resolution is 1 ps
```



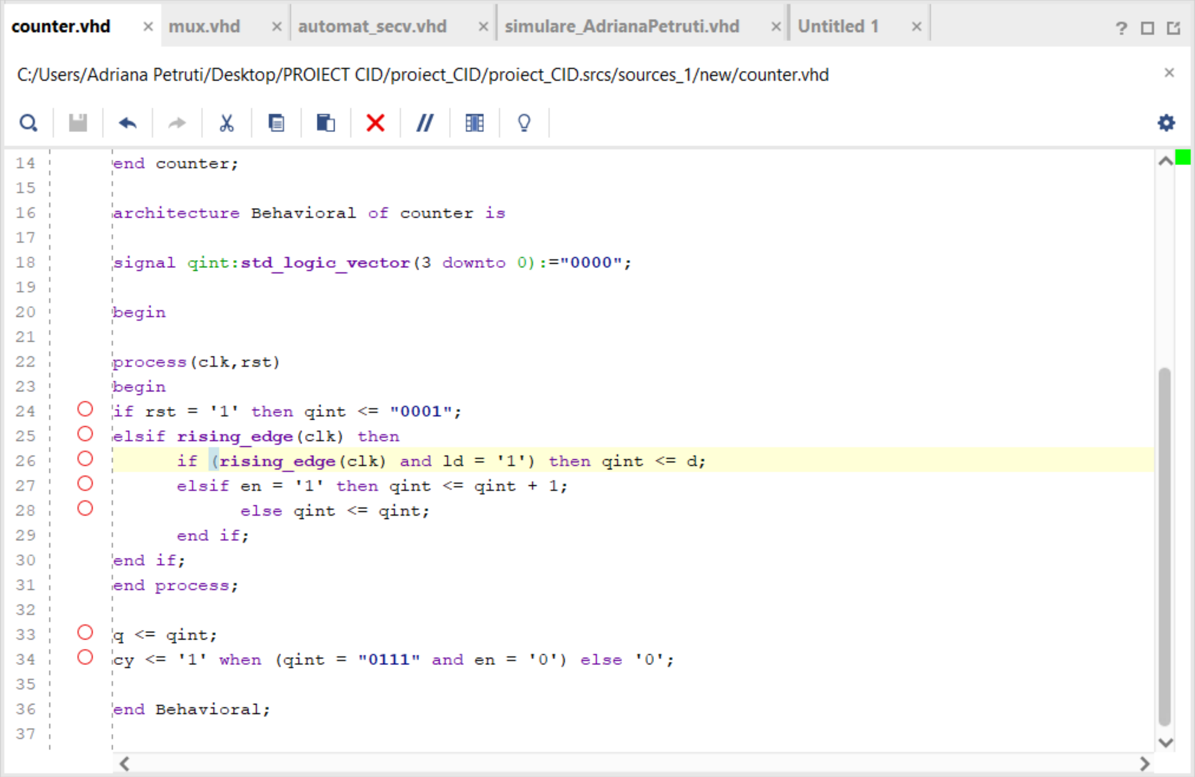
Name	Value
clk	0
rst	1
q[3:0]	1
[3]	0
[2]	0
[1]	0
[0]	1

Petruți Adriana
Grupa 2123, sg 2
PROIECT CID

- Sursă counter:


counter.vhd
mux.vhd
automat_secv.vhd
simulare_AdrianaPetruti.vhd
Untitled 1
C:/Users/Adriana Petruti/Desktop/PROIECT CID/proiect_CID/proiect_CID.srcs/sources_1/new/counter.vhd

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

entity counter is
    Port ( d : in STD_LOGIC_VECTOR (3 downto 0);
           clk : in STD_LOGIC;
           en : in STD_LOGIC;
           ld : in STD_LOGIC;
           rst : in STD_LOGIC;
           cy : out STD_LOGIC;
           q : out STD_LOGIC_VECTOR (3 downto 0));
end counter;

architecture Behavioral of counter is

signal qint:std_logic_vector(3 downto 0):="0000";

begin

process(clk,rst)
begin
if rst = '1' then qint <= "0001";
```

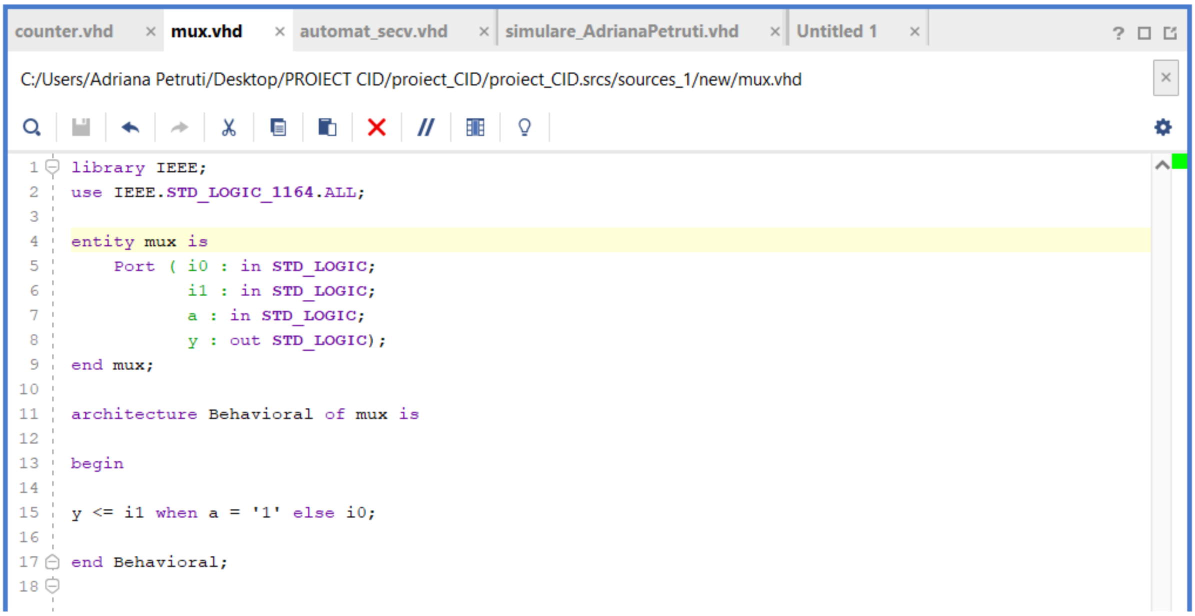

counter.vhd
mux.vhd
automat_secv.vhd
simulare_AdrianaPetruti.vhd
Untitled 1
C:/Users/Adriana Petruti/Desktop/PROIECT CID/proiect_CID/proiect_CID.srcs/sources_1/new/counter.vhd

```
end counter;

architecture Behavioral of counter is

signal qint:std_logic_vector(3 downto 0):="0000";

begin

process(clk,rst)
begin
if rst = '1' then qint <= "0001";
```

```
elsif rising_edge(clk) then
      if (rising_edge(clk) and ld = '1') then qint <= d;
      elsif en = '1' then qint <= qint + 1;
            else qint <= qint;
      end if;
end if;
end process;

q <= qint;
cy <= '1' when (qint = "0111" and en = '0') else '0';

end Behavioral;

```

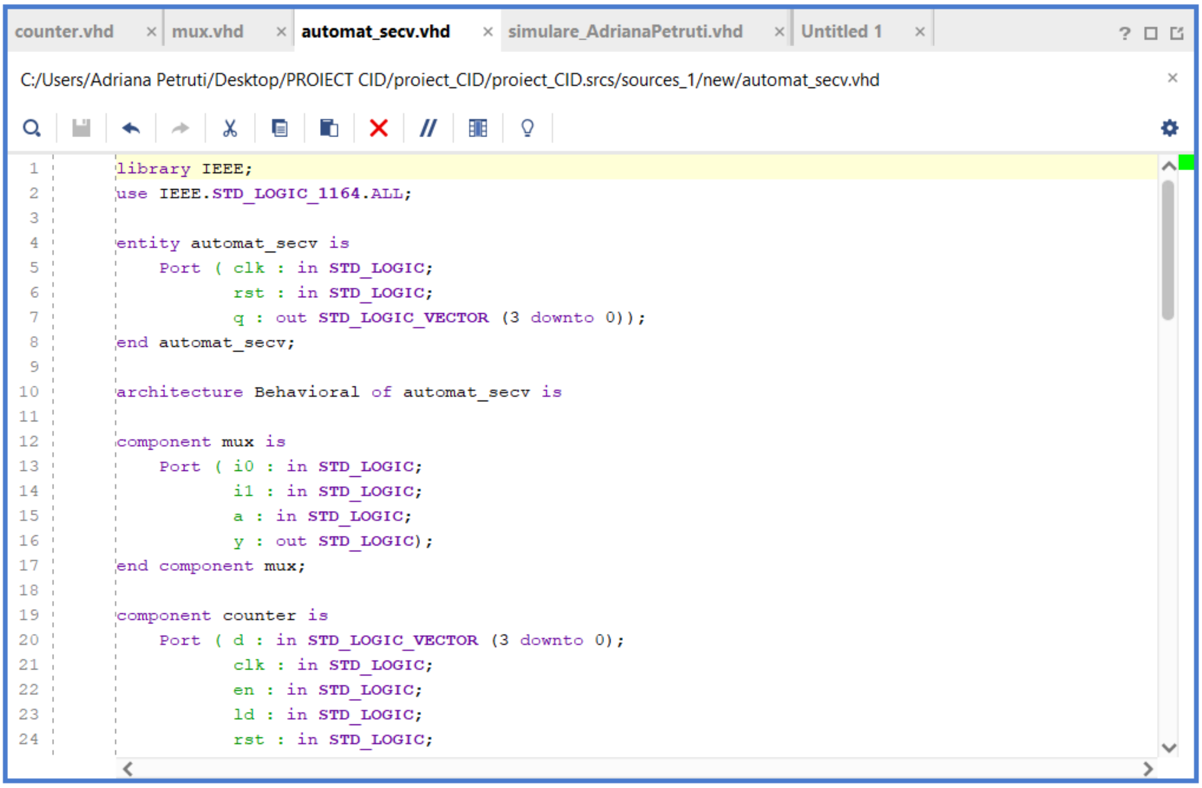
Petruți Adriana
Grupa 2123, sg 2
PROIECT CID

- Sursă mux:


counter.vhd
mux.vhd
automat_secv.vhd
simulare_AdrianaPetruti.vhd
Untitled 1
C:/Users/Adriana Petruti/Desktop/PROIECT CID/proiect_CID/proiect_CID.srcs/sources_1/new/mux.vhd

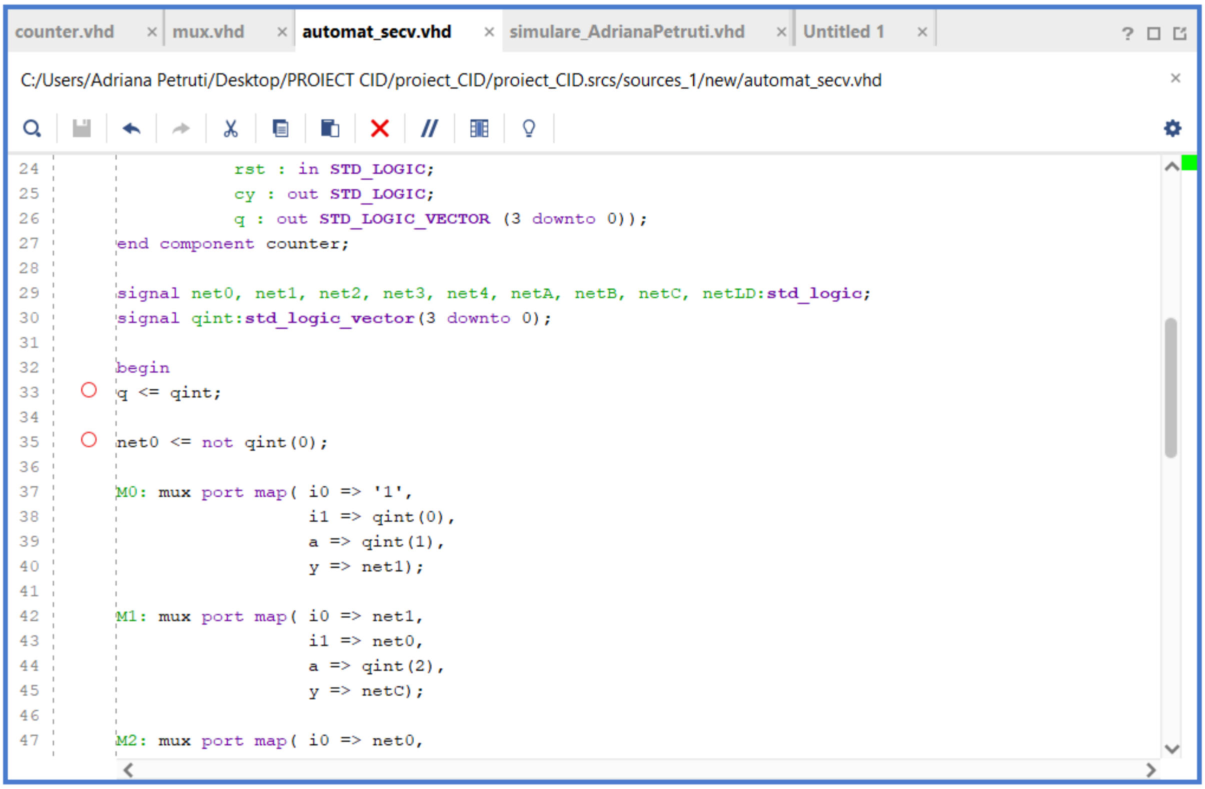
```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity mux is
    Port ( i0 : in STD_LOGIC;
           i1 : in STD_LOGIC;
           a : in STD_LOGIC;
           y : out STD_LOGIC);
end mux;

architecture Behavioral of mux is

begin

y <= i1 when a = '1' else i0;

end Behavioral;

```

- Sursă automat_secv:

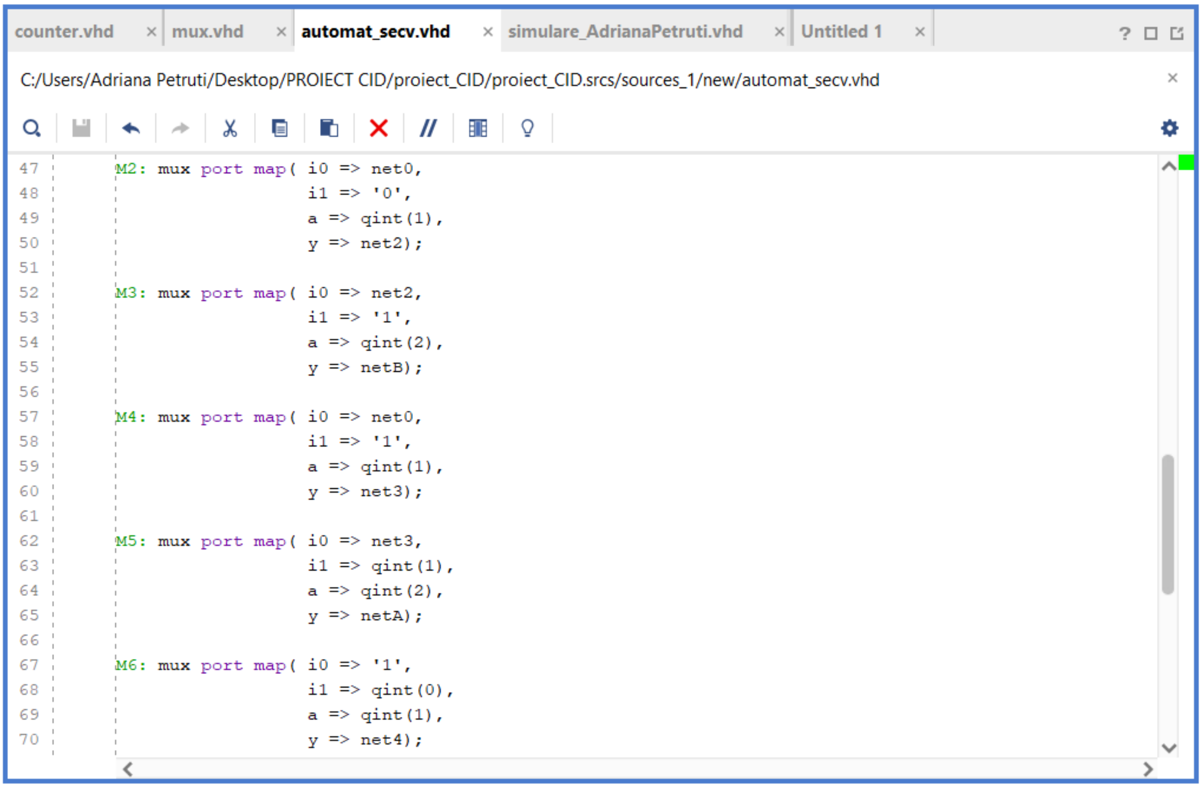

counter.vhd
mux.vhd
automat_secv.vhd
simulare_AdrianaPetruti.vhd
Untitled 1
C:/Users/Adriana Petruti/Desktop/PROIECT CID/proiect_CID/proiect_CID.srcs/sources_1/new/automat_secv.vhd

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity automat_secv is
    Port ( clk : in STD_LOGIC;
           rst : in STD_LOGIC;
           q : out STD_LOGIC_VECTOR (3 downto 0));
end automat_secv;

architecture Behavioral of automat_secv is

component mux is
    Port ( i0 : in STD_LOGIC;
           i1 : in STD_LOGIC;
           a : in STD_LOGIC;
           y : out STD_LOGIC);
end component mux;

component counter is
    Port ( d : in STD_LOGIC_VECTOR (3 downto 0);
           clk : in STD_LOGIC;
           en : in STD_LOGIC;
           ld : in STD_LOGIC;
           rst : in STD_LOGIC;
```

Petruți Adriana
Grupa 2123, sg 2
PROIECT CID

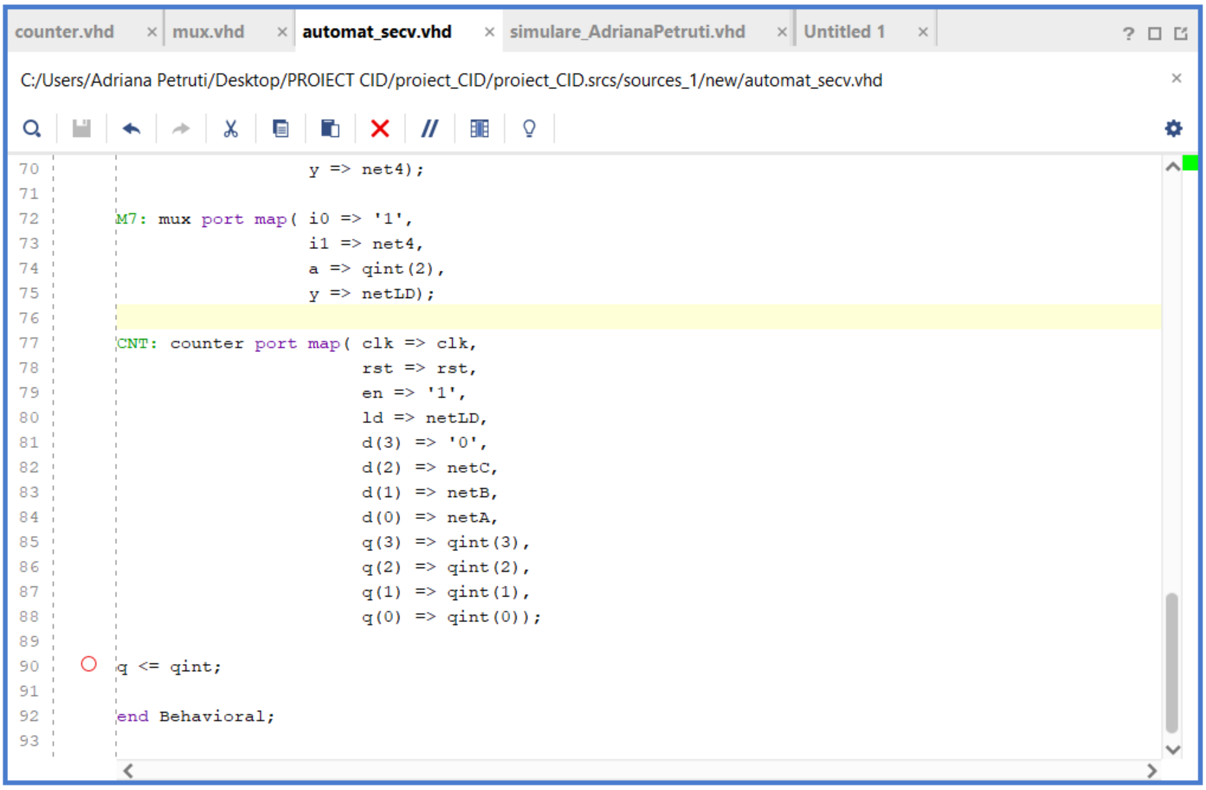

counter.vhd
mux.vhd
automat_secv.vhd
simulare_AdrianaPetruti.vhd
Untitled 1
C:/Users/Adriana Petruti/Desktop/PROIECT CID/proiect_CID/proiect_CID.srcs/sources_1/new/automat_secv.vhd

```
           rst : in STD_LOGIC;
           cy : out STD_LOGIC;
           q : out STD_LOGIC_VECTOR (3 downto 0));
end component counter;

signal net0, net1, net2, net3, net4, netA, netB, netC, netLD:std_logic;
signal qint:std_logic_vector(3 downto 0);

begin
q <= qint;

net0 <= not qint(0);

M0: mux port map( i0 => '1',
                  i1 => qint(0),
                  a => qint(1),
                  y => net1);

M1: mux port map( i0 => net1,
                  i1 => net0,
                  a => qint(2),
                  y => netC);

M2: mux port map( i0 => net0,
```


counter.vhd
mux.vhd
automat_secv.vhd
simulare_AdrianaPetruti.vhd
Untitled 1
C:/Users/Adriana Petruti/Desktop/PROIECT CID/proiect_CID/proiect_CID.srcs/sources_1/new/automat_secv.vhd

```
M2: mux port map( i0 => net0,
                  i1 => '0',
                  a => qint(1),
                  y => net2);

M3: mux port map( i0 => net2,
                  i1 => '1',
                  a => qint(2),
                  y => netB);

M4: mux port map( i0 => net0,
                  i1 => '1',
                  a => qint(1),
                  y => net3);

M5: mux port map( i0 => net3,
                  i1 => qint(1),
                  a => qint(2),
                  y => netA);

M6: mux port map( i0 => '1',
                  i1 => qint(0),
                  a => qint(1),
                  y => net4);
```

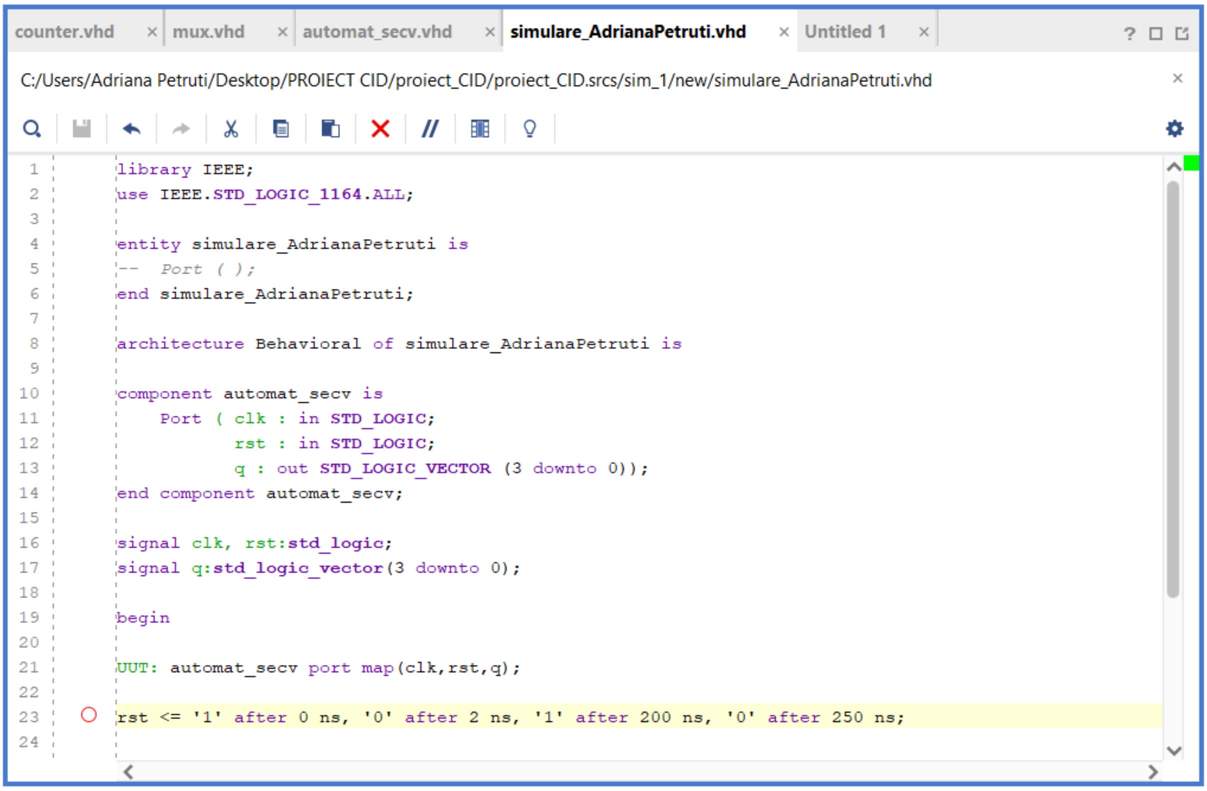
Petruți Adriana
Grupa 2123, sg 2
PROIECT CID



C:/Users/Adriana Petruti/Desktop/PROIECT CID/proiect_CID/proiect_CID.srcs/sources_1/new/automat_secv.vhd

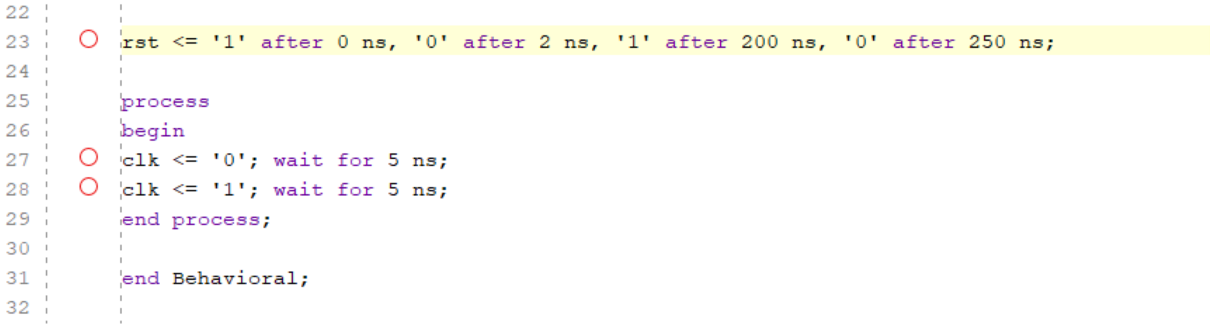
```
                  y => net4);

M7: mux port map( i0 => '1',
                  i1 => net4,
                  a => qint(2),
                  y => netLD);

CNT: counter port map( clk => clk,
                       rst => rst,
                       en => '1',
                       ld => netLD,
                       d(3) => '0',
                       d(2) => netC,
                       d(1) => netB,
                       d(0) => netA,
                       q(3) => qint(3),
                       q(2) => qint(2),
                       q(1) => qint(1),
                       q(0) => qint(0));

q <= qint;

end Behavioral;

```

- Testbench:



C:/Users/Adriana Petruti/Desktop/PROIECT CID/proiect_CID/proiect_CID.srcs/sim_1/new/simulare_AdrianaPetruti.vhd

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity simulare_AdrianaPetruti is
--  Port ( );
end simulare_AdrianaPetruti;

architecture Behavioral of simulare_AdrianaPetruti is

component automat_secv is
    Port ( clk : in STD_LOGIC;
           rst : in STD_LOGIC;
           q : out STD_LOGIC_VECTOR (3 downto 0));
end component automat_secv;

signal clk, rst:std_logic;
signal q:std_logic_vector(3 downto 0);

begin

UUT: automat_secv port map(clk,rst,q);

rst <= '1' after 0 ns, '0' after 2 ns, '1' after 200 ns, '0' after 250 ns;

```



```

rst <= '1' after 0 ns, '0' after 2 ns, '1' after 200 ns, '0' after 250 ns;

process
begin
clk <= '0'; wait for 5 ns;
clk <= '1'; wait for 5 ns;
end process;

end Behavioral;

```