ECE 153a/253/ CMPSCI 153a: HW 1

Homework 1

Due October 5, 2016

Reading: Read the Vivado Getting Started and MicroBlaze References, and the papers by Lee, Tennenhouse and Lavagno.

Problems

1. Caches are very commonly used to improve the average performance of processors by providing a small, fast memory for often reused portions of program of data. The issue with a cache is that when the needed program fragment is not present in the cache, the processor waits while the data is fetched. Finally, for simplicity and overall performance, the replacement often is a small *cache-line* of 32 or 64 bytes. In this problem, you are to make measurements augmenting a program to model the timing of processor memory accesses.

A. an access to main memory takes a fixed setup of 7 cycles plus 1 cycle for each sequential word, reads to random addresses must again pay the setup overhead.
B. the cache access is 1 cycle if the data is in the cache, and if not, it reads a 8-word cache line from the main memory (taking same time as a processor access to main memory) then an additional 2 cycles to update and respond to the read. As part of the update, some line in the cache is overwritten.
C. when the cache is disabled, a single buffer of 4 sequential words stores the result of the previous memory read.
D. the model assumes a 16 bit word address and 256 line cache of 8 word lines.

A program for the model (in C) will be provided, you should use this model and write C code that interfaces to this, providing addresses and gathering statistics.

a) determine the expected access time for cache enabled and disabled given random reads of the 16-bit memory space.

b) assuming that:
s=0.6 is the probability that the next address follows the current one
p=0.35 is the probability that the next address is not sequential but is within 40 words (either direction) of the current one

thus 0.05 is the probability of a random far address
Determine the values for access time as above.

c) what is the worst case access time for the memory? Why is this hard to find in a real system?

Hint: The distributions you expect above are hardly Gaussian (normal) statistics. A classic method to find the expectation of accuracy of a measurement that does not require normal statistics is *resampling*. The idea is to do experiment, say 1000 address trials, and determine the expectation. Then redo the experiment a few dozen times - each time you should get a new expectation that isn't too different – but indicates the uncertainty of the measurement. In practice, you can do this by randomly sampling the original measurement (when data is expensive to generate) to do this.

d) determine 50% and 90% confidence limits on the values you found in a,b above.

2. A hand mixer is to be run by a grand loop controller on a small microcontroller. The following tasks must be run, each taking a certain amount of time:

Task	Description	Time to run	Deadline
Ctrl	Control calculations	8 ms	25 ms
Spd	Speed measurement	3 ms	20 ms
Temp	Temperature check	4 ms	30 ms
UI	User Interface	5 ms	30 ms

Each of these tasks is currently implemented as a monolithic block of code, and so must be executed all at once.

a) What is the raw utilization of the system?

In practice, the grand loop time is fixed by the fact that we can only switch power at the zero crossing of the mains voltage. Given 60Hz mains and 2 zero crossings per cycle, this gives a loop time of 8ms:

b) Show a valid schedule with an 8ms loop time.

c) What is the processor utilization under this schedule?

Assuming the mixer is successful in the US market, it is desired to introduce it to the European market. Given 50Hz mains, the loop cycle time will be 10ms:

d) Show that it is no longer possible to find a schedule under the above assumptions

e) If control calculations can be split into two blocks whose execution time sums to 8ms, show a 10ms schedule that works.

f) What is the utilization of that schedule? Is it higher or lower than the 8ms schedule. Which task's utilization changes the most?