

Name: Adrian Tran

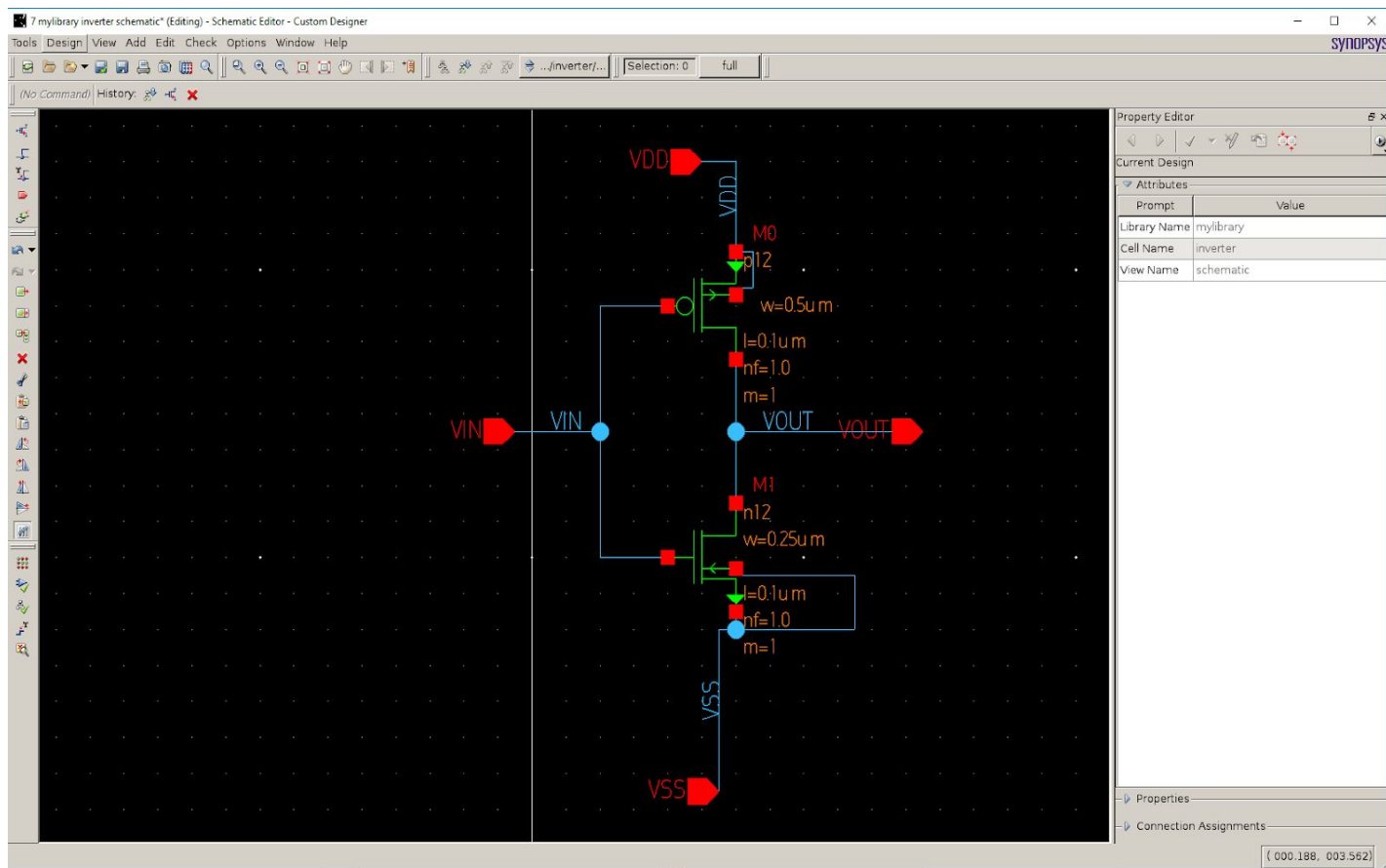
Session: 022

ENGR ID: adtran

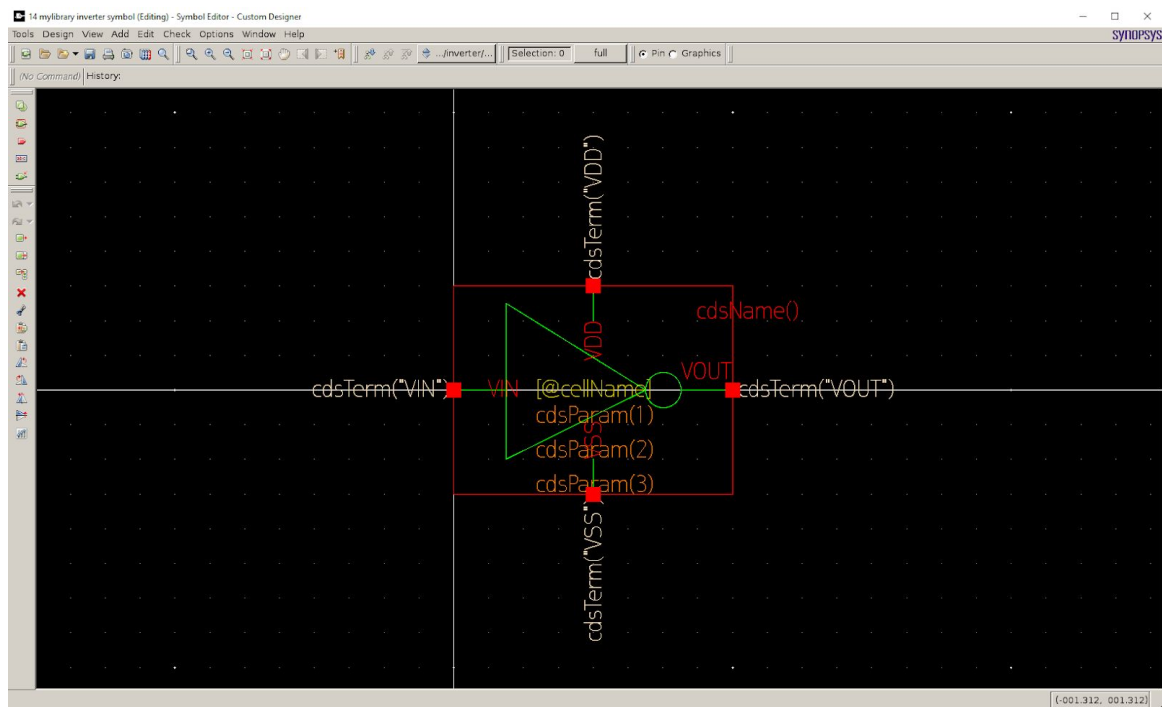
UCR NetID: atran059

Throughout this lab, I learned how to draw custom IC layout by becoming more familiar with the design workspace, creating cell views and libraries, and creating my own instances. I was also able to design a symbol for my generated instance as well as implement the aforementioned into a system. Finally, I was able to create a testbench for that instance, as well simulate and analyze the waveform of the testbench.

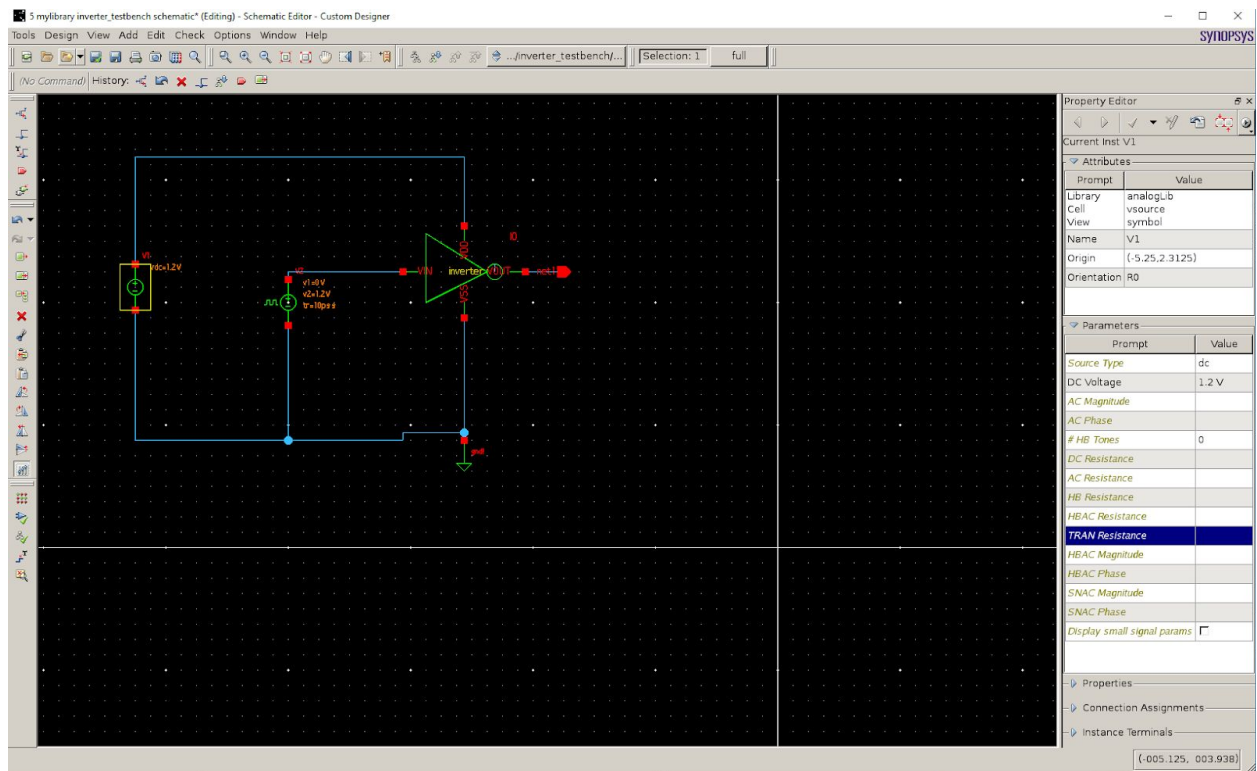
An inverter schematic view as seen in Fig.13:



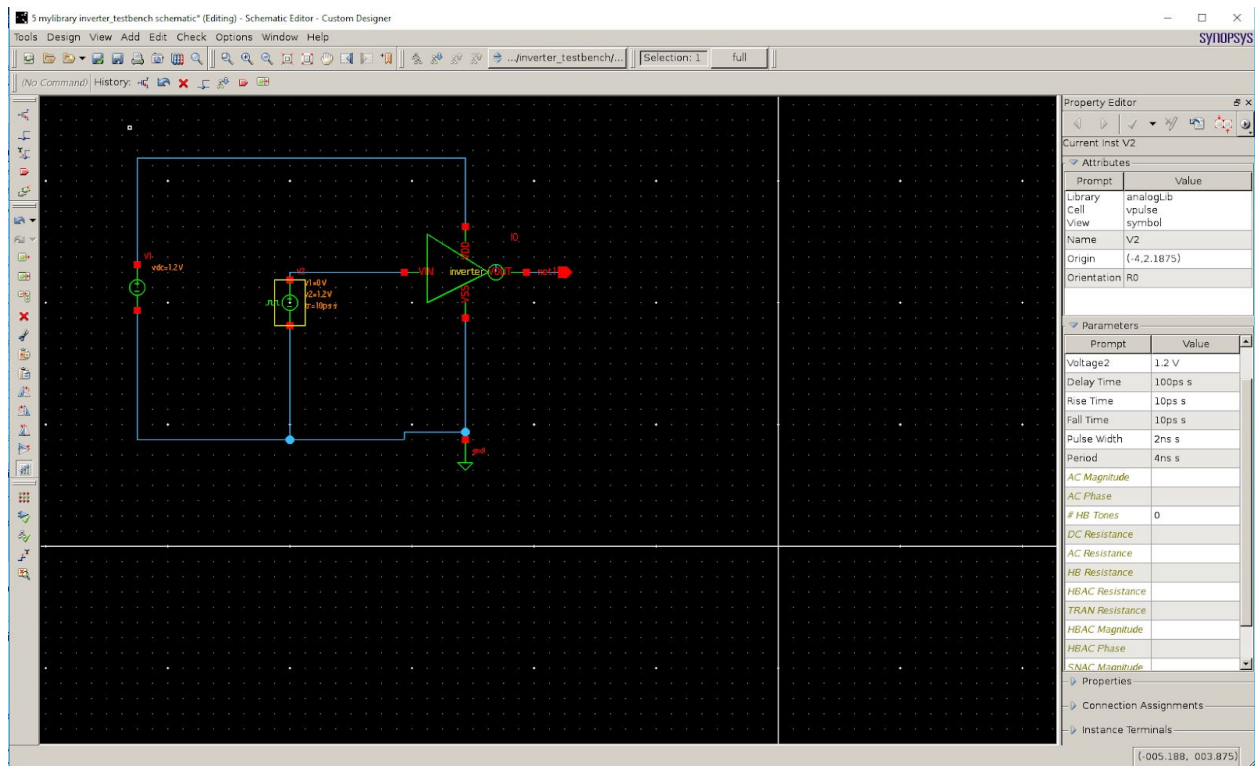
An inverter symbol view as seen in Fig. 15:



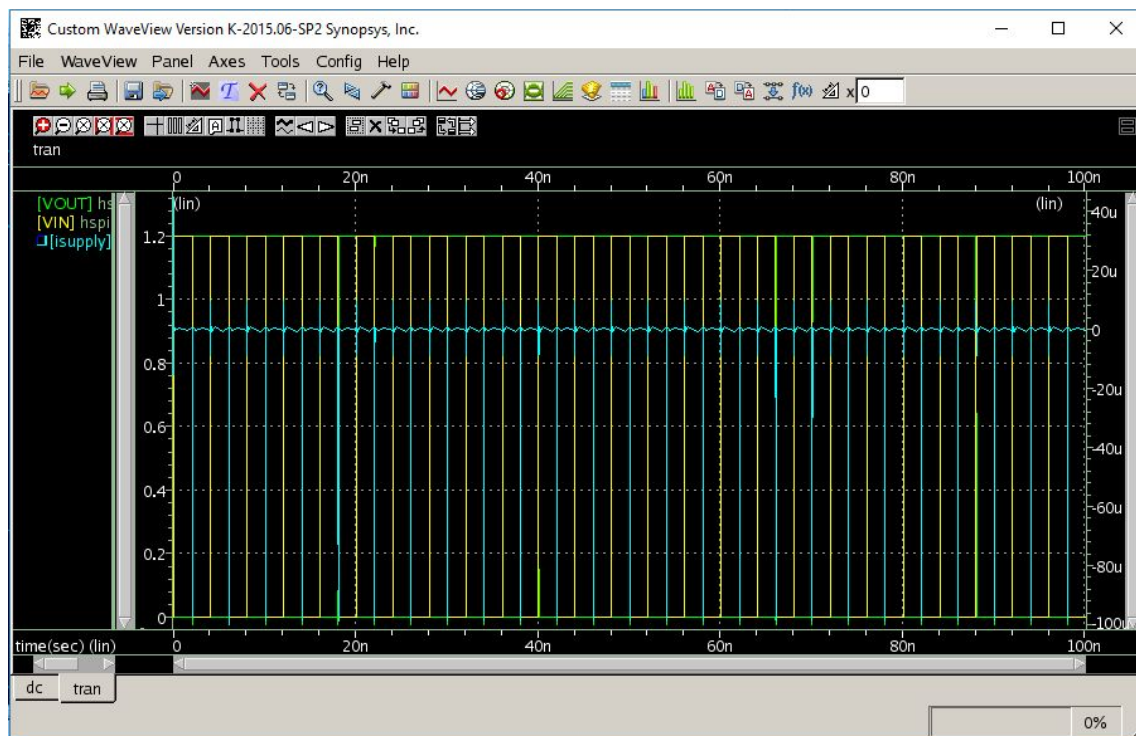
A test-bench for the inverter design as seen in Figure 18_1:



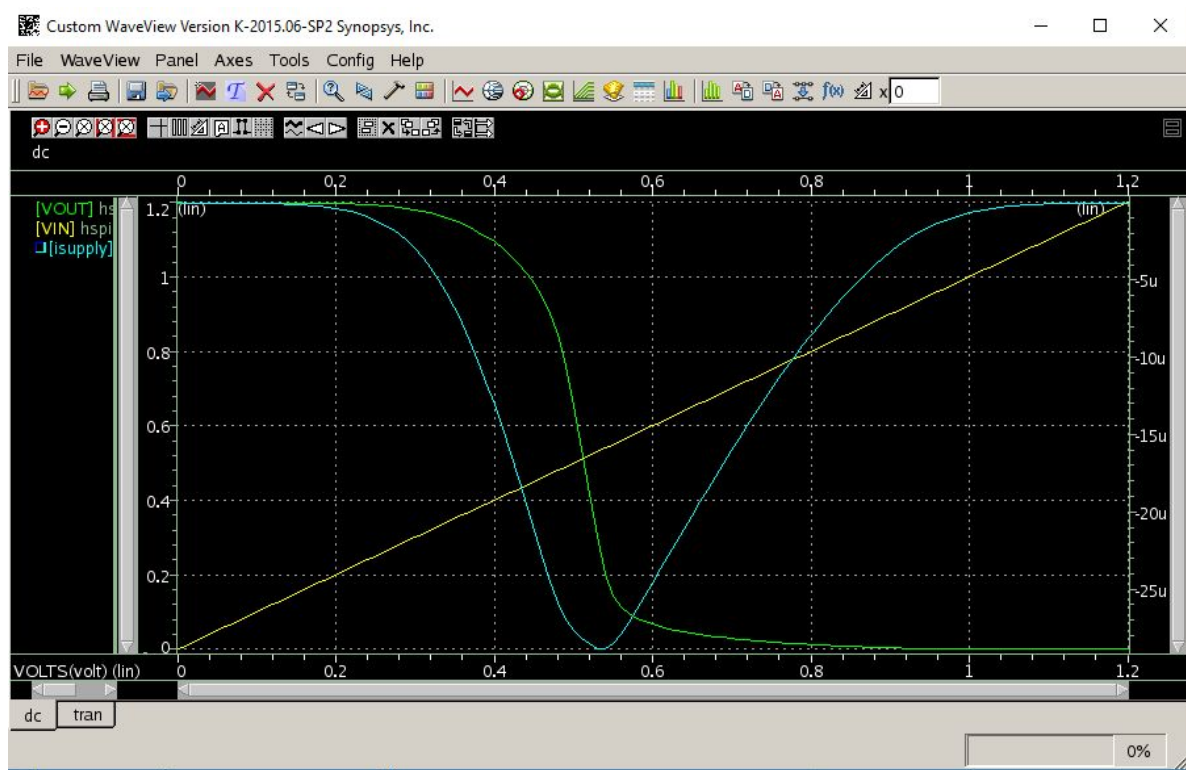
A test-bench for the inverter design as seen in Figure 18_2:



A transient analysis waveform as seen in Fig. 28:



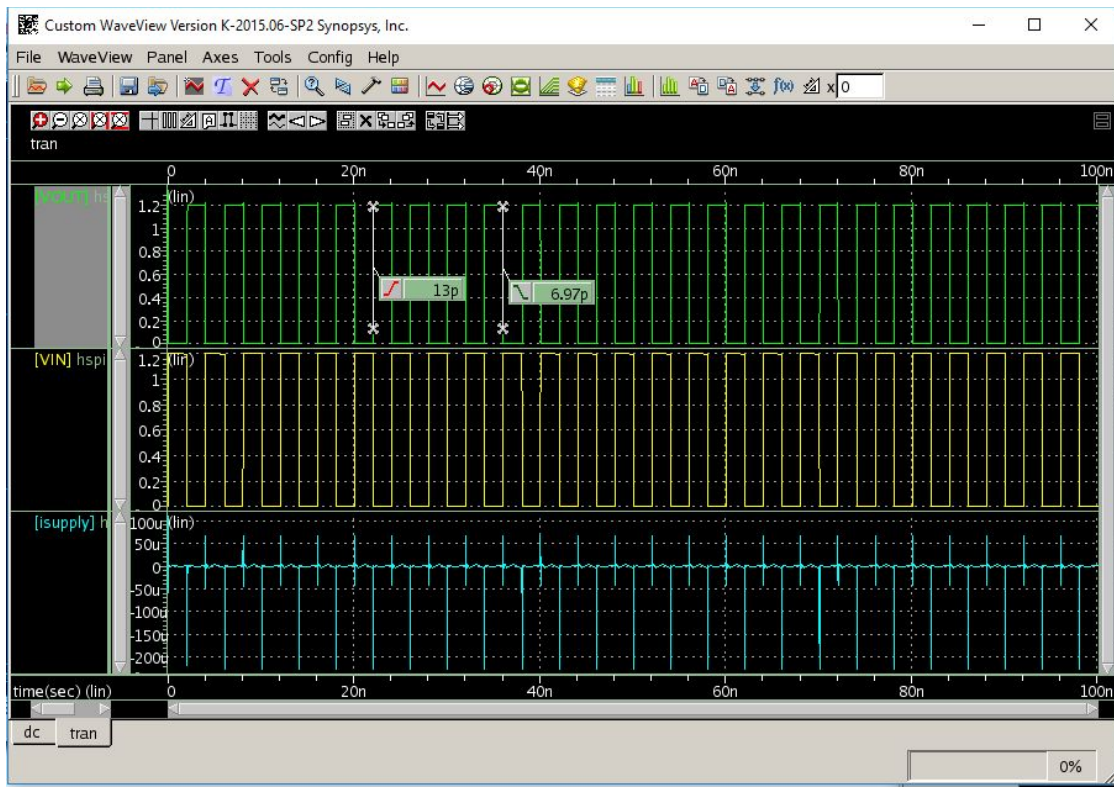
A DC Sweep analysis waveform as seen in Fig. 29:



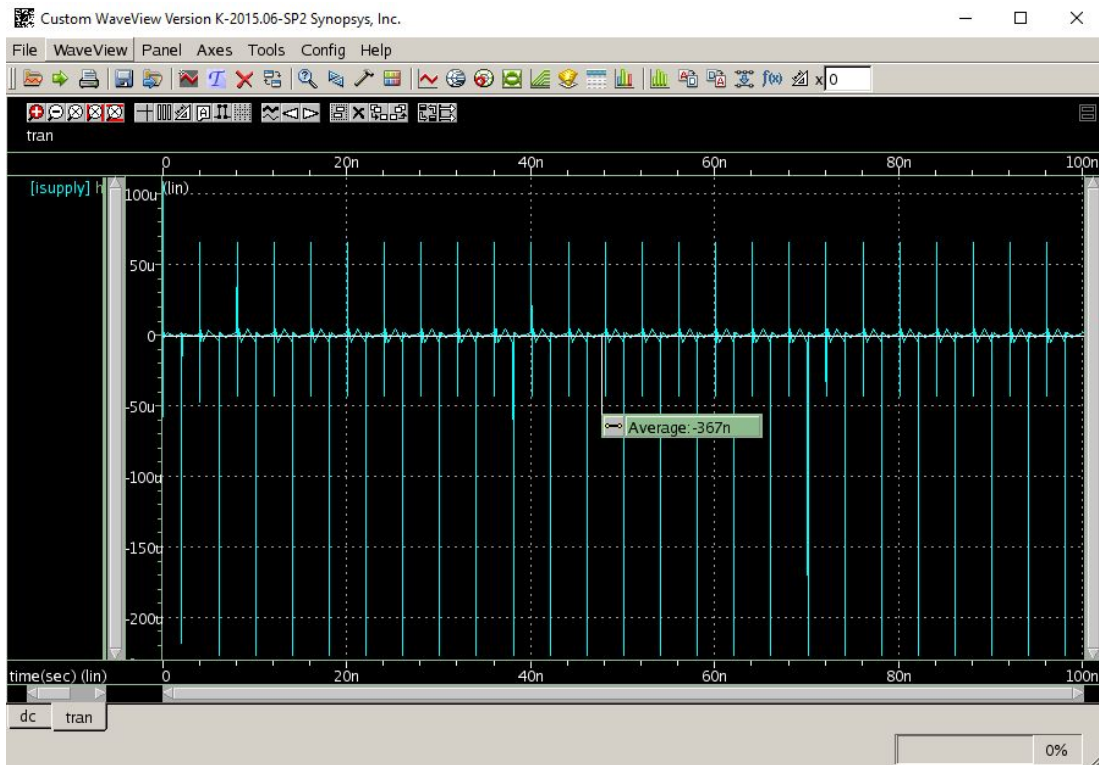
A delay measurement of VOUT and VIN at 50% to 50% annotated waveform as seen in Fig. 33:



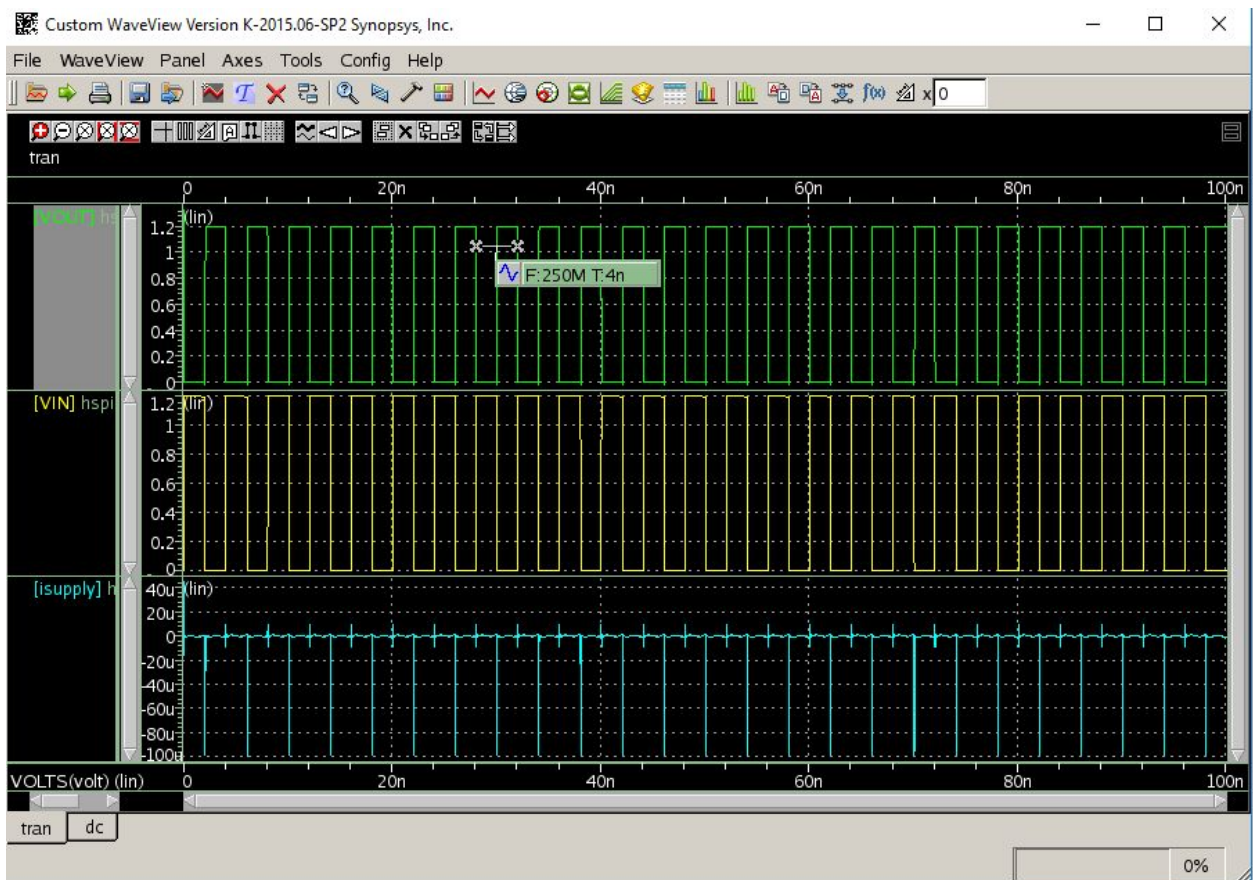
A rise AND fall measurement at 90% and 10% for VOUT annotated waveform as seen in Fig. 35:



An average current measurement annotated waveform as seen in Fig. 37:



A frequency measurement for VOUT annotated waveform as seen in Fig.39:



I initially ran into many problems while trying to complete the lab. Mainly, some of the instructions were ambiguous to me, which made progressing in the lab difficult. However, after going to the lab session and asking the TA, I was able to complete the remainder of the lab fairly easily. Thank you, Mr. Kind TA.