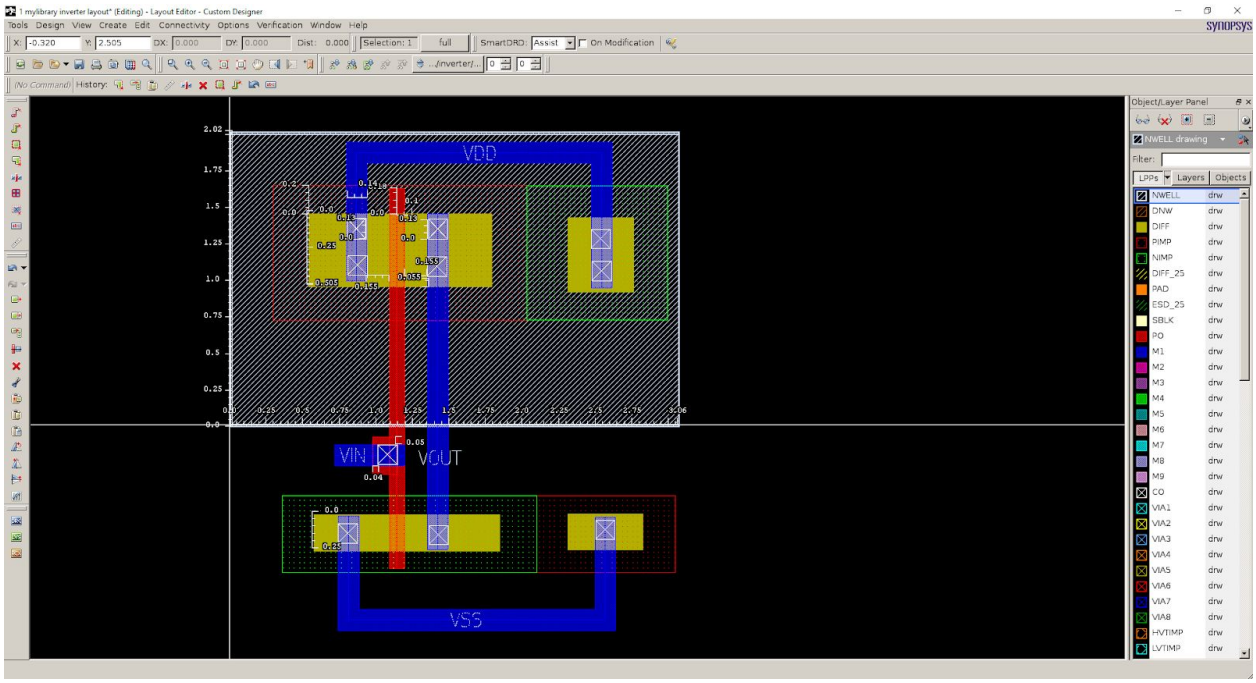
Name: Adrian Tran
Session: 022
ENGR ID: adtran
UCR NETID: atran059

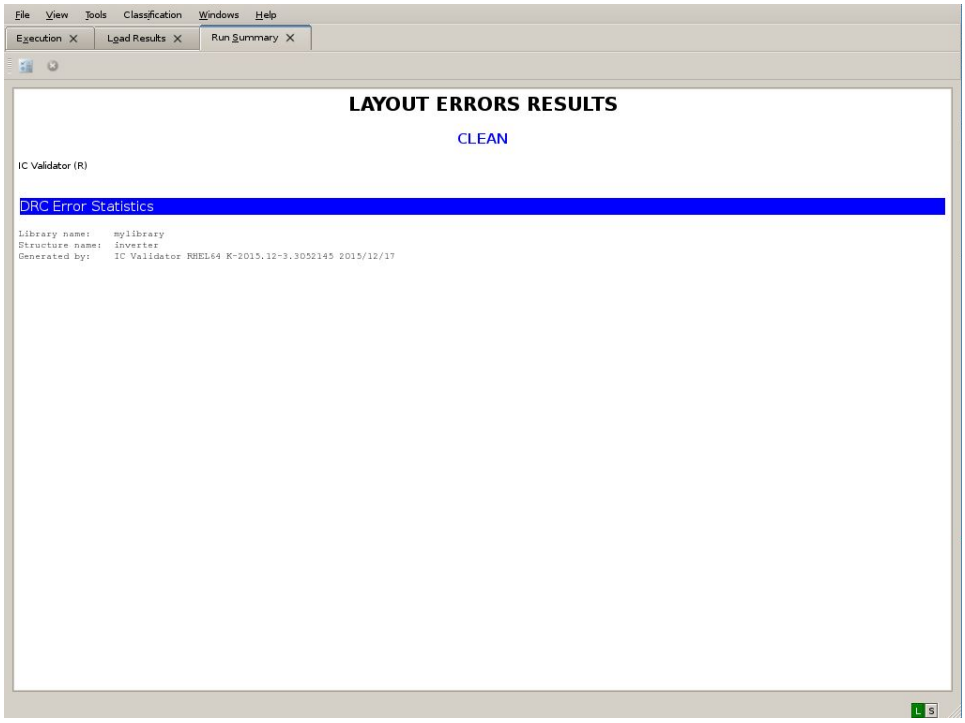
Summary

Throughout this lab, I learned how to design a layout, then validate the layout with DRC and LVS. Specifically, I learned the different layout rules to conform to the protocols set by the DRC and LVS. Then, I debugged the errors.

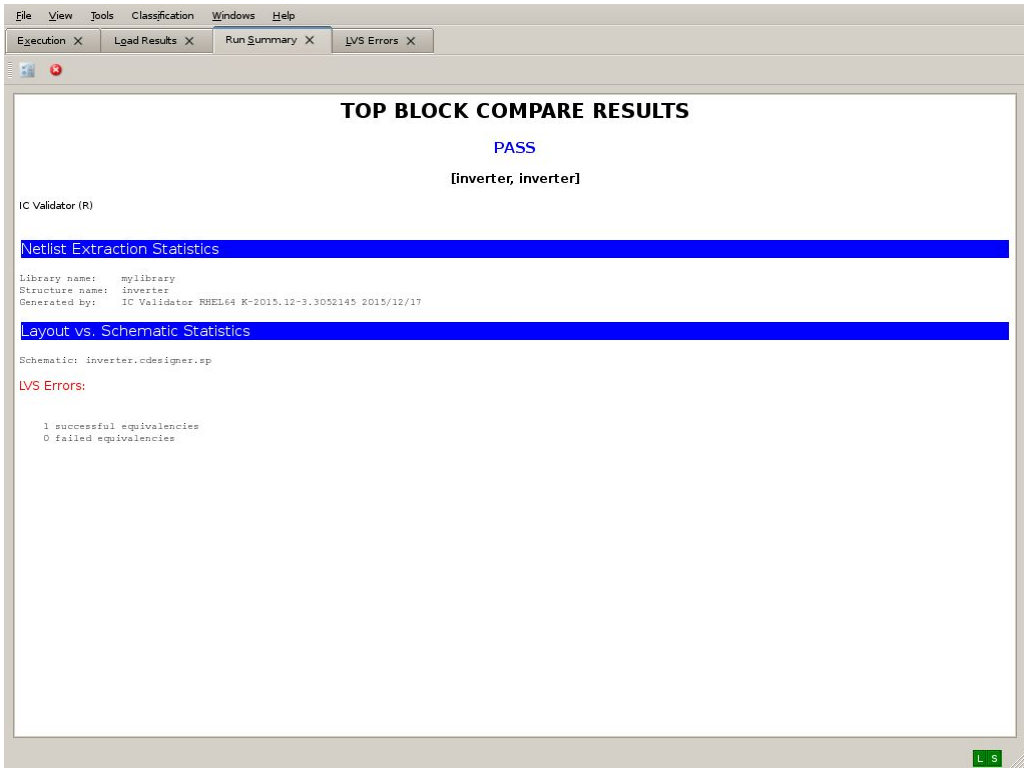
Inverter layout (Figure. 51)



A DRC Result with CLEAN for inverter layout (Figure 57):



A LVS Result with PASS for inverter layout (Figure 64):



I was not able to complete the NAND portion of the lab (Part 8). This is due primarily to time constraints. I had trouble finishing up the DRC and LVS errors because I wasn't sure what some of them were referring to. The onus is on me, though; I should have allocated more time for the completion of this lab.