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# CS168 Lab 4 Report

## Week 1 Checkoff From Here

### Verilog Questions

*All multi-answers are given from the top downwards

**Chapter 1:**

1) a
2) b
3) False, False, True, False
4) Legal, Illegal, Legal, Legal
5) No
6) No, No
7) Yes, Yes
8) Yes, Yes
9) No, Yes, Yes
10) No, No

**Chapter 2**

1) 1, 3 4
2) 2, 3, 5 6
3) B
4)

```
module Q4 (count, clock);
  input clock;
  output count;
  reg [3:0] count, count_reg;

  initial count_reg = 0;

  always @(posedge clock)
    count_reg = count_reg + 1;

  always @(negedge clock)
    count = count_reg;
endmodule
```

```
module Q2;
  reg clock;
  wire [3:0] count;
  Q4 counter (count, clock);

  initial begin
      clock = 0;
   #8 forever begin
        #2  clock = 1;
        #2  clock = 0;
      end
  end
endmodule
```

5)

```
module Q5 (count, clock);
   input clock;
   output [3:0] count;
   reg [3:0] count_reg;

   initial count_reg = 0;

   always @(posedge clock)
      count_reg = count_reg + 1;

   assign #2 count = count_reg;
endmodule
```

6)

```
module Q6 (count, clock);
   input clock;
   output [3:0] count;
   parameter clktoq = 2;
   reg [3:0] count_reg;

   initial count_reg = 0;

   always @(posedge clock)
      count_reg = count_reg + 1;

   assign #clktoq count = count_reg;
endmodule
```

## Chapter 3

1) Constant, delay, scalar, scalar, non-fixed,size, fixed-size
2) Illegal, 9, 0, 4'b0100x, illegal, 4'b1010, illegal, 1'b0, 1'bx, 1'bx
3) B
4) 4, Yes, 6 or 10, No
5) #1x = x + 1;

## Chapter 4

1)

```
module vabc (d, s);
   input [1:0] s;
   output [3:0] d;

   not  (s1_, s[1]), (s0_, s[0]);

   and (d[3], s1_, s0_);
   and (d[2], s1_, s[0]);
   and (d[1], s[1], s0_);
   and (d[0], s[1], s[0]);
endmodule
```

2)

```
module dabc (a, b, c, d, s1, s0);
   input s1, s0;
   output a, b, c,d;

   not  (s1_, s1), (s0_, s0);

   and #3 (a, s1_, s0_);
   and #3 (b, s1_, s0);
   and #3 (c, s1, s0_);
   and #3 (d, s1, s0);
endmodule
```

3) 1

```
module mod (in1, in2, s, out);
   input in1, in2, s;
   output out;

   or (out, o1, o2);
   and (o1, in1, s);
   and (o2, in2 s_);
   not (s_, s);

endmodule
```

4)

```
module xyz (a, b);
   input a;
   output b;

   not (a_, a);
   nand (t1, a, b);
   nand (b, a_, t1);
endmodule
```

5)

**Chapter 5**

1) 1
2) 3
3) assign #1 s = a + 1b;
4) always #10 clock = ~clock;

**Sample solution:**

```
module test;
        reg x, y, clk;

        always
            #10 clk = ~clk;

        initial begin
                $display("clk    x    y");
                x = 0;
                y = 0;
                clk = 1;
                forever
                @clk    $strobe(" %b     %b    %b", clk, x, y);
        end

        initial begin
                @(negedge clk) ;
                @(negedge clk)
                        x = 1;
                @(negedge clk)
                        x = 0;
                @(posedge clk) ;
                @(posedge clk)
                        $finish();
        end

        reg t;
        initial t = 0;
        always @(posedge clk)
                t = x;

        always @(negedge clk)
                y = t;
endmodule
```

5)

6) Behavioral

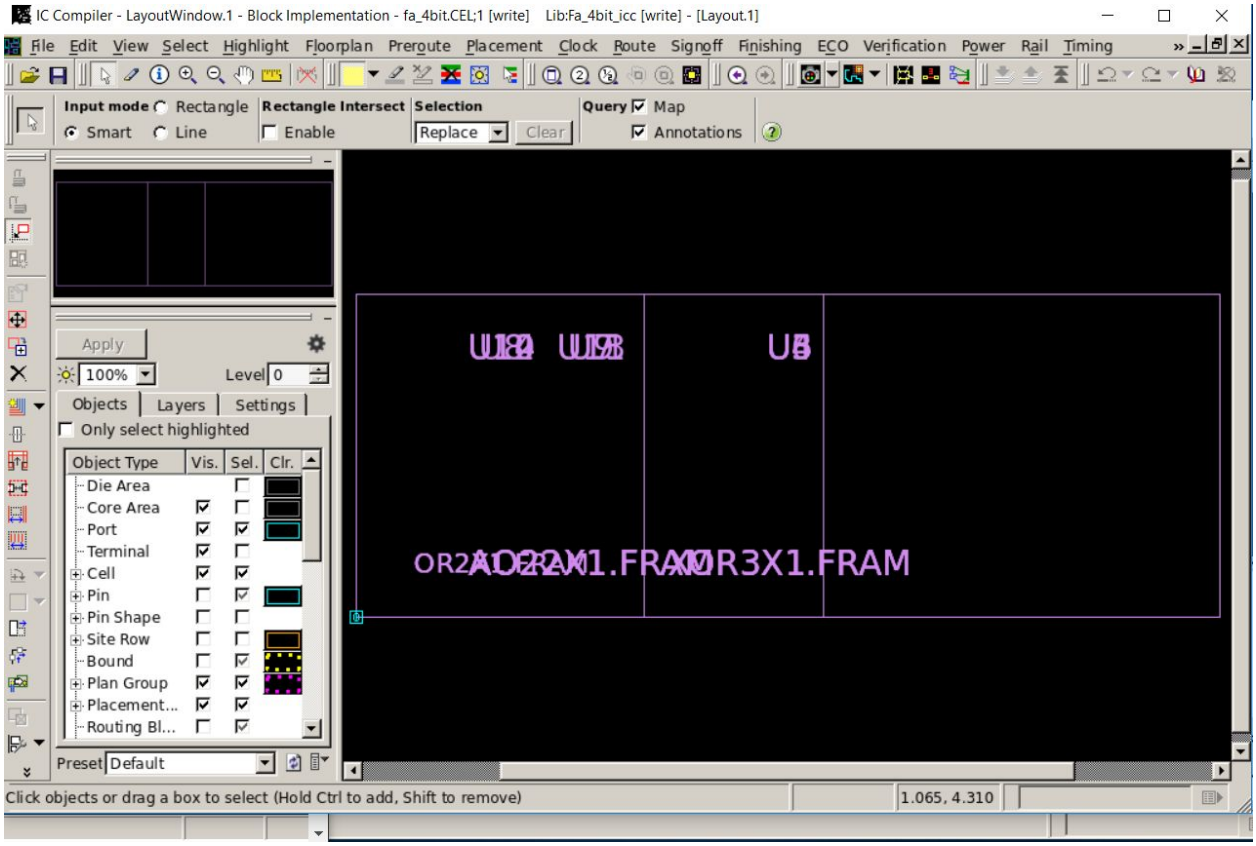
7) Register transfer, behavioral

**One possible solution is:**

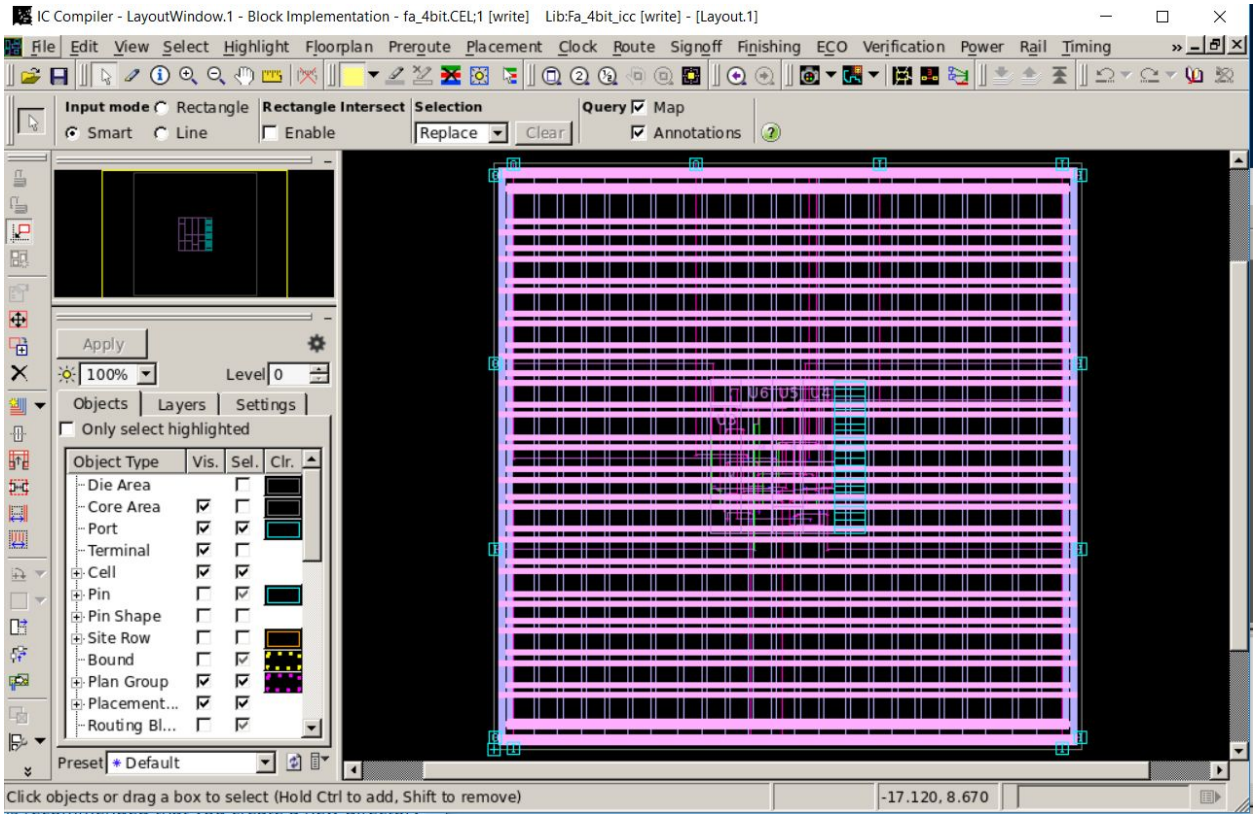
```
or  #1 mux (a, t1, t2, t3);
not (s0_, s[0]);
not (s1_, s[1]);
and (sel1, s1_, s[0]);
and (sel2, s[1], s0_);
nor (sel3, sel1, sel2);
and (t1, sel1, x);
and (t2, sel2, y);
and (t3, sel3, z);
```

8)

## Simulation result of example counter:

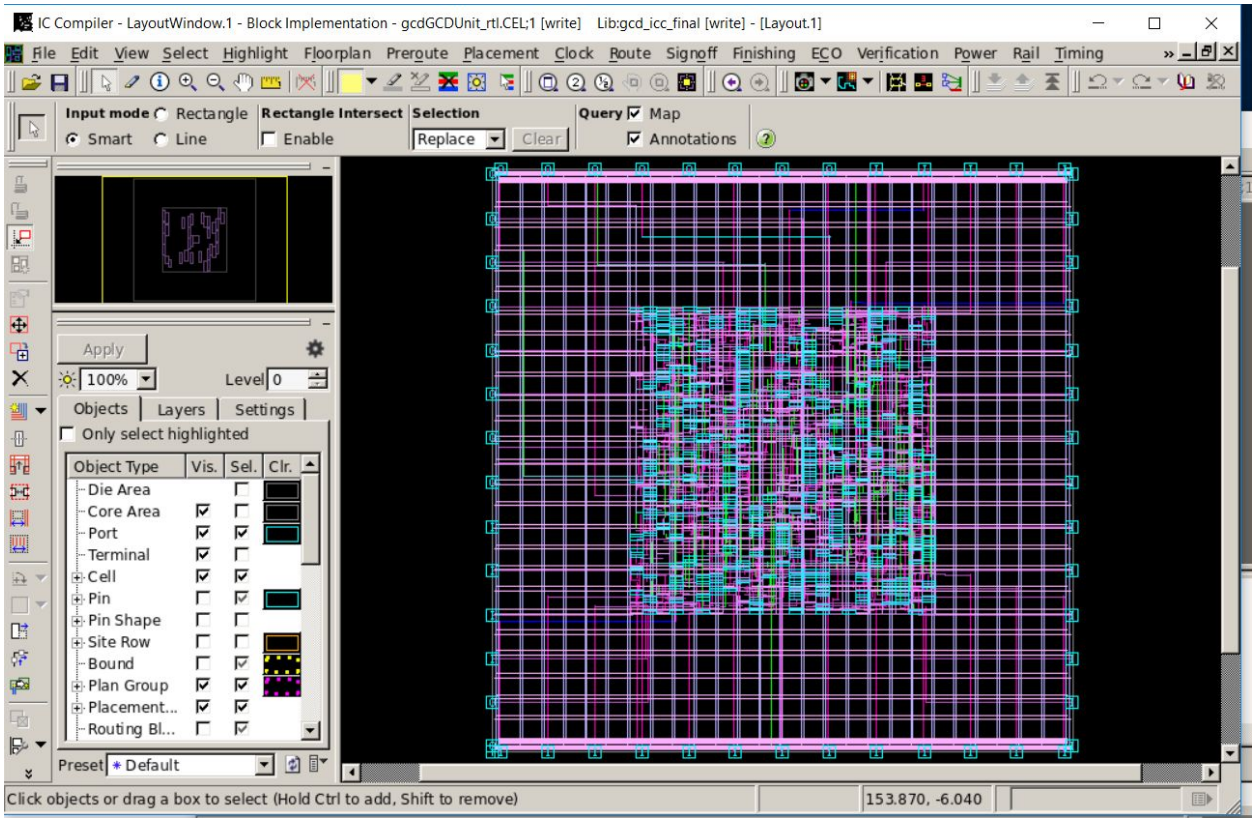


**Final Layout in Figure 49 for 4-bit full adder:**




**<u>Week 2 Checkoff From here:</u>**

**Final Layout in Figure 51:**




**5 Design Compiler Report (timing, power, area, reference, and resource):**

**<u>Timing Report</u>**

```
****************************************
Report : timing
        -path full
        -delay max
        -nets
        -max_paths 1
        -transition_time
Design : gcdGCDUnit_rtl
Version: K-2015.06-SP4
Date   : Sun Mar 10 00:15:10 2019
****************************************

Operating Conditions: TYPICAL   Library: saed90nm_typ
Wire Load Model Mode: top

  Startpoint: GCDdpath0/A_reg_reg[4]
              (rising edge-triggered flip-flop clocked by ideal_clock1)
```

Endpoint: GCDdpath0/A_reg_reg[9]
(rising edge-triggered flip-flop clocked by ideal_clock1)
Path Group: ideal_clock1
Path Type: max

Attributes:
d - dont_touch
u - dont_use
mo - map_only
so - size_only
i - ideal_net or ideal_network
inf - infeasible path

| Point | Fanout | Trans | Incr | Path | Attributes |
|---|---|---|---|---|---|
| clock ideal_clock1 (rise edge) | | | 0.00 | 0.00 | |
| clock network delay (ideal) | | | 0.00 | 0.00 | |
| GCDdpath0/A_reg_reg[4]/CLK (DFFARX1) | | | 0.00 | 0.00 | 0.00 r |
| GCDdpath0/A_reg_reg[4]/Q (DFFARX1) | | | 0.04 | 0.24 | 0.24 f |
| result_bits_data[4] (net) | 5 | | 0.00 | 0.24 f | |
| U153/QN (NAND2X1) | | | 0.04 | 0.03 | 0.28 r |
| n294 (net) | 2 | | 0.00 | 0.28 r | |
| U251/QN (INVX0) | | | 0.03 | 0.03 | 0.31 f |
| n183 (net) | 2 | | 0.00 | 0.31 f | |
| U133/QN (NAND2X0) | | | 0.06 | 0.04 | 0.35 r |
| n149 (net) | 1 | | 0.00 | 0.35 r | |
| U252/QN (NAND2X1) | | | 0.05 | 0.04 | 0.39 f |
| n314 (net) | 3 | | 0.00 | 0.39 f | |
| U253/QN (NAND2X2) | | | 0.03 | 0.02 | 0.41 r |
| n153 (net) | 1 | | 0.00 | 0.41 r | |
| U258/QN (NAND2X1) | | | 0.03 | 0.03 | 0.44 f |
| n154 (net) | 1 | | 0.00 | 0.44 f | |
| U259/Q (AO21X1) | | | 0.04 | 0.08 | 0.52 f |
| n227 (net) | 4 | | 0.00 | 0.52 f | |
| U177/Q (LSDNX1) | | | 0.04 | 0.08 | 0.60 f |
| n308 (net) | 2 | | 0.00 | 0.60 f | |
| U320/Q (AO21X1) | | | 0.03 | 0.09 | 0.69 f |
| n233 (net) | 1 | | 0.00 | 0.69 f | |
| U322/Q (XOR2X1) | | | 0.04 | 0.12 | 0.81 r |
| n234 (net) | 1 | | 0.00 | 0.81 r | |
| U140/QN (NAND2X0) | | | 0.05 | 0.04 | 0.84 f |
| n238 (net) | 1 | | 0.00 | 0.84 f | |
| U324/QN (NAND4X0) | | | 0.07 | 0.04 | 0.88 r |

```
n91 (net)                                1          0.00       0.88 r
GCDdpath0/A_reg_reg[9]/D (DFFARX1)                  0.07       0.00       0.88 r
data arrival time                                   0.88

clock ideal_clock1 (rise edge)                      1.00       1.00
clock network delay (ideal)                         0.00       1.00
GCDdpath0/A_reg_reg[9]/CLK (DFFARX1)                0.00       1.00 r
library setup time                                 -0.12       0.88
data required time                                  0.88
--------------------------------------------------------------------------------
data required time                                  0.88
data arrival time                                  -0.88
--------------------------------------------------------------------------------
slack (MET)                                         0.00
```

**Area Report**

```
****************************************
Report : area
Design : gcdGCDUnit_rtl
Version: K-2015.06-SP4
Date   : Sun Mar 10 00:16:39 2019
****************************************

Library(s) Used:

    saed90nm_typ (File:
/usr/local/synopsys/pdk/SAED90_EDK/SAED_EDK90nm_REF/references/ChipTop/ref/saed90n
m_fr/LM/saed90nm_typ.db)

Number of ports:                        54
Number of nets:                        384
Number of cells:                       317
Number of combinational cells:         283
Number of sequential cells:             34
Number of macros/black boxes:            0
Number of buf/inv:                      34
Number of references:                   30

Combinational area:            1995.864012
Buf/Inv area:                   199.999007
Noncombinational area:         1081.958015
Macro/Black Box area:             0.000000
Net Interconnect area:      undefined  (No wire load specified)
```

Total cell area: 3077.822028
Total area: undefined

Hierarchical area distribution
---

| Hierarchical cell | Global cell area Total | Absolute Total | Percent | Local cell area Combinational | Noncombinational | Black-boxes | Design |
|---|---|---|---|---|---|---|---|
| gcdGCDUnit_rtl | 3077.8220 | 100.0 | 1995.8640 | 1081.9580 | 0.0000 | | |
| gcdGCDUnit_rtl | | | | | | | |
| Total | | | 1995.8640 | 1081.9580 | 0.0000 | | |

**Power Report**

**********
Report : power
-hier
-analysis_effort low
Design : gcdGCDUnit_rtl
Version: K-2015.06-SP4
Date : Sun Mar 10 00:42:27 2019
**********

Library(s) Used:

saed90nm_typ (File: /usr/local/synopsys/pdk/SAED90_EDK/SAED_EDK90nm_REF/references/ChipTop/ref/saed90nm_fr/LM/saed90nm_typ.db)

Operating Conditions: TYPICAL Library: saed90nm_typ
Wire Load Model Mode: top

Global Operating Voltage = 1.2
Power-specific unit information :
Voltage Units = 1V
Capacitance Units = 1.000000pf

Time Units = 1ns
Dynamic Power Units = 1mW (derived from V,C,T units)
Leakage Power Units = 1pW

| Hierarchy | Switch Power | Int Power | Leak Power | Total Power | % |
|---|---|---|---|---|---|
| gcdGCDUnit_rtl | 2.57e-02 | 0.153 | 8.50e+06 | 0.187 | 100.0 |

**Reference Report**

**********

Report : reference
Design : gcdGCDUnit_rtl
Version: K-2015.06-SP4
Date : Sun Mar 10 00:41:05 2019

**********

Attributes:
b - black box (unknown)
bo - allows boundary optimization
d - dont_touch
mo - map_only
h - hierarchical
n - noncombinational
r - removable
s - synthetic operator
u - contains unmapped logic

| Reference | Library | Unit Area | Count | Total Area | Attributes |
|---|---|---|---|---|---|
| AND2X1 | saed90nm_typ | 7.445000 | 1 | 7.445000 | |
| AO21X1 | saed90nm_typ | 10.138000 | 1 | 10.138000 | |
| AO221X1 | saed90nm_typ | 12.902000 | 4 | 51.608002 | |
| AO222X1 | saed90nm_typ | 14.746000 | 20 | 294.920006 | |
| DFFARX1 | saed90nm_typ | 32.256001 | 32 | 1032.192017 | n |
| DFFX1 | saed90nm_typ | 24.882999 | 2 | 49.765999 | n |
| FADDX1 | saed90nm_typ | 29.490999 | 11 | 324.400991 | r |
| INVX0 | saed90nm_typ | 5.530000 | 9 | 49.770002 | |
| ISOLANDX1 | saed90nm_typ | 7.373000 | 4 | 29.492001 | |

ISOLORX1 saed90nm_typ 7.387000 4 29.548000
MUX21X1 saed90nm_typ 11.059000 4 44.236000
NAND2X0 saed90nm_typ 5.443000 47 255.820992
NAND3X0 saed90nm_typ 7.373000 17 125.341002
NAND4X0 saed90nm_typ 8.294000 3 24.881999
NOR2X0 saed90nm_typ 5.530000 7 38.710001
NOR3X0 saed90nm_typ 8.294000 2 16.587999
NOR4X0 saed90nm_typ 9.216000 4 36.863998
OA21X1 saed90nm_typ 9.216000 3 27.647999
OA22X1 saed90nm_typ 11.059000 19 210.121000
OA221X1 saed90nm_typ 12.902000 1 12.902000
OR4X1 saed90nm_typ 10.152000 1 10.152000
XNOR2X1 saed90nm_typ 13.824000 1 13.824000
---
Total 22 references 2696.369010

**Resource Report**

**********

Report : resources
Design : gcdGCDUnit_rtl
Version: K-2015.06-SP4
Date : Sun Mar 10 00:27:26 2019

**********

Resource Report for this hierarchy in file ./gcd_dpath.v

| Cell | Module | Parameters | Contained Operations |
|---|---|---|---|
| sub_x_2 | DW01_sub | width=16 | GCDdpath0/sub_45 (gcd_dpath.v:45) |
| lt_x_3 | DW_cmp | width=16 | GCDdpath0/lt_51 (gcd_dpath.v:51) |

Implementation Report

| | | Current | Set |
|---|---|---|---|

| Cell | Module | Implementation | Implementation |
|---|---|---|---|
| sub_x_2 | DW01_sub | pparch (area,speed) | |
| lt_x_3 | DW_cmp | pparch (area,speed) | |

**Conclusion:**

I completed the lab fairly easily. However, I did run into some errors with the ICC for the GCD Portion of the lab. I eventually figured it out, though: and the issue is documented on the class Github page. I enjoyed this lab. Much more fun than the last, haha.