SEC-MFAEG-NAND-AN

Power up & Reset command for NAND(K9GBG08X0M) Application Note

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Purpose

This application note for K9GBG08X0M(32Gb MLC NAND) will show about reset command difference between general NAND flashs.

This is helpful for mobile system software engineers.

Definitions and Acronyms

Definitions and Acronyms	Description
MLC	Multi Level Cell
h	Hexadecimal

References

NAND Flash Datasheet.

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1. Power up sequence & first RESET command

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 2V. The RESET command(FFh) must be issued to all /CEs as the first command after the NAND Flash device is powered on. Each /CE will be busy for a maximum of 5ms after a RESET command is issued. In this time period, the acceptable command is 70h/F1h.

/WP pin provices hardware protection and is recommanded to be kept at VIL during power-up and power-down. The two step command sequence for program/erase provides additional software protection.

Table 1.1 AC waveforms for Power Transition

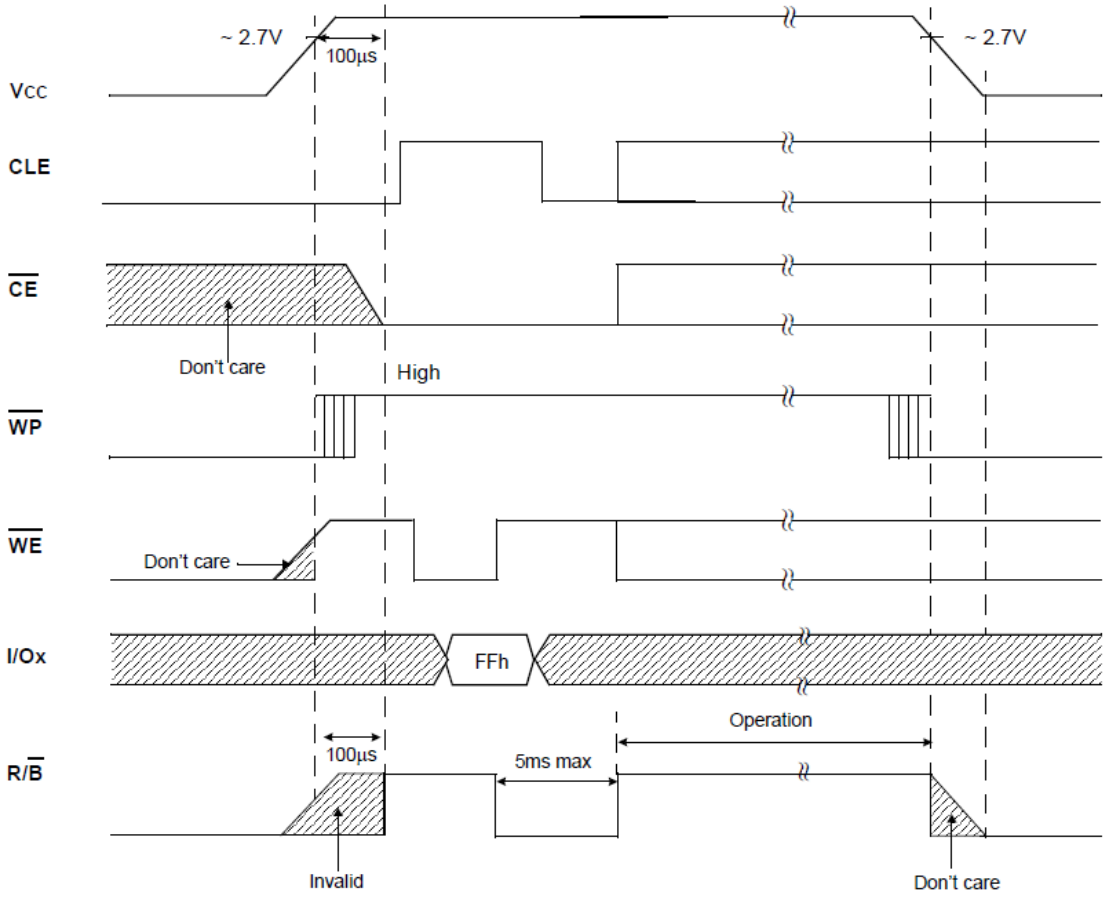
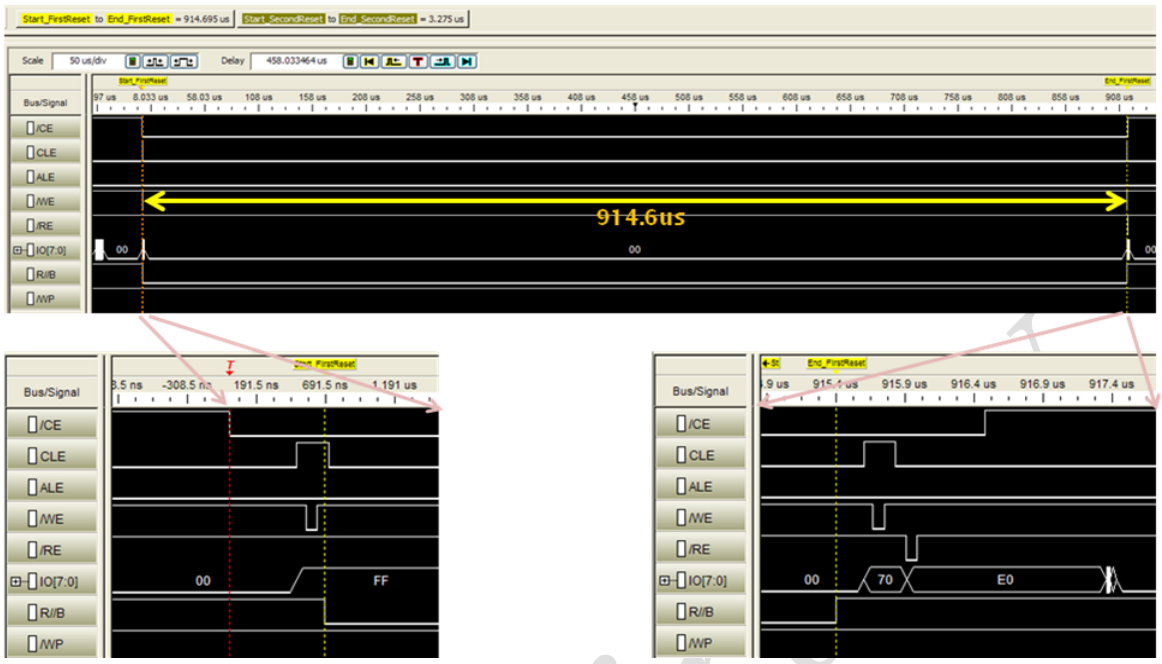


Table 1.2 Example Logic Analyzer waveform – First RESET command sequence after power up.



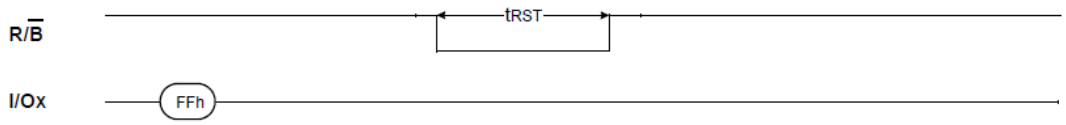
To use NAND flash after power up, system must be issue to RESET Command and wait to R//B pin rising edge(MAX 5ms) for all /CEs in NAND Flash.

2. Reset Command (General)

The device offers a reset feature, executed by writing FFh to the command register.
When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased.

The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when /WP is high. Refer to table for device status after reset operation. If the device is already in reset state a new reset command will be accepted by the command register. The R/B pin changes to low for tRST after the Reset command is written.

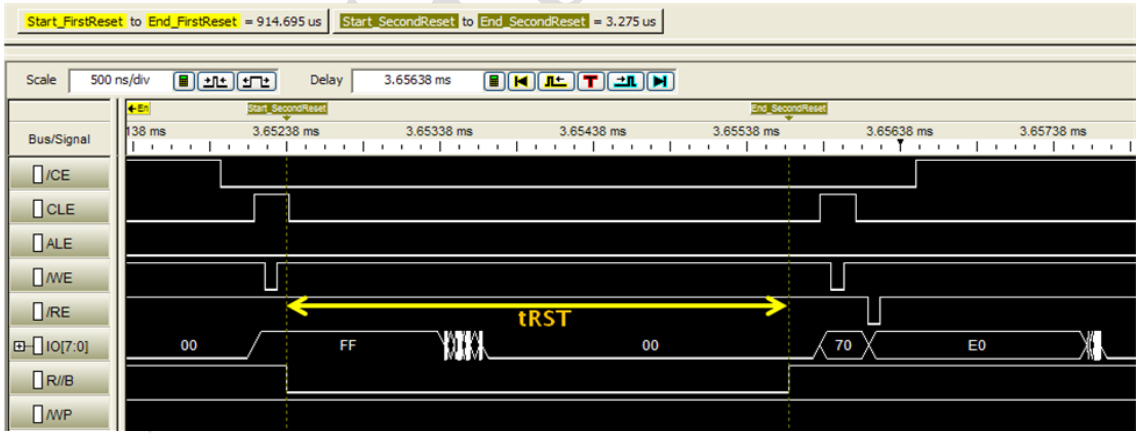
Table 2.1 Reset operation



Device Status

	After Power-up	After Reset
Operation mode Mode	00h Command is latched	Waiting for next command

Table 2.2 Example Logic Analyzer waveform – General RESET command.



3. Example Code & Logic Analyzer Waveform

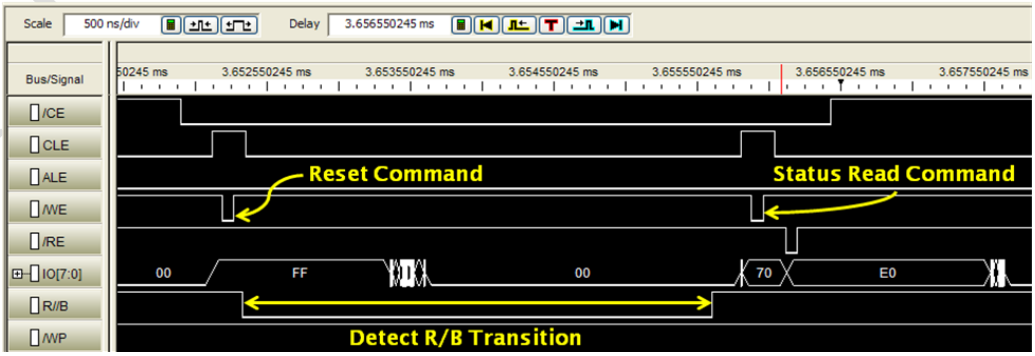
There are two ways to verify NAND flash's Ready/Busy State.

3.1 NAND controller's R/B Register Checking

3.1.1 Example Code (Samsung System LSI. S3C2443 Application Processor)

```
#define NF_nFCE_L()             {rNFCONT&=~(1<<1);}
#define NF_nFCE_H()             {rNFCONT|=(1<<1);}
#define NF_CMD(cmd)             {rNFCMD=cmd;}
#define NF_RDDATA()             rNFDATA;
#define NF_CLEAR_RB()           {rNFSTAT |= (1<<4);}
#define NF_DETECT_RB()          {while(!(rNFSTAT&(1<<4)));}
bool   NAND_Reset()
{
        bool isPASS = false;
        NF_nFCE_L();                    // /CE Low
        NF_CLEAR_RB();                  // R/B Register Clear
        NF_CMD(0xFF);                   // Reset Command
        NF_DETECT_RB();                 // Detect R/B Transition
        NF_CMD(0x70);                   // Status Read Command
        if((NF_RDDATA()&0x1)==0x0)      // Read Status Data(IO[0] = 0 : PASS)
                isPASS = true;
        NF_nFCE_H();                    // /CE High
        return isPASS;
}
```

3.1.2 Logic Analyzer Waveform



3.2 Issuing Read Status Command

3.2.1 Example Code (Samsung System LSI. S3C2443 Application Processor)

```
#define NF_nFCE_L()             {rNFCONT&=~(1<<1);}
#define NF_nFCE_H()             {rNFCONT|=(1<<1);}
#define NF_CMD(cmd)             {rNFCMD=cmd;}
#define NF_RDDATA()             rNFDATA;
void NAND_Reset()
{
        NF_nFCE_L();                    // /CE Low
        NF_CMD(0xFF);                   // Reset Command
        NF_CMD(0x70);                   // Status Read Command
        while(1){
                if((NF_RDDATA()&0x1)==0x0)      // Read Status Data(IO[0] = 0 : PASS)
                        break;
        }
        NF_nFCE_H();                    // /CE High
}
```

3.2.2 Logic Analyzer Waveform