ARM JTAG Interface Specifications

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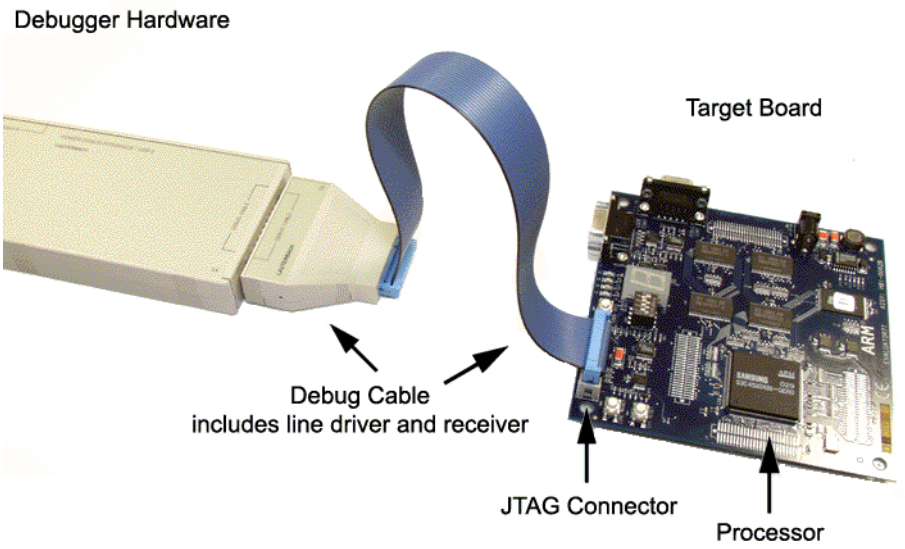
Version 20-Jan-2014

Introduction

The debugger communicates with the target processor via JTAG interface. It is connected with a probe cable (debug cable") to the JTAG connector on the target board.



This application note outlines the requirements to make the interface compatible with the LAUTERBACH debugger for ARM and XScale cores. It describes the requirements with respect to logical functionality, physical connector, electrical characteristics, timing behavior, and printed circuit board (PCB) design. It will be useful for target board designers and for engineers suspecting an issue in an existing interface.

The following text assumes a debug cable version V3 (September 2003 or later) and the connector type of standard delivery. The chapter **Debug Cable Hardware Versions** describes the main differences to other versions. The chapter **Alternative Connector Types** lists optional connectors and available adapters.

Mechanical Connector

The mechanical connector is specified by ARM (ARM-20).

Signal	Pin	Pin	Signal
VTREF	1	2	VSUPPLY(not used)
TRST-	3	4	GND
TDI	5	6	GND
TMS	7	8	GND
TCK	9	10	GND
RTCK	11	12	GND
TDO	13	14	GND
SRST-	15	16	GND
DBGRQ	17	18	GND
DBGACK	19	20	GND

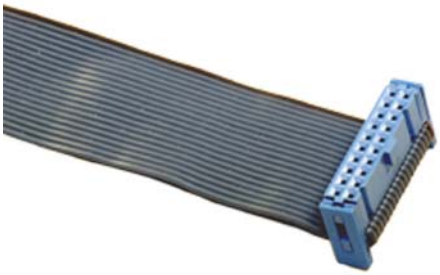
On the target board a male standard 20-pin double row connector (two rows of ten pins), pin to pin spacing: 0.100 in. x 0.100 in., pin width 0.025 in. square post is required. A connector with housing (shrouded) and a center polarization is recommended. These connectors, especially the headers without housing are available from many connector manufacturers.

Examples with housing: Samtec: HTST-110-01-L-D (through-hole)

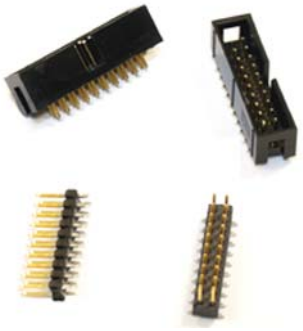
Samtec: HTST-110-01-L-DV (surface mount)

Examples without housing: Samtec: TSW-110-23-L-D

Berg: 67996-120H



Debug Cable



Target Connector

The connector of the debug cable mounted on the blue ribbon cable is an IDC female polarized socket connector of type Tyco / T&B: 1-1658526-3 / 609-2041.

Signals

This JTAG interface is a superset of IEEE Std 1149.1. TCK, TMS, TDI, TDO, TRST- are the standard JTAG signals. A few more signals are added for advanced debug capabilities.

Signal	Pin	Description	Direction (debugger point of view)	Compli-ance
VTREF	1	”Voltage Reference” is the target reference voltage. It indicates if the target power is applied, it is used to create the logic-level reference (VTREF/2) for the debugger input comparators and it auto adjusts the voltage levels of the debugger output driver. It shall be directly connected to the power supply of the processors IO pins. It might have a series resistor, although this is not recommended. It has to be strong enough to overdrive the 100 kΩ pull-down resistor of the debug cable.	input	required
VSUPPLY	2	”Voltage Supply” is used by some debug tools to draw it's supply current. This is not used (not connected) by LAUTERBACH tools which are all self-powered. You might connect this signal to a 5 V or 3.3 V power supply (no series resistor) which is able to supply power to non-LAUTERBACH debug tools.	input	not used

Signal	Pin	Description	Direction (debugger point of view)	Compli-ance
TRST-	3	”Test Reset” (low active) is used for an asynchronous reset of the JTAG Test Access Port (TAP). It resets the TAP state machine and on most ARM families the debug register. See important notes in the chapter **Reset Considerations**. The debugger drives it by a push-pull driver. From the debugger point of view it is optional, because it resets the TAP also by a certain JTAG sequence. You should place a pull-down resistor (1 kΩ - 47 kΩ) on this signal on target side, although this is not JTAG conform. It ensures the on-chip debug logic is inactive when the debugger is not connected.	output	optional
TDI	5	”Test Data In” is the data signal from debugger to processor. You can place a pull-up or pull-down resistor (1 kΩ - 47 kΩ) on this line to ensure a defined state even when the line is not driven by the debugger.	output	required
TMS	7	”Test Mode Select” is the control signal for the TAP controller. You can place a pull-up or pull-down resistor (1 kΩ - 47 kΩ) on this line in order to give it a defined state even when the line is not driven by the debugger.	output	required
TCK	9	”Test Clock” is the clock signal from debugger to processor. You should place a pull-up or pull-down resistor (1 kΩ - 47 kΩ) on this line in order to give it a defined state even when the line is not driven by the debugger.	output	required

Signal	Pin	Description	Direction (debugger point of view)	Compli-ance
RTCK	11	”Return Test Clock” can be used to synchronize the JTAG signals to internal clocks. For more details see chapter **Adaptive Clocking**. If this is not required, then it can be used to compensate the propagation delays on driver and cable. This allows to reach higher JTAG clock frequencies. Therefore you need to feed-back the TCK signal buffered or unbuffered to this line. On an unbuffered feed-back it might have negative effect on signal reflection. Better provide a chance to cut the connection on the target (jumper or solder bridge) in case problems arise.	input	optional
TDO	13	”Test Data Out” is the data signal from processor to debugger. You can place a 33 Ω series resistor close to the processor for series termination. You can place a pull-up or pull-down resistor (1 kΩ - 47 kΩ) on this line.	input	required
SRST-	15	”System Reset” (low active) is used to reset the target system. See important notes in the chapter **Reset Considerations**. The signal is also used by the debugger to detect if the processor is held in reset. There is no need to provide this indication, but if a reset condition is not signalized by this line it should be high (= no reset). The debugger drives it open-drain. A 47 kΩ pull-up is within the debug cable. There might be the need to place a pull-up (1 kΩ - 47 kΩ) on target side to avoid unintentional resets when the debugger is not connected and probably to strengthen the weak 47 kΩ pull-up in the debug cable.	input/ output	optional (required for XSCALE cores)

Signal	Pin	Description	Direction (debugger point of view)	Compli-ance
DBGRQ	17	”Debug Request” (high active) is an output of the debugger to cause the processor to enter debug mode (to halt the processor). The debugger can send a debug request also in an other way which is just slower. On many chips this signal is not provided externally. If available it can be used for fast stopping the processor with a hardware trigger e.g. for synchronous halt of all cores in a multicore system. If this signal is provided by the processor you should place a pull-down resistor (1 kΩ - 47 kΩ) on target side for the case the debugger is not connected.	output	optional
DBGACK	19	”Debug Acknowledge” (high active) is an input of the debugger to sense the processors halt status. On many chips this signal is not provided externally. If available it can be used for fast triggering e.g. for synchronous halt of all cores in a multicore system.	input	optional
GND	4, 6, 8, 10, 12, 14, 16, 18, (20)	”Ground”. All pins should be connected to minimize noise pickup. In the debug cable Pin 20 is connected to ground via a 100 Ω resistor to avoid damage of the debug cable in case it will be connected inversely.		required

There is an additional, small gold plug on the side of the debug cable case. This signal is not required. It can be used for customer specific solutions.

DC Electrical Characteristics

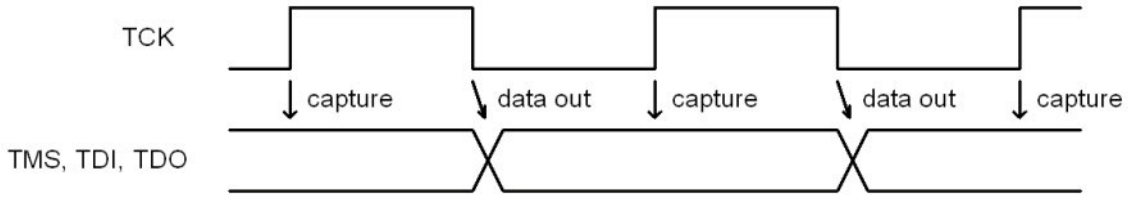
The table below describes the DC electrical characteristics at the 20-pin JTAG connector of the debug cable. The values for current measures positive in direction from the debug cable to the target system. The characteristics apply to the full operation range of the target system. The values below are for reference only and are not guaranteed by LAUTERBACH.

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Vvtref	VTREF operating voltage		0.38		5.25	V
Vvtref_pwrdwn	VTREF power down indication		-0.3	0.27	0.35	V
Ivtref	VTREF current	Vvtref = 5.25V		-0.05	-0.1	mA
Vil	Low-level input voltage	Vvtref = 1.5V Vvtref = 1.8V Vvtref = 2.5V Vvtref = 3.3V Vvtref = 5.0V	-0.3	0.6 0.75 1.1 1.5 2.3	0.3 * Vvtref	V
Vih	High-level input voltage	Vvtref = 1.5V Vvtref = 1.8V Vvtref = 2.5V Vvtref = 3.3V Vvtref = 5.0V	0.7 * Vvtref	0.9 1.0 1.4 1.8 2.6	5.25	V
Vol	Low-level output voltage	typ. values for: Iol = -0.1mA Iol = -1.6mA Iol = -6mA	0	0.01 0.08 0.32	0.3 * Vvtref	V
Voh	High-level output voltage (1)	Vvtref = 0.4V Vvtref = 1.5V Vvtref = 1.8V Vvtref = 2.5V Vvtref = 3.3V Vvtref = 5.0V 0.4V: Ioh=2mA other: Ioh=6mA	0.7* Vvtref	0.31 1.14 1.45 2.15 2.95 4.58	Vvtref	V

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Iil	Low-level input current				0.2	mA
Iih	High-level input current				-0.2	mA
Iol	Low-level output current	Vvtref < 1.5V Vvtref >= 1.5V Vol < 0.3*Vvtref			-2 -6	mA
Ioh	High-level output current (1)	Vvtref < 1.5V Vvtref >= 1.5V Voh > 0.7*Vvtref			2 6	mA
(1) except SRST- which is driven open-drain. There is a 47 kΩ pull-up in the debug cable. An additional pull-up on target side might be required.						

AC Timing Characteristics

Important for the timing is that the data on TDI and TMS will be sampled with the rising edge of TCK (will be output on the falling edge) and that TDO will change on the falling edge of TCK (exception see **Adaptive Clocking**).



All delays will affect the maximum possible JTAG frequency (TCK) which is selectable in the LAUTERBACH tool (default setting: 10 MHz). Issues with minimal setup and hold times can always be resolved by simply decreasing the TCK frequency, because this increases the separation between signal changing and being sampled. Nether the less you should minimize the delays in order to get a good performance e.g. when downloading the application program by the debugger.

The following table should give you an example for the timing considerations in case you like to work with a 20 MHz JTAG clock frequency, which results in a very good performance. The timing is measured at the JTAG connector of the debug cable. Setup times and hold times are measured with respect to 50% signal level value, rise and fall times are measured at 20% and 80%. The measured values are for reference only and are not guaranteed by LAUTERBACH.

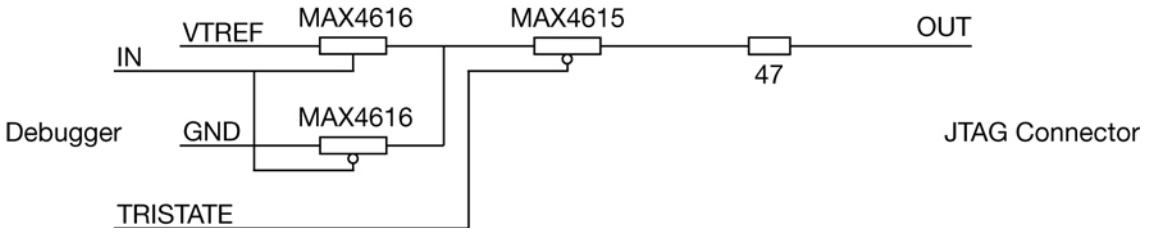
Symbol	Description	Min.	Max.	Unit
Ttck_high	TCK high time	22	28	ns
Ttck_low	TCK low time	22	28	ns
Tsetup	TDI, TMS setup time before rising TCK	21		ns
Thold	TDI, TMS hold time after rising TCK	21		ns
Ttdo_out	TDO output delay time from falling TCK	0	16	ns
Ttrst_low	TRST- low time	1		ms
Tsrst_low	SRST- low time	1		ms
Trf	output rise / fall time load = 10 pF load = 22 pF load = 33 pF		 6 7 8	ns

Values in table for 20 MHz JTAG clock (TCK).

Debug Cable Driver/Receiver

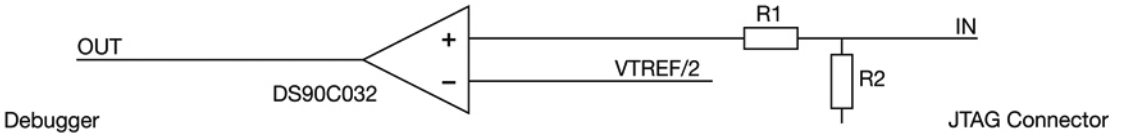
This chapter describes the actual driver/receiver circuitry inside the debug cable (version V3). For additional information refer to the data sheets of MAX4616, MAX4615 and DS90C032.

Output Circuitry



The output signals TCK, TMS, TDI, TRST-, DBGRQ are driven by analog switches which switch the signal level to VTREF (supplied by debugger), GND respectively. Another analog switch is used to tristate this output signal. A 47 Ω resistor is used for current limitation and serial termination. SRST- has a 47 kΩ pull-up instead the analog switch to VTREF (see **Input Circuitry**).

Input Circuitry



The input signals TDO, RTCK, DBGACK, SRST- are compared against VTREF/2.

Signal	R1	R2
RTCK	0 Ω	47 kΩ pull-down, parallel to R2: termination 220 Ω, 220 pF
TDO	0 Ω	100 kΩ pull-down
DBGACK	1 kΩ	47 kΩ pull-down
SRST-	0 Ω	47 kΩ pull-up

Electrical

The JTAG interface is not error tolerant. A spike on TCK will most likely cause a break-down of the JTAG communication which will need a re-initialization of the JTAG interface and a re-start of the debug session. Therefore a careful interface design is required to get the debugger working stable.

A direct and short connection (no buffer or level-shifter) between JTAG connector and processor is recommended.

The debugger output signals are series terminated to reduce signal reflections. A direct, unbuffered connection of TCK to RTCK could have a negative effect. Connect TCK and RTCK with possibility to disconnect them easily in case of coming up problems or use a buffer in between.

Optional, not used signals can be left open (recommended). If you put a fix level on a optional, not used terminal you have to use the inactive state: RTCK = low, DBGRQ = low, DBGACK = low, TRST- = high, SRST- = high.

Recommended pull-up/pull-down value is 10 kΩ (1 kΩ - 47 kΩ). Pull-up or pull-down resistors can be used to give signals a defined level in case of not connected or tristated debugger. Furthermore it reduces crosstalk on the cable between debugger and connector.

To ensure compatibility to other debug cable revisions check chapter **Other Debug Cable Hardware Versions**. The main difference is that older versions draw power from the VTREF signal. To be compatible you should connect VTREF directly to the power supply without a series resistor and allow the older debug cables to draw current which is mainly determined by the pull-ups/pull-downs on the signals driven by the debug cable (about 2 mA).

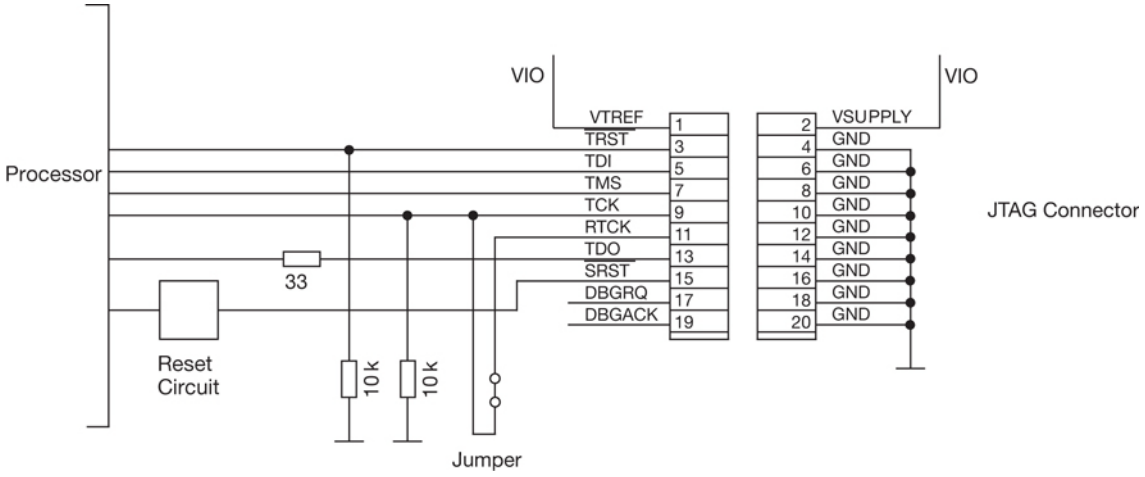
For connecting several debug cables to the same target JTAG interface you need to use the “tristate” mode of the debugger which requires a pull-up at TRST- and a pull-up or pull-down at TCK. ”Tristate” mode ensures that TCK maintains its level and TRST- does not cause a reset during a control hand over between the different debug cables.

NOTE: The procedure for connecting several debug cables differs from that recommended in chapter **Signals**.

There are important design hints dedicated to each signal in chapter **Signals**.

Example for Interface on Target Board

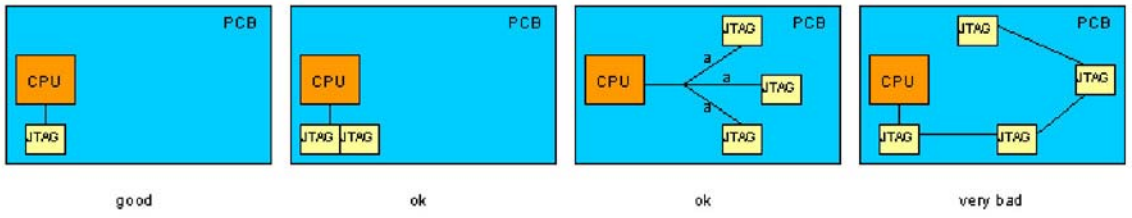
Assumed is a processor which does not need synchronization of JTAG clock and internal clocks (e.g. ARM9TDMI) and does not provide DBSRQ and DBGACK externally.



Layout Considerations

Keep the distance between JTAG connector and processor short (recommended < 5 inch). Preferred position is the edge of the PCB.

The debugger output signals are series terminated to reduce signal reflections. This is negatively effected if you wire the signals to different, optional used connectors.



Assuming a connector type with housing the debug cable requires no additional space around the connector.

If you place the connector the way that the even pin numbers show to the edge of the PCB, then the flat cable goes straight off the PCB.

Avoid tall components around the connector for easy access.

SRST- versus TRST-

For debugging the two reset lines have to be handled independently.

TRST-: Resets the JTAG TAP controller and the CPU internal debug logic.
SRST-: Resets the CPU core and peripherals.

If it does not work this way you will meet issues in the following two scenarios:

Debugging from the very beginning

The standard sequence to start-up debugging is:

- force TRST- and SRST-
- release TRST- (JTAG communication can start)
- initialize debug logic via JTAG and send a break request
- release SRST- (processor becomes active and starts executing the program)
- the break request hits immediate, program execution stops before execution of the first instruction

This scenario allows debug control from the very first instruction of the application code.

Problems arise if TRST- is directly connected to SRST-. The debugger can not send the break request before SRST- is released. As a result the processor starts program execution and parts of the boot code will be executed before a break request can take effect. The debug session does not reflect the real program behavior anymore, since peripherals and interrupts might already be initialized.

When this situation can not be avoided due to an existing design, the following workarounds can help:

- Place a endless loop at the reset vector, probably also disable the watchdog there. After start-up load your program and set the program counter to the begin of your program.
- Maybe there is a way to softreset the processor. This could be done after the start-up procedure to put the processor in reset state. This assumes the softreset does not cause a TRST- like reset.

Debugging a reset event

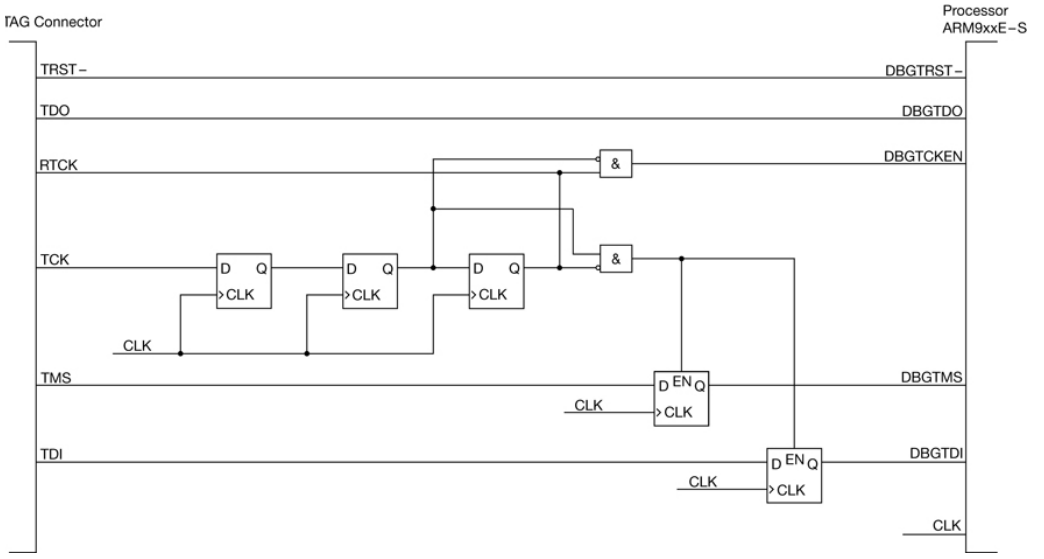
In general debugging of a reset event is supported. Problems arise if this reset event

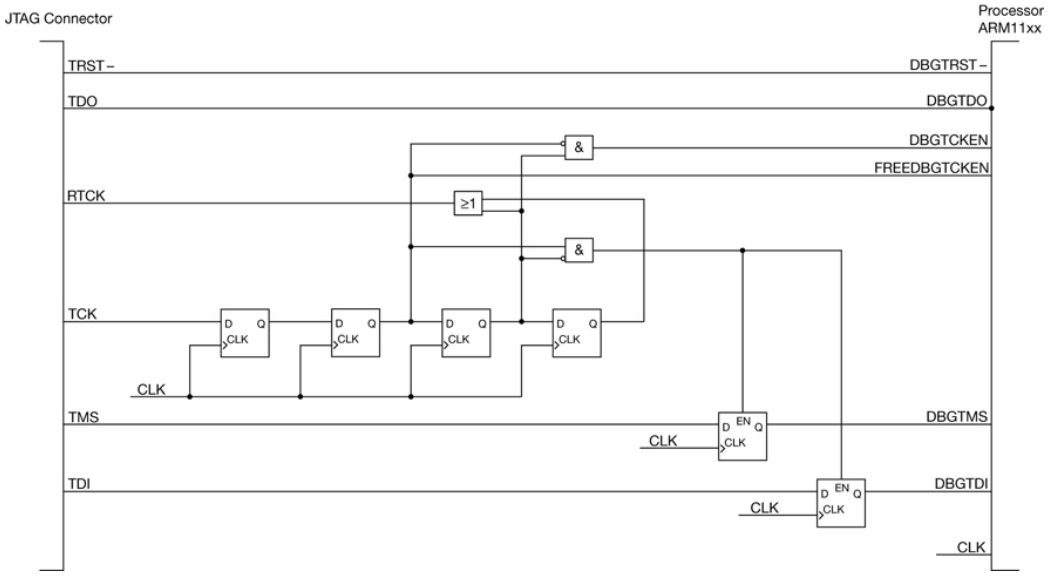
- forces a reset to the JTAG TAP controller, because this cuts the communication between debugger and processor
- forces a reset to any debug related logic like on-chip breakpoints, because it becomes inactive then

In both cases a new debugger start-up is required.

Adaptive Clocking (Return Test Clock RTCK)

The JTAG clock for synthetic cores (e.g. ARM9xxE-S, ARM11xx) must be synchronized externally to the core clock. This might be done on-chip or off-chip. ARM recommends the following synchronization logic in the technical reference manuals of the cores:





The debugger can be switched to "RTCK" clock mode which causes it to issue a TCK edge and to wait for the RTCK (Returned TCK) edge to come back before it progress to the next edge.

Instead of using the "RTCK" clock mode and RTCK signal the debugger can work with a fix TCK frequency. Theoretically a maximum of 1/6 (ARM9), 1/8 (ARM11) of the core clock frequency can be reached. Due to propagation delays and tolerances an even lower TCK frequency must be selected. A fix TCK clock selection will hardly work if the core clock is not known, dynamically changed or if a power saving mode switch off the clock for a certain time. In this cases it is strongly recommended to provide and use RTCK.

Hot Plug-in

The JTAG connector of the debug cable is not suitable for hot plug-in. Connect GND and VTREF first and then the JTAG connector. Otherwise glitches might happen due to the connection of all of the uncharged signals which could e.g. reset the device.

To solve this challenge a special adapter might be required which connects ground of the debugger and target first and provides a voltage level to the reference voltage pin which causes a pre-charging of the signals (then especially the reset signal SRST- is high at the moment of plugging).

Alternative Connector Types

Besides the 20-pin header (ARM-20) which is the standard connector of the current debug cable and the recommended one by LAUTERBACH, there are also other connector types used on the marked. LAUTERBACH meet this by offering adapters for following connectors:

- **Mictor-38**
- **Half Size**
- **TI-14**
- **ARM-14**
- **TI-20 Compact**
- **MIPI-10/20/34**

Mictor-38

When the target board provides a trace port (ETM) and has just a Mictor connector for debug **and** trace interfaces the Mictor-38 adapter can be used to connect a debug cable without a trace probe (preprocessor).

For a LAUTERBACH tool with trace probe (preprocessor) no adapter is necessary. You can plug the debug cable to the preprocessor instead. The preprocessor passes the debug cable signals to the appropriate pins of the Mictor.

Pin 7, 8, 9, 11, 13, 14, 15, 17, 19, 21 and the GND plane of the connector are used for the JTAG interface. The other signals are for the trace interface. Please note that VTREF is at pin 14 (JTAG-VTREF).

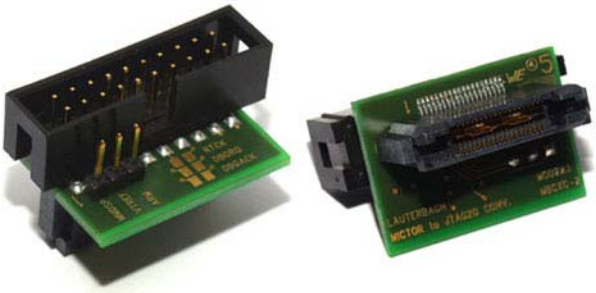
Signal	Pin	Pin	Signal
N/C	1	2	N/C
N/C	3	4	N/C
N/C	5	6	TRACECLK
DBGRQ	7	8	DBGACK
SRST-	9	10	EXTRIG
TDO	11	12	ETM-VTREF
RTCK	13	14	JTAG-VTREF
TCK	15	16	TRACEPKT7
TMS	17	18	TRACEPKT6
TDI	19	20	TRACEPKT5
TRST-	21	22	TRACEPKT4
TRACEPKT15	23	24	TRACEPKT3
TRACEPKT14	25	26	TRACEPKT2
TRACEPKT13	27	28	TRACEPKT1
TRACEPKT12	29	30	TRACEPKT0
TRACEPKT11	31	32	TRACESYNC
TRACEPKT10	33	34	PIPESTAT2
TRACEPKT9	35	36	PIPESTAT1
TRACEPKT8	37	38	PIPESTAT0

There are other Mictor pinouts depending on the ETM version, but the JTAG interface signals will remain at the same pins.

Examples:

AMP 2-5767004-2 (vertical, surface mount)
AMP 767054-1 (vertical, surface mount)
AMP 767061-1 (vertical, surface mount)
AMP 767044-1 (right angle, straddle mount)

The counterpart on the adapter is of type: AMP 5767007-8



LA-3722 Converter 20 Pin JTAG to Mictor 38

Half Size

Half size connector is recommended in case of limited space on the target board.

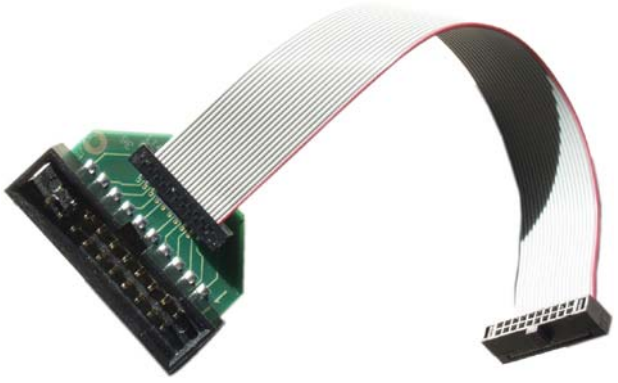
Function and pinout are the same as for the standard connector. The half size adapter has just a smaller footprint for space reduction.

Signal	Pin	Pin	Signal
VTREF	1	2	VSUPPLY(not used)
TRST-	3	4	GND
TDI	5	6	GND
TMS	7	8	GND
TCK	9	10	GND
RTCK	11	12	GND
TDO	13	14	GND
SRST-	15	16	GND
DBGRQ	17	18	GND
DBGACK	19	20	GND

On the target board a male 20-pin double row connector (two rows of ten pins), pin to pin spacing: 0.050 in. x 0.050 in., pin width 0.016 in. square post is necessary. A connector with housing (shrouded) and center polarization is recommended.

Example: Samtec FTSH-110-01-L-DV-K (surface mount)

The counterpart, the gray ribbon cable with the two female connectors on the adapter, has the order number: Samtec FFSD-10-D-04-00-01-N



LA-2101 Adapter Half-Size 20 pin

This connector is defined by Texas Instruments and is used on many target boards from Texas Instruments.

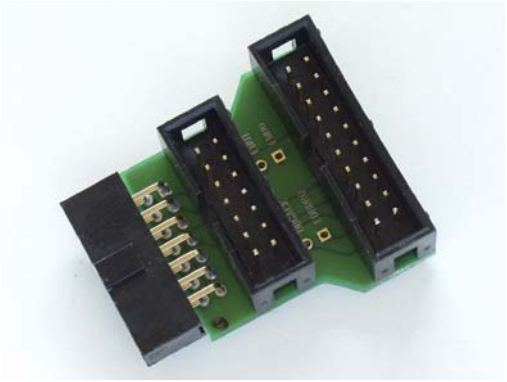
The TI-14 connector does not provide the signal SRST- and has EMU0 and EMU1 instead of DBGRQ and DBGACK. EMUx are signals of processors from Texas Instruments for additional, programmable debug features. LAUTERBACH's debugger supports just EMU0 which is used for the same purpose as DBGRQ and DBGACK.

Signal	Pin	Pin	Signal
TMS	1	2	TRST-
TDI	3	4	GND
VTREF	5	6	GND (KEY)
TDO	7	8	GND
RTCK	9	10	GND
TCK	11	12	GND
EMU0	13	14	EMU1

On the target board a male standard 14-pin double row connector (two rows of seven pins), pin to pin spacing: 0.100 in. x 0.100 in., pin width 0.025 in. square post is necessary. These connectors, especially the headers without housing are available from many connector manufacturers.

The same connector types as for the standard 20-pin connector can be used, but with 14-pin. For details refer to **Mechanical Connector**.

Pin 6 of the female connector of the adapter is plugged to prevent improper connection. Therefore remove the terminal at pin 6 of the target connector.



LA-7748 JTAG ARM Converter ARM-TI

This connector was the first connector definition by ARM. It is used on LAUTERBACH's first debug cable version (V1) and on old target board designs. Do not use it on new designs.

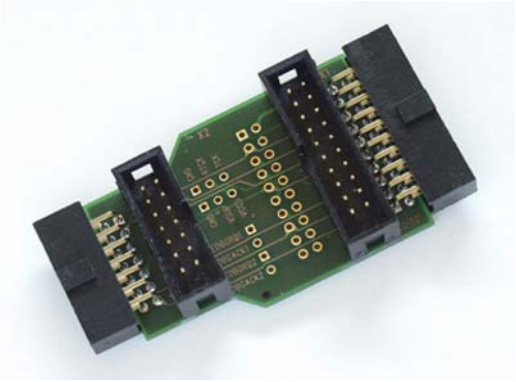
ARM-14 does not provide the signals RTCK, DBGRQ, DBGACK.

VCCS should be used as VSUPPLY when the adapter below is used. On LAUTERBACH's debug cable version V1 VCCS and VTREF are internally connected. When using this debug cable version you need to connect VCCS=VTREF or leave VCCS not connected.

Signal	Pin	Pin	Signal
VCCS	1	2	GND
TRST-	3	4	GND
TDI	5	6	GND
TMS	7	8	GND
TCK	9	10	GND
TDO	11	12	SRST-
VTREF	13	14	GND

On the target board a male standard 14-pin double row connector (two rows of seven pins), pin to pin spacing: 0.100 in. x 0.100 in., pin width 0.025 in. square post is necessary. A connector with housing (shrouded) and center polarization is recommended. These connectors, especially the headers without housing are available from many connector manufacturers.

The same connector types as for the standard 20-pin connector can be used, but with 14-pin. See **Mechanical Connector**.



LA-7747 JTAG ARM Converter 14-20

The adapter can be used to connect a newer debug cable version (V2, V3, V4) to the 14-pin connector on the target. It can also be used to connect the old debug cable version V1 to a 20-pin connector on the target.

TI-20 Compact

TI-20 Compact is a connector definition by Texas Instruments. The connector is smaller and provides more signals than conventional TI-20.

The TI-20 Compact has five EMU signals and supports SRST- and TDIS. EMUx are signals for additional, programmable debug features. LAUTERBACH's debuggers support just EMU0 which is used for the same purpose as DBGRQ and DBGACK. TDIS "Target Disconnect" signal has to be connected to GND on target side. It can be used to detect if the debug cable is connected to a target board. When using the adapter below TDIS will be connected to GND on the debugger side. It will not be used for target detection.

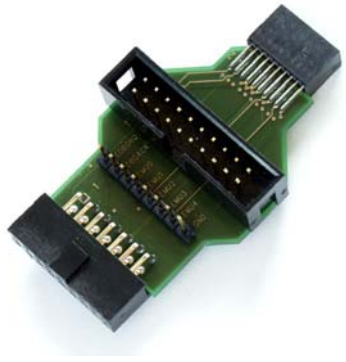
Pin 6 (KEY) of the female connector of the adapter is plugged to prevent improper connection. Therefore remove the terminal at pin 6 of the target connector.

Signal	Pin	Pin	Signal
TMS	1	2	TRST-
TDI	3	4	TDIS (GND)
VTREF	5	6	N/C (KEY)
TDO	7	8	GND
RTCK	9	10	GND
TCK	11	12	GND
EMU0	13	14	EMU1
SRST-	15	16	GND
EMU2	17	18	EMU3
EMU4	19	20	GND

On the target board a male 20-pin double row connector (two rows of ten pins), pin to pin spacing: 0.100 in. x 0.050 in. is necessary.

Example: Samtec FTR-110-01-G-D-06

The female connector of the adapter is of type Samtec: SMS-110-02-S-D.



LA-3780 JTAG Converter to TI Target Adapter 14/20

This adapter can also be adapted to the **TI-14**.

The MIPI connectors have been defined by the Mobile Industry Processor Interface Alliance (MIPI). There are compatible connector versions with different pin counts (10, 20, 34) providing different debug capabilities. MIPI-10 provides the minimum signals the debugger needs. MIPI-20 and MIPI-34 provides additionally the signals RTCK, TRST-, BCE, DBGRQ (or EMU0), DBGACK (or EMU1) and/or a trace port which is not used by the standard debug cable.

Alternatively to JTAG a two wire “cJTAG” interface can be used. The bidirectional data pin is TMSC and the clock pin is TCKC.

BCE ”Boundary Scan Compliancy Enable” pin is an optional static signal, active high. It can be used on target side to deactivate JTAG debug mode by a pull-down on this line for the case no tool is connected. The MIPI-10/20/34 adapter controls this signal the same way as TRST-.

ARM specifies in the CoreSight Components Technical Reference Manual four, quite similar connectors. The Serial Wire Debug interface replaces the five signal JTAG interface by the bidirectional data signal (SWDIO) and a clock signal (SWCLK). The freed up TDO signal can be re-used as a system trace output “Serial Wire Output” (SWO) which is not supported by the standard debug cable.

MIPI-10-nRESET, ARM-10-JTAG (preferred pinout)

Signal	Pin	Pin	Signal
VREF DEBUG	1	2	TMS
GND	3	4	TCK
GND	5	6	TDO
(KEY) GND	7	8	TDI
GND	9	10	RESET-

MIPI-10-nTRST

Signal	Pin	Pin	Signal
VREF DEBUG	1	2	TMS
GND	3	4	TCK
GND	5	6	TDO
(KEY) GND	7	8	TDI
GND	9	10	TRST-

MIPI-10-BCE

Signal	Pin	Pin	Signal
VREF DEBUG	1	2	TMS
GND	3	4	TCK
GND	5	6	TDO
(KEY) GND	7	8	TDI
GND	9	10	BCE

MIPI-10-Narrow

Signal	Pin	Pin	Signal
VREF DEBUG	1	2	TMSC
GND	3	4	TCKC
GND	5	6	EXT
(KEY) GND	7	8	BCE
GND	9	10	RESET-

ARM-10-SWD

Signal	Pin	Pin	Signal
VREF DEBUG	1	2	SWDIO
GND	3	4	SWCLK
GND	5	6	SWO
(KEY) GND	7	8	N/C
GND	9	10	RESET-

MIPI-20-ARM (preferred pinout)

Signal	Pin	Pin	Signal
VREF DEBUG	1	2	TMS
GND	3	4	TCK
GND	5	6	TDO
(KEY) GND	7	8	TDI
GND	9	10	RESET-
GND	11	12	RTCK
GND	13	14	BCE
GND	15	16	TRST-
GND	17	18	DBGRQ
GND	19	20	DBGACK

MIPI-20-TI

Signal	Pin	Pin	Signal
VREF DEBUG	1	2	TMS
GND	3	4	TCK
GND	5	6	TDO
(KEY) GND	7	8	TDI
GND	9	10	RESET-
GND	11	12	RTCK
GND	13	14	BCE
GND	15	16	TRST-
GND	17	18	EMU0
GND	19	20	EMU1

MIPI-20-Narrow

Signal	Pin	Pin	Signal
VREF DEBUG	1	2	TMSC
GND	3	4	TCKC
GND	5	6	EXT
(KEY) GND	7	8	BCE
GND	9	10	RESET-
GND	11	12	TRC CLK
GND	13	14	TRC DATA0
GND	15	16	TRC DATA1
GND	17	18	TRC DATA2
GND	19	20	TRC DATA3

ARM-20-SWD

Signal	Pin	Pin	Signal
VREF DEBUG	1	2	SWDIO
GND	3	4	SWCLK
GND	5	6	SWO
(KEY) GND	7	8	N/C
GND	9	10	RESET-
GND	11	12	TRACE CLK
GND	13	14	TRACE D0
GND	15	16	TRACE D1
GND	17	18	TRACE D2
GND	19	20	TRACE D3

ARM-20-JTAG

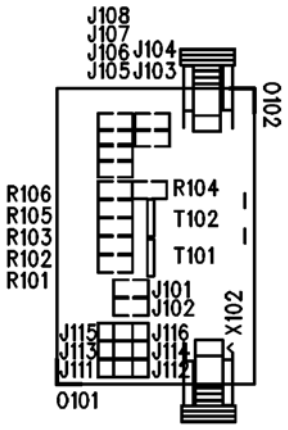
Signal	Pin	Pin	Signal
VREF DEBUG	1	2	TMS
GND	3	4	TCK
GND	5	6	TDO
(KEY) GND	7	8	TDI
GND	9	10	RESET-
GND	11	12	TRACE CLK
GND	13	14	TRACE D0
GND	15	16	TRACE D1
GND	17	18	TRACE D2
GND	19	20	TRACE D3

MIPI-34-ARM (preferred pinout)

Signal	Pin	Pin	Signal
VREF DEBUG	1	2	TMS
GND	3	4	TCK
GND	5	6	TDO
(KEY) GND	7	8	TDI
GND	9	10	RESET-
GND	11	12	RTCK
GND	13	14	BCE
GND	15	16	TRST-
GND	17	18	DBGRQ
GND	19	20	DBGACK
GND	21	22	TRC CLK
GND	23	24	TRC DATA0
GND	25	26	TRC DATA1
GND	27	28	TRC DATA2
GND	29	30	TRC DATA3
GND	31	32	TRC EXT
GND	33	34	VREF TRACE

Signal	Pin	Pin	Signal
VREF DEBUG	1	2	TMS
GND	3	4	TCK
GND	5	6	TDO
(KEY) GND	7	8	TDI
GND	9	10	RESET-
GND	11	12	RTCK
GND	13	14	BCE
GND	15	16	TRST-
GND	17	18	EMU0
GND	19	20	EMU1
GND	21	22	TRC CLK
GND	23	24	TRC DATA0
GND	25	26	TRC DATA1
GND	27	28	TRC DATA2
GND	29	30	TRC DATA3
GND	31	32	TRC EXT
GND	33	34	VREF TRACE

The MIPI adapter will be delivered to support without change MIPI-10-nRESET(=ARM-10-JTAG), MIPI-20-ARM and MIPI-34-ARM (in case DBGRQ and DBGACK is not needed; you need to close J103 and J104 otherwise). The other pinouts specified by MIPI and ARM are all supported, but need to be configured by solder bridges:



	J101-J102	J103-J104	J105-J108	J111	J112	J113	J114	J115	J116
MIPI-10-nRESET, ARM-10-JTAG	X	—	O	X	O	X	O	X	O
MIPI-10-nTRST	X	—	O	X	O	X	O	O	X
MIPI-10-BCE	X	—	O	X	O	X	O	O	X
MIPI-10-Narrow	—	O	X	O	X	O	X	X	O
ARM-10-SWD	—	O	O	O	X	O	X	X	O
MIPI-20-ARM	X	X	O	X	O	X	O	X	O
MIPI-20-TI	X	O	X	X	O	X	O	X	O
MIPI-20-Narrow	O	O	X	O	X	O	X	X	O
ARM-20-SWD	O	O	O	O	X	O	X	X	O
ARM-20-JTAG	O	O	O	X	O	X	O	X	O
MIPI-34-ARM	X	X	O	X	O	X	O	X	O
MIPI-34-TI	X	O	X	X	O	X	O	X	O

Table legend:
X = closed
O = open
— = don´t care

On the target board is a male double row connector, pin to pin spacing: 0.050 in. x 0.050 in., pin width 0.016 in. square post is necessary. A connector with housing (shrouded) and a center polarization is recommended.

Example (surface mount):

MIPI-10: Samtec FTSH-105-01-L-DV-K
MIPI-20: Samtec FTSH-110-01-L-DV-K
MIPI-34: Samtec FTSH-117-01-L-DV-K

The counterpart, the gray ribbon cable with the two female connectors on the adapter, has the order number:

MIPI-10: Samtec FFSD-05-D-04-00-01-N
MIPI-20: Samtec FFSD-10-D-04-00-01-N
MIPI-34: Samtec FFSD-17-D-04-00-01-N

LA-3770 Converter ARM-20 to MIPI-10/20/34

Delivered with three flat cables for MIPI-10, MIPI-20, MIPI-34

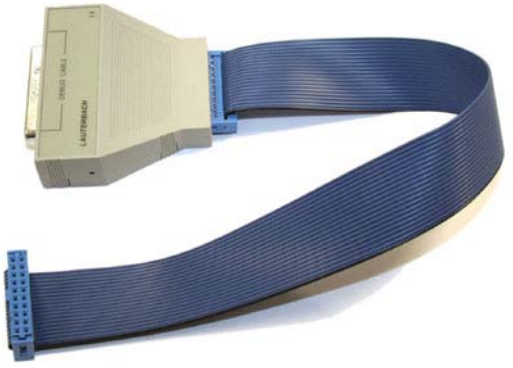
Debug Cable Hardware Versions

The above description assumes the debug cable version V3. You can identify the debug cable version by typing ”version.hardware” into the TRACE32 command line or compare your debug cable with the pictures below. Debug cable versions and a description of the main differences are described in the following.

Hardware Version	**V1**	**V2**	**V3**	**V4**
Delivery (year)	1998 … 2000	2001 … 2003	since 2004	since 2008
Last digits of serial number	< 11250	<= 39000	> 39000	> 90853 (Cortex-M) > 94121 (Cortex-A/R) >C0801xxxxxx (others)
Supported target voltage range [V]	2.5…5.0	1.8…3.3	0.4….5.0	0.4….5.0
Supported target connector	ARM-14	ARM-20	ARM-20	ARM-20
Support for Serial Wire Debug and cJTAG	no	no	no	yes
Serial termination of output signals	no	no	yes	yes
Output drivers supplied by	VTREF (draws about 3 mA)	VTREF (draws about 3 mA)	debugger hardware	debugger hardware
output driver type	74VHC125	74ALVC164256	see **Debug Cable Driver/ Receiver**	driver as V3 but placed next to the JTAG connector
Input signals	TDO needs to be TTL compatible RTCK, DBGRQ, DBGACK are not supported	TDO, RTCK, DBGACK are connected to 74ALVC164256 which is supplied by VTREF	see **DC Electrical Characteristics** and **Debug Cable Driver/ Receiver**	receiver as V3 but placed next to the JTAG connector

Version V1

Version V2



Version V3

Version V4