CPSR:

The CPSR register (register 16) is used to configure the operating mode of the ARM processor, and to check conditions for conditional ARM instructions. For this exercise you should initialise the CPSR to zero. You only need to be concerned with its top four bits, which carry the status flags from computations run on the arithmetic logic unit (ALU)

The flag bits represent:

N: the last result was negative

Z: the last result was zero

C: the last result caused a bit to be carried out

V: the last result overflowed

**Data Processing Instructions:**

* S: Set condition codes. If the bit is set then the CPSR flags should be updated during execution of this instruction.

The data processing instruction is only executed if the Cond field is satisfied by the CPSR register

If the S bit is 0, the CPSR register is unaffected. If the S bit is set then the CPSR flags should be set as follows:

• The V bit will be unaffected.

• The C bit in logical operations (and, eor, orr, teq, tst and mov) will be set to the carry out from any shift operation (i.e.the result from the barrel shifter). In arithmetic operations (add, sub, rsb and cmp) the C bit will be set to the carry out of the bit 31 of the ALU. For addition, C is set to 1 if the addition produced a carry (unsigned overflow), it is set to 0 otherwise. For subtraction (including comparison), the bit C is set to 0 if the subtraction produced a borrow, otherwise is set to 1.

• The Z bit will be set only if the result is all zeros.

• The N bit will be set to the logical value of bit 31 of the result.

The value of operand2 is computed with the contents of Rm. The contents of Rm are not modified as a side effect of the instruction. If a logical shift left operation is applied, then operand2’s least significant bits are filled with the specified number of zeros, while the high bits of Rm are discarded. However, the least significant discarded bit of Rm becomes the shifter carry output which is latched into the C bit of the CPSR if the instruction has to set CPSR flags. The logical shift right operation is similar, but the contents of Rm are moved to the least significant positions of operand2’s value. The arithmetic shift right operation is similar to logical shift right operation, however the high bits of operand2’s value are filled with bit 31 of Rm instead of zeros. The rotate right operation shifts the bits from left to right in a cyclic fashion. Figure 2 illustrates the results in operand2’s value after applying different shift operations.

**Multiply Instructions:**

• S: Set condition codes. If the bit is set then the CPSR flags are be updated during execution of this instruction.

If the S bit has been set, then the N and Z flags of the CPSR should be updated. N is set to bit 31 of the result and Z is set if and only if the result is zero.

**Single Data Transfer instructions:**

These instructions are only executed if the Cond field is satisfied by the CPSR register

**Branch Instructions:**

Branch instructions are only executed if the Condition field is satisfied by the CPSR register