

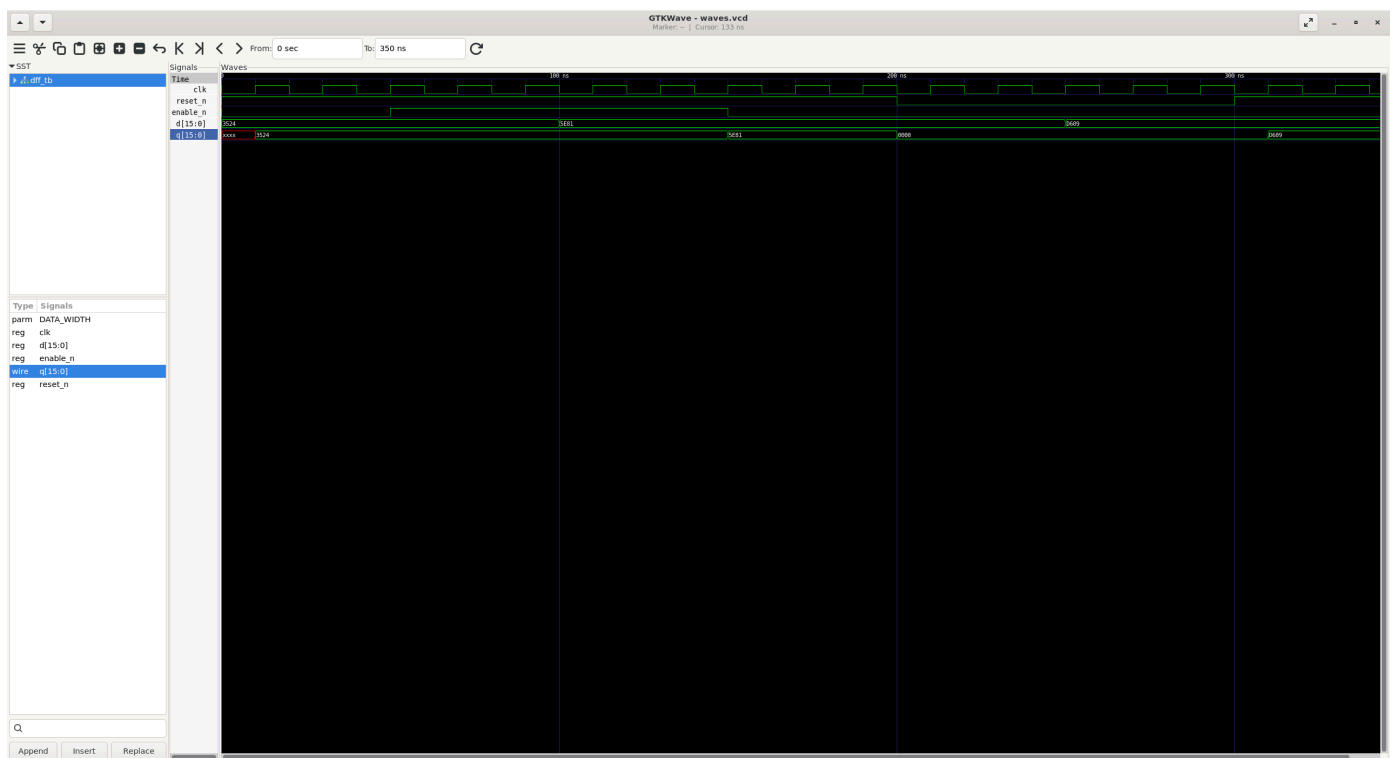
Notes

- ## MUX Results

Icarus Verilog

Waveform





Terminal

```
sim > off > $@ off.tbv
32 module off_tb;
33
34 initial begin
35
36     $display("Initial signal setup:");
37     reset_n = 1; // Disable reset
38     enable_n = 0; // Assert enable
39     d = $random; // Set a random input
40     #5; // wait 5 time units
41
42     // Test enable:
43     $display("Testing enable:");
44     enable_n = 1; // Disable enable
45     #5; // wait 5 units
46     d = $random; // Set a random input
47     #5; // wait 5 units
48     enable_n = 0; // Assert enable
49     #5; // wait 5 units
50
51     // Test reset:
52     $display("Testing reset:");
53     reset_n = 0; // Assert reset
54     #5; // wait 5 units
55     d = $random; // Set a random input
56     #5; // wait 5 units
57     reset_n = 1; // Disable reset
58     #5; // wait 5 units
59
60     // End the simulation:
61     $finish;
62 end
63
64 // Export the wave file (needed for Icarus Verilog):
65 initial begin
66     $writefile("waves.vcd"); // Set the file name
67     $dumpvars(0, off_tb); // Include all the signals
68 end
69
70 endmodule
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```

PROBLEMS OUTPUT DEVICES/CONSOLES TERMINAL PORTS SPELL CHECKER

```
server@SEKTOP:~/verilog-assignment-1$ cd ./src/
server@SEKTOP:~/verilog-assignment-1/src$ make
make -g build
[verilog -g build/off_tb.v].../src/off_tb.v
vvp build/off_tb.v
Initial signal setup:
[0] reset_n=1 enable_n=0 d=403524 q=403524
[10] reset_n=1 enable_n=0 d=403524 q=403524
Testing enable:
[50] reset_n=1 enable_n=1 d=403524 q=403524
[100] reset_n=1 enable_n=1 d=403524 q=403524
Testing reset:
[200] reset_n=0 enable_n=1 d=403524 q=403524
[250] reset_n=0 enable_n=1 d=403524 q=403524
[300] reset_n=1 enable_n=1 d=403524 q=403524
off_tb.v:94: $finish called at 350 (1ns)
gWave waves.vcd
GWave analyzer v1.3.116 (c)1999-2023 BSI
[0] start time.
[350] end time.
M Destroy
server@SEKTOP:~/verilog-assignment-1/src$
```

Vivado

Waveform + Console

