Verilog Assignment 1 - Adrien Abbey

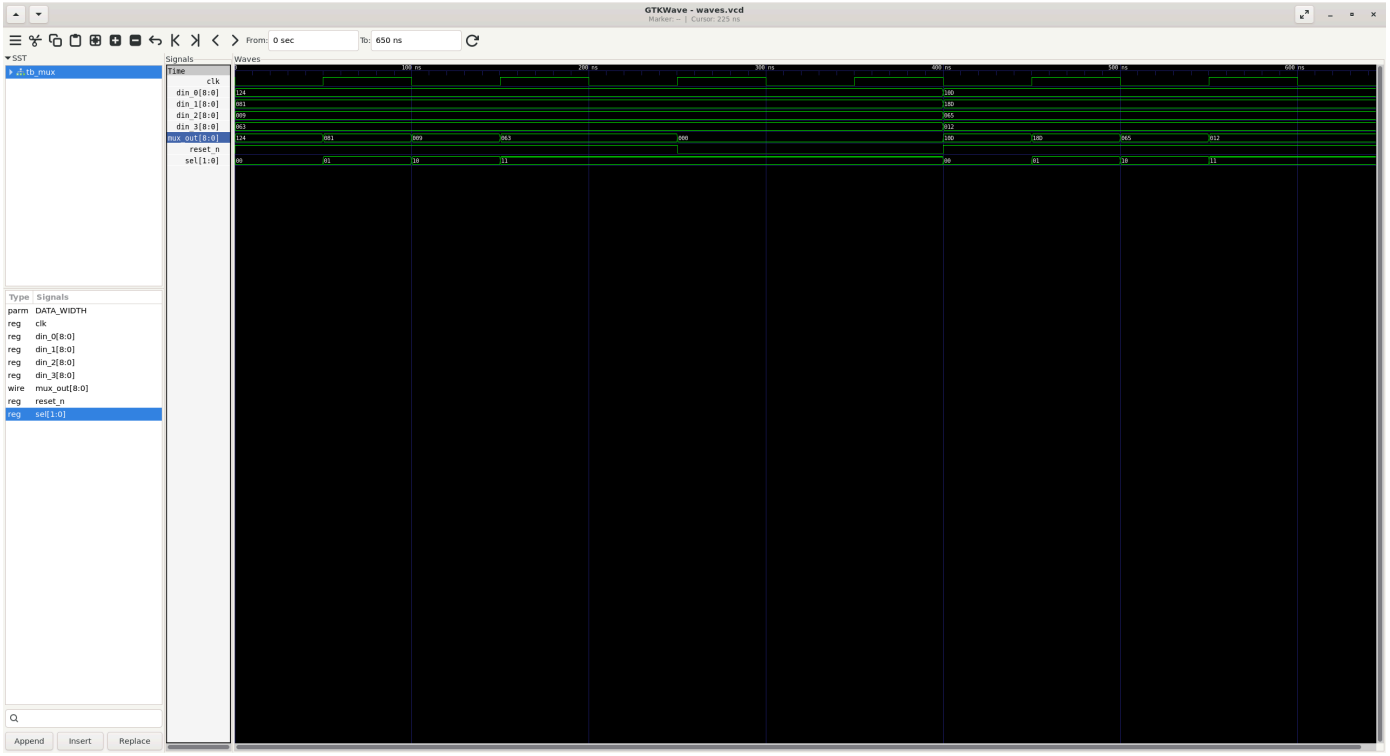
Notes

- All of these screenshots and all my code is available on my public GitHub repository here: https://github.com/adrienabbey/ceg-7360-verilog-assignment-1
- Additional documentaiton and comments are also available here: https://github.com/adrienabbey/ceg-7360-verilog-assignment-1/blob/main/docs/project.md

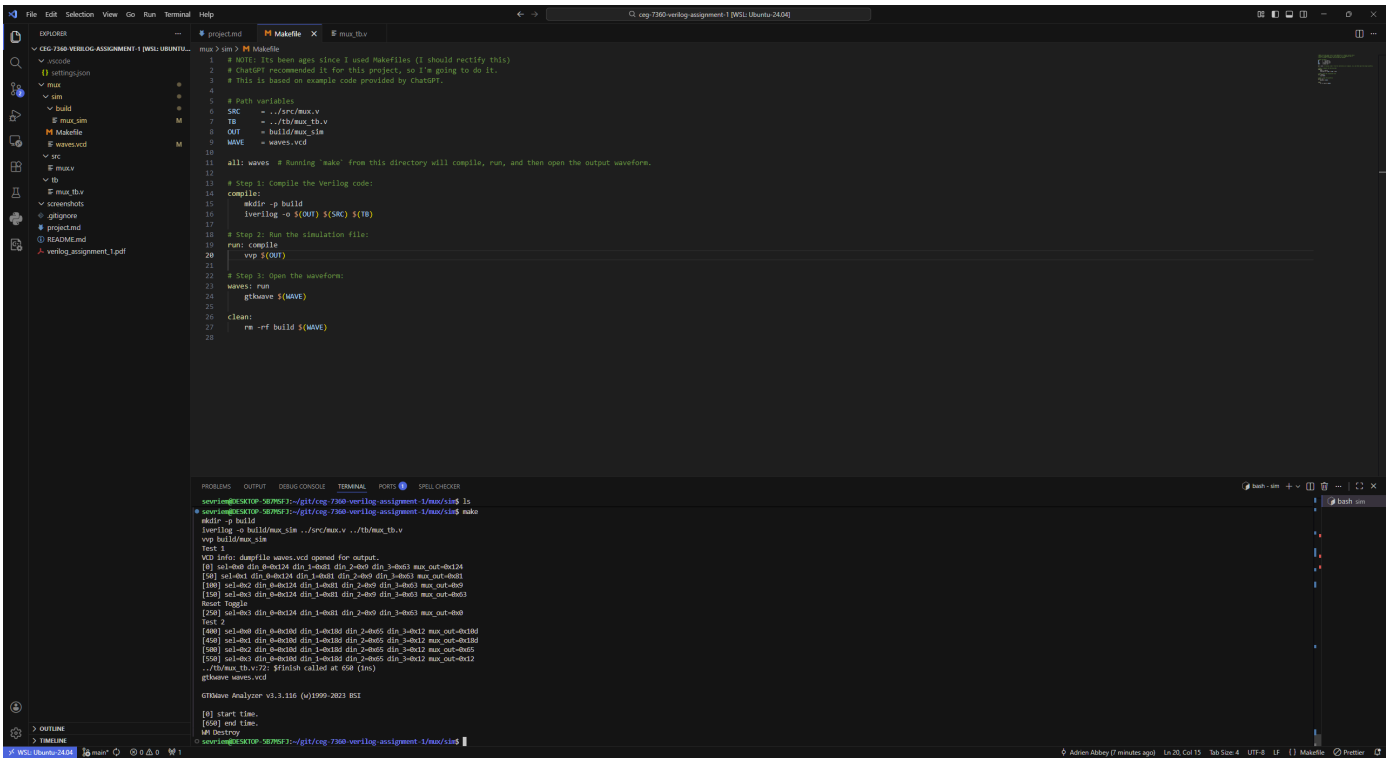
MUX Results

Icarus Verilog

Waveform

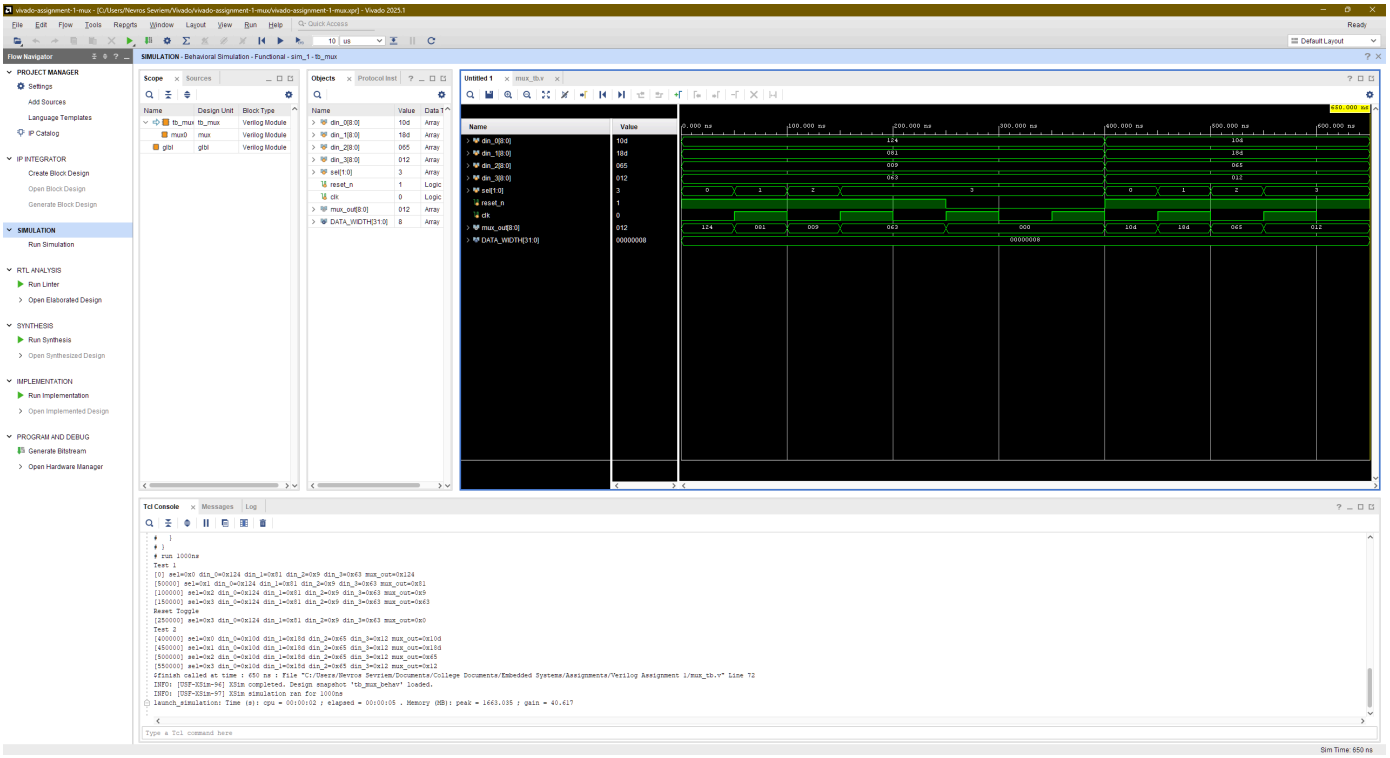


Terminal



Vivado

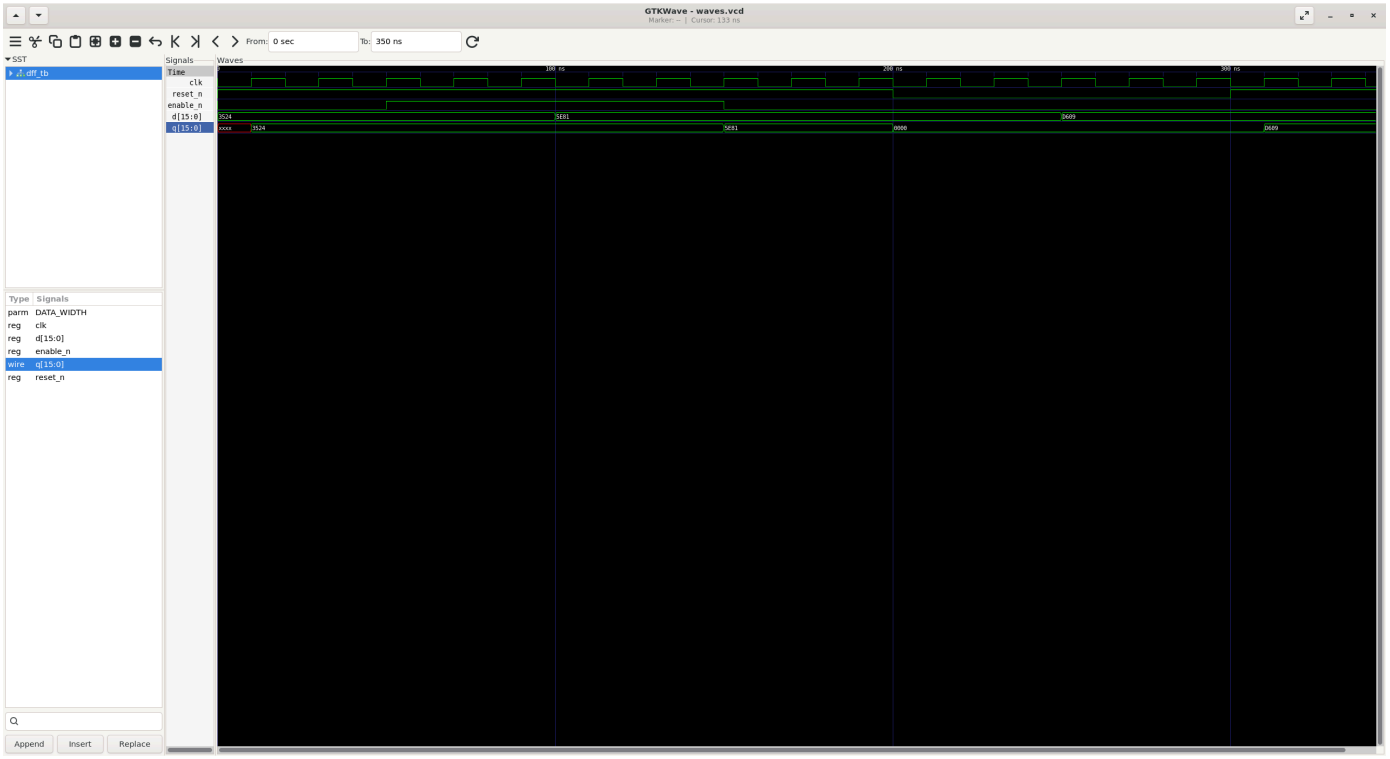
Waveform + Console



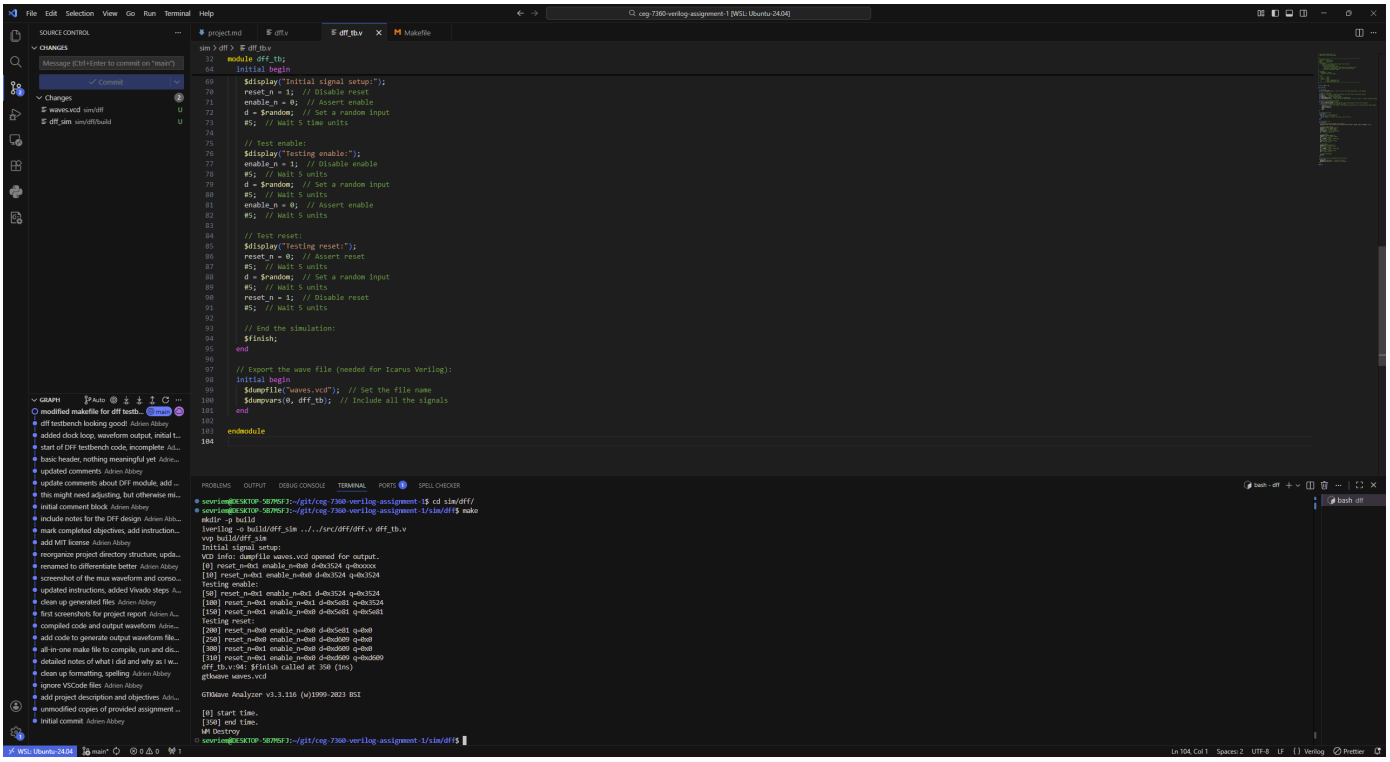
DFF Results

Icarus Verilog

Waveform

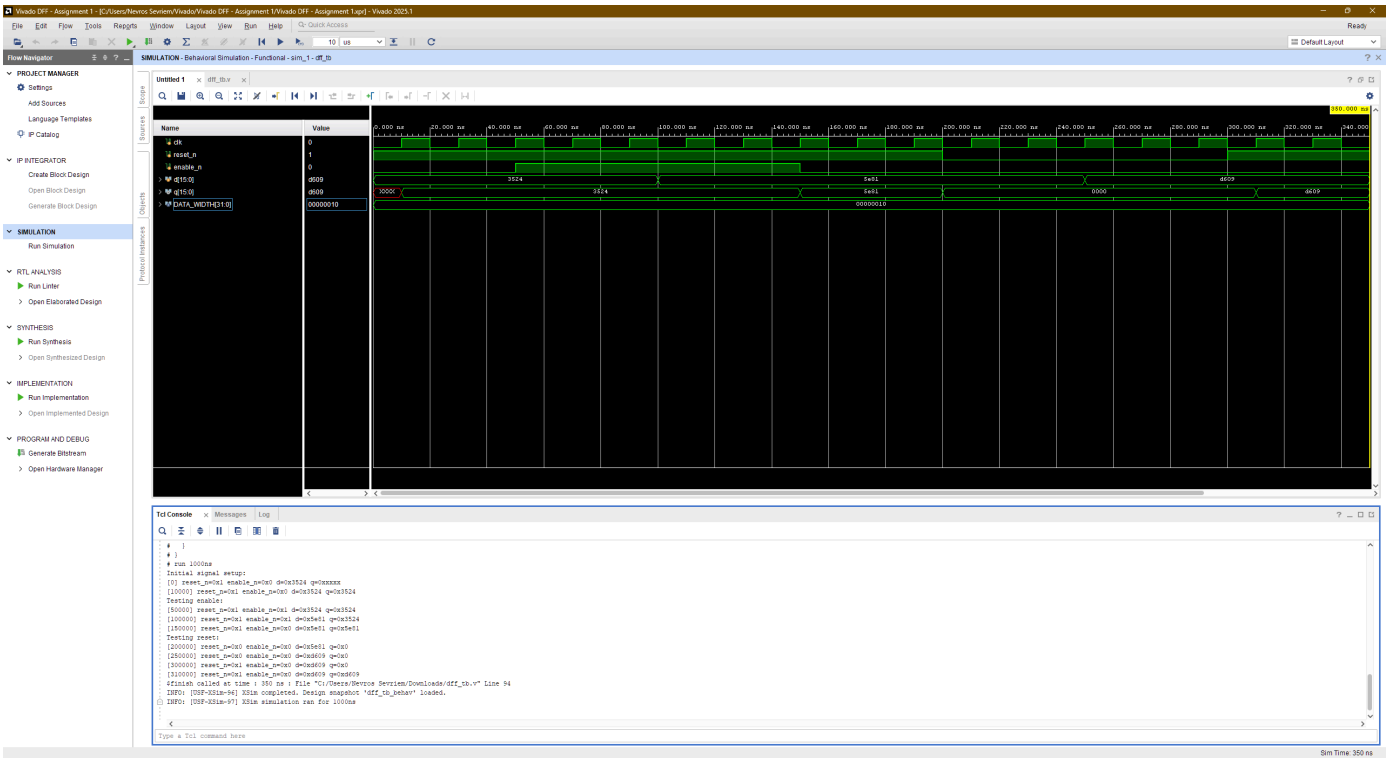


Terminal



Vivado

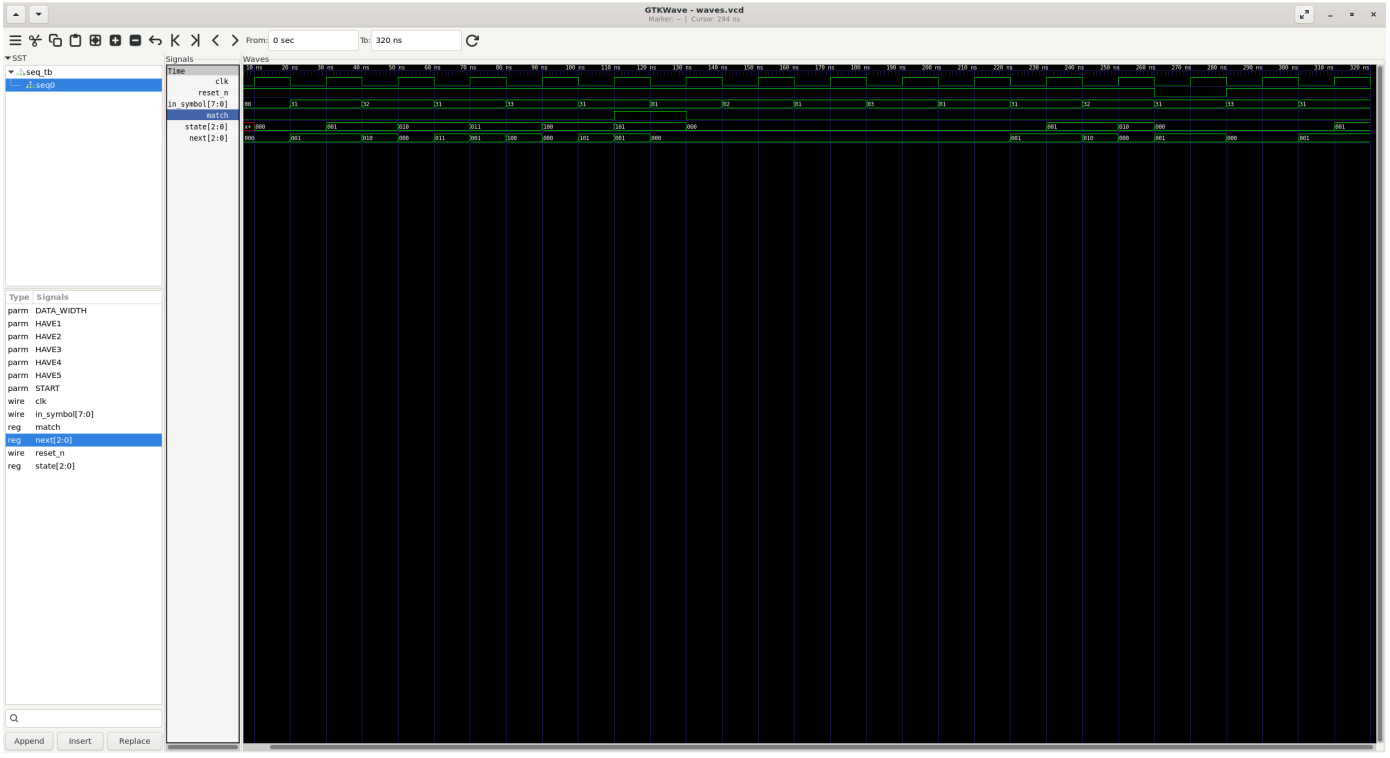
Waveform + Console



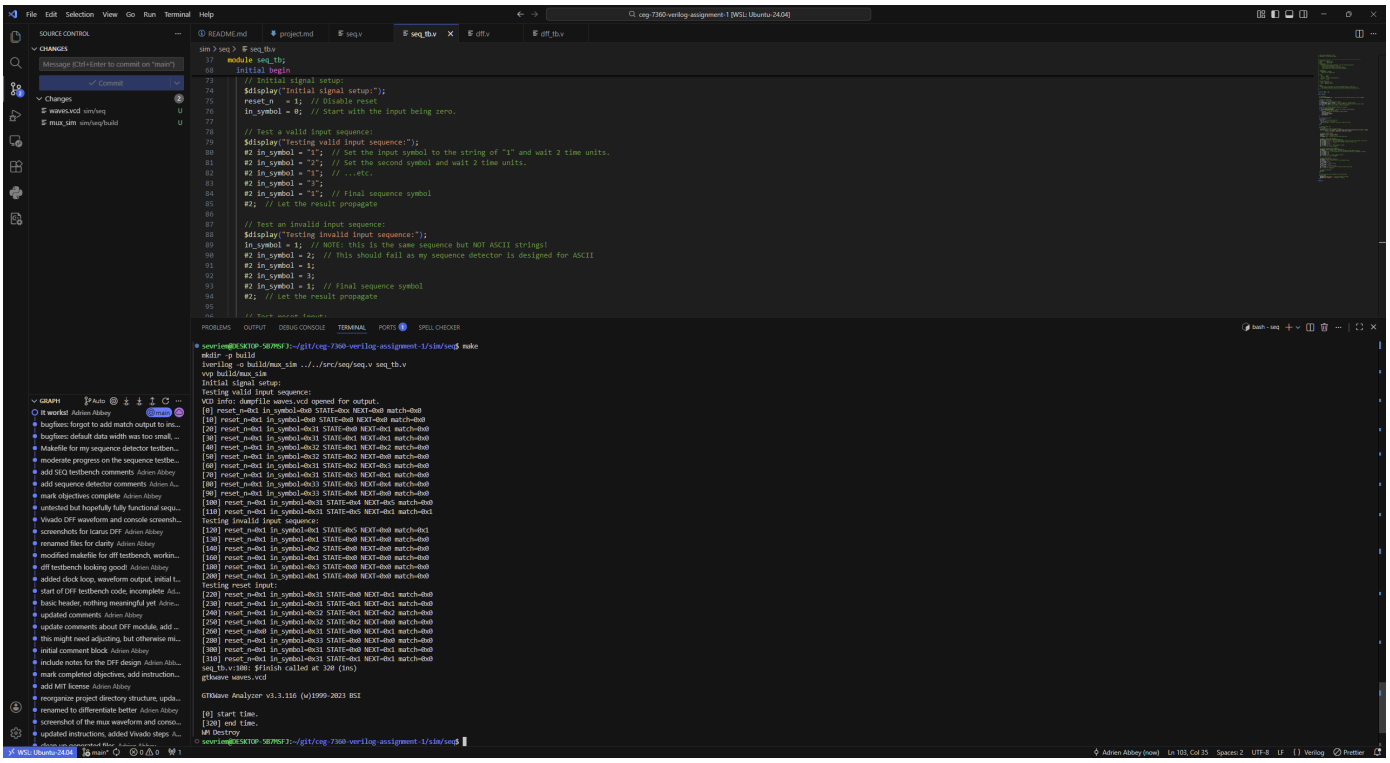
SEQ Results

Icarus Verilog

Waveform

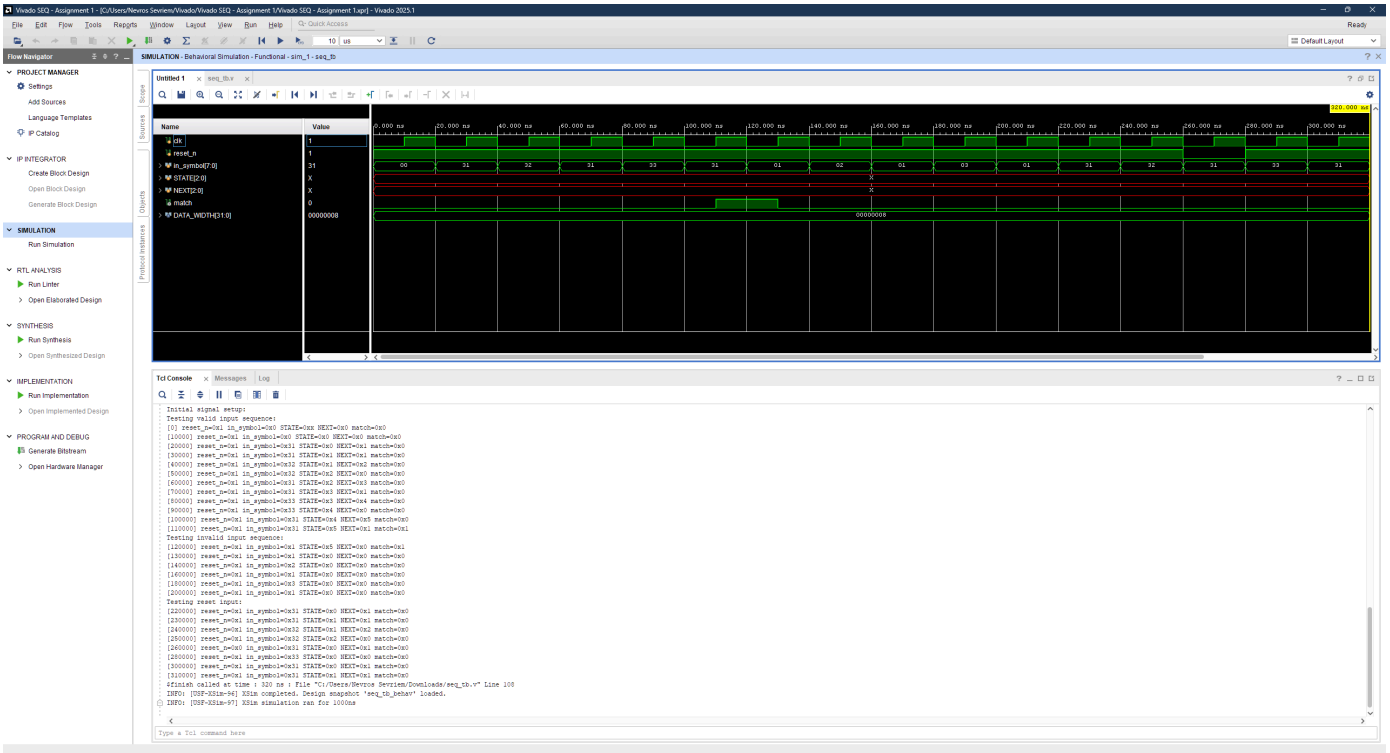


Terminal



Vivado

Waveform + Console



NOTE: the `state` and `next` values are not displaying correctly in the Vivado waveform, but they show up in the console just fine.