

EE613: HIGH FREQUENCY ANALOG CIRCUIT DESIGN

DESIGN PROJECT #1

Design of 2-stage Miller Compensated Opamp
(nMOS as input pair)

Load : $R_L = 5\text{k}\Omega$ and $C_L = 20\text{pF}$

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Goal: Designing a two-stage Miller compensated opamp that takes in a differential input and provides a single-ended output. This opamp will be used eventually in a unity feedback loop driving a load $R_L = 5k\Omega$, and $C_L = 20$ pF.

- a) When a step input is applied to the closed-loop system, the output must settle to the desired value with less than 0.1% error.
- b) The closed-loop frequency response must not exhibit any peaking.
- c) The closed-loop 3-dB bandwidth must not be smaller than 20MHz.

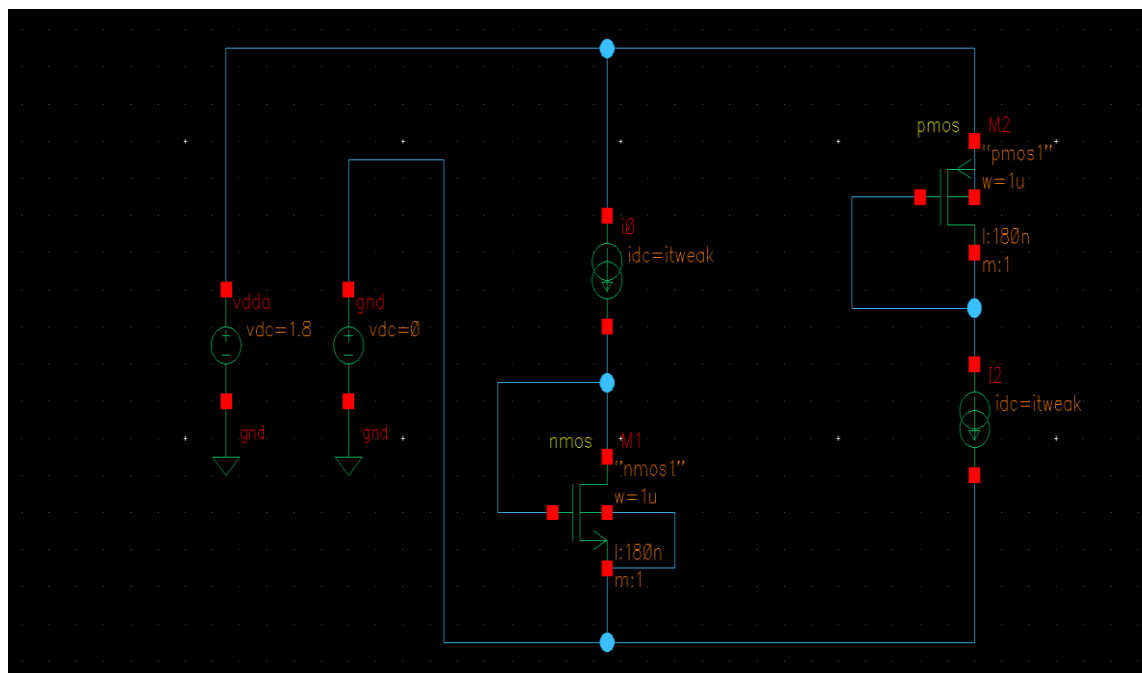
Components provided:

- a) Two ideal voltage sources: one with the value $V_{dd} = 1.8V$ and another with the value $V_{cm} = V_{dd}/2 (=0.9V)$
- b) An ideal ground.
- c) A reference current source of $1\mu A$ for biasing.
- d) An ideal resistor and a capacitor for load, $R_L = 5k\Omega$, and $C_L = 20$ pF.
- e) One ideal resistor and a capacitor for compensation, $R_L = 5k\Omega$, and $C_L = 20$ pF.
- f) 180nm technology nMOS and pMOS.

General Information about MosFETs used :

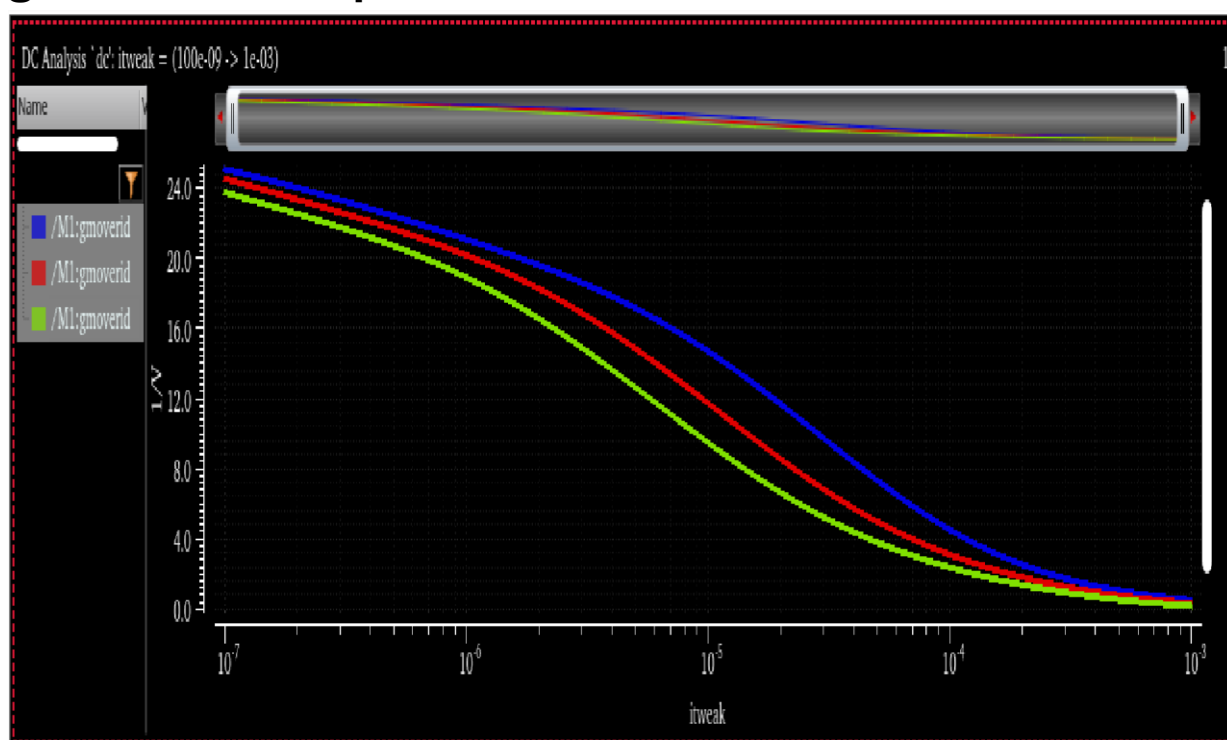
- 1. For circuit design, have used the 180nm technology MOSFETs.
- 2. Design is done using nMOS input stage and the second stage is a pMOS common source amplifier.
- 3. For all nMOS, the bulk (body) terminal is shorted with ideal ground. Similarly, for all pMOS, the bulk (body) terminal is shorted with corresponding source terminal.
- 4. $L_{min} = 180$ nm and $W_{min} = 400$ nm.

LOOK-UP TABLE Circuit :

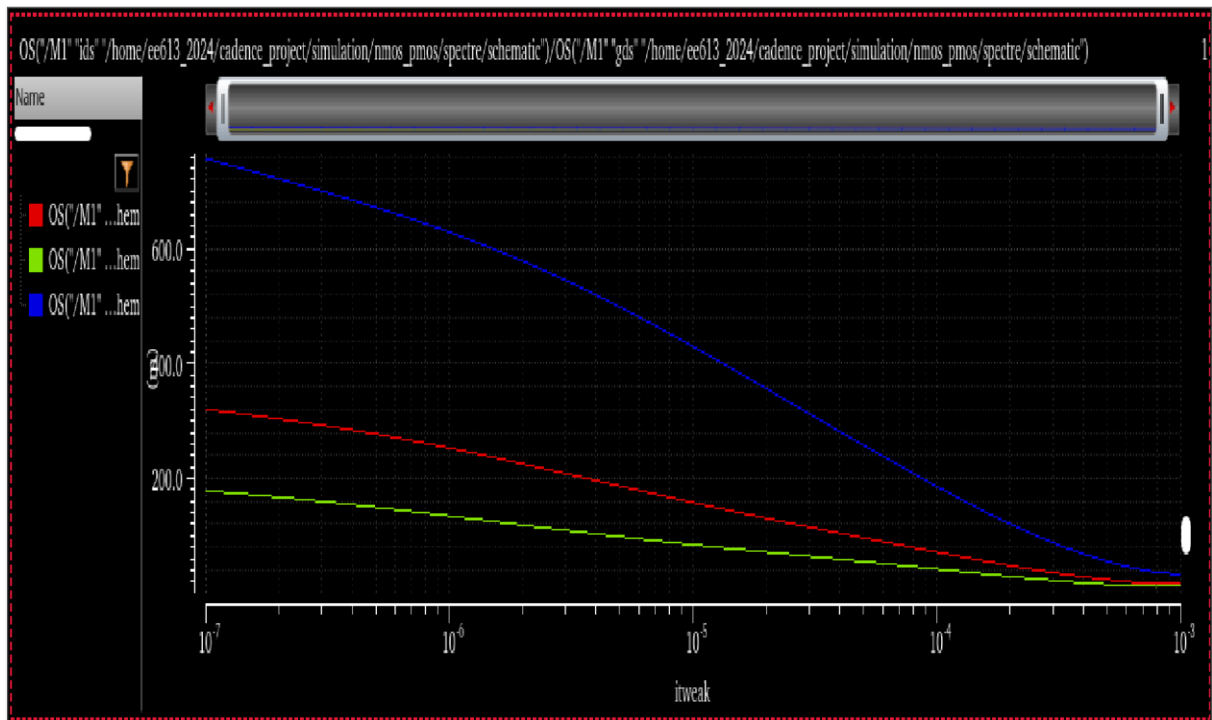


Here we have characterised for $L = L_{min}$, $2 * L_{min}$ and $3 * L_{min}$. We have kept $W = 1\mu m$ and tweaked the drain-to-source current. As we can see, both pMOS and nMOS are in saturation region.

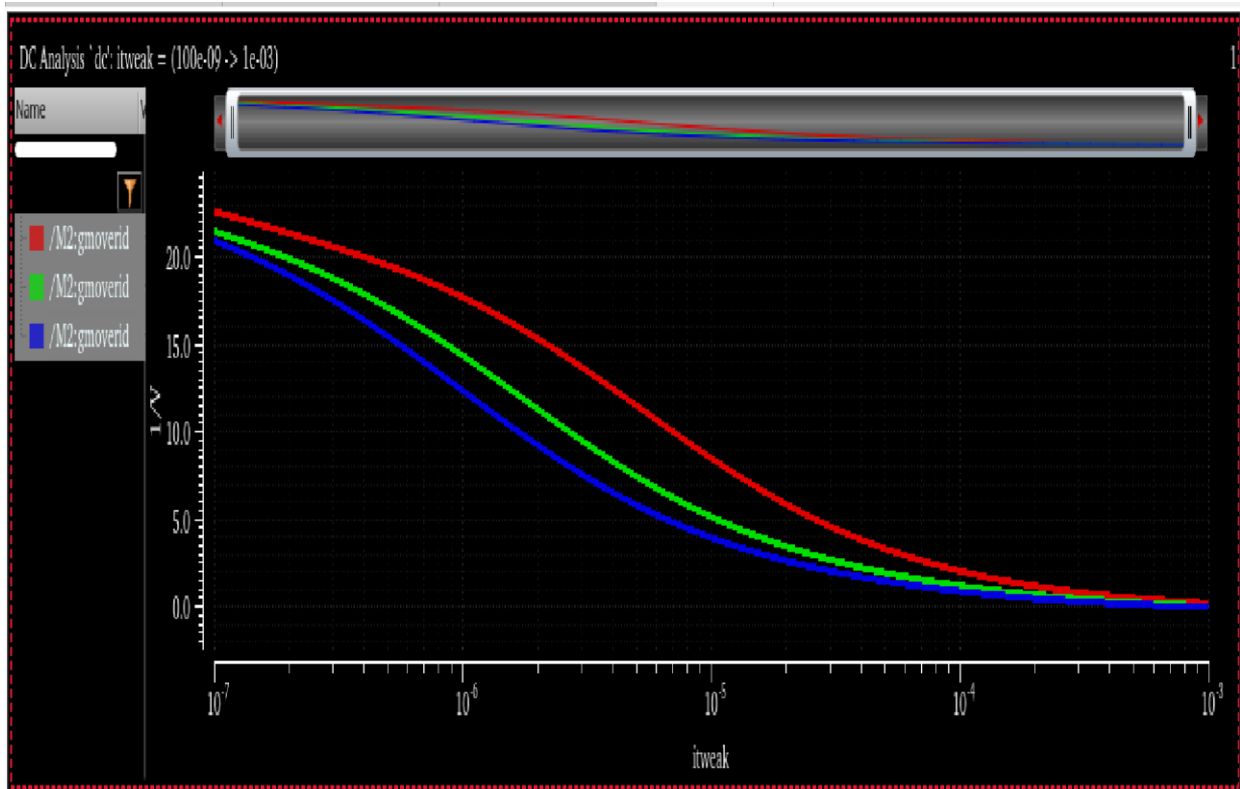
gm/Id versus Id plot for nMOS :



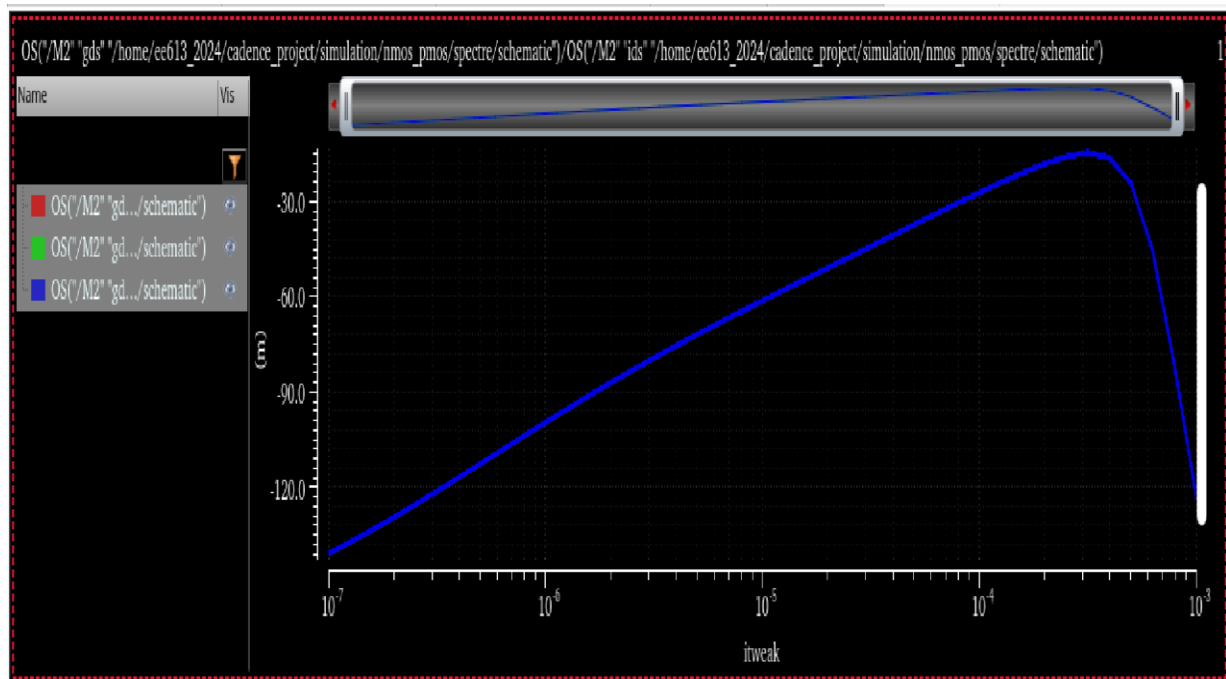
gds/Id versus Id plot for nMOS :



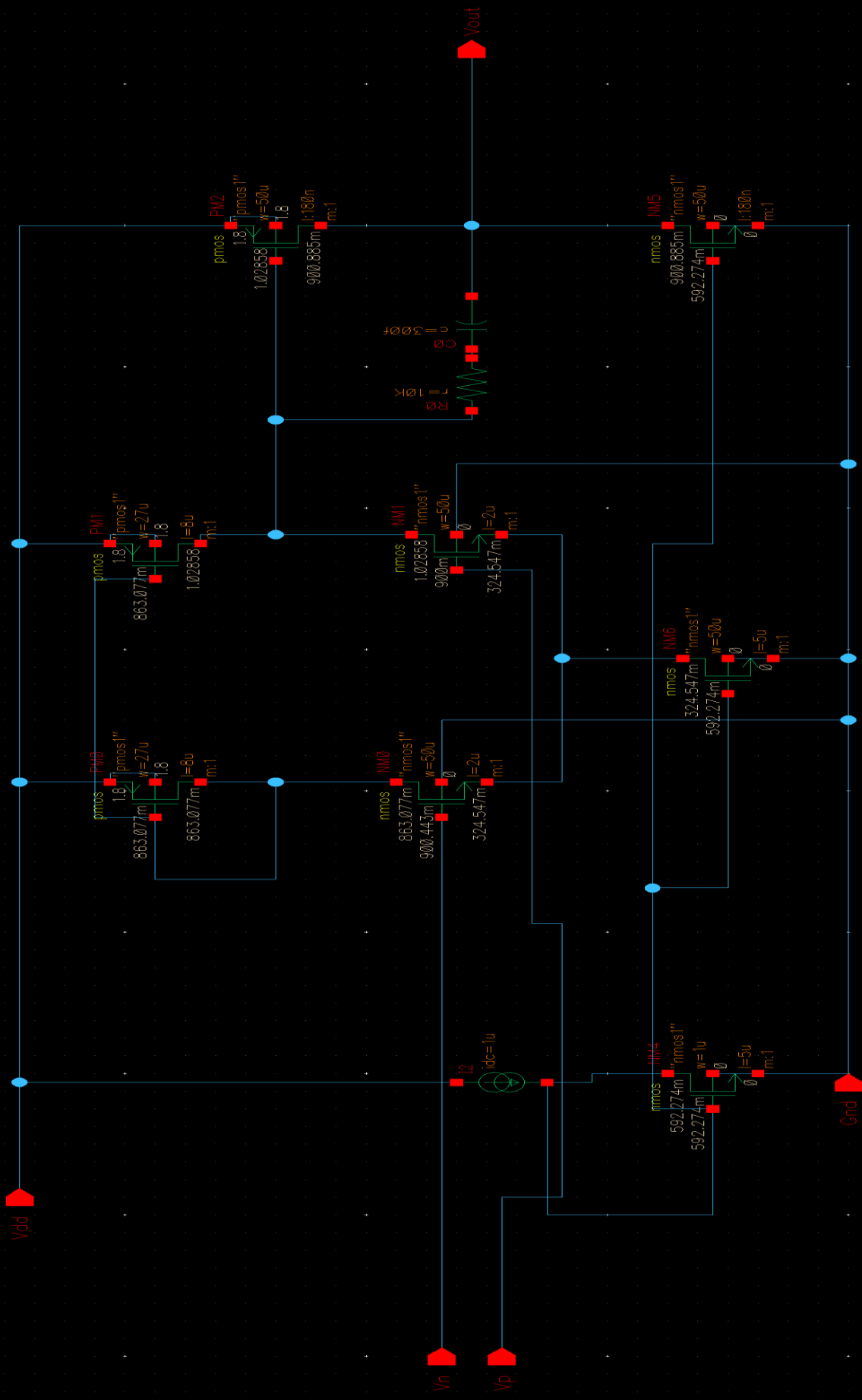
gm/Id versus Id plot for pMOS:



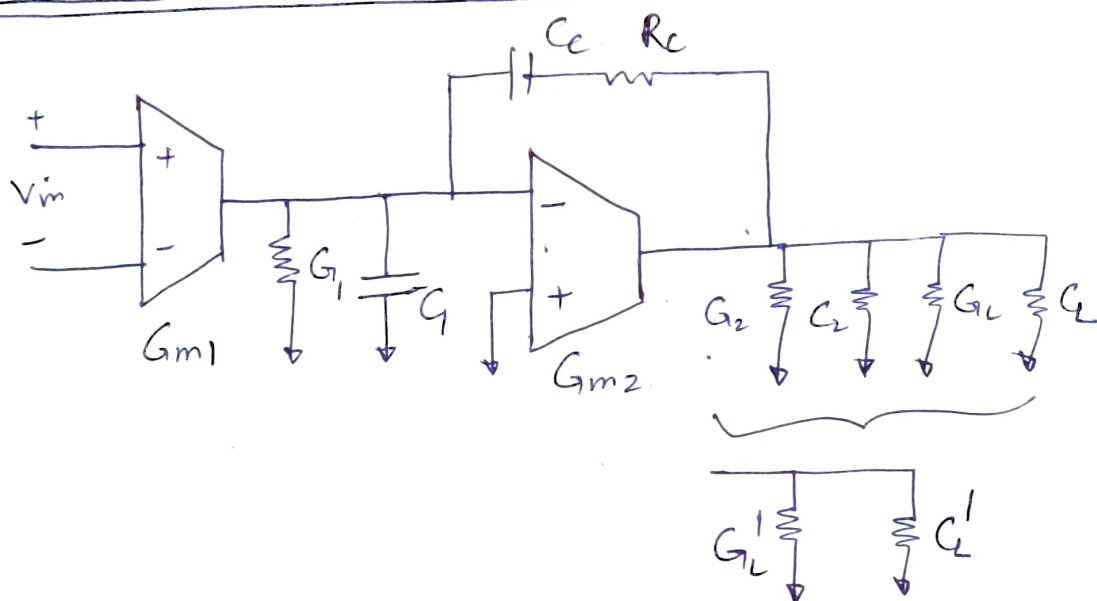
gds/Id versus Id plot for pMOS:



- We have used these plots to get rough estimates of starting values of sizing. Henceforth, depending on obtained results and theoretical calculations, further tweaking of sizing has been done.
- For example, if certain initial value of W gives a certain gain for first stage, increasing W might possibly increase the gain. Hence, the needful is done based on obtained results in successive iterations.
- Now we look at the transistor level schematic of the OPAMP designed. This is a 2-stage Miller compensated OPAMP which meets the required specifications as stated above.
- In the circuit given below, we can see the transistor level implementation along with the DC bias voltages. As we can see, all the transistors are happily in saturation, I mean that's what we wanted, right?!
- Here, we chose the value of (W/L) for bias nMOS to be $1/5$, so that it generates enough voltage at bias current = $1 \mu\text{A}$ and remains in saturation. In this case, it is $V_{GS} = 592.274 \text{ mV}$.



DESIGN METHODOLOGY



This is a miller compensated OTA with zero cancellation resistor.

$$A_0 = \frac{G_{m1}}{G_1} \times \frac{G_{m2}}{G_L'}$$

$$p_1 \approx \frac{G_1}{C_1 + C_c \frac{G_{m2}}{G_L'}}$$

$$p_2 \approx \frac{G_L' + \frac{G_{m2} C_c}{C_1 + C_c}}{C_L' + \frac{C_1 C_c}{C_1 + C_c}}$$

$$p_3 \approx \frac{1}{R_c C_1}$$

$$Z = \frac{1}{C_L \left(\frac{1}{G_{m2}} - R_c \right)}$$

→ For this to be LHZ

we need $R_c > \frac{1}{G_{m2}}$

$$\omega_u \approx A_0 p_1 \approx \frac{G_{m1}}{C_c}$$

$$\Phi_M \approx 90^\circ - \tan^{-1} \left(\frac{\omega_u}{p_2} \right) - \tan^{-1} \left(\frac{\omega_u}{p_3} \right) - \tan^{-1} \left(\frac{\omega_u}{Z} \right)$$

Now here,

$$G_m = g_{m1,2}$$

$$G_{m2} = g_{m5}$$

$$G_1 = gds_2 + gds_4.$$

$$G_2 = gds5 + gds6$$

$$C_1 \approx C_{g85}$$

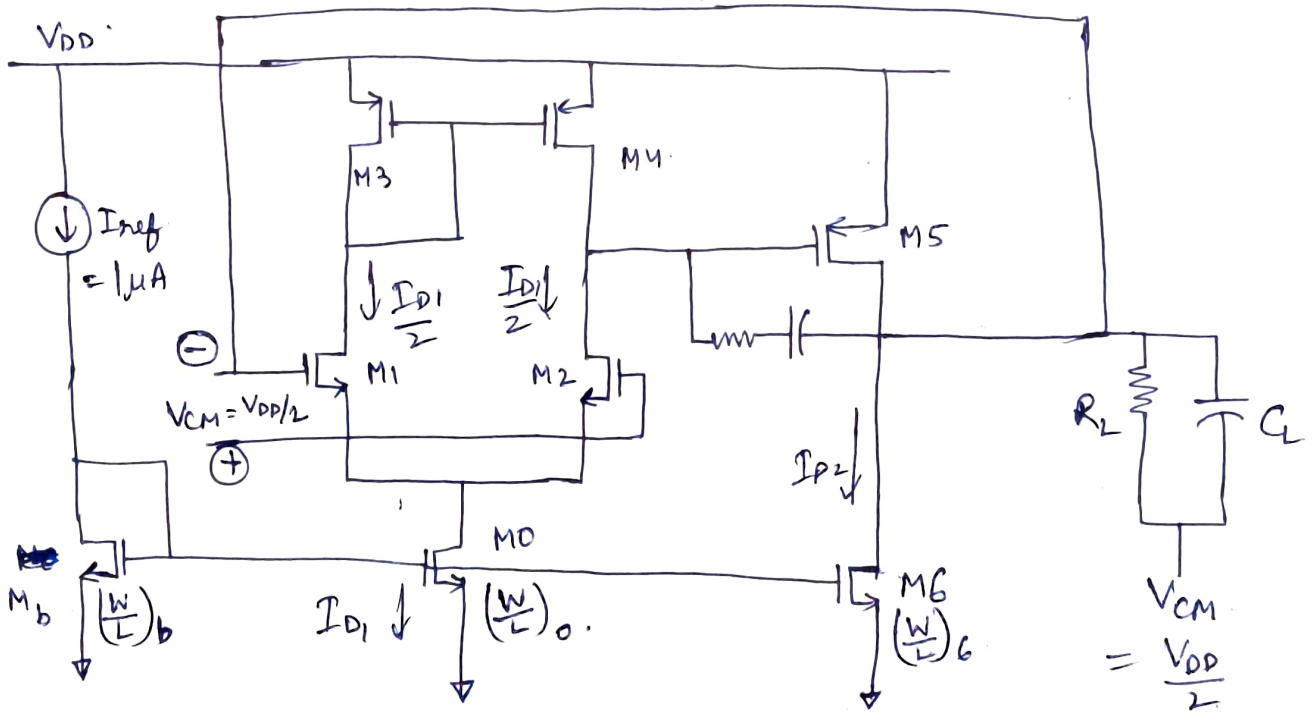
$$C_2 = C_{db5} + C_{db6}$$

$$C_L' = C_L + C_{db5} + C_{db6} \approx C_L = 20 \text{ pF}$$

$$G_L' = G_L + gds_5 + gds_6 \approx G_L = 200 \mu S$$

We want to use this OPAMP in negative f/b.

Circuit looks like this :-



$$\left(\frac{I}{N}\right)_{3,4,5} = \text{same for DC bias.}$$

According to ~~0.1~~ 0.1% error in steady state,

$$1 - \frac{A}{1+A} \leq \frac{0.1}{100}$$

$$\Rightarrow A > 999$$

$$\Rightarrow \text{DC open loop gain} \geq 60 \text{ dB}$$

$$\Rightarrow \phi_M > 60^\circ \text{ (for no peaking).}$$

$$\Rightarrow \omega_{3\text{dB}} > 20 \text{ MHz}$$

$$\text{(Theoretically } \omega_{3\text{dB}} \approx \omega_u \Rightarrow \omega_u > 20 \text{ MHz)}$$

Now, if we assume $C_c, C_L \gg C_1$

$$\Rightarrow p_1 \approx \frac{G_{m1}}{C_c \frac{G_{m2}}{G_L}}, \quad p_2 \approx \frac{G_{m2}}{C_L}$$

$$p_3 \approx \frac{1}{R_c C_1}, \quad z = \frac{1}{C_L \left(\frac{1}{G_{m2}} - R_c \right)}$$

Also, for first order behaviour near ω_u ,
(# poles - # zeros) before $\omega_u = 1$.

$$p_1 \ll 130 \text{ M rad/s.}$$

$$\Rightarrow \frac{g_{ds2} + g_{ds4}}{C_c \frac{g_{m5}}{200 \mu\text{s}}} \ll 20 \times 10^6 \text{ rad/s.}$$

$$p_2 > 130 \text{ M rad/s.}$$

$$\Rightarrow \boxed{G_{m2} > 400 \mu\text{S}}$$

Also

$$\phi_H > 60^\circ = 90^\circ - \tan^{-1}\left(\frac{C_{uH}}{p_2}\right)$$

Assuming, z and p_3 don't contribute much.
around $\omega = \omega_H$.

$$p_2 \approx 2\omega_H \approx 40 \text{ MHz.}$$

$$\boxed{G_{m2} > 800 \mu S}$$

$$\Rightarrow \boxed{R_C > 1250 \Omega}$$

Transistor level design

$$G_{m2} = g_{m5} > 800 \mu S = \frac{2I_{D2}}{V_{OV}}$$

$$I_{D2} \approx 180 \mu A \quad \text{for } V_{OV} \approx 0.2 \times 375$$

$$\text{But } I_{out} \approx \frac{0.9V}{5k} \approx 45 \mu A$$

$$\Rightarrow I_{bias} \text{ for 2nd stage} \approx 100 \mu A$$

Also, gain of second stage > gain of first stage.

$$\Rightarrow \frac{G_{m2}}{G_L} > \frac{G_{m1}}{G_1}$$

$$\left(\frac{g_{m5}}{I_5}\right) = 8 \Rightarrow \text{We choose } L = 0.18 \mu m$$

$$W = 50 \mu m.$$

$$\boxed{\left(\frac{W}{L}\right) \approx 270}$$

$$A_0 = 1000 = \frac{g_{m1}}{g_{ds2} + g_{ds4}} \times \frac{800 \mu}{200 \mu}$$

On generating look-up-table, we observe,
on varying I_{D1}/W , g_{ds}/I_{D1} does not vary much
Hence, we tweak g_{m1} to get appropriate
gain.

$$g_{m1} \propto \sqrt{\left(\frac{I}{W}\right)} \Rightarrow$$

$$\text{And } g_{ds} \propto W$$

\Rightarrow Instead of reducing W , we choose
to increase I_{D1} .

For given specs, $I_{D1} \approx 50 \mu A$ sets
DC loop gain appropriately.

$$\boxed{g_{m1} \approx 430 \mu S} = \frac{2 I_{D1/2}}{V_{OV}}$$

$$\text{Assume } V_{OV} \approx 0.12 V$$

$$\Rightarrow I_{D1/2} \approx 25 \mu A \Rightarrow I_{D1} \approx 50 \mu A$$

$$\text{For } V_{offset} = 0 \Rightarrow \left(\frac{I}{W}\right)_{3,4,5} = \text{same}$$

$$\Rightarrow \left(\frac{I_{D1/2}}{W}\right)_{3,4} = \left(\frac{I_{D2}}{W}\right)_5$$

for M_0 , to carry $1 \mu A$ and maintain
 $V_{gs} \approx 600 mV$ ($V_{th} \approx 490 mV$) ($V_{OV} \approx 0.1 V$)

$$\left. \begin{array}{l} W_b = 1 \mu\text{m} \\ L_b = 5 \mu\text{m} \end{array} \right] \left(\frac{W}{L} \right)_b = \left(\frac{1}{5} \right)$$

On simulation, $I_{D2} \approx 99.6 \mu\text{A}$

$$I_{D2} \approx 1.08 \mu\text{A}$$

Now, after simulations certain values did not match due to various assumptions in pole locations, V_{ov} values etc.

Hence fine tuning in W and L values were required after observing behaviour through simulations.

Overall g_m and g_{ds} values were then noted and attached below.

Method of Fine tuning

$$g_m = \frac{2I_D}{V_{ov}} \quad I_D \propto \frac{W}{L} (V_{ov})^2$$

→ If I_D is constant and g_m should \uparrow
 $\Rightarrow V_{ov} \downarrow$

→ If $V_{ov} \downarrow$ and I_D is constant, $\left(\frac{W}{L} \right) \uparrow$

→ If L is kept unchanged $\Rightarrow g_m \propto W$
 and $W \uparrow$

→ Tuned W majorly to increase g_m .

while $g_{ds} \propto \frac{1}{L^2} \Rightarrow L \downarrow \Rightarrow g_{ds} \uparrow$ more significantly.

After phase margin and loop gain simulations, initial guess of $C_c = 800 \text{ fF}$.

This was later fine tuned to $C_c = 300 \text{ fF}$ (based on positive / negative effect on phase margin).

Similarly initial guess of $R_c = 1250 \text{ }\Omega$.

This introduced a third pole which significantly degraded phase margin. Hence, the need to introduce LHZ by setting

$R_c = 10 \text{ k}\Omega$ which ensured no peaking closed loop response ($\phi_M > 60^\circ$).

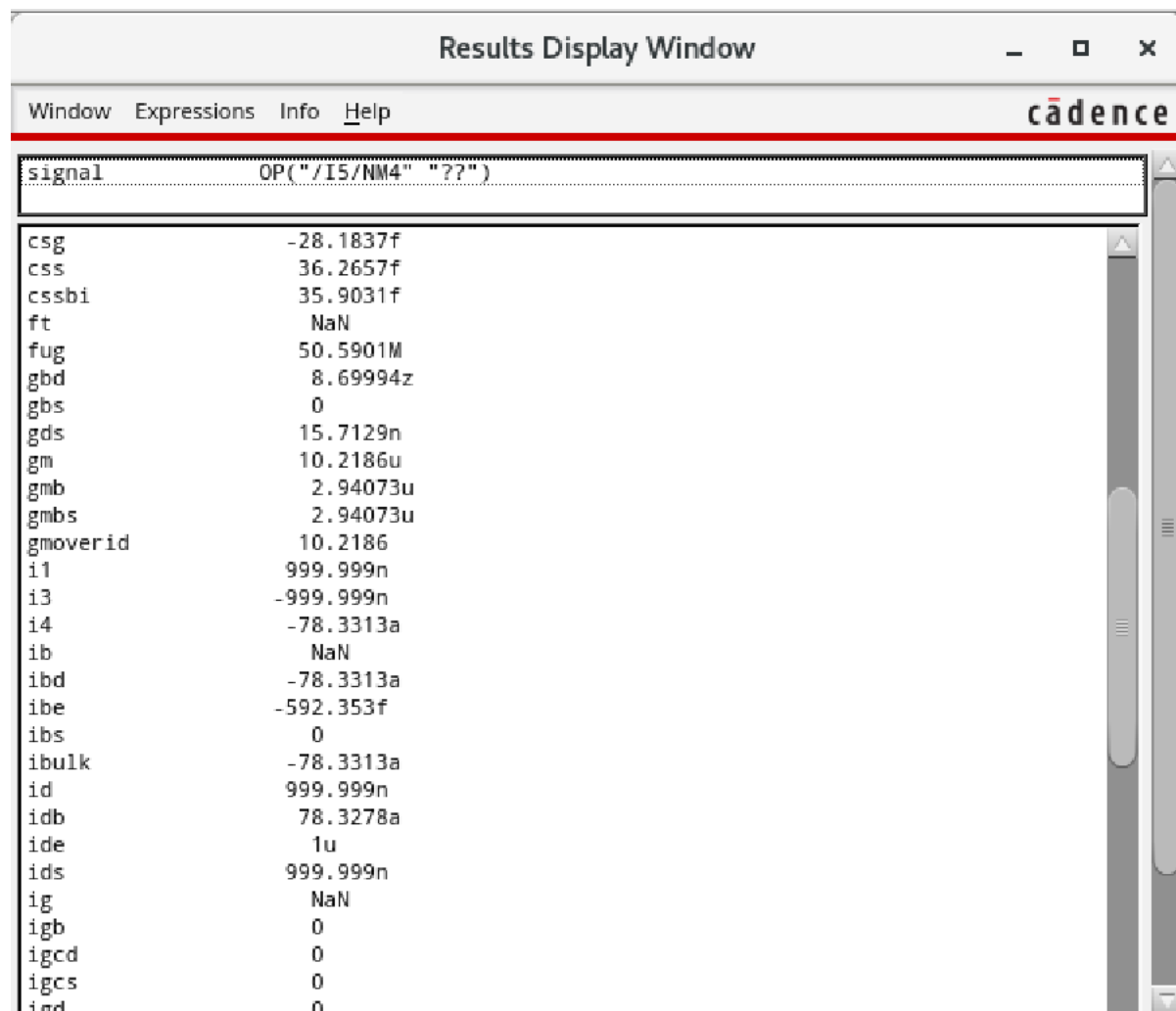
$$\boxed{C_c = 300 \text{ fF}} , \boxed{R_c = 10 \text{ k}\Omega} .$$

Block Level Design Summary :

Gm1	430 μ S	Gm2	6.6 mS
G1	1.2 μ S	G2	525 μ S
GL	200 μ S	CL	20 pF
Cc	300 fF	Rc	10 k Ω

Transistor Level Design Summary: (refer to naming in circuit drawn)

1. DC operating parameters of M_b :



The screenshot shows the 'Results Display Window' from Cadence. The window has a menu bar with 'Window', 'Expressions', 'Info', and 'Help'. The title bar says 'Results Display Window'. The main content area displays a table of parameters for the signal 'OP("/I5/NM4' '??")'. The parameters are listed in two columns: the parameter name and its value. The values are in scientific notation or standard units.

signal	OP("/I5/NM4' '??")
csg	-28.1837f
css	36.2657f
cssbi	35.9031f
ft	NaN
fug	50.5901M
gbd	8.69994z
gbs	0
gds	15.7129n
gm	10.2186u
gmb	2.94073u
gmbs	2.94073u
gmoverid	10.2186
i1	999.999n
i3	-999.999n
i4	-78.3313a
ib	NaN
ibd	-78.3313a
ibe	-592.353f
ibs	0
ibulk	-78.3313a
id	999.999n
idb	78.3278a
ide	1u
ids	999.999n
ig	NaN
igb	0
igcd	0
igcs	0
ied	0

2. DC operating parameters of M_0 :

Results Display Window	
Window Expressions Info Help caden	
signal	OP("/I5/NM6" "?")
ft	NaN
fug	54.1055M
gbd	410.842z
gbs	0
gds	3.17666u
gm	538.095u
gmb	156.986u
gmbs	156.986u
gmoverid	10.831
i1	49.681u
i3	-49.681u
i4	-2.60589f
ib	NaN
ibd	-2.60589f
ibe	-327.153f
ibs	0
ibulk	-2.60589f
id	49.681u
idb	2.60582f
ide	49.681u
ids	49.681u
ig	NaN
igb	0
igcd	0

3. DC operating parameters of $M_{1,2}$:

Results Display Window	
Window Expressions Info Help cadenc	
signal	OP("/I5/NM1" "?")
ft	NaN
fug	135.664M
gbd	82.492f
gbs	0
gds	921.291n
gm	430.566u
gmb	108.526u
gmbs	108.526u
gmoverid	17.3444
i1	24.8244u
i3	-24.8244u
i4	-7.71363f
ib	NaN
ibd	-5.10781f
ibe	-1.36084p
ibs	-2.60582f
ibulk	-7.71363f
id	24.8244u
idb	2.60582f
ide	24.8244u
ids	24.8244u
ie	NaN

4. DC operating parameters of $M_{3,4}$:

Results Display Window	
Window Expressions Info Help cadence	
signal	OP("/I5/PM1" "??")
csg	-1.24398p
css	1.63818p
cssbi	1.62928p
ft	NaN
fug	9.90043M
gbd	1.87453a
gbs	0
gds	244.321n
gm	89.4141u
gmb	30.1062u
gmbs	30.1062u
gmoverid	3.60186
i1	-24.8244u
i3	24.8244u
i4	69.3179f
ib	NaN
ibd	69.3179f
ibe	840.738f
ibs	-0
ibulk	69.3179f
id	-24.8244u
idb	69.3172f
ide	-24.8244u
ids	-24.8244u
ig	NaN
igb	0
igcd	0
igcs	0
ied	0

5. DC operating parameters of M_5 :

Results Display Window	
Window Expressions Info Help cadence	
signal	OP("/I5/PM2" "??")
gbs	0
gds	214.36u
gm	6.67415m
gmb	2.25484m
gmbs	2.25484m
gmoverid	6.16325
i1	-1.08289m
i3	1.08289m
i4	130.549f
ib	NaN
ibd	130.549f
ibe	1.02966p
ibs	-0
ibulk	130.549f
id	-1.08289m
idb	127.084f
ide	-1.08289m
ids	-1.08289m
ig	NaN
ieb	0

6. DC operating parameters of M_6 :

Results Display Window	
Window Expressions Info Help	cadence
signal	OP("/I5/NM5" "?")
csg	-58.5187f
css	70.1418f
cssbi	51.6492f
ft	NaN
fug	23.1712G
gbd	3.50713n
gbs	0
gds	310.114u
gm	12.8554m
gmb	3.73593m
gmbs	3.73593m
gmoverid	11.8781
i1	1.08227m
i3	-1.08227m
i4	-176.686p
ib	NaN
ibd	-176.686p
ibe	-177.586p
ibs	0
ibulk	-176.686p
id	1.08227m
idb	2.60582f
ide	1.08227m
ids	1.08227m
ig	NaN

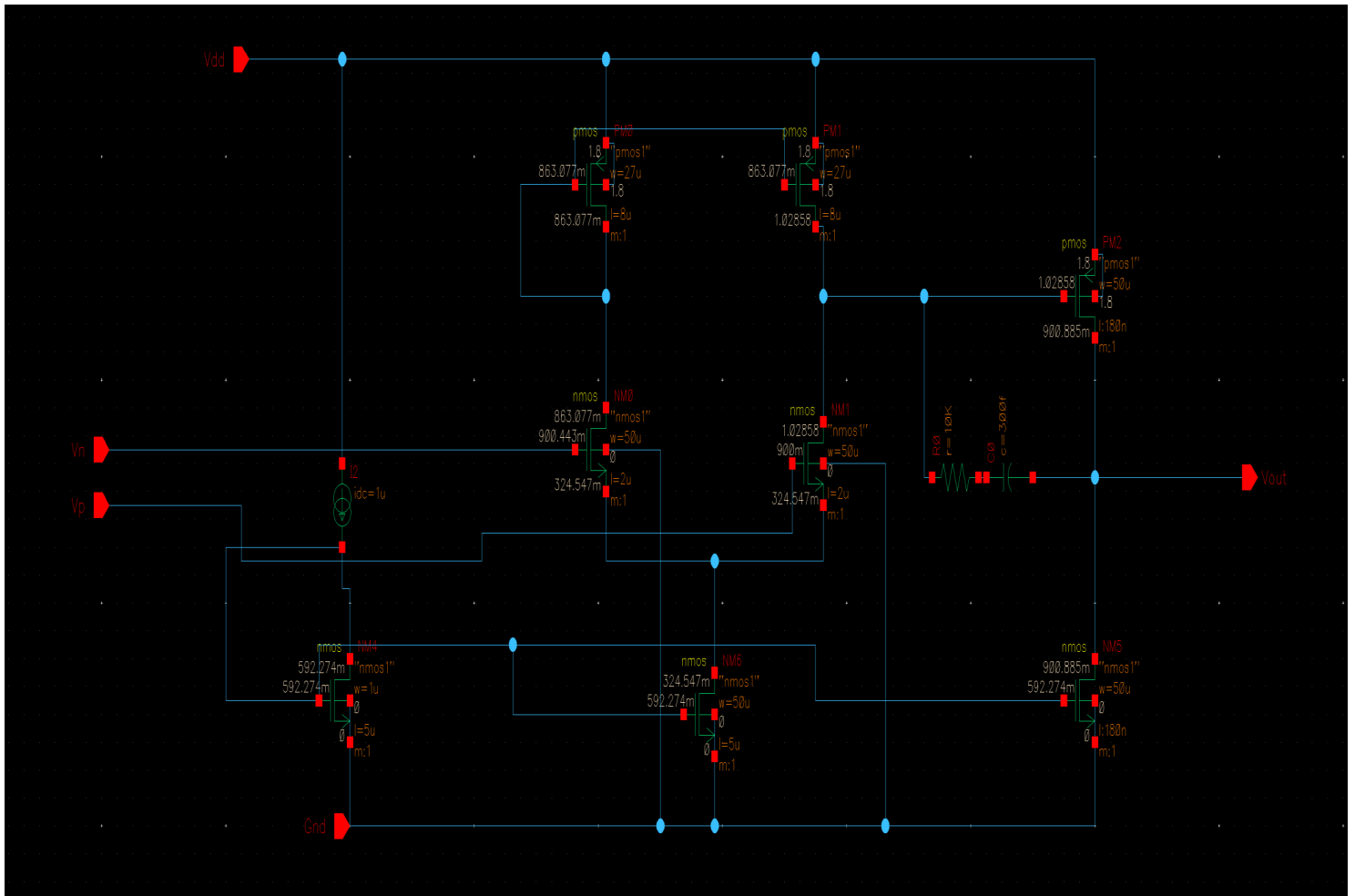
Name	W (m)	L (m)	W/L
M_b	1μ	5μ	0.2
M_0	50μ	5μ	10
M_1	50μ	2μ	25
M_2	50μ	2μ	25
M_3	27μ	8μ	3.375
M_4	27μ	8μ	3.375
M_5	50μ	0.18μ	277.77
M_6	50μ	0.18μ	277.77

I_{o1}	$50 * 10^{-6} \text{ A}$	I_{o2}	$1.08 * 10^{-3} \text{ A}$
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Note: The values of W/L were tuned after simulating the initial values of W and L, to get the required values of G_{m1} , G_{m2} , G_1 and G_2 . Method of tuning is explained in the Design methodology.

Results :

a. Result #1 :



Gm1	430.566 μ S	Gm2	6.674 mS
G1	1.165 μ S	G2	524.474 μ S
GL	200 μ S	CL	20 pF
Cc	300 fF	Rc	10 k Ω

$$V_{OUT} = 0.900443 V$$

The above circuit shows all DC bias voltages, indicating saturation operation for each transistor. gm, gds and ids values of each transistor is tabulated and mentioned under transistor level design summary.

Upon comparison, we find the values to be similar and tabulated above:

$$DC \text{ Loop Gain} = \frac{G_{m1} * G_{m2}}{G_1 * (G_L + G_2)} = 3404.68$$

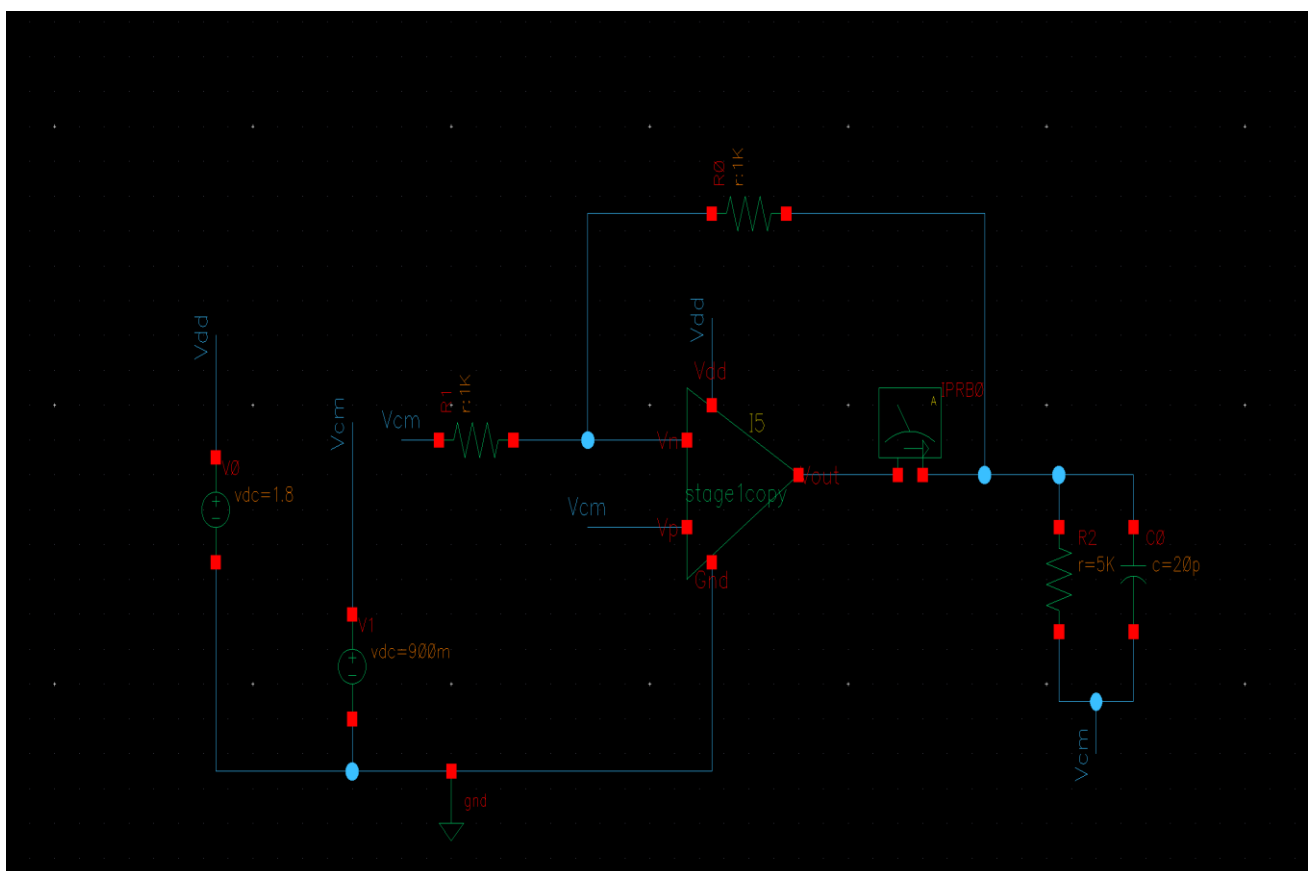
This implies a loop gain of 70.6415 dB. But we don't obtain such gain as various approximations such as $G_2 \ll G_L$, gain of stage 2 > gain of stage 1, etc. fail.

b. Result #2 :

Bode plot of Loop gain: **DC gain = 60.044 dB.**

Unity Gain frequency = 40.4671 MHz and Phase margin = 60.16°

Test-bench Circuit for simulating open-loop gain:



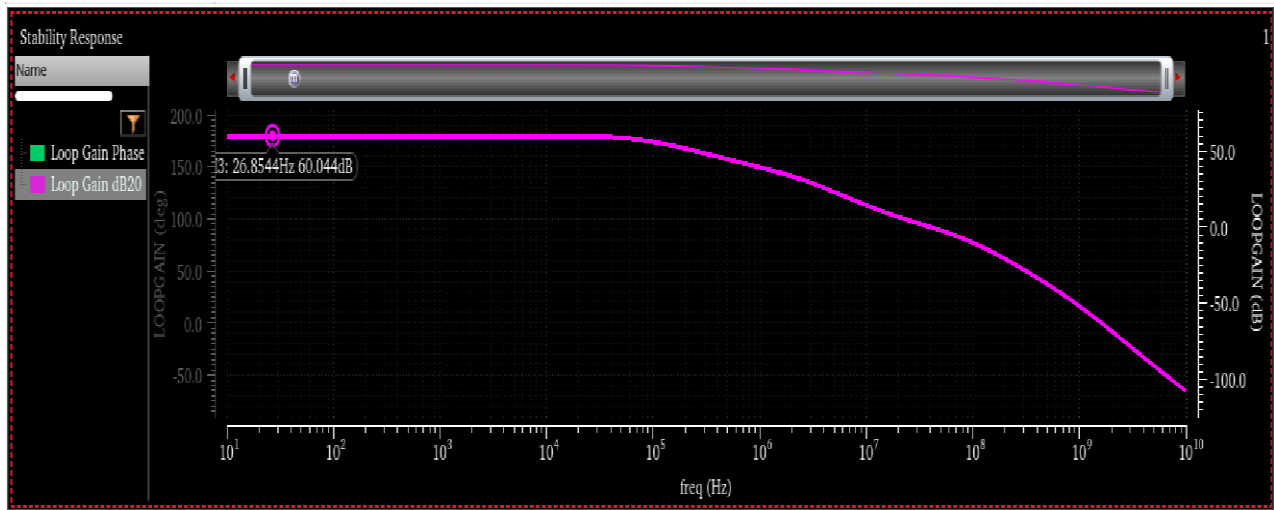


Figure (a) : Open loop gain = 60.044 dB

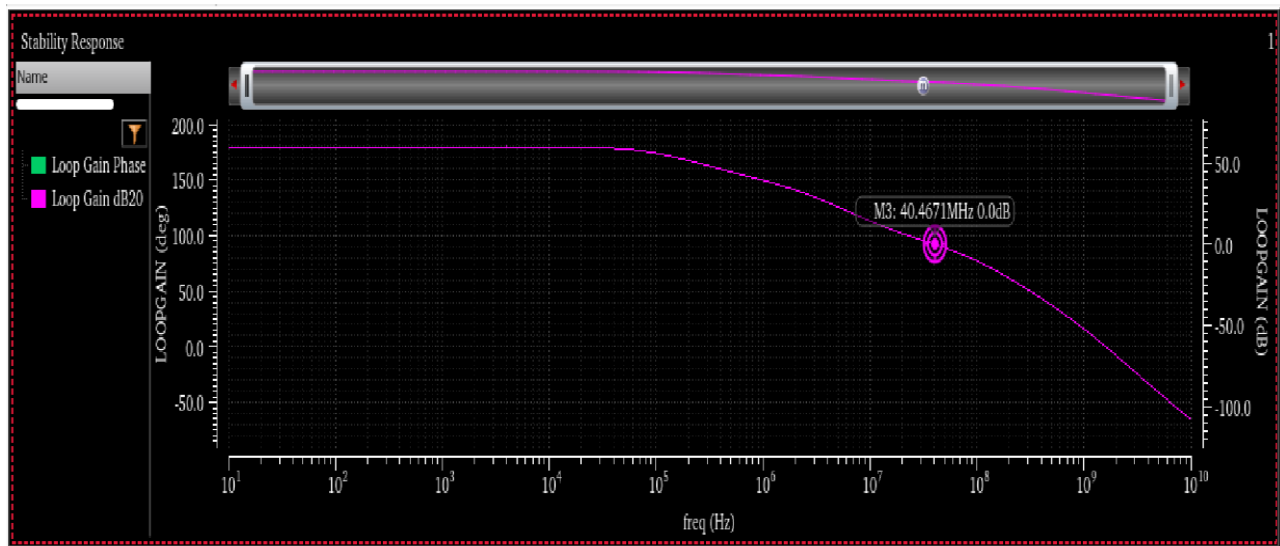


Figure (b) : Unity gain frequency = 40.4671 MHz

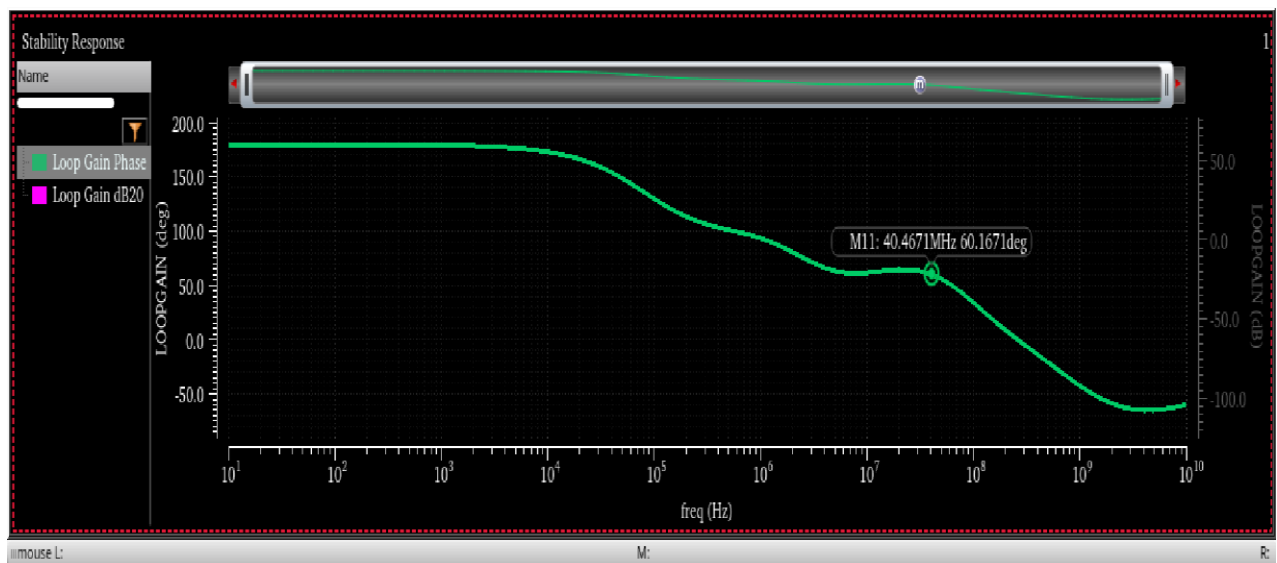


Figure (c) : Phase Margin = 60.1671°

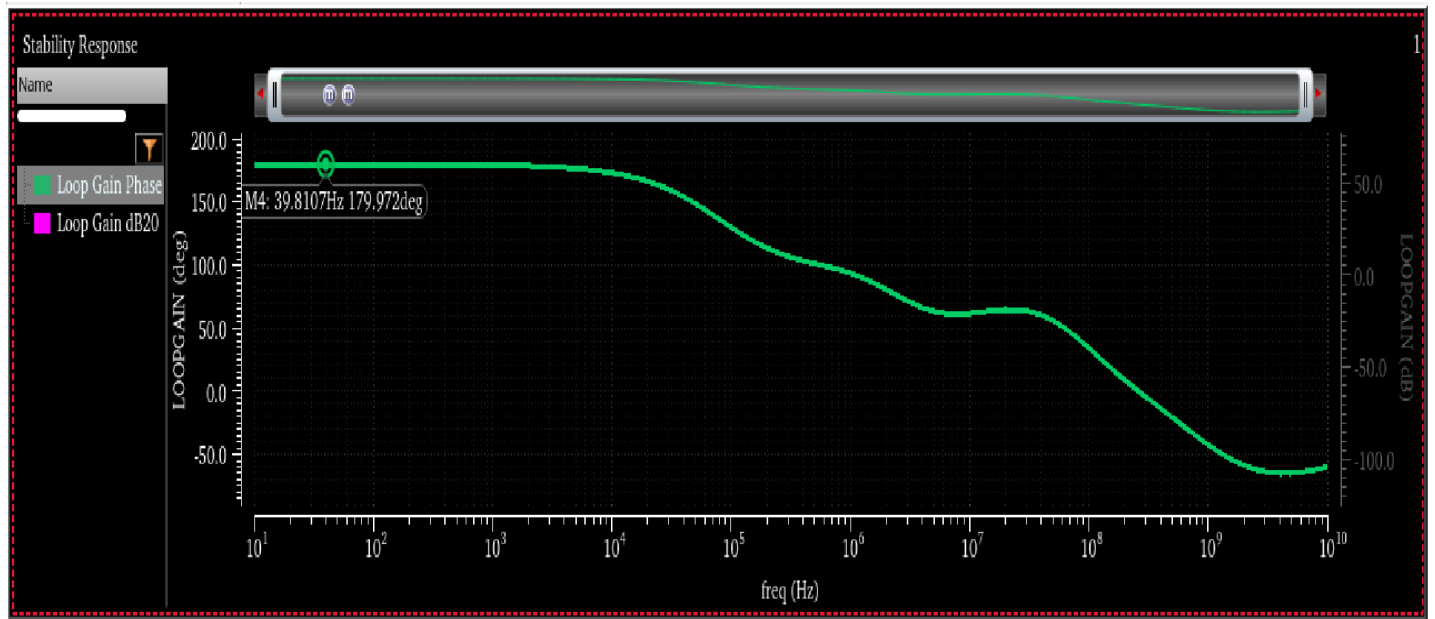


Figure (d) : Loop gain Phase plot

Direct Plot Form [X]

Plotting Mode: Replace [v]

Analysis

☒ stb

Function

☐ Loop Gain ☒ Stability Summary
☐ Phase Margin ☐ Gain Margin
☐ PM Frequency ☐ GM Frequency

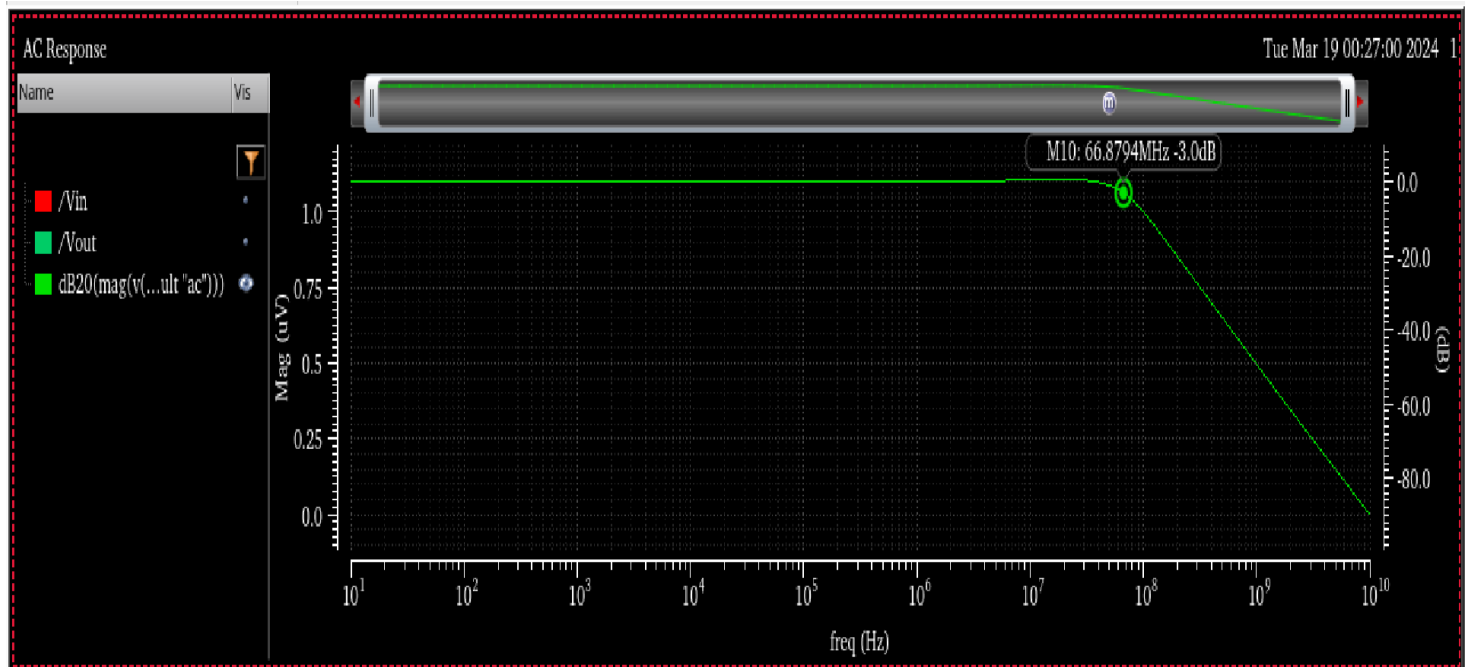
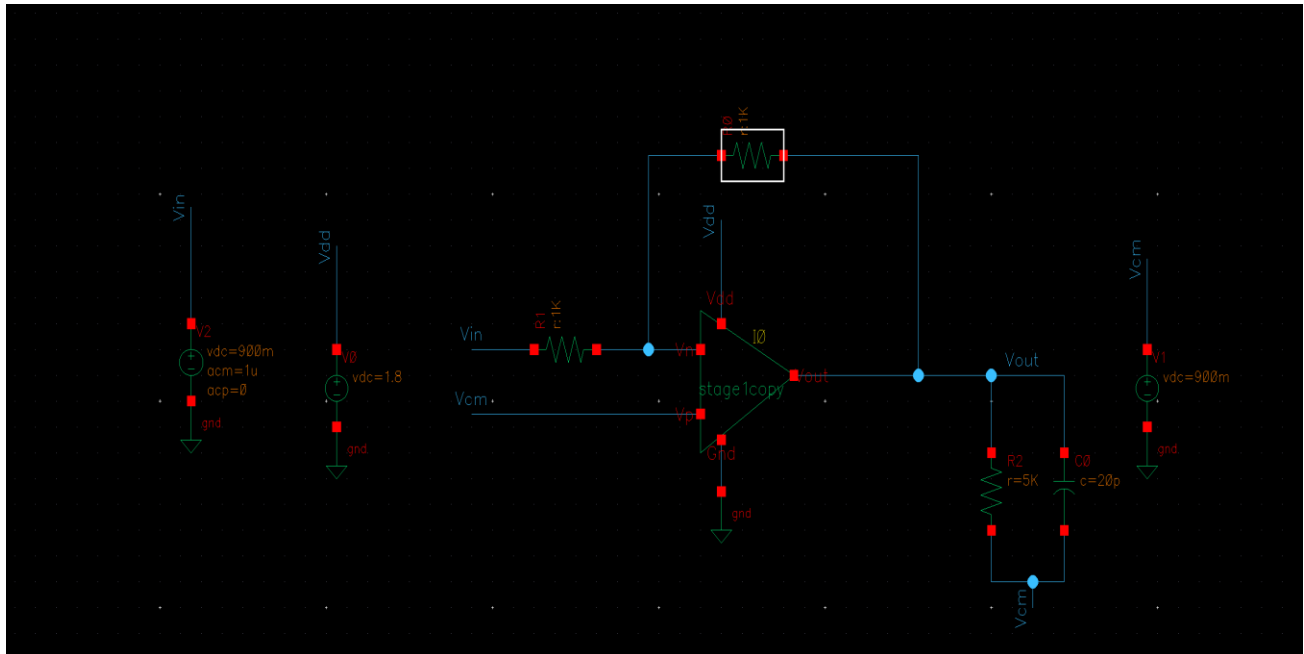
Phase Margin = 60.2126 (Deg) @ freq = 40.41M (Hz)
 Gain Margin = 25.2984 (dB) @ freq = 260.898M (Hz)

[Close] [Help]

Stability Summary of open loop frequency response

c. Result #3 :

Test-bench Circuit for simulating closed-loop frequency response:



Closed Loop frequency response

3-dB bandwidth frequency = 66.8794 MHz.

This value is on the bit higher side due to less chosen value of C_c . This is because it also influences phase margin due to location of non-dominant pole. Hence, for increasing phase margin, a relatively small value of C_c is chosen as a design iteration.

Also, as shown in graph, we observe no peaking as phase margin $> 60^\circ$.

d. Result #4 :

$$\text{error \%} = \frac{1.000436 - 1}{1} * 100 = 0.0436\% < 0.1\%$$

(when step input of 100 mV is applied to closed loop system)

