# EE613: HIGH FREQUENCY ANALOG CIRCUIT DESIGN

## DESIGN PROJECT #1

Design of 2-stage Miller Compensated Opamp

(nMOS as input pair)

Load : $R_L = 5\text{k}\Omega$ and $C_L = 20\text{pF}$

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**Goal :** Designing a two-stage Miller compensated opamp that takes in a differential input and provides a single-ended output. This opamp will be used eventually in a unity feedback loop driving a load $R_L$ = 5kΩ, and $C_L$ = 20 pF.

a) When a step input is applied to the closed-loop system, the output must settle to the desired valuewith less than 0.1% error.
b) The closed-loop frequency response must not exhibit any peaking.
c) The closed-loop 3-dB bandwidth must not be smaller than 20MHz.

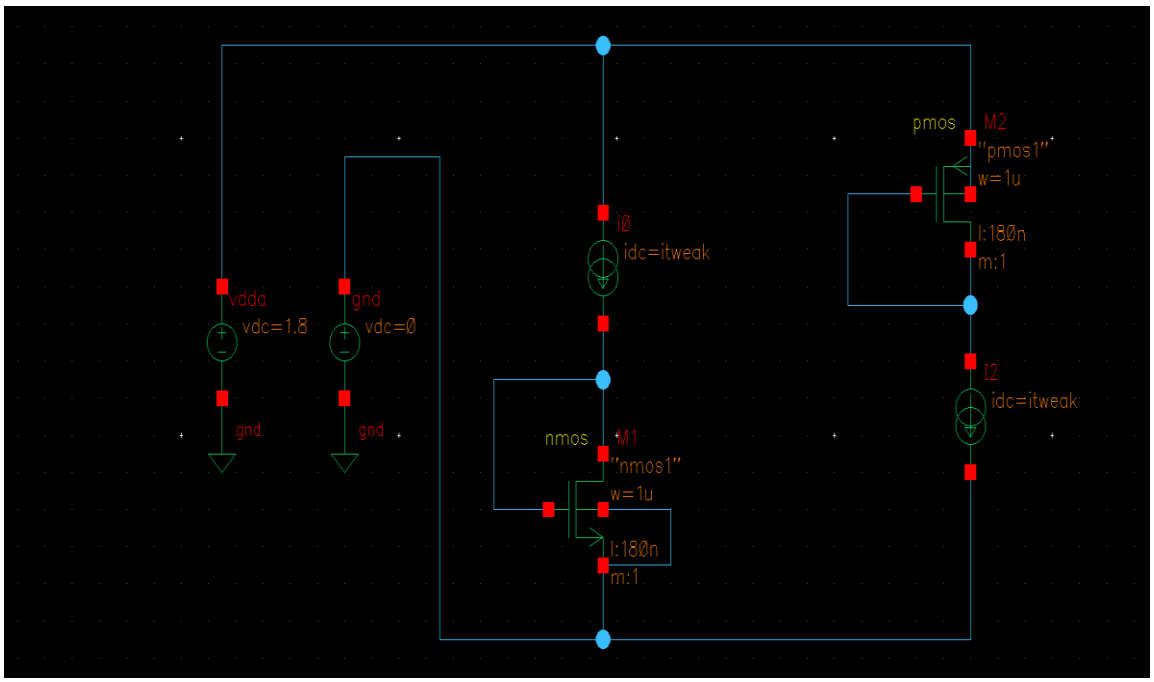
## Components provided:

a) Two ideal voltage sources: one with the value $V_{dd}$ = 1.8V and another with the value $V_{cm}$ = $V_{dd}$/2 (=0.9V)
b) An ideal ground.
c) A reference current source of 1μA for biasing.
d) An ideal resistor and a capacitor for load, $R_L$ = 5kΩ, and $C_L$ = 20 pF.
e) One ideal resistor and a capacitor for compensation, $R_L$ = 5kΩ, and $C_L$ = 20 pF.
f) 180nm technology nMOS and pMOS.

## General Information about MosFETs used :

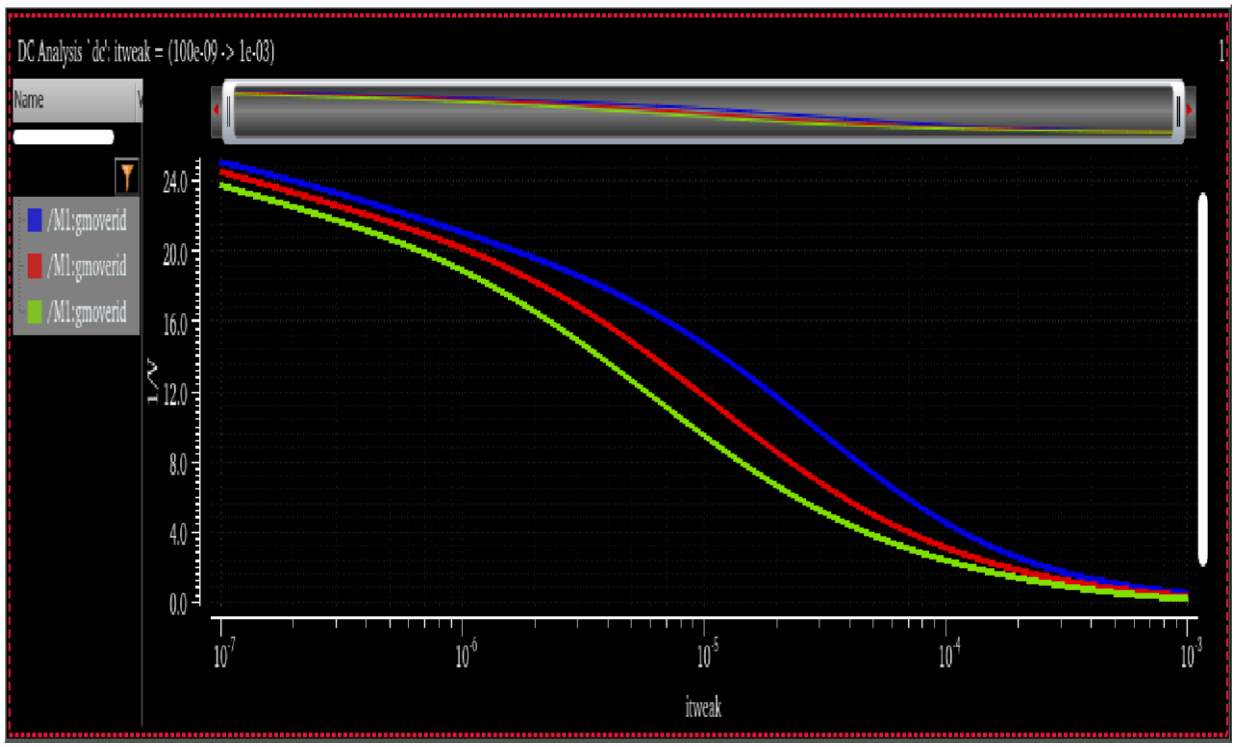
1. For circuit design, have used the 180nm technology MOSFETs.
2. Design is done using nMOS input stage and the second stage is a pMOS common source amplifier.
3. For all nMOS, the bulk (body) terminal is shorted with ideal ground. Similarly, for all pMOS, the bulk (body) terminal is shorted with corresponding source terminal.
4. $L_{min} = 180\ nm$ and $W_{min} = 400\ nm$.

## LOOK-UP TABLE Circuit :

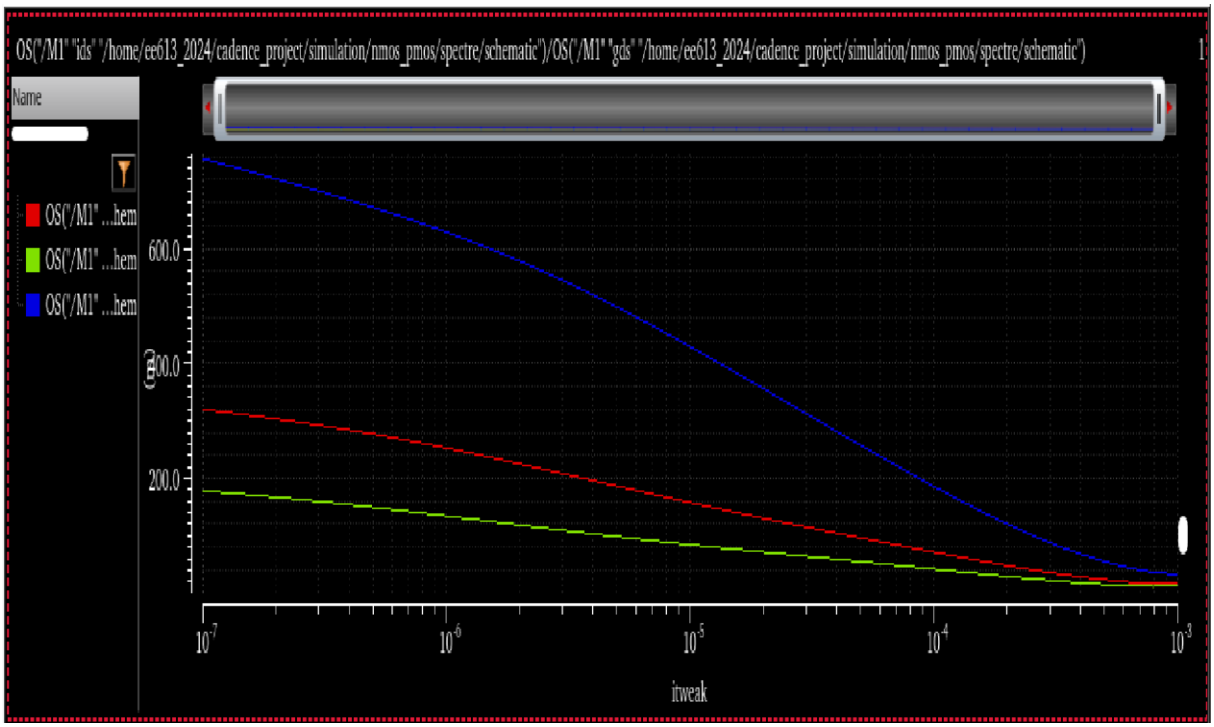



Here we have characterised for L = $L_{min}, 2 * L_{min}$ $and$ $3 * L_{min}$. We have kept W = 1µm and tweaked the drain-to-source current. As we can see, both pMOS and nMOS are in saturation region.

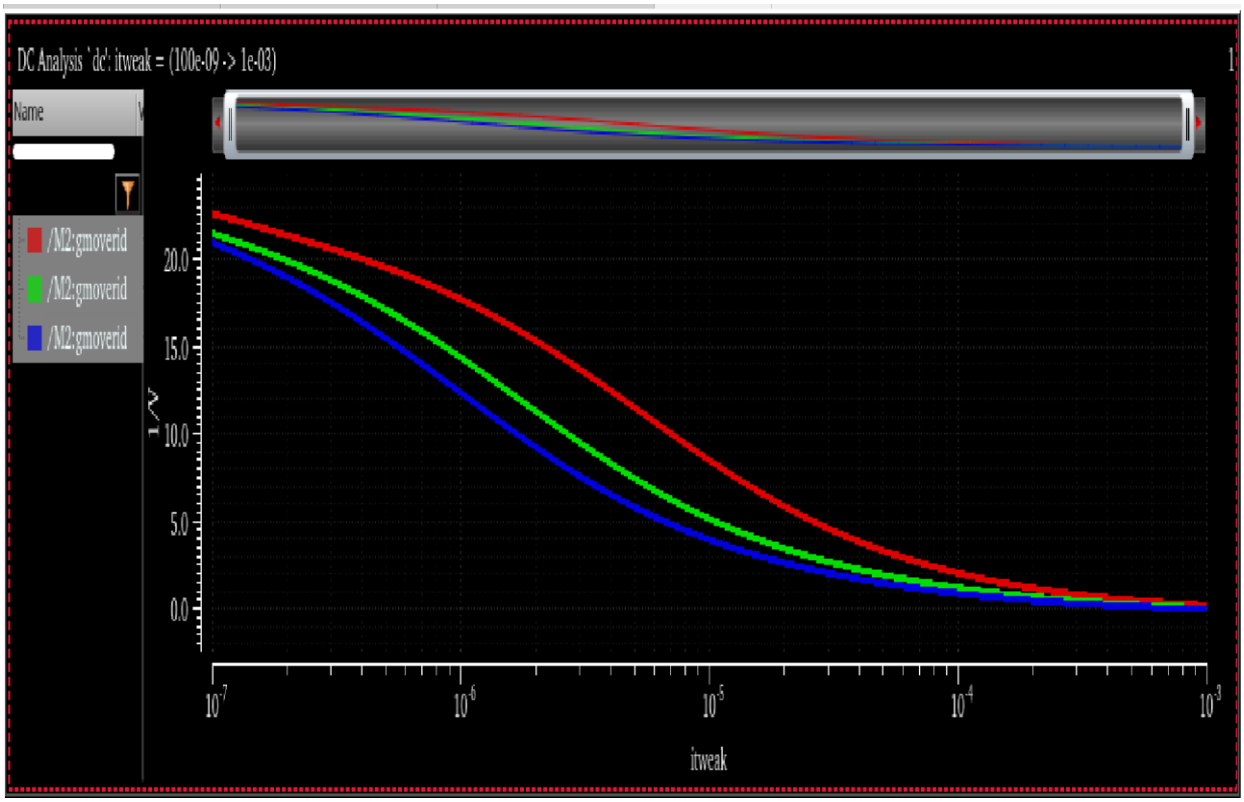
## gm/Id versus Id plot for nMOS :



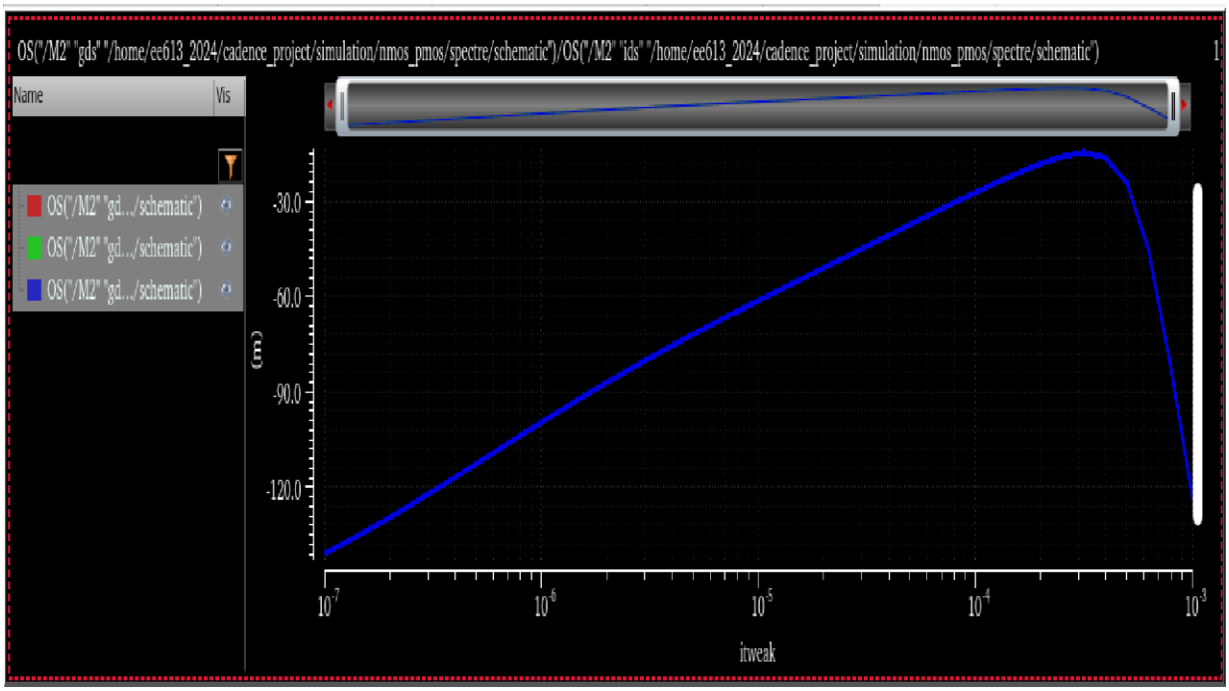
## gds/Id versus Id plot for nMOS :




## gm/Id versus Id plot for pMOS:



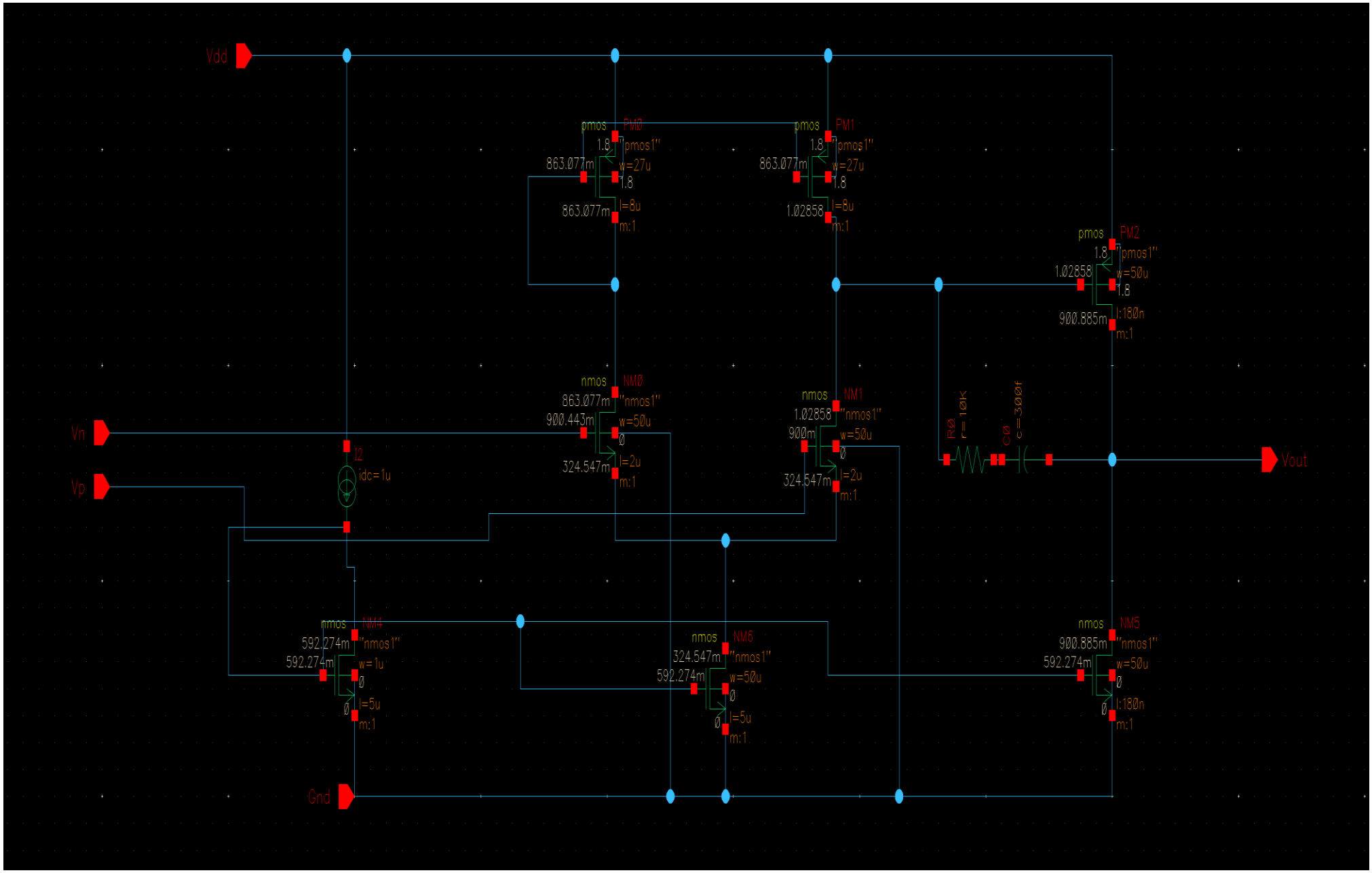
## gds/Id versus Id plot for pMOS:



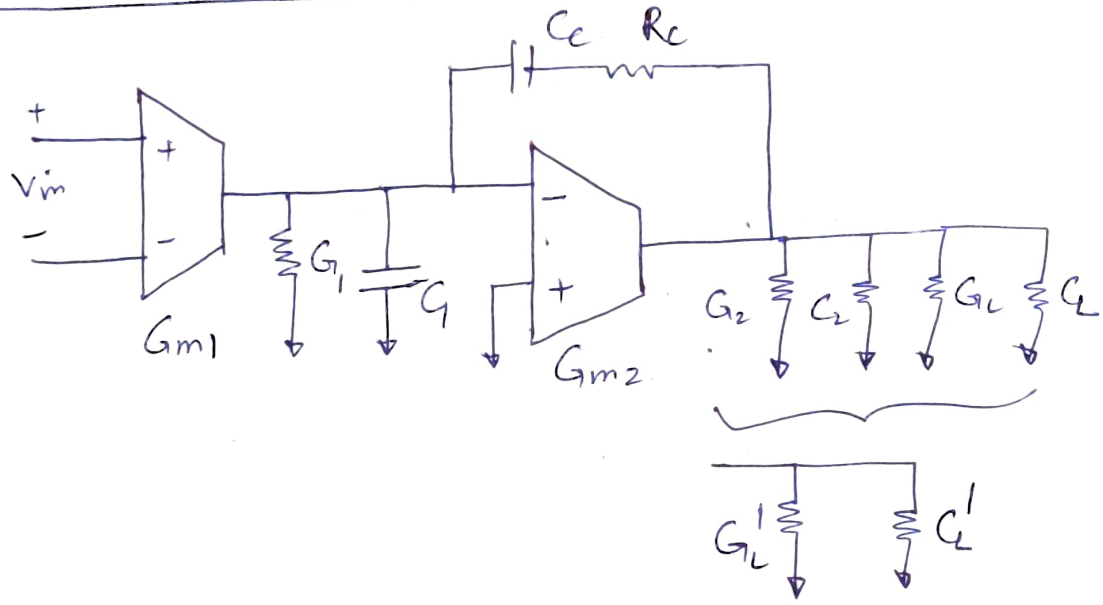

- We have used these plots to get rough estimates of starting values of sizing. Henceforth, depending on obtained results and theoretical calculations, further tweaking of sizing has been done.
- For example, if certain initial value of W gives a certain gain for first stage, increasing W might possibly increase the gain. Hence, the needful is done based on obtained results in successive iterations.

- Now we look at the transistor level schematic of the OPAMP designed. This is a 2-stage Miller compensated OPAMP which meets the required specifications as stated above.

- In the circuit given below, we can see the transistor level implementation along with the DC bias voltages. As we can see, all the transistors are happily in saturation, I mean that's what we wanted, right?!
- Here, we chose the value of (W/L) for bias nMOS to be 1/5, so that it generates enough voltage at bias current = 1 μA and remains in saturation. In this case, it is $V_{GS} = 592.274\ mV$.


Vdd
pmos
PM0
1.8
"pmos1"
863.077m
w=27u
1.8
863.077m
l=8u
m:1
pmos
PM1
1.8
"pmos1"
863.077m
w=27u
1.8
1.02858
l=8u
m:1
pmos
PM2
1.8
"pmos1"
1.02858
w=50u
1.8
900.885m
l:180n
m:1
nmos
NM0
863.077m
"nmos1"
900.443m
w=50u
0
324.547m
l=2u
m:1
nmos
NM1
1.02858
"nmos1"
900m
w=50u
0
324.547m
l=2u
m:1
R0
r=10K
C0
c=300f
Vout
Vn
Vp
I2
idc=1u
nmos
NM4
592.274m
"nmos1"
592.274m
w=1u
0
0
l=5u
m:1
nmos
NM6
324.547m
"nmos1"
592.274m
w=50u
0
0
l=5u
m:1
nmos
NM5
900.885m
"nmos1"
592.274m
w=50u
0
0
l:180n
m:1
Gnd

# DESIGN METHODOLOGY




This is a miller compensated OTA with zero cancellation resistor.

$$A_0 = \frac{G_{m1}}{G_1} \times \frac{G_{m2}}{G_L'}$$

$$p_1 \approx \frac{G_1}{C_1 + C_c \frac{G_{m2}}{G_L'}}$$

$$p_2 \approx \frac{G_L' + G_{m2}\frac{C_c}{C_1 + C_c}}{C_L' + \frac{C_1 C_c}{C_1 + C_c}}$$

$$p_3 \approx \frac{1}{R_c C_1}$$

$$z = \frac{1}{C_L\left(\frac{1}{G_{m2}} - R_c\right)}$$

→ For this to be LHZ we need $\boxed{R_c > \frac{1}{G_{m2}}}$

$$\omega_u \approx A_0 p_1 \approx \frac{G_{m1}}{C_c}$$

$$\boxed{\phi_M \approx 90^\circ - \tan^{-1}\left(\frac{\omega_u}{p_2}\right) - \tan^{-1}\left(\frac{\omega_u}{p_3}\right) - \tan^{-1}\left(\frac{\omega_u}{z}\right)}$$

Now here,

$G_{m_1} = g_{m1,2}$

$G_{m_2} = g_{m5}$

$G_1 = g_{ds2} + g_{ds4}$.

$G_2 = g_{ds5} + g_{ds6}$

$C_1 \approx C_{gs5}$

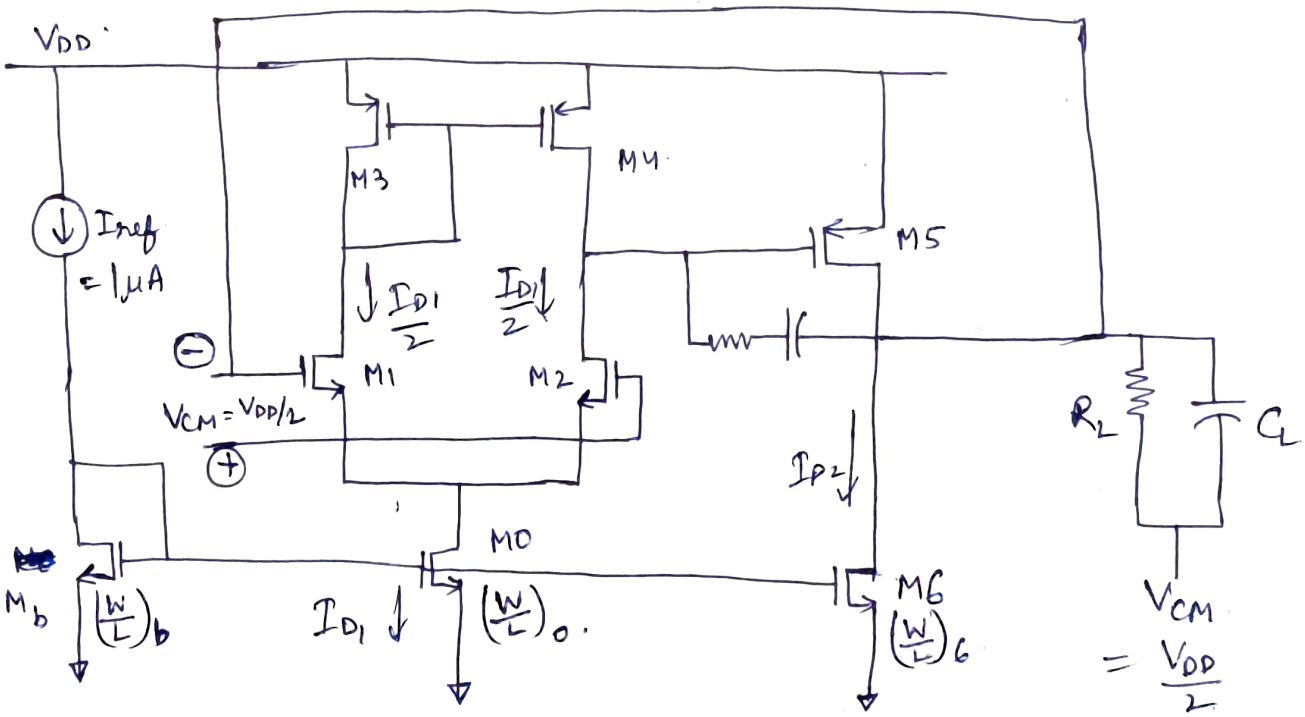
$C_2 = C_{db5} + C_{db6}$

- $C_L' = C_L + C_{db5} + C_{db6} \approx C_L = 20pf$.

$G_L' = G_L + g_{ds5} + g_{ds6} \approx G_L = 200\mu S$.

We want to use this OPAMP in negative f/b.

Circuit looks like this :-




$\left(\frac{I}{W}\right)_{3,4,5}$ = same for DC bias.

According to 0.1% error in steady state,

$$1 - \frac{A}{1+A} \leq \frac{0.1}{100}$$

$$\Rightarrow \quad A > 999$$

$\Rightarrow$ DC open loop gain $\geq$ 60 dB

$\Rightarrow$ $\phi_M > 60^\circ$ (for no peaking).

$\Rightarrow$ $\omega_{3dB} > 20\,MHz$

(Theoretically $\omega_{3dB} \approx \omega_u \Rightarrow \omega_u > 20\,MHz$)

Now, if we assure $C_c, C_L >> C_1$

$$\Rightarrow \quad p_1 \approx \frac{G_1}{C_c \frac{G_{m2}}{G_L}}, \quad p_2 \approx \frac{G_{m2}}{C_L}$$

$$p_3 \approx \frac{1}{R_c C_1}, \quad z = \frac{1}{C_L\left(\frac{1}{G_{m2}} - R_c\right)}$$

Also, for first order behaviour near $\omega_u$,

(# poles − # zeroes) before $\omega_u = 1$.

$p_1 << 130\,M$ rad/s.

$$\Rightarrow \quad \frac{g_{ds2} + g_{ds4}}{C_c \frac{g_{ms}}{200\mu s}} << [illegible] \times 10^6 \text{ rad/s}$$

$p_2 > 920\,M$ rad/s

$$\Rightarrow \quad \boxed{G_{m2} > 4100\,\mu S}$$

Also

$$\phi_M > 60^\circ = 90^\circ - \tan^{-1}\left(\frac{\omega_u}{p_2}\right)$$

Assuming, z and $p_3$ don't contribute much around $\omega = \omega_u$.

$$p_2 \approx 2\omega_u \approx 40\,MHz.$$

$$\boxed{G_{m_2} > 800\,\mu S}$$

$$\Rightarrow \boxed{R_C > 1250\,\Omega}$$

Transistor level design

$$G_{m_2} = g_{m5} > 800\,\mu S = \frac{2I_{D2}}{V_{ov}}$$

$I_{D2} \approx 180\,\mu A$ for $V_{ov} \approx 0.375$

But $I_{out} \approx \frac{0.9V}{5k} \approx 45\,\mu A$

$\Rightarrow$ $I_{bias}$ for 2nd stage $\approx 100\,\mu A$

Also, gain of second stage > gain of first stage.

$$\Rightarrow \frac{G_{m2}}{G_L} > \frac{G_{m1}}{G_1}$$

$\left(\frac{g_{m5}}{I_5}\right) = 8$ $\Rightarrow$ We choose $L = 0.18\,\mu m$

$W = 50\,\mu m$.

$$\boxed{\left(\frac{W}{L}\right) \simeq 270}$$

$$A_0 = 1000 \cdot \frac{g_{m1}}{g_{ds2}+g_{ds4}} \times \frac{800\mu}{200\mu}$$

On generating look-up-table, we observe, on varying $I_D/W$, $g_{ds}/I_d$ does not vary much

Hence, we tweak $g_{m1}$ to get appropriate gain.

$$g_{m1} \propto \sqrt{\left(\frac{I}{W}\right)}$$

And $g_{ds} \propto W$

$\Rightarrow$ Instead of reducing W, we choose to increase $I_{D1}$.

For given specs, $I_{D1} \approx 50\,\mu A$ sets DC loop gain appropriately.

$$\boxed{g_{m1} \approx 430\,\mu S} = \frac{2 I_{D1/2}}{V_{OV}}$$

Assume $V_{OV} \approx 0.12V$

$$\Rightarrow I_{D1/2} \approx 25\mu A \Rightarrow I_{D1} \approx 50\mu A.$$

For $V_{offset} = 0 \Rightarrow \left(\frac{I}{W}\right)_{3,4,5} = \text{same}$

$$\Rightarrow \left(\frac{I_{D1,2}}{W}\right)_{3,4} = \left(\frac{I_{D2}}{W}\right)_5$$

For $M_0$, to carry $1\,\mu A$ and maintain $V_{gs} \approx 600\,mV$ $(V_{TH} \approx 490\,mV)$ $(V_{OV} \approx 0.1V)$

$W_b = 1\mu m$
$L_b = 5\mu m$ $\Big]$ $\left(\frac{W}{L}\right)_b = \left(\frac{1}{5}\right)$

On simulation, $I_{D1} \approx 49.6\mu A$

$I_{D2} \approx 1.08\mu A$

Now, after simulations certain values did not match due to various assumptions in pole locations, $V_{OV}$ values etc.

Hence fine tuning in W and L values were required after observing behaviour through simulations.

Overall gm and gds values were then noted and attached below.

## Method of Fine tuning

$g_m = \frac{2I_D}{V_{OV}}$ $\quad I_D \propto \frac{W}{L}(V_{OV})^2$.

→ If $I_D$ is constant and gm should ↑

⇒ $V_{OV}$ ↓.

→ If $V_{OV}$ ↓ and $I_D$ is constant, $\left(\frac{W}{L}\right)$ ↑.

→ If L is kept unchanged ⇒ $g_m \propto W$.

and W ↑.

→ Tuned W majorly to increase gm.

while $g_{ds} \propto \frac{1}{L^2}$ ⇒ L ↓ ⇒ gds ↑ more significantly.

After phase margin and loop gain simulations, initial guess of $C_c = 800fF$. This was later fine tuned to $C_c = 300fF$ (based on positive / negative effect on phase margin).

Similarly initial guess of $R_c = 1250\Omega$. This introduced a third pole which significantly degraded phase margin. Hence, the need to introduce LHZ by setting $R_c = 10k\Omega$ which ensured no peaking closed loop response ($\phi_M > 60°$).

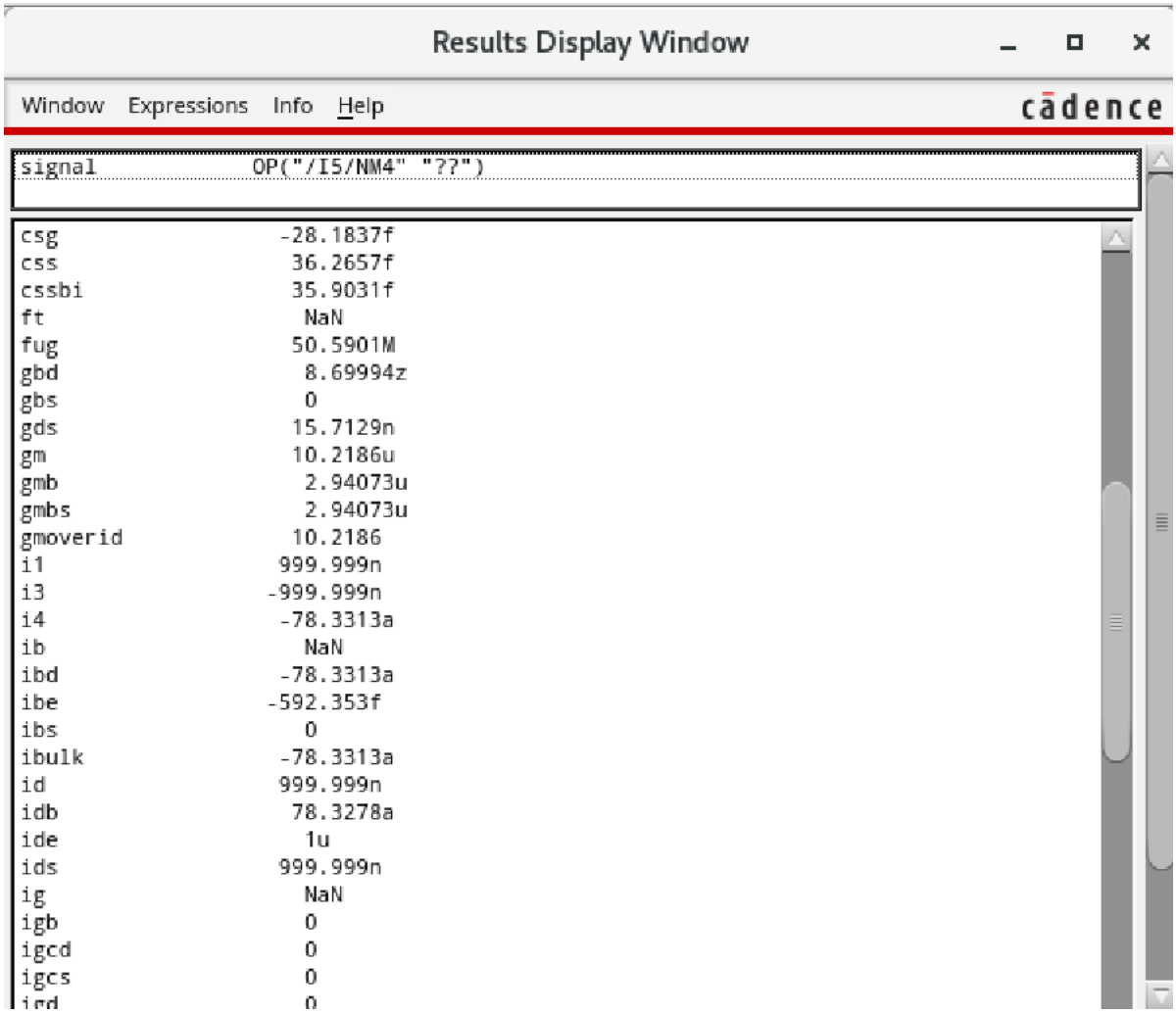
$\boxed{C_c = 300fF}$ , $\boxed{R_c = 10k\Omega}$ .

## Block Level Design Summary :

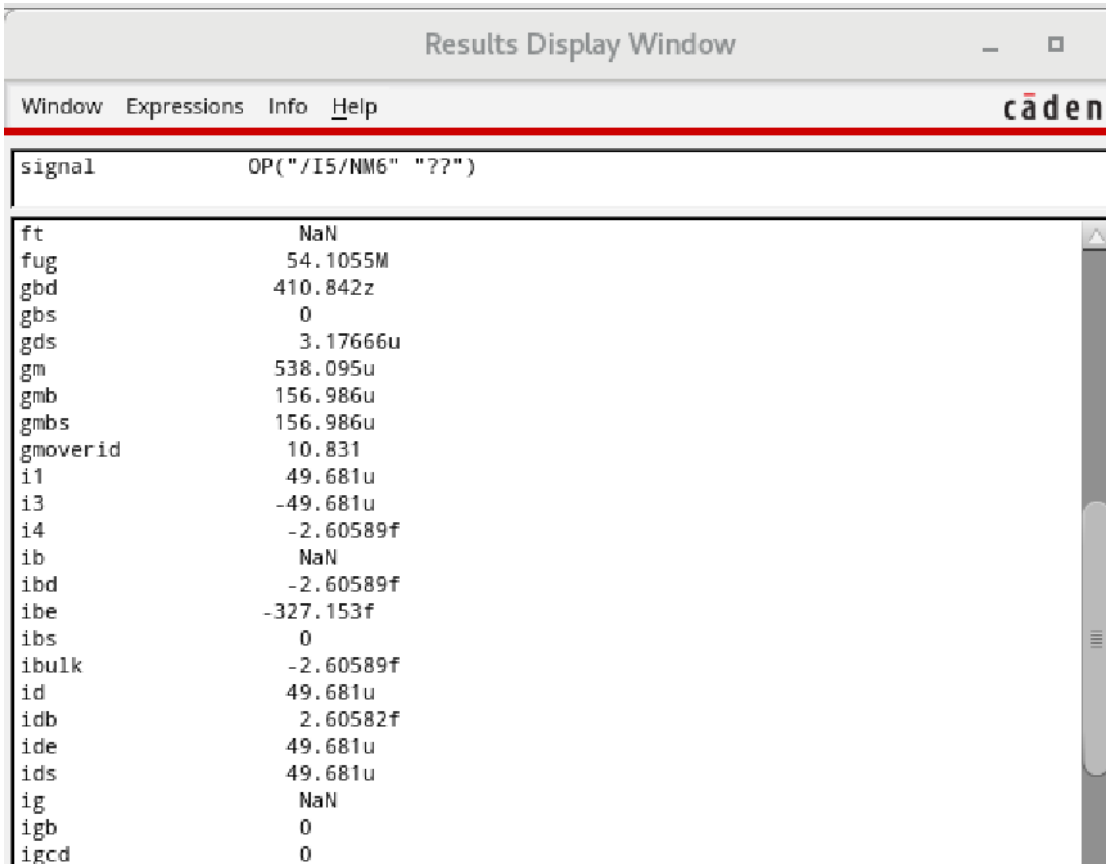
| | | | |
|---|---|---|---|
| Gm1 | 430 µS | Gm2 | 6.6 mS |
| G1 | 1.2 µS | G2 | 525 µS |
| GL | 200 µS | CL | 20 pF |
| Cc | 300 fF | Rc | 10 kΩ |

## Transistor Level Design Summary: (refer to naming in circuit drawn)

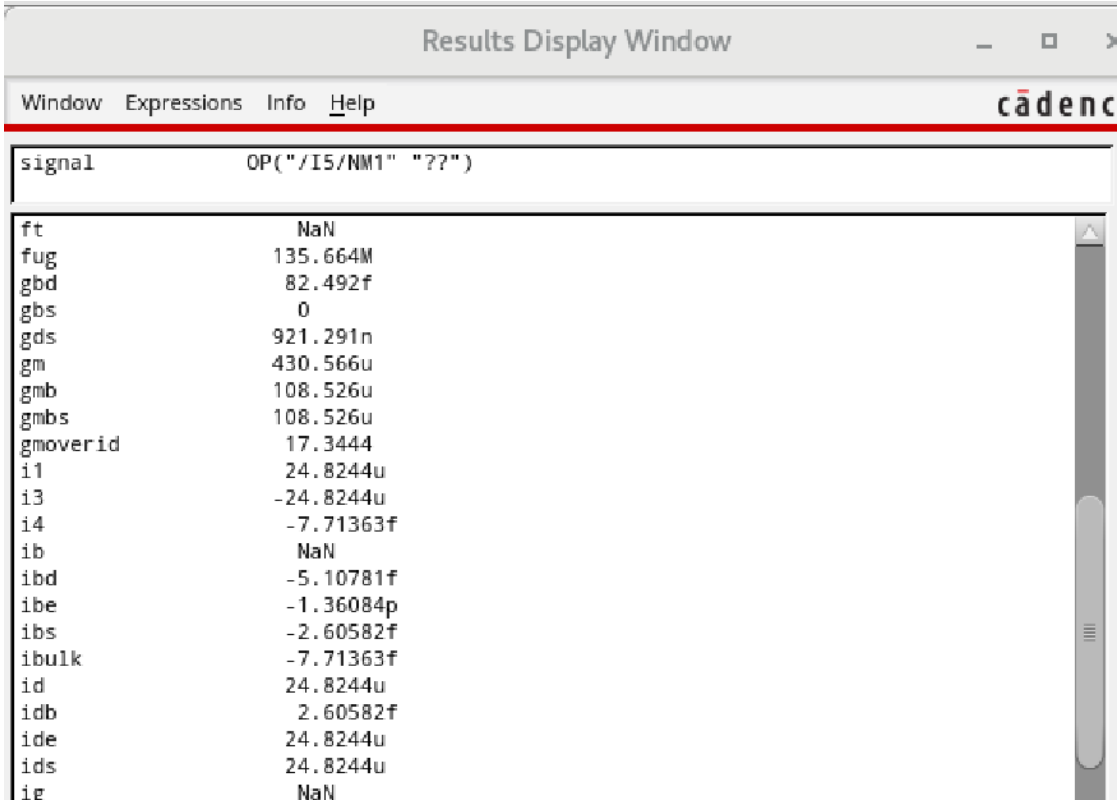
1. DC operating parameters of $M_b$ :



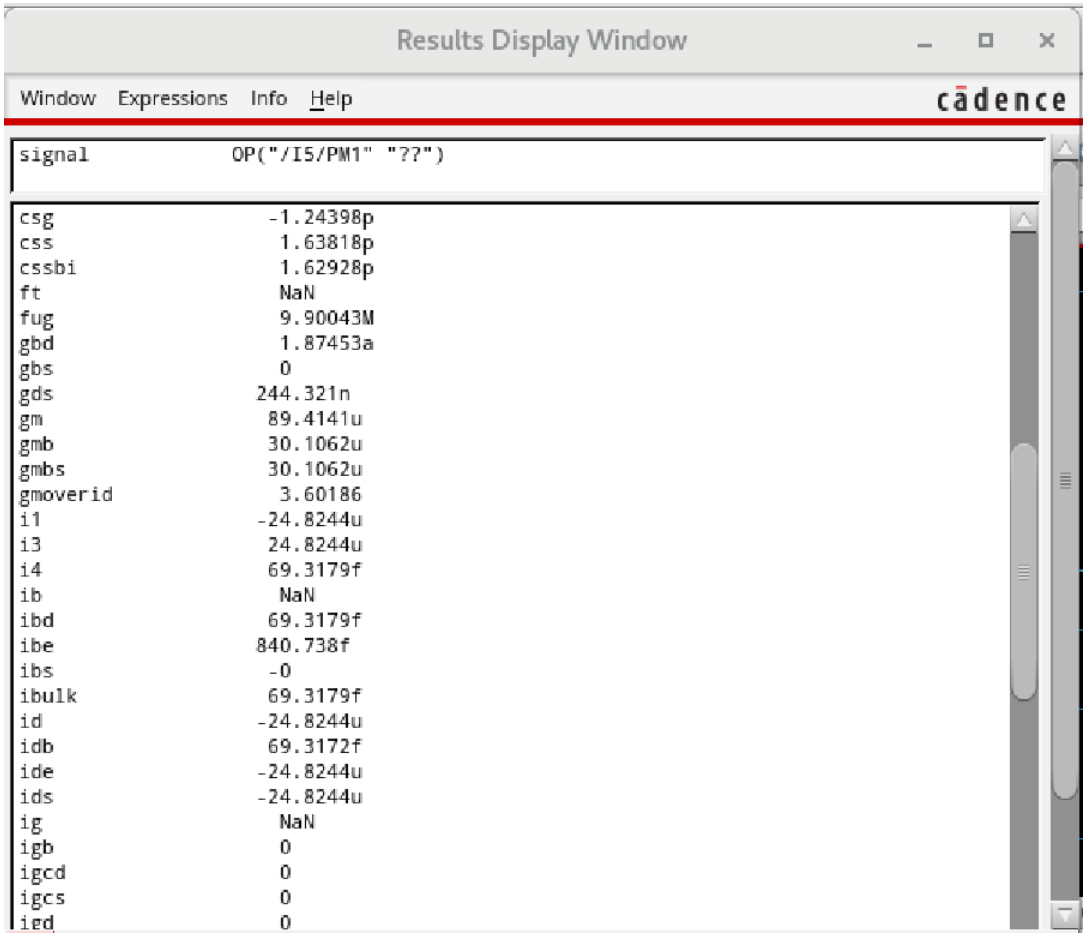
2. DC operating parameters of $M_0$ :



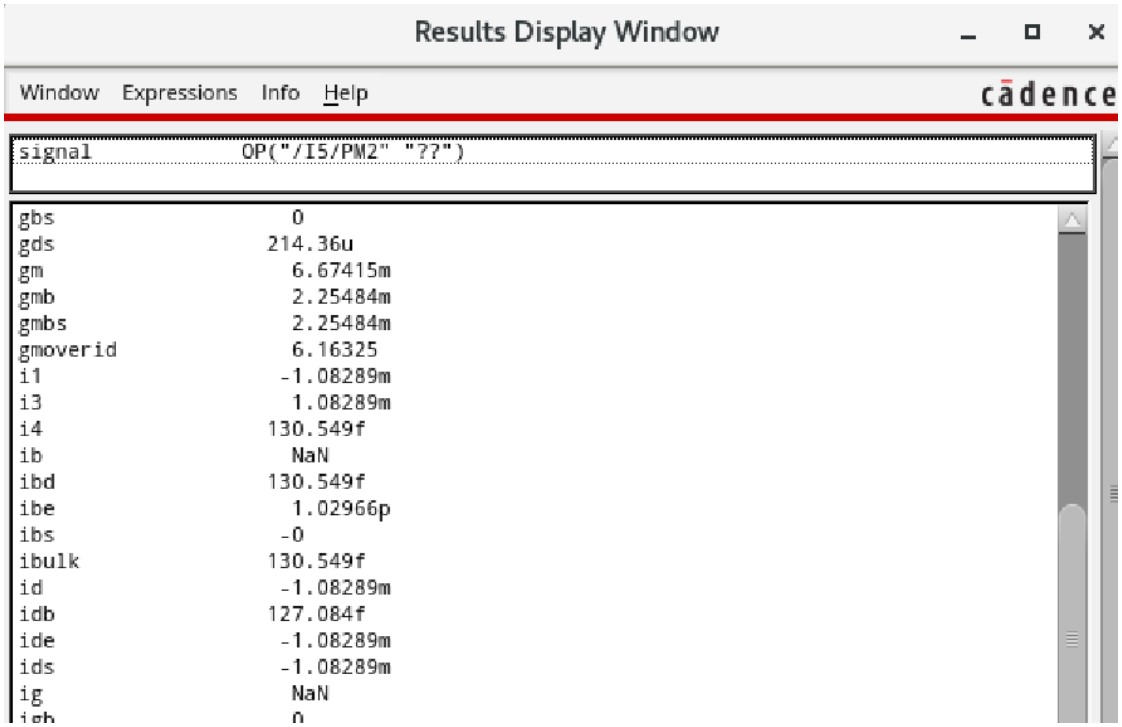

3. DC operating parameters of $M_{1,2}$ :



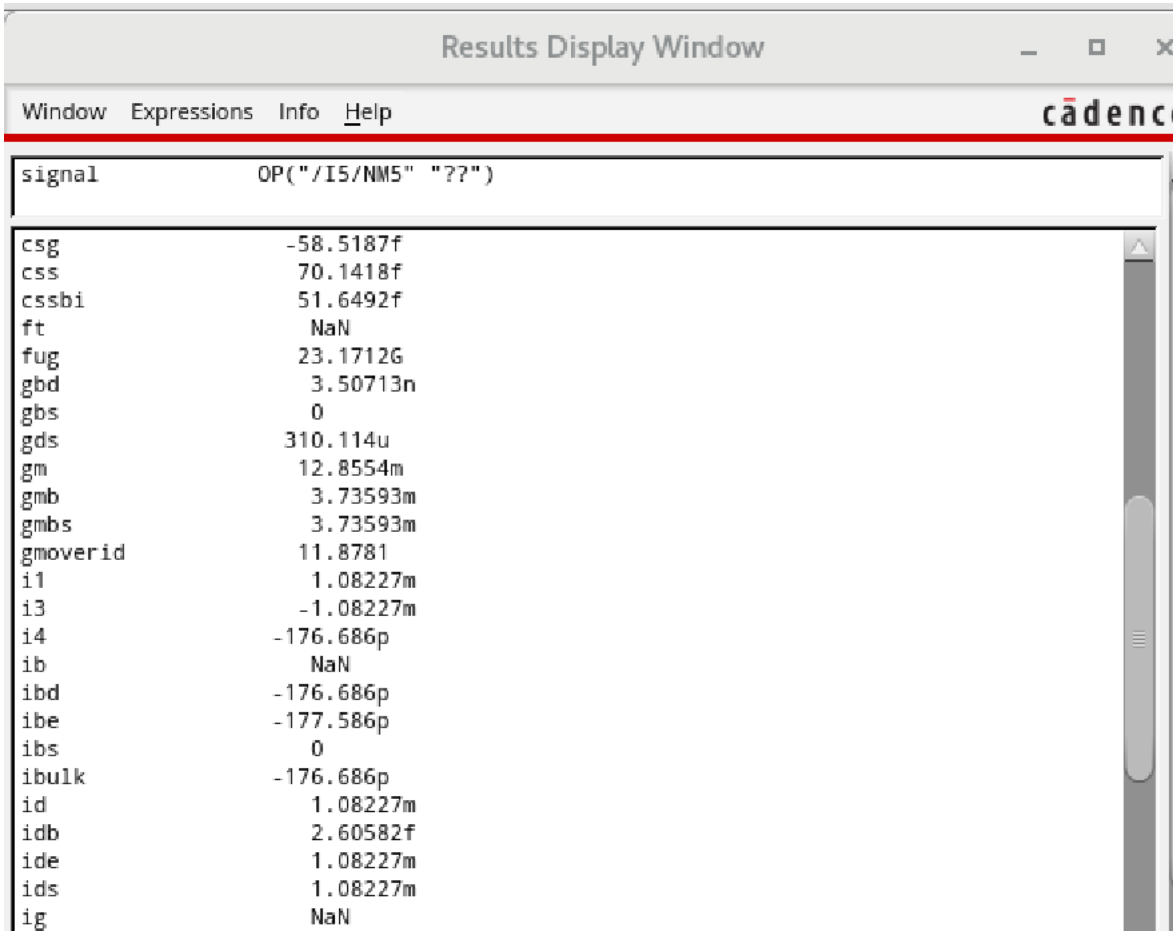
4. DC operating parameters of $M_{3,4}$ :




5. DC operating parameters of $M_5$ :



6. DC operating parameters of $M_6$ :



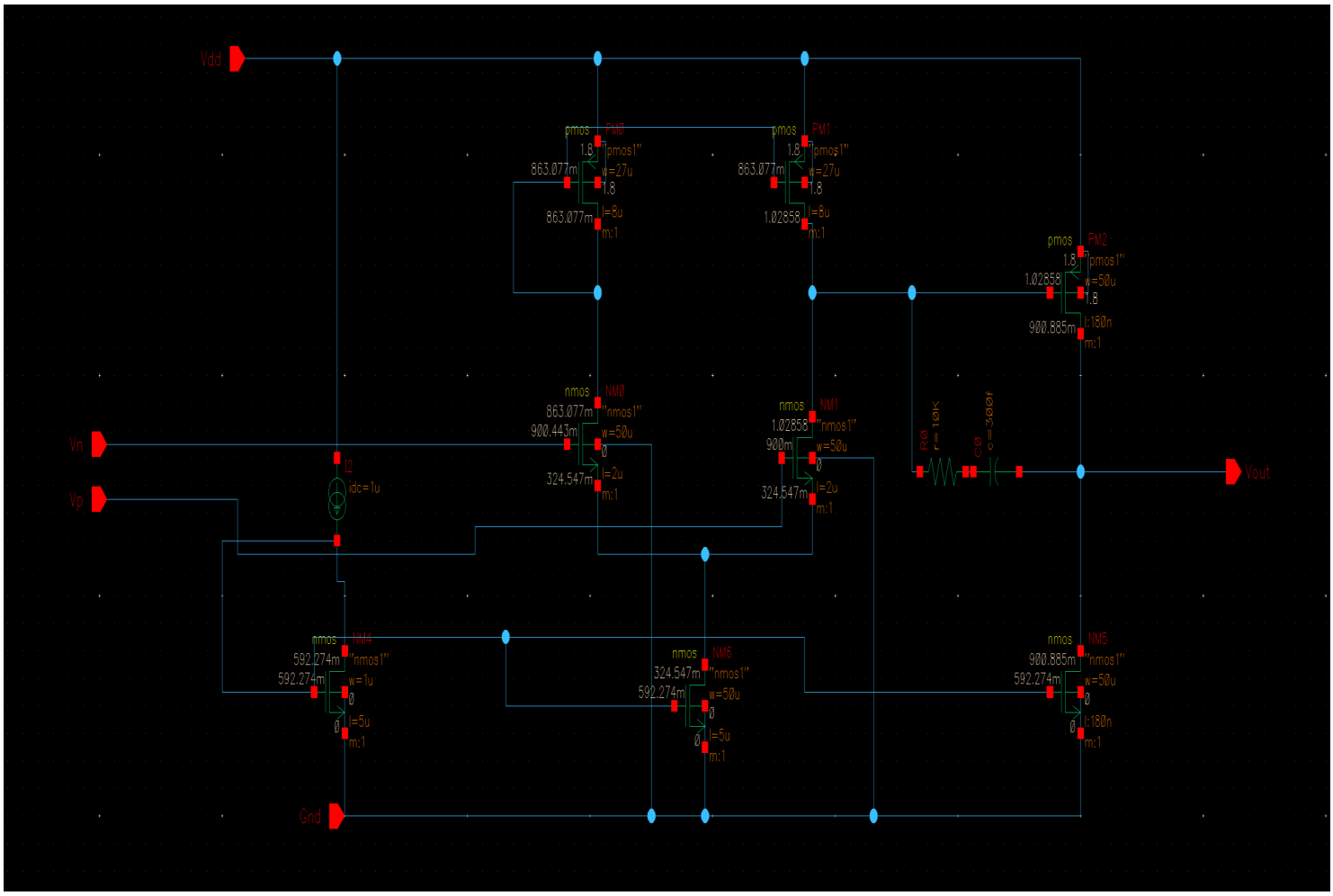

| Name | W (m) | L (m) | W/L |
|---|---|---|---|
| $M_b$ | $1\mu$ | $5\mu$ | 0.2 |
| $M_0$ | $50\mu$ | $5\mu$ | 10 |
| $M_1$ | $50\mu$ | $2\mu$ | 25 |
| $M_2$ | $50\mu$ | $2\mu$ | 25 |
| $M_3$ | $27\mu$ | $8\mu$ | 3.375 |
| $M_4$ | $27\mu$ | $8\mu$ | 3.375 |
| $M_5$ | $50\mu$ | $0.18\mu$ | 277.77 |
| $M_6$ | $50\mu$ | $0.18\mu$ | 277.77 |

| | | | |
|---|---|---|---|
| $I_{O1}$ | $50 * 10^{-6}$ A | $I_{O2}$ | $1.08 * 10^{-3}$ A |

**Note:** The values of W/L were tuned after simulating the initial values of W and L, to get the required values of Gm1, Gm2, G1 and G2. Method of tuning is explained in the Design methodology.

## Results :

## a. Result #1 :




| Gm1 | 430.566 µS | Gm2 | 6.674 mS |
|---|---|---|---|
| G1 | 1.165 µS | G2 | 524.474 µS |
| GL | 200 µS | CL | 20 pF |
| Cc | 300 fF | Rc | 10 kΩ |

$V_{OUT}$ = 0.900443 V

The above circuit shows all DC bias voltages, indicating saturation operation for each transistor. gm, gds and ids values of each transistor is tabulated and mentioned under transistor level design summary.

Upon comparison, we find the values to be similar and tabulated above:

$$DC\ Loop\ Gain = \frac{\mathrm{Gm1} * \mathrm{Gm2}}{\mathrm{G1} * (\mathrm{GL} + \mathrm{G2})} = 3404.68$$

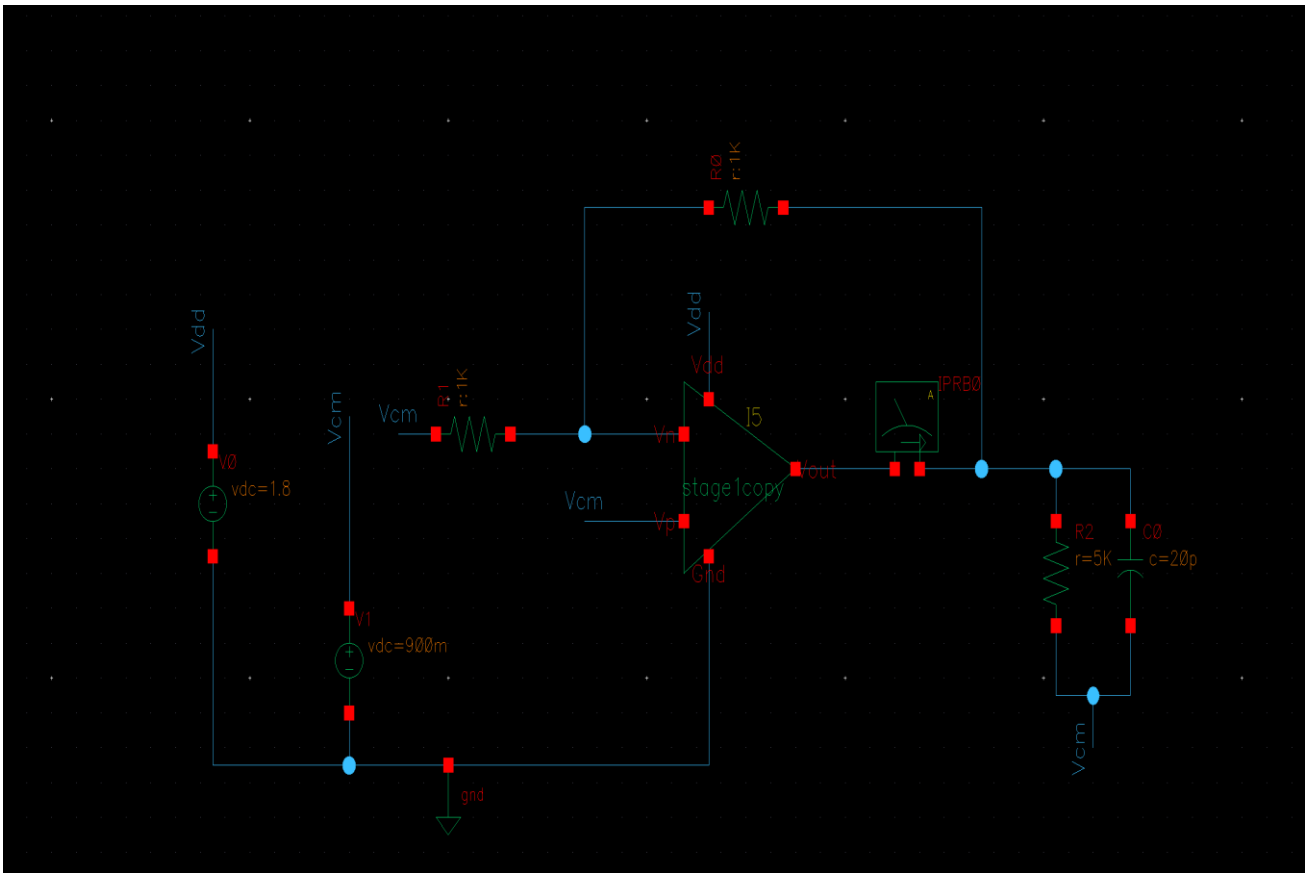
This implies a loop gain of 70.6415 dB. But we don't obtain such gain as various approximations such as G2 << GL , gain of stage 2 > gain of stage 1, etc. fail.

## b. Result #2 :

Bode plot of Loop gain: **DC gain = 60.044 dB**.

**Unity Gain frequency = 40.4671 MHz** and **Phase margin = 60.16°**

Test-bench Circuit for simulating open-loop gain:



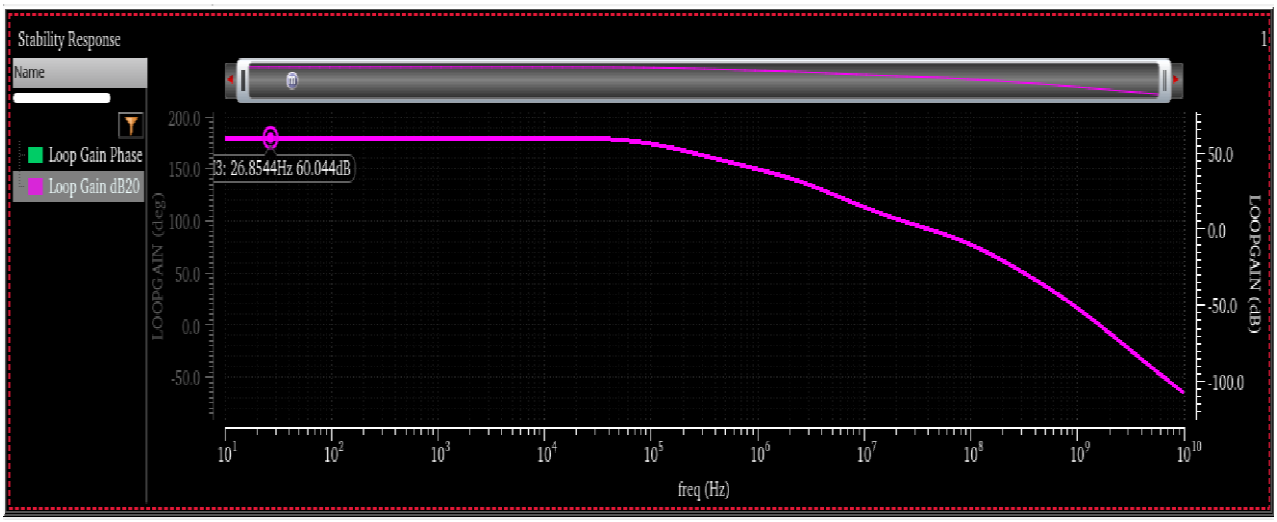



Figure (a) : Open loop gain = 60.044 dB

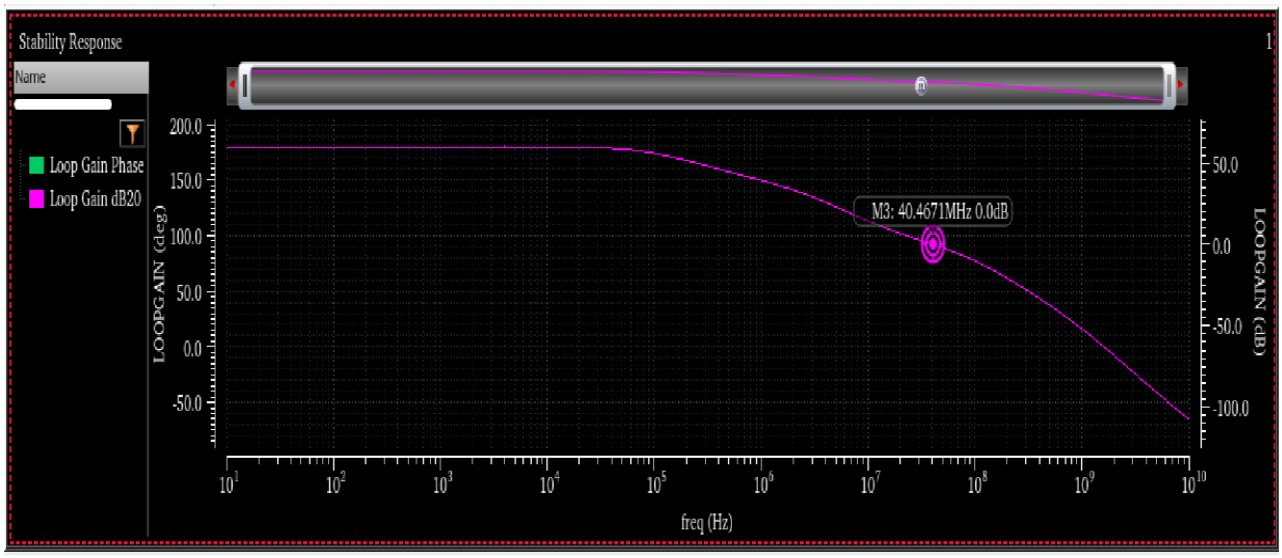



Figure (b) : Unity gain frequency = 40.4671 MHz

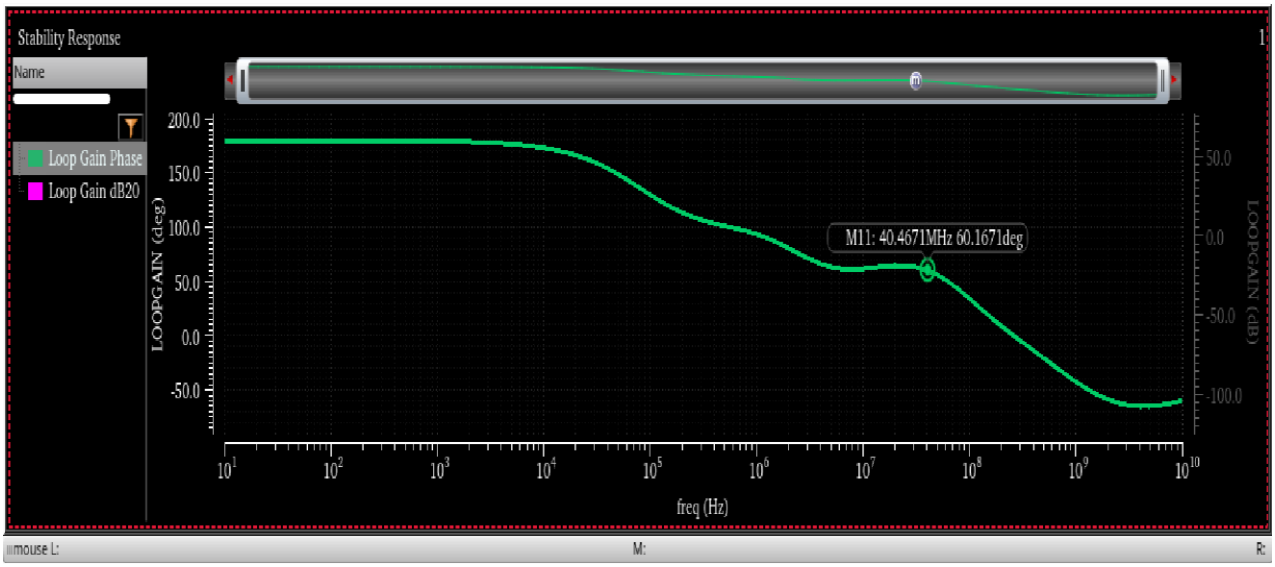



Figure (c) : Phase Margin = 60.1671°

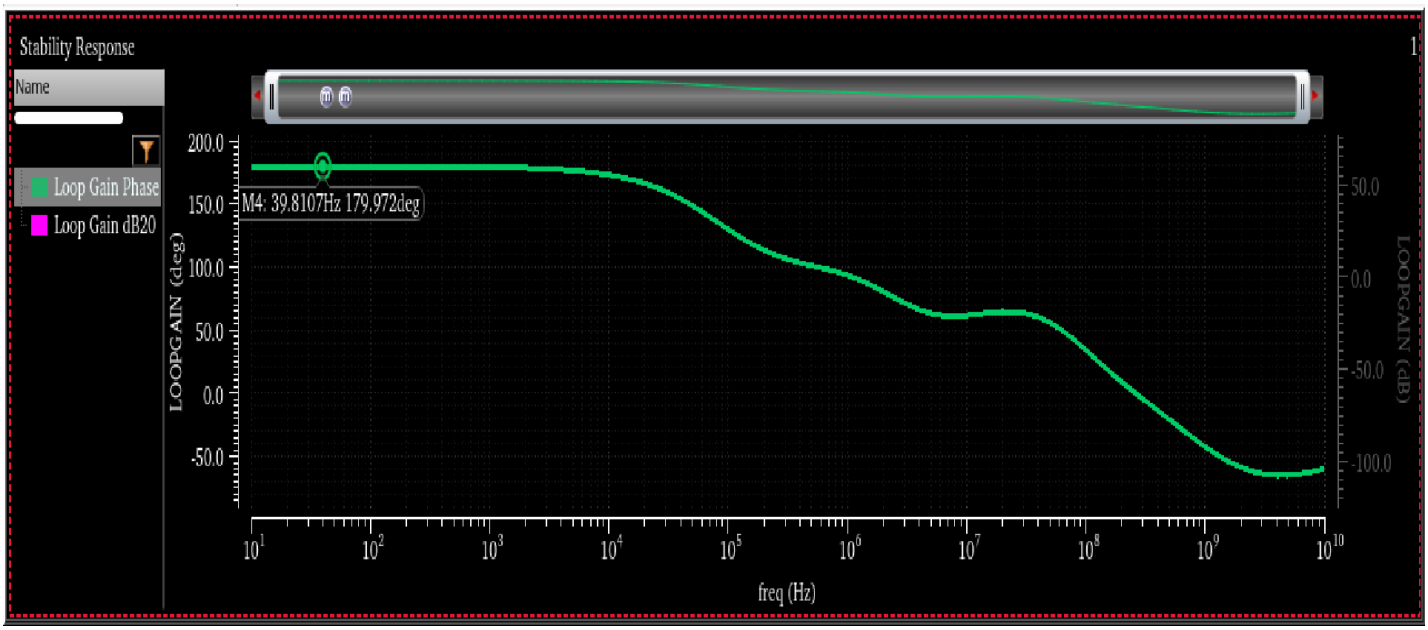
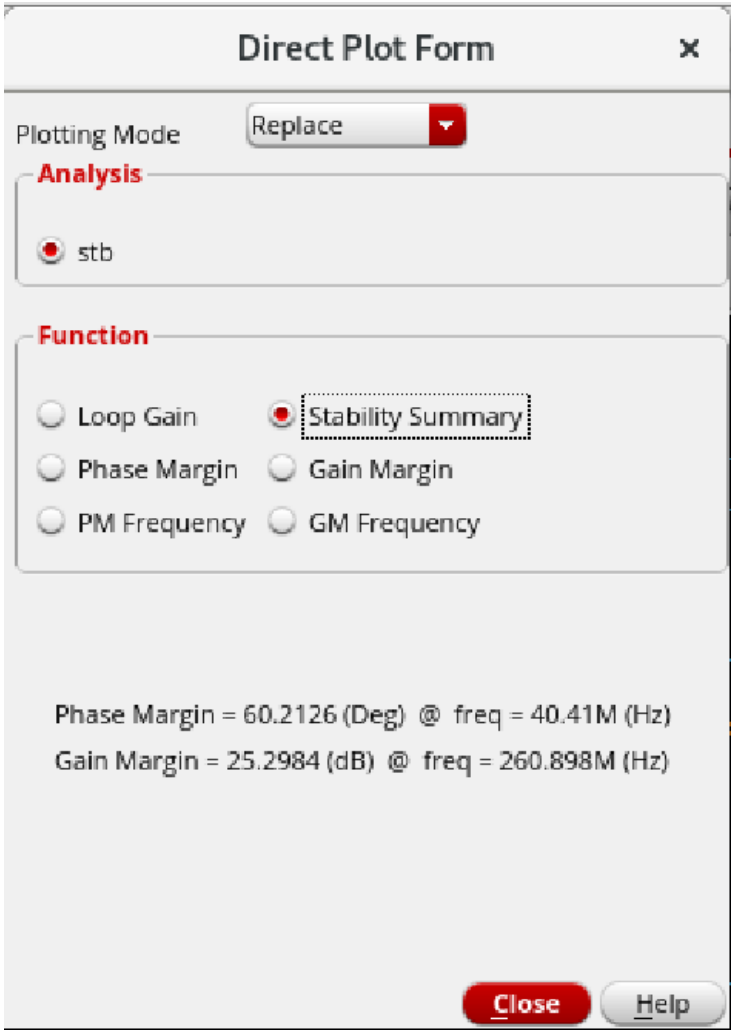


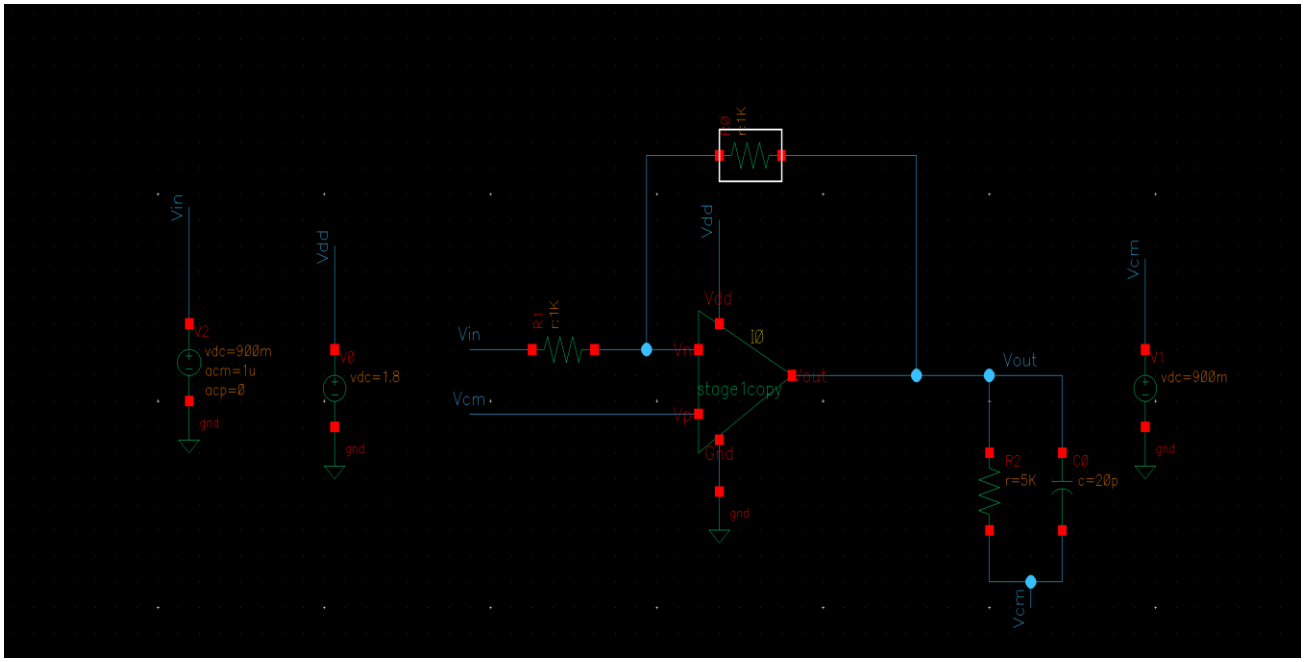

Figure (d) : Loop gain Phase plot

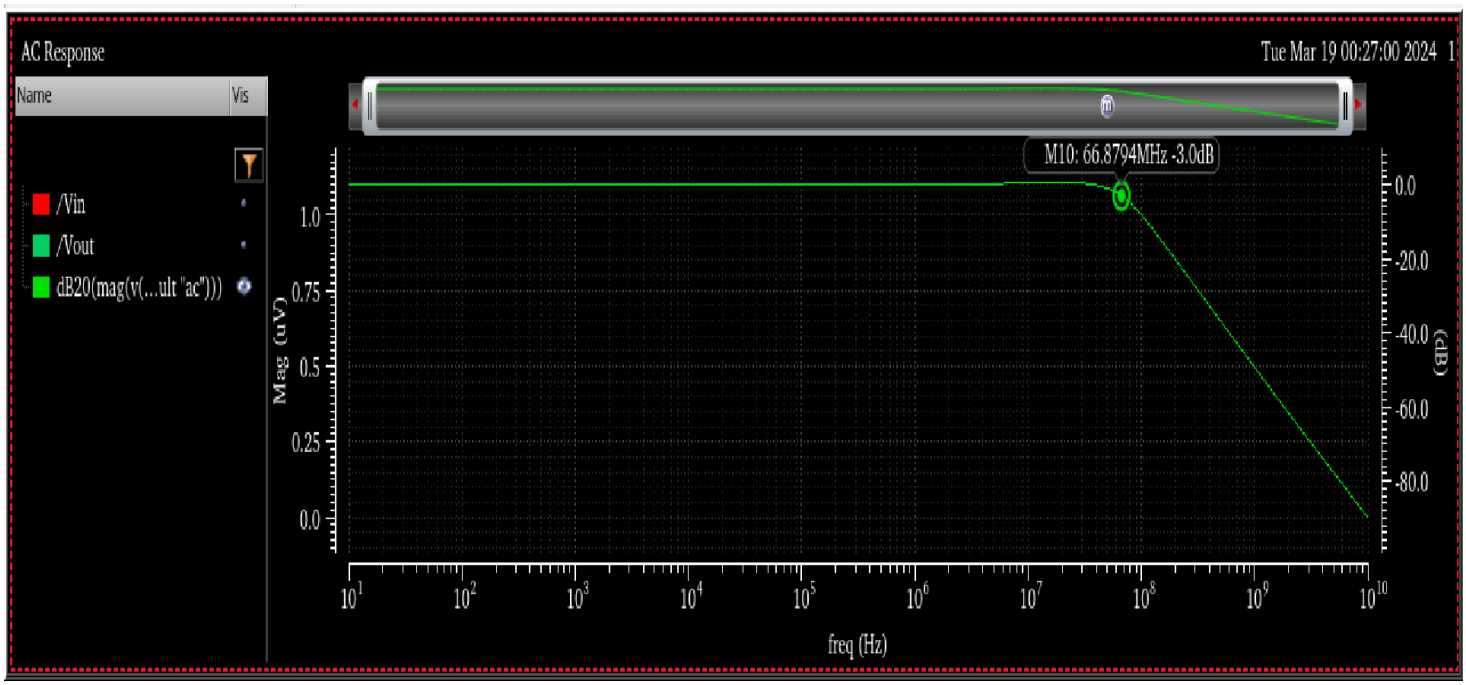



Stability Summary of open loop frequency response

## c. Result #3 :

Test-bench Circuit for simulating closed-loop frequency response:




Closed Loop frequency response

**3-dB bandwidth frequency = 66.8794 MHz.**

This value is on the bit higher side due to less chosen value of Cc. This is because it also influences phase margin due to location of non-dominant pole. Hence, for increasing phase margin, a relatively small value of Cc is chosen as a design iteration.

Also, as shown in graph, we observe no peaking as phase margin > $60^{o}$ .

## d. Result #4 :

**error %** $= \frac{1.000436-1}{1} * 100 = 0.0436\% < 0.1\%$

(when step input of 100 mV is applied to closed loop system)