Parameter Extraction and Circuit Fabrication

2DA1201Y PNP TRANSISTOR

Group - 2
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Parameters extraction using reverse engineering

1 . Estimation of Ideality factor

since $I_C = I_0 \exp \frac{V_{EB}}{NV_T}$ taking log both sides

$$\Rightarrow V_{EB} = 2.303nV_T \log I_C - 2.303nVT \log I_0$$

$$y = mx + c$$

$$m = 2.303nV_T,\ y = V_{EB} \&\ x = \log I_C$$

m = 0.0807 & n=1.07

$$\boxed{Ideality factor\ n \approx 1}$$

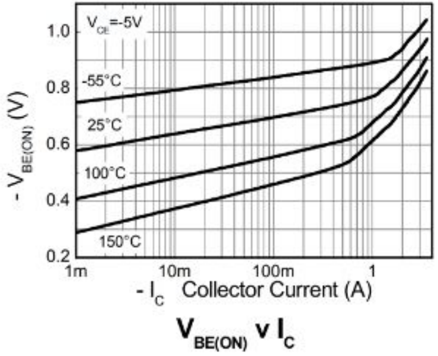


Figure 8: $V_{BE(ON)}$ vs. I_C

2.Power limit variation with temperature

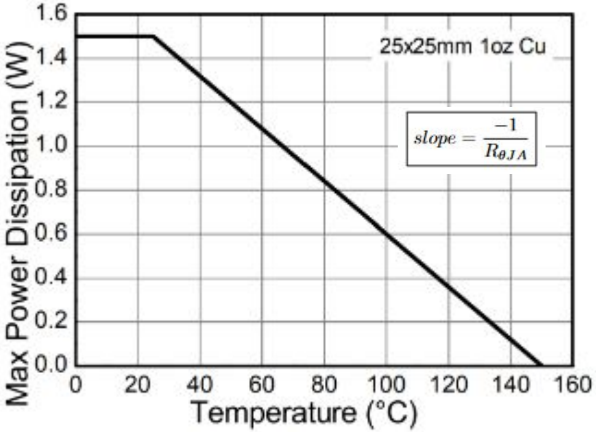


Figure 4: Derating curve

- $R_{\theta JA}$ is the thermal resistance from the junction to ambient, measured in °C/W.
- T_{junction} is the temperature at the junction of the transistor.

From graph , Thermal resistance is 83 'C/W

Estimation of doping

$$W_{BC} = \sqrt{\frac{2\epsilon_s\,(V_{in}+V_{CBO})}{q}\,(\frac{1}{N_{DB}}+\frac{1}{N_{AC}})}$$

$$W_{BC} \approx \sqrt{\frac{2\epsilon_s\,(V_{in}+V_{CBO})}{qN_{AC}}}\;;\; Assuming\ N_{DB} > 10N_{AC}$$

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	-120	V
Collector-Emitter Voltage	V_{CEO}	-120	V
Emitter-Base Voltage	V_{EBO}	-7	V
Continuous Collector Current	I_C	-800	mA
Peak Pulse Current (Note 6)	I_{CM}	-3	A
Base Current	I_B	-160	mA

To avoid Avalanche breakdown just at the boundary, $V_o + V_{CBO} = \frac{1}{2}E_{crit}W_{BC}$

Figure 9: Maximum Ratings of the device

Where, V_{CBO} = 120 V is much greater than Built in potential across base-collector $V_o \approx 0.7V$ & $E_{crit} \approx 5x10^5$ V/cm for silicon.Hence,

$$V_{CBO} = \frac{1}{2}\,(E_{crit}^2\frac{\epsilon_s}{q})(\frac{1}{N_{AC}})$$

Therefore, on substituting corresponding value we can estimate N_{AC}

$$\boxed{N_{AC} = 6.74 \times 10^{15}\ cm^{-3}}$$

Similarly,

$$W_{EB} \approx \sqrt{\frac{2\epsilon_s\,(V_o+V_{EB})}{qN_{DB}}}\;;\; Assuming\ N_{AE} > 10N_{DB}$$

Where, V_{EBO} = 7 V Built in potential across emitter-base $V_o \approx 0.8V \Rightarrow V_{EBO} + V_o \approx 7.8V$.Hence,

$$V_{EBO} + V_o = \frac{1}{2}\,E_{crit}^2\frac{\epsilon_s}{qN_{DB}}$$

$$\boxed{N_{DB} = 1.29 \times 10^{17}\ cm^{-3}}$$

$$\boxed{N_{AE} = 7 \times 10^{18}\ cm^{-3}}$$

$N_{AE} > 10N_{DB}$ assuming,

Current Gain (αf and β), Base width

From the h_{FE} Vs -I_C graph at $T = 25{\cdot}C$ we have,

$$\beta = 175 \;\; Since,\; \beta = \frac{\alpha_f}{1-\alpha_F} \;\Rightarrow \alpha_f = \frac{175}{176} = 0.9943$$

$$\alpha_f = \frac{I_C}{I_E} \approx \frac{I_{Cp}}{I_{Ep}+I_{En}} = B\gamma \qquad B = 1 - \frac{{W_B}^2}{2{L_p}^2}, where\; {L_p}^2 = D_P\tau_p \qquad \gamma = \left[1 + \frac{D_n W_B N_{DB}}{D_P W_E N_{AE}}\right]^{-}$$

Assuming $\gamma \approx 1$ as observed from its expression, from Base transport factor $B \approx 1 - \frac{{W_B}^2}{2{L_p}^2}$

$$\Rightarrow \frac{{W_B}^2}{2{L_p}^2} = 5.7 \times 10^{-3}$$

Typically, $L_p \approx\; 100\mu m\; to\; 300\mu m \;\Rightarrow W_B \approx\; 10.67\mu m\; to\; 30\mu m$, Assuming $L_p = 125\mu m$

$$\frac{{W_B}^2}{2{L_p}^2} = 5.7 \times 10^{-3} \Rightarrow W_B = 13.34\mu m$$

$\tau_d = \frac{{W_B}^2}{2D_p}$, generally $D_p \approx 5\; cm^2 s^{-1}\; to\; 20\; cm^2 s^{-1}$ Assuming $D_p = 15cm^2/s$ $\qquad \tau_d = 62ns \Rightarrow W_B = 13.63\mu m$

$\boxed{W_B = 13.7\mu m}$ which also ensures base is safe from Punch-through.

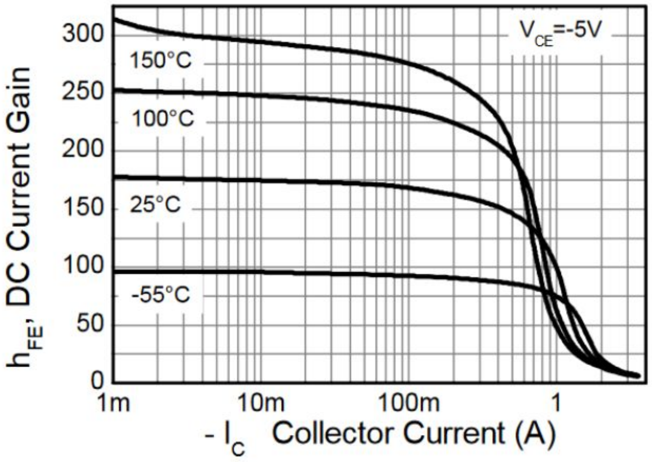


Figure 10: h_{FE} Vs -I_C

Cross-Sectional Area A & other parameters

From figure 8, $I_C = 2mA$ at $V_{EB} = 0.6V$ & T=25'C in forward bias,

$$I_C \approx I_E \ \& \ I_E = \frac{qAD_p{n_i}^2}{N_{DB}W_B} \exp\left(\frac{V_{EB}}{V_t}\right)$$

$$I_E = K \exp\left(\frac{V_{EB}}{V_t}\right), K = \frac{qAD_p{n_i}^2}{N_{DB}W_B} \Rightarrow K = 1.95 \times 10^{-13} A$$

hence, the cross-sectional area A is given by, $D_p \approx 5\ cm^2 s^{-1}\ to\ 20\ cm^2 s^{-1}$ Assuming $D_p = 15cm^2/s$

$$A = \frac{kN_{DB}}{qn_i^2}\left(\frac{W_B}{D_P}\right) \Rightarrow \boxed{A = 6.5mm^2}$$

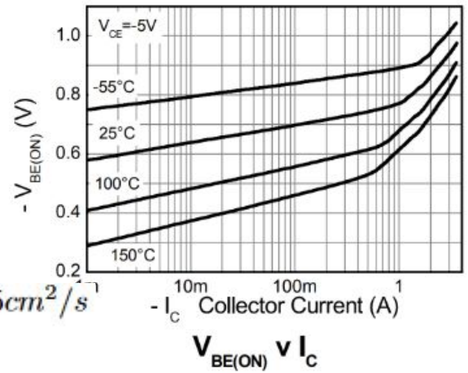


Figure 8: $V_{BE(ON)}$ vs. I_C

$$\boxed{f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)}} \qquad g_m = \frac{\beta_o}{r_\pi}.$$

From graph of h_{FE} vs. I_C, at 25°C, $\beta = 175$. Also,

$$r_\pi = \frac{V_A}{I_C} \Rightarrow \boxed{r_\pi = 2.45K\Omega}$$

$$(C_\pi + C\mu) = \frac{g_m}{2\pi f_T} \Rightarrow \boxed{C_{\text{parasitic}} = 71pF}$$

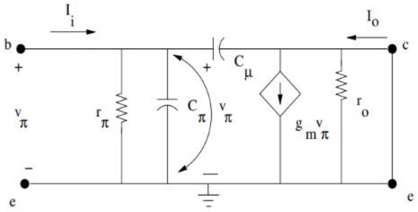
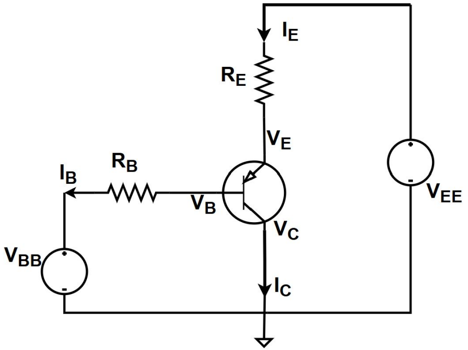


Figure 11: Circuit used for f_T calculation of transistor

Circuit Diagram and Parameters calculations



Voltage follower

From h_{FE} vs. I_C plot as shown in figure 8,

$$\boxed{\beta = 175}$$

From $V_{BE(ON)}$ vs. I_C plot, assuming forward active mode of operation

$$V_{EB(ON)} = 0.7V \Rightarrow I_C = 100mA.$$

$$\Rightarrow I_B = \frac{I_C}{\beta} \approx 0.57mA$$

Also, using KCL,

$$I_E = I_C + I_B \approx I_C = 100mA$$

$$\Rightarrow \frac{I_E}{\beta} = \frac{V_{\mathrm{EE}} - V_E}{\beta R_E} = \frac{V_{\mathrm{BB}} - (V_E - V_{EB})}{R_B} = I_B$$

Rearranging terms to get the expression for V_E,

$$V_E = \frac{\beta R_E(V_{\mathrm{BB}} + V_{EB}) - V_{\mathrm{EE}} R_B}{\beta R_E - R_B}$$

Let's say, we wish to obtain V_{CE} = -5V for forward active mode $\Rightarrow V_E = 5V \Rightarrow V_B = 4.3V, V_{EB} = 0.7V$.

Let's choose V_{BB} = 10V.

$$\Rightarrow R_B = \frac{V_{\mathrm{BB}} - V_B}{I_B} = 10k\Omega$$

Similarly, let's choose V_{EE} = 25V.

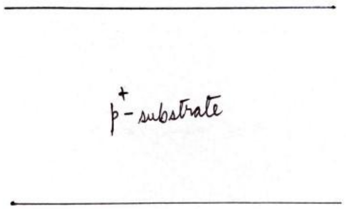
$$\Rightarrow R_E = \frac{V_{\mathrm{EE}} - V_E}{I_C} = 200\Omega$$

Hence, for the values $\beta = 175, R_E = 0.2k\Omega, R_B = 10k\Omega$,

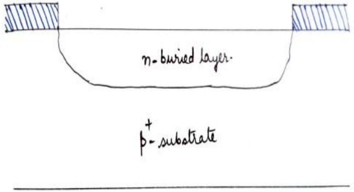
$$\boxed{V_{\mathrm{CE}} = -5V, I_E = 100mA}$$

This fixes I_B and V_B as well.

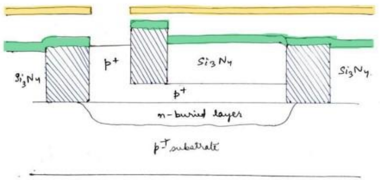
Fabrication Process Overview



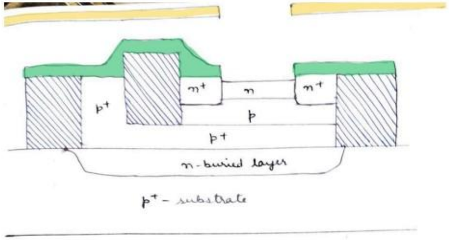
1. Selecting p+-Si as substrate



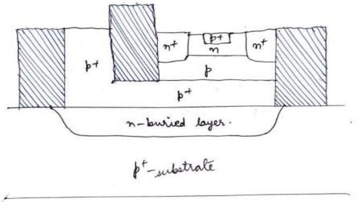
2. Forming the n-buried Si layer by CVD and CMP method



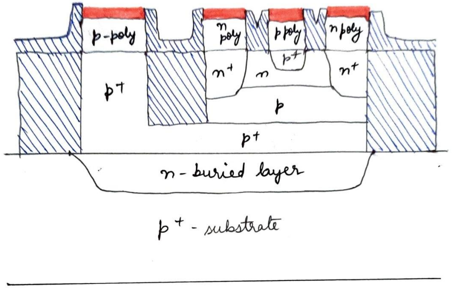
3. Forming the sub-collector region deposition followed by the isolation trenching



4. Deposition of the Base region followed after collector region



5. Deposition of the emitter Layer

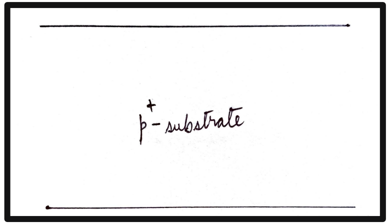


6. Formation of the metal contacts post deposition of n-poly and p-poly Si layer

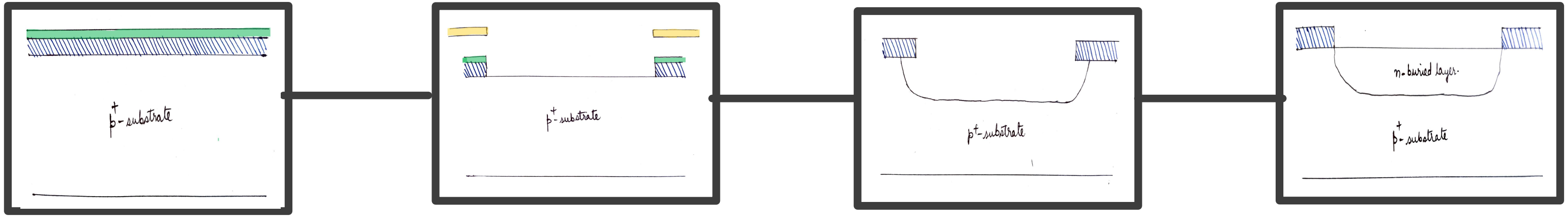
Substrate Selection

P-substrate requires :

- High resistivity (25 Ω-cm to 50 Ω-cm) → doping level : 10^{15} cm^{-3}
- Si has (100) orientation → better interfaces, lesser defects



N-well formation



Thermal oxidation

PR application

Photolithography

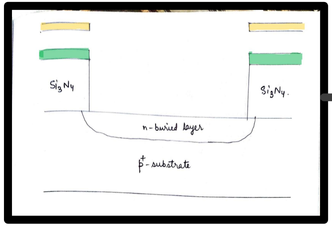
Etching of SiO_2

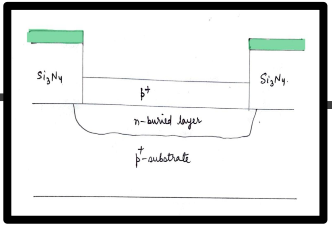
Etching of Si

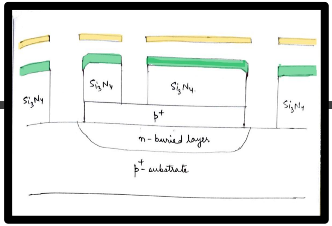
(removal of PR also)

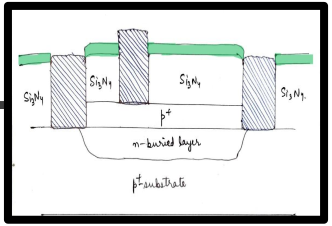
Formation of n-buried layer using CVD

Isolating the Active Regions









Si_3N_4 layer using CVD

Apply PR, lithography

Etching of Si_3N_4

Growth of p^+ sub collector region using CVD

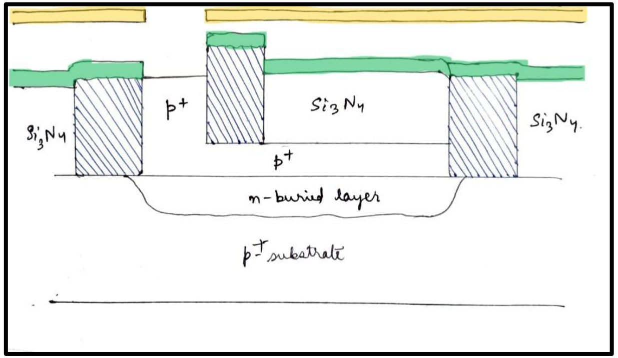
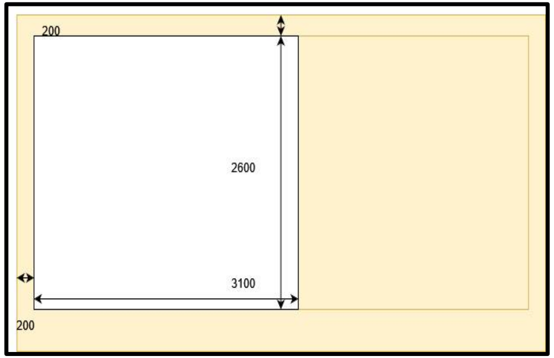
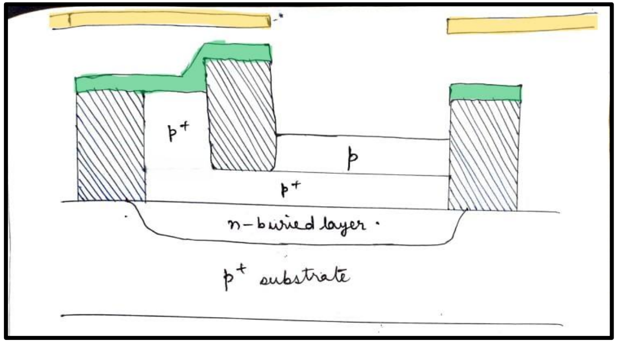
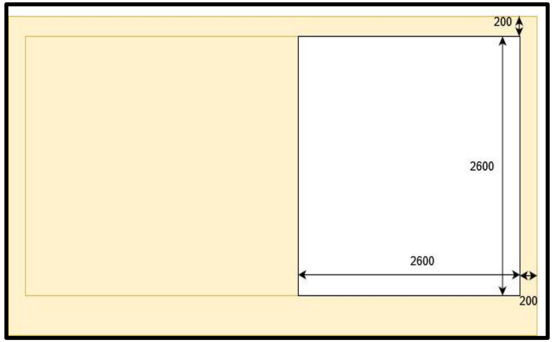
Regrowth of Si_3N_4

Lithography to expose isolation plugs of SiO_2

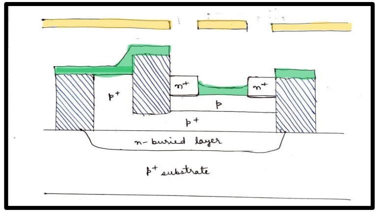
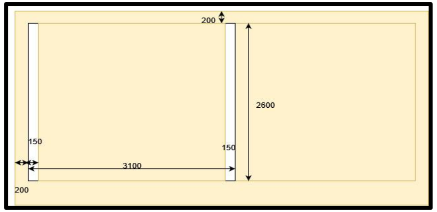
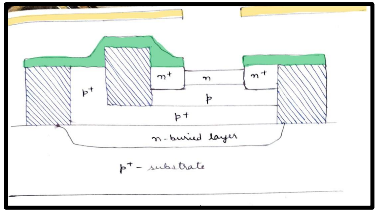
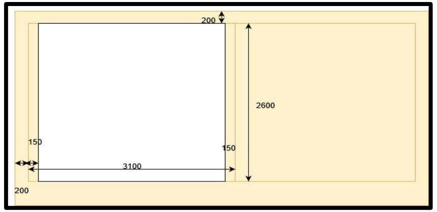
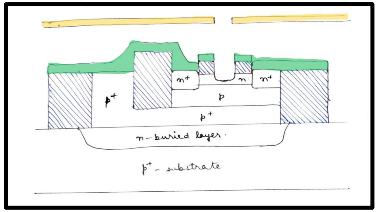
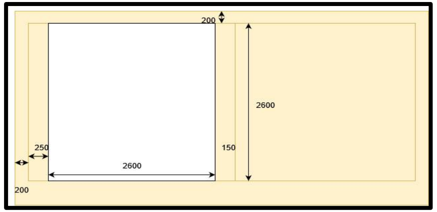
Growth of SiO_2 regions using CVD

(these act as isolation for active regions)

PNP Region Formation

Part of Device	Lateral view	Top view of Mask used
Sub - Collector		
Collector		

PNP Region Formation

Part of Device	Lateral view	Top view of Mask used
n+ region		
Base (n region)		
Emitter (p^+ region)		

Resistor Fabrication

CSA of resistor

$$L = \frac{R \cdot A}{\rho}$$

Area = 500 um^2

Resistivity = 0.1 ohm-cm for a $conc^n$ of $10^{17} cm^{-3}$

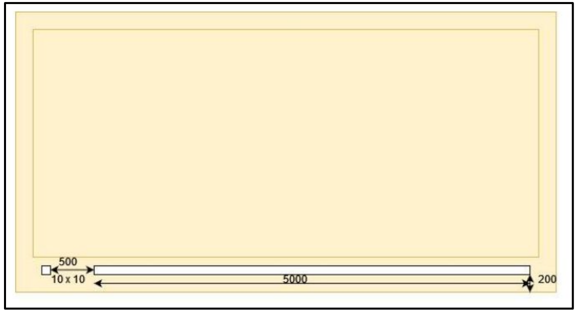
<u>For R = 200 ohms</u>

$$L = \frac{200\,\Omega \cdot 5 \times 10^{-6}\,\mathrm{cm}^2}{0.1\,\Omega \cdot \mathrm{cm}} = 100\,\mu\mathrm{m}$$

<u>For R = 10k ohms</u>

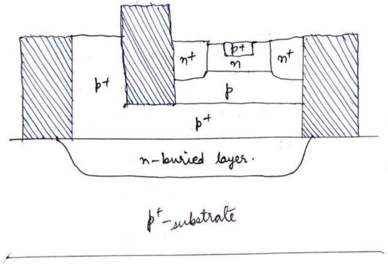
$$L = \frac{10,000\,\Omega \cdot 5 \times 10^{-6}\,\mathrm{cm}^2}{0.1\,\Omega \cdot \mathrm{cm}} = 5000\,\mu\mathrm{m}$$

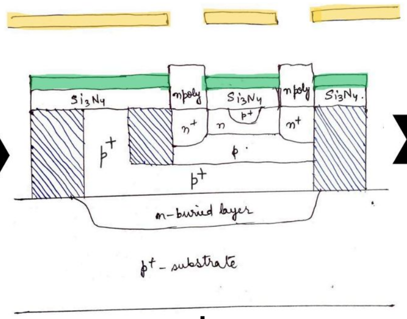
Followed by etching of the SiO_2 mask and Silicon wafer, the resistance is formed by LPCVD on the substrate with AsH_3 as impurity.

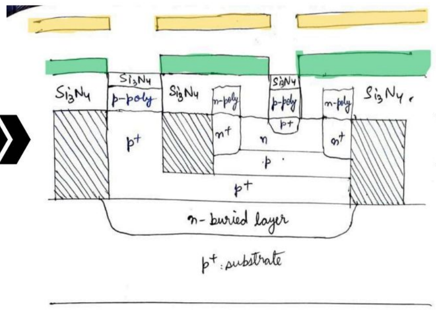


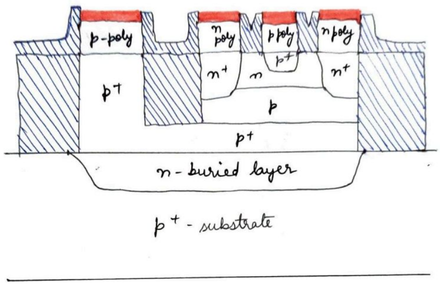
<u>Mask for Resistance Formation</u>

Metal Contact Formation









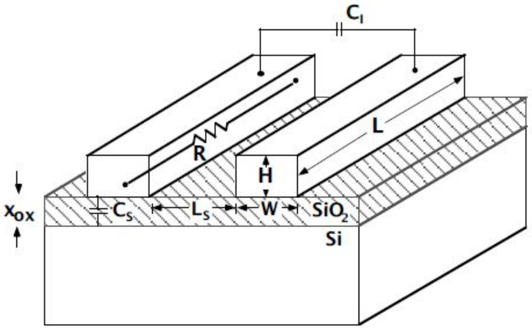
CVD of Si_3N_4 →
PR application →
Photolithography →
Etching of Si_3N_4 →
CVD n-poly Si

CVD of Si_3N_4 →
PR application →
Photolithography →
Etching of Si_3N_4 →
CVD p-poly Si

Deposition of Al metal contacts - DC magnetron Bias Sputtering

InterConnects

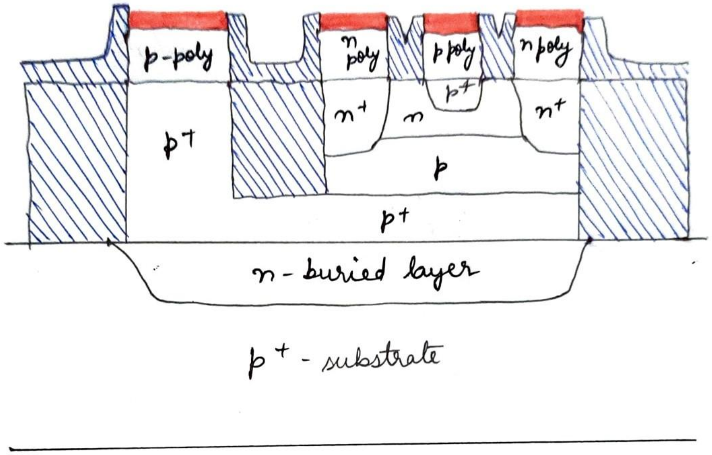
SiO_2 is deposited over the top to separates the active regions from the global interconnect, and electrical contact is made between the interconnect and the active regions in the silicon through openings in that dielectric layer.



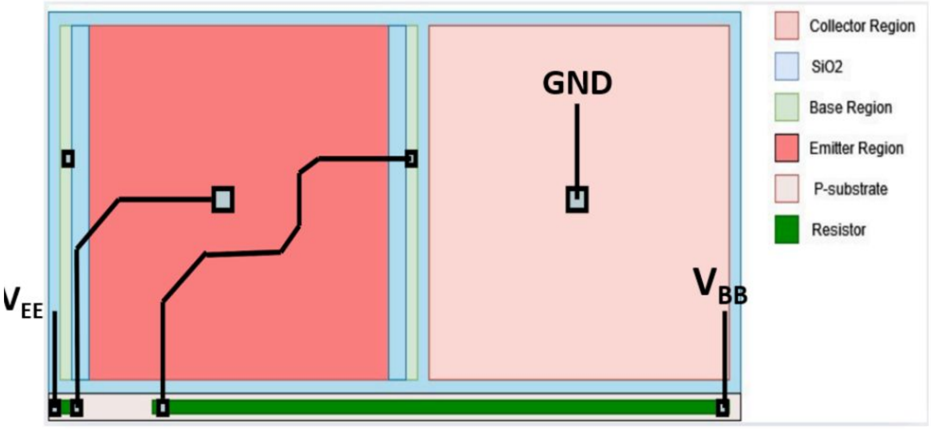
Interconnect delay = 0.89*RC

where, $R = \rho \frac{L}{WH}$ and $C = K_{ox}\varepsilon_o \frac{WL}{X_{ox}}$

Final View of the Proposed Structure



Lateral View



Top View

THANK YOU!