Pre-Report
2DA1201Y PNP TRANSISTOR

Adrija Bera	Pratyush Amrit	Devendra Kumar Saini	Aniket Sen
210071	210762	241040608	210134

Abstract

Analysis and extraction of model parameters and performance characterization of 2DA1201Y PNP transistor.

1 Theoretical Expressions

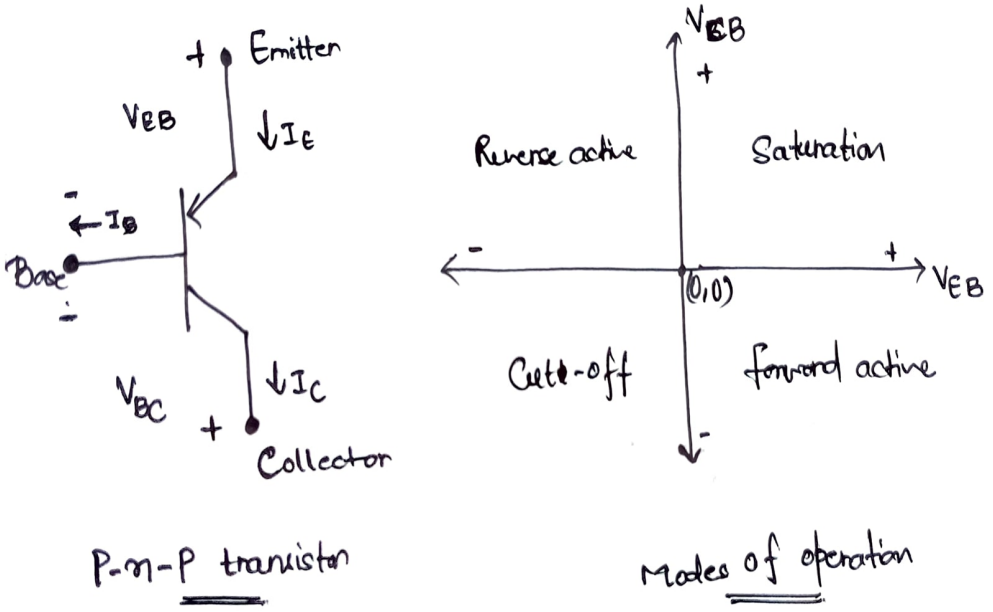

Figure 1: Schematic of P-N-P BJT & Regions of the modes Of Operation

For the P-N-P transistor, as shown in Figure 2, we have:

- N_{AE} = Doping concentration of acceptor atoms in the emitter region.
- N_{DB} = Doping concentration of donor atoms in the base region.
- N_{AC} = Doping concentration of acceptor atoms in the collector region.

In all of the further discussions we have assumed $N_{AE} >> N_{DB} >> N_{AC}$

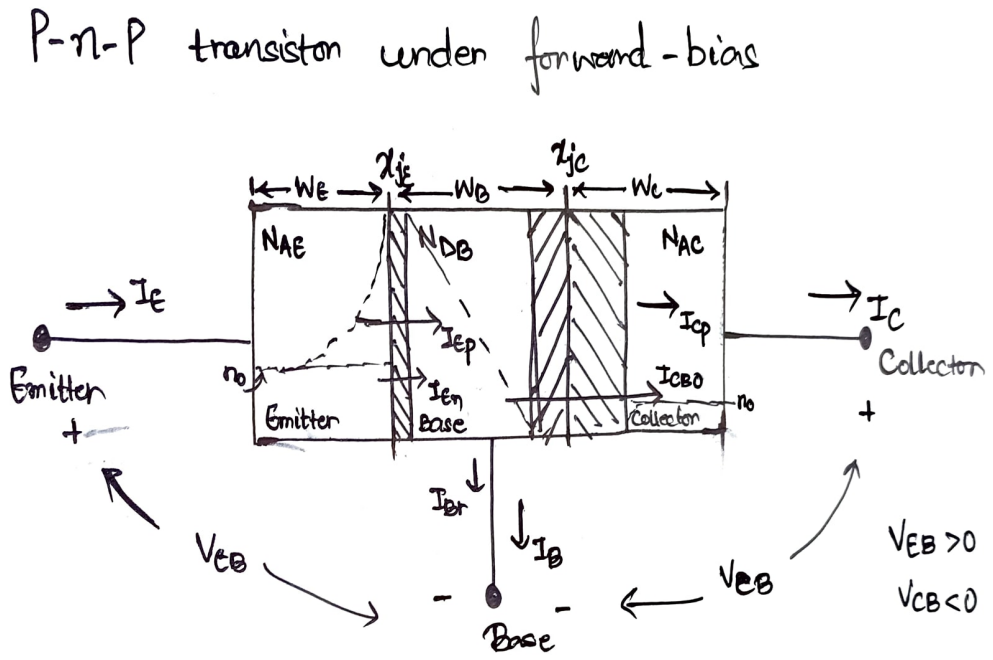

Figure 2: Working of PN-P BJT in forward active mode

In the forward active mode of operation of the P-N-P BJT, when $V_{EB} > 0$ and $V_{CB} < 0$, we will have the injection of electrons into the emitter from the base and holes into the base from the emitter. The electron concentration at the emitter-base depletion layer surface is given by:

- n_p = Concentration of electrons injected from the base into the emitter at the depletion layer surface.

$$n_p = n_{po} \exp\left(\frac{V_{EB}}{V_t}\right); n_{po} = \frac{{n_i}^2}{N_{AE}} \tag{1}$$

where V_t is the thermal voltage & n_i is the intrinsic concentration of carrier at given temperature for all expressions. Therefore, excess electron concentration at depletion layer surface after injection on emitter side is given by,

$$\Delta n_p = n_p - n_{po} = n_{po}[\exp\left(\frac{V_{EB}}{V_t}\right) - 1] \tag{2}$$

- p_n = Concentration of holes injected from the emitter into the base at the depletion layer surface.

$$p_n = p_{no} \exp\left(\frac{V_{EB}}{V_t}\right); p_{no} = \frac{{n_i}^2}{N_{DB}} \tag{3}$$

Since, the Collector-Base junction is under reverse bias, due to carrier extraction at surface, the hole concentration at surface on base side is given by :

$$p_{nCB} = p_{no} \exp\left(\frac{V_{CB}}{V_t}\right); V_{CB} < 0 \Rightarrow p_{nCB} \approx 0 \tag{4}$$

The base width (W_E) of the transistor is kept much smaller than the diffusion length (L_p) of the holes, so that all the holes injected from emitter side travels through the base region with minimum injection resulting in a Collector current much greater than reverse saturation current of Base-Collector such that, $I_C \approx I_E$.

We can define 5 main components of current in BJT as shown in figure 2.

- I_{Ep} = Current due to hole injection on Base side from Emitter.
- I_{En} = Current due to electron injection on Emitter side from Base.
- I_{Br} = Current due to recombination of holes in base region.
- I_{Cp} = Current due to Collection of holes from base region.
- I_{CBO} = Reverse saturation current across Base-Collector.

2 Current Components and Device Parameters

2.1 Emitter Current (I_E)

The total emitter current is composed of two components: the hole current injected from the emitter into the base (I_{Ep}) and the electron current injected from the base into the emitter (I_{En}). Thus, the emitter current is:

$$I_E = I_{Ep} + I_{En} \tag{5}$$

The diffusion current is given by Fick's first law of diffusion:

$$J_p(x) = -qD_p \frac{dp_n(x)}{dx} \tag{6}$$

where $J_p(x)$ is the hole current density at a distance x into the base, D_p is the diffusion coefficient of holes, and $p_n(x)$ is the hole concentration at distance x from the depletion surface for cross-sectional area A.

$$I_{Ep} = J_p(0)A = qAD_p \left.\frac{dp_n(x)}{dx}\right|_{x=0} \tag{7}$$

From current-continuity equation in steady-state conditions,

$$\frac{d^2\Delta p_n(x)}{dx^2} = \frac{\Delta p_n(x)}{L_p^2} \tag{8}$$

where L_p is the diffusion length of holes in the base. The solution to this differential equation for a uniform base width W_B and boundary conditions at the base-emitter and base-collector junctions is:

$$\Delta p_n(x) = \Delta p_{no} \exp\left(\frac{-x}{L_p}\right); \Delta p_{no} = \frac{{n_i}^2}{N_{DB}}[\exp\left(\frac{V_{EB}}{V_t}\right) - 1] \tag{9}$$

$$\Delta p_n(0) = \Delta p_{no} = \frac{{n_i}^2}{N_{DB}}[\exp\left(\frac{V_{EB}}{V_t}\right) - 1] \tag{10}$$

Simplification for $W_B \ll L_p$ from Taylor's expansion,

$$\Delta p_n(x) = \Delta p_{no}[1 - \frac{x}{W_B}] \tag{11}$$

$$\Rightarrow I_{Ep} = qAD_p \frac{\Delta p_n(0)}{W_B} = \frac{qAD_p {n_i}^2}{N_{DB}W_B}[\exp\left(\frac{V_{EB}}{V_t}\right) - 1] \tag{12}$$

$$I_{Ep} \approx \frac{qAD_p {n_i}^2}{N_{DB}W_B} \exp\left(\frac{V_{EB}}{V_t}\right) \tag{13}$$

Similarly I_{En} can be found as,

1. For short length Emitter i.e Emitter thickness W_E « electron diffusion length on emitter side L_n,

$$I_{En} \approx \frac{qAD_n {n_i}^2}{N_{AE} W_E} \exp\left(\frac{V_{EB}}{V_t}\right) \tag{14}$$

2. for Long length Emitter

$$I_{En} \approx \frac{qAD_n {n_i}^2}{N_{AE} L_n} \exp\left(\frac{V_{EB}}{V_t}\right) \tag{15}$$

Final expression for emitter current, $I_E = I_{Ep} + I_{En}$

$$I_E = \frac{qAD_n {n_i}^2}{N_{AE} W_E} \exp\left(\frac{V_{EB}}{V_t}\right) + \frac{qAD_p {n_i}^2}{N_{AE} L_n} \exp\left(\frac{V_{EB}}{V_t}\right)$$

Since $N_{AE} >> N_{DB} \Rightarrow I_E \approx I_{Ep}$ hence,

$$\boxed{I_E \approx I_{Ep} \approx \frac{qAD_p {n_i}^2}{N_{DB} W_B} \exp\left(\frac{V_{EB}}{V_t}\right)} \tag{16}$$

2.2 Base Current (I_B)

The base current is the sum of the current due to recombination of holes in the base region (I_{Br}) and the electron current injected into the emitter from the base minus the collector current:

$$I_B = I_{Br} + I_{En} - I_{CBO} \tag{17}$$

Base current can be found from the charge control model:

$$I_B = \frac{Q_p}{\tau_p} = \frac{qAW_B p_n}{2\tau_p} = \frac{qAW_B p_{n0}}{2\tau_p} \exp\left(\frac{V_{EB}}{V_T}\right)$$

$$\boxed{I_B = \frac{qAW_B {n_i}^2}{2N_{DB}\tau_p} \exp\left(\frac{V_{EB}}{V_T}\right)} \tag{18}$$

2.3 Collector Current (I_C)

The collector current is due to the collection of holes injected into the base and reverse saturation current which is very small.

$$I_C = I_{cp} + I_{CBO}$$

$$I_C \approx I_{cp} \tag{19}$$

2.4 Base Transport Factor (B)

The base transport factor α_T is defined as the fraction of holes injected into the base that reach the collector without recombining.

$$B = \frac{I_{Cp}}{I_{Ep}} = \frac{I_{Ep} - I_B}{I_{Ep}} = 1 - \frac{I_B}{I_{Ep}}$$

$$B = 1 - \frac{{W_B}^2}{2{L_p}^2}, where\ {L_p}^2 = D_P \tau_p \tag{20}$$

where W_B is the base width and L_p is the diffusion length of holes in the base.

2.5 Emitter Efficiency (γ)

The emitter efficiency γ is defined as the ratio of the hole current injected into the base to the total emitter current:

$$\gamma = \frac{I_{Ep}}{I_E} = \frac{I_{Ep}}{I_{Ep} + I_{En}} = \left[1 + \frac{I_{En}}{I_{Ep}}\right]^{-1}$$

$$\gamma = \left[1 + \frac{D_n W_B N_{DB}}{D_P L_p N_{AE}}\right]^{-1} \text{(long emitter)} \tag{21}$$

$$\gamma = \left[1 + \frac{D_n W_B N_{DB}}{D_P W_E N_{AE}}\right]^{-1} \text{(short emitter)} \tag{22}$$

2.6 Current Gain (α_f and β)

The current gain α_f is the ratio of the collector current to the emitter current:

$$\alpha_f = \frac{I_C}{I_E} \approx \frac{I_{Cp}}{I_{Ep} + I_{En}} = B\gamma \tag{23}$$

The common-emitter current gain β_f is the ratio of the collector current to the base current:

$$\beta_f = \frac{I_C}{I_B} = \frac{I_C}{I_E - I_C} = \frac{\alpha_f}{1 - \alpha_f} \tag{24}$$

2.7 Switching Characteristics

We have seen that BJT does not respond instantaneously to the fast-switching signals. This is because the BJT speed of response is limited mainly by the storage or diffusion capacitance, which accompanies the storage minority carriers in the base. For pnp, the hole current is the majority current, therefore excess hole current is related to:

$$J_C = qD_p\frac{dp'}{dx},\ I_C = AqD_p\frac{dp'}{dx}, \frac{dp'}{dx} = -\frac{p'(0)}{W_B},\ I_C = \frac{qAD_p p'(0)}{W_B} \tag{25}$$

The excess minority charge carriers charge stored in the base is given by

$$Q_B = concentration * Volume = (\frac{p'(0)W_B}{2})qA \tag{26}$$

Now taking the ratio of Q_B and I_C, we get

$$\tau_f = \frac{{W_B}^2}{2D_p} = t_d \tag{27}$$

This is known as the transit time or delay time (t_d) of the BJT Transistor where τ_f is defined as 62ns in the datasheet as shown in figure 3.

We can estimate the base width of the transistor from this equation :

$$W_B = \sqrt{2D_p t_d} \tag{28}$$

We also have been given some data through which we can calculate Turn-OFF time and Turn-ON time.

Delay Time	$t_{(d)}$	-	62	-	ns
Rise Time	$t_{(r)}$	-	50	-	ns
Storage Time	$t_{(s)}$	-	440	-	ns
Fall Time	$t_{(f)}$	-	42	-	ns

Figure 3: Transit timing

Turn-off time(T_{off}) = Storage time (t_s) + fall time (t_f) = 482ns
Turn-off time(T_{off}) = Delay time (t_d) + Rise time (t_r) = 112ns

3 Parameter extraction from plots

3.1 Power limit variation with temperature

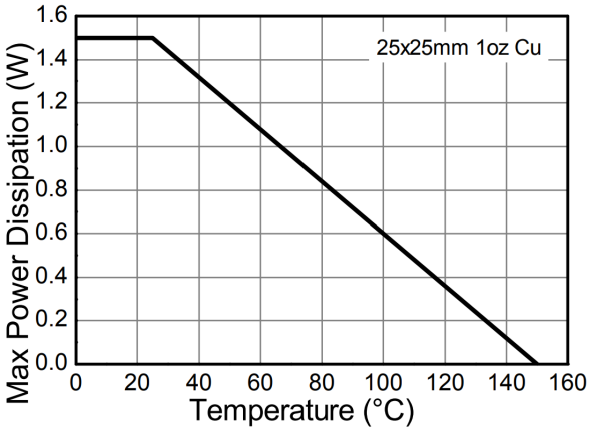

Figure 4: Derating curve

The total junction temperature (T_{junction}) of the BJT is related to the ambient temperature and the total power dissipation by the thermal resistance ($R_{\theta JA}$) from the junction to ambient:

$$T_{\text{junction}} = T_{\text{ambient}} + (P_{\text{total}} \times R_{\theta JA})$$
$$\Rightarrow P_{\text{total}} = \frac{T_{\text{ambient}} - T_{\text{junction}}}{R_{\theta JA}}$$
$$\boxed{slope = \frac{-1}{R_{\theta JA}}}$$

where:

- $R_{\theta JA}$ is the thermal resistance from the junction to ambient, measured in °C/W.
- T_{junction} is the temperature at the junction of the transistor.

Here, P_{total} has maximum = 1.5 W and T_{junction} is limited by 150°C.

3.2 Safe Operating Area plots

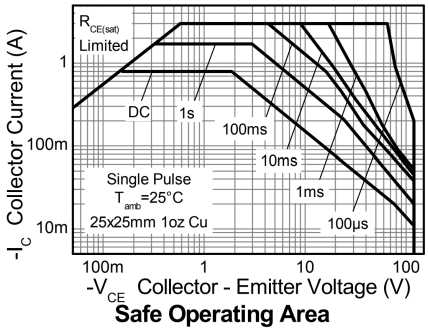

Figure 5: SOA at T_{amb} = 25°C

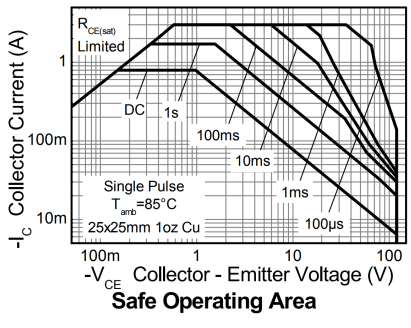

Figure 6: SOA at T_{amb} = 85°C

The following are the operating limits for a bipolar junction transistor:

- Saturation mode limited by $R_{CE(\text{sat})}$
- current limit of 0.8A : $I_C = I_{C\text{max}}$
- dissipation limit of 1.5W, thermal breakdown : $I_C V_{CE} = P_{\text{max}}$
- limit given by the secondary breakdown : $I_C V_{CE}^{\alpha} = \text{const}$
- voltage limit of 120V : $V_{CE} = V_{CE\text{max}}$

In this case, power limit changes (from derating curve), hence shorter flat portion. Higher ambient temperature results in multiple breakdown points.

3.3 Estimation of Early Voltage, V_A

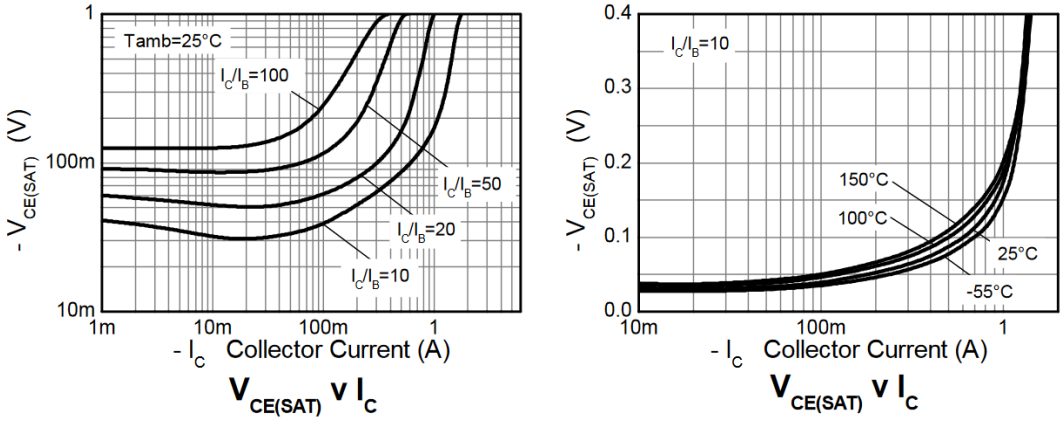

Figure 7: $V_{\text{CE(sat)}}$ as a function of I_C

From figure for $V_{\text{CE(sat)}}$ as a function of I_C we can estimate the early voltage V_A by finding the negative intercept.
The relation between V_{CE} and I_C at 25°C is given by

$$V_{CE} = 100 I_C - 245$$

$$\boxed{V_A = 245V}$$

3.4 Estimation of ideality factor, n

since $I_C = I_0 \exp \frac{V_{EB}}{NV_T}$ taking log both sides $\Rightarrow V_{EB} = 2.303 n V_T \log I_C - 2.303 n V T \log I_0$, comparing this with $y = mx + c$ we have,

$$m = 2.303 n V_T,\ y = V_{EB} \& \ x = \log I_C$$

From Figure 8, At $25^0 C$ Temperature we took two-point (2 mA, 0.6) and (100 mA, 0.7)$\Rightarrow$ m=0.058859 and n= 0.98 and similarly for at $100^0 C$ two points (1 mA, 0.4), (300 mA, 0.6); m= 0.0807 and n=1.07, therefore

$$\boxed{Ideality factor\ n \approx 1}$$

3.5 Estimation of doping and physical parameters

We know the depletion width across base-collector in reverse bias voltage V_{CBO} is given by,

$$W_{BC} = \sqrt{\frac{2\epsilon_s\ (V_{in} + V_{CBO})}{q}\ (\frac{1}{N_{DB}} + \frac{1}{N_{AC}})} \tag{29}$$

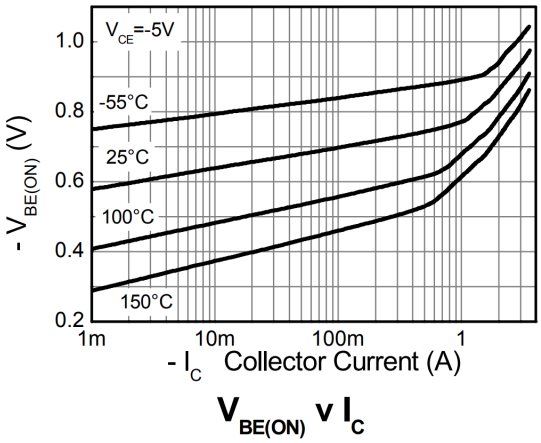

Figure 8: $V_{BE(ON)}$ vs. I_C

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	-120	V
Collector-Emitter Voltage	V_{CEO}	-120	V
Emitter-Base Voltage	V_{EBO}	-7	V
Continuous Collector Current	I_C	-800	mA
Peak Pulse Current (Note 6)	I_{CM}	-3	A
Base Current	I_B	-160	mA

Figure 9: Maximum Ratings of the device

$$W_{BC} \approx \sqrt{\frac{2\epsilon_s\,(V_{in}+V_{CBO})}{qN_{AC}}}\;;\; Assuming\; N_{DB} > 10N_{AC} \tag{30}$$

To avoid Avalanche breakdown just at the boundary,

$$V_o + V_{CBO} = \frac{1}{2}E_{crit}W_{BC} \tag{31}$$

Where, V_{CBO} = 120 V is much greater than Built in potential across base-collector $V_o \approx 0.7V$ & $E_{crit} \approx 5x10^5$ V/cm for silicon.Hence,

$$V_{CBO} \approx \frac{1}{2}E_{crit}W_{BC} \tag{32}$$

Using eq. 30 & eq. 32, we have

$$V_{CBO} = \frac{1}{2}\,(E_{crit}^2\frac{\epsilon_s}{q})(\frac{1}{N_{AC}}) \tag{33}$$

Therefore, on substituting corresponding value we can estimate N_{AC}

$$\boxed{N_{AC} = 6.74 \times 10^{15}\; cm^{-3}} \tag{34}$$

Again, Depletion width W_{EB} across emitter-base is given by,

$$W_{EB} = \sqrt{\frac{2\epsilon_s\,(V_{in}+V_{EB})}{q}\,(\frac{1}{N_{AE}}+\frac{1}{N_{DB}})} \tag{35}$$

$$W_{EB} \approx \sqrt{\frac{2\epsilon_s\,(V_o + V_{EB})}{qN_{DB}}}\;;\; Assuming\; N_{AE} > 10N_{DB} \tag{36}$$

To avoid Avalanche breakdown just at the boundary,

$$V_o + V_{EBO} = \frac{1}{2} E_{crit} W_{EB} \tag{37}$$

Where, V_{EBO} = 7 V Built in potential across emitter-base $V_o \approx 0.8V \Rightarrow V_{EBO} + V_o \approx 7.8V$.Hence, from eq. 36 & eq. 37 we have,

$$V_{EBO} + V_o = \frac{1}{2}\, E_{crit}^2 \frac{\epsilon_s}{qN_{DB}} \tag{38}$$

On solving the above equation we can estimate N_{DB},

$$\boxed{N_{DB} = 1.29 \times 10^{17}\; cm^{-3}} \tag{39}$$

since, N_{AE} > $10N_{DB}$ assuming,

$$\boxed{N_{AE} = 7 \times 10^{18}\; cm^{-3}} \tag{40}$$

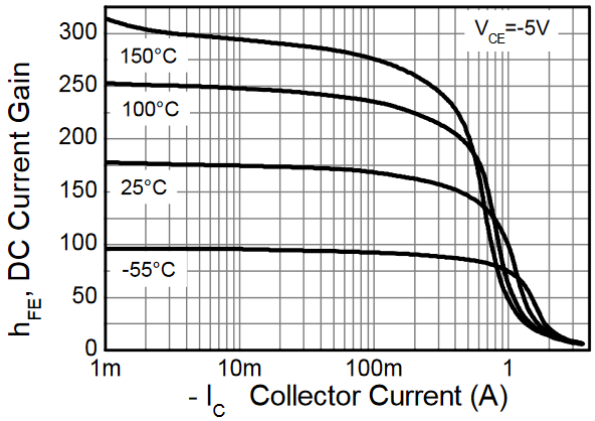

Figure 10: h_{FE} Vs -I_C

From the h_{FE} Vs -I_C graph at $T = 25{\cdot}C$ we have,

$$\beta = 175\;\; Since,\; \beta = \frac{\alpha_f}{1 - \alpha_F} \;\Rightarrow \alpha_f = \frac{175}{176} = 0.9943$$

assuming γ = 1, We have transpost base factor B = α_f = 0.9943, From eq.20

$$\beta = 175\;\; Since,\; \beta = \frac{\alpha_f}{1 - \alpha_F} \;\Rightarrow \alpha_f = \frac{175}{176} = 0.9943 \tag{41}$$

Assuming $\gamma \approx 1$ as observed from its expression, from Base transport factor $B \approx 1 - \frac{{W_B}^2}{2{L_p}^2}$

$$\Rightarrow \frac{{W_B}^2}{2{L_p}^2} = 5.7 \times 10^{-3}$$

Typically, $L_p \approx\ 100\mu m\ to\ 300\mu m\ \Rightarrow W_B \approx\ 10.67\mu m\ to\ 30\mu m$, Assuming $L_p = 125\mu m$

$$\frac{{W_B}^2}{2{L_p}^2} = 5.7 \times 10^{-3} \Rightarrow W_B = 13.34\mu m$$

Also, from Delay time/ Transit time τ_d as given in data sheet from figure 3, We can estimate base-width W_B by $\tau_d = \frac{{W_B}^2}{2D_p}$, generally $D_p \approx 5\ cm^2s^{-1}\ to\ 20\ cm^2s^{-1}$ Assuming $D_p = 15cm^2/s$ we have,

$$\tau_d = 62ns \Rightarrow W_B = 13.63\mu m$$

From both of the above conditions we can estimated value of Base width, $\boxed{W_B = 13.7\mu m}$ which also ensures base is safe from Punch-through.

Now, To find Emitter width W_E & Collector width W_C, the widths should be greater than depletion layer width x_{EB}, x_{CB} in the respective regions when maximum reverse biased voltage is applied, since,

$$x_{EB} = \frac{N_{DB}}{N_{AE} + N_{DB}} W_{EB} = 18.4pm \Rightarrow W_E > 18.4pm$$

Similarly,

$$x_{CB} = \frac{N_{DB}}{N_{AC} + N_{DB}} W_{BC} = 10.5\mu m \Rightarrow W_C > 10.5\mu m$$

Hence,

$$\boxed{W_E = 25\mu m\ \&\ W_C = 40\mu m} \tag{42}$$

From figure 8, $I_C = 2mA$ at $V_{EB} = 0.6V$ & T=25'C in forward bias,

$$I_C \approx I_E\ \&\ I_E = \frac{qAD_p{n_i}^2}{N_{DB}W_B} \exp\left(\frac{V_{EB}}{V_t}\right)$$

$$I_E = K \exp\left(\frac{V_{EB}}{V_t}\right), K = \frac{qAD_p{n_i}^2}{N_{DB}W_B} \Rightarrow K = 1.95 \times 10^{-13}A$$

hence, the cross-sectional area A is given by,

$$A = \frac{kN_{DB}}{qn_i^2}(\frac{W_B}{D_P}) \Rightarrow \boxed{A = 6.5mm^2}$$

3.6 Estimation of Parasitic Capacitance at Base

f_T is defined as the frequency at which the magnitude of the short-circuit current gain is unity.

$$\boxed{f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)}}$$

where $g_m = \frac{\beta_o}{r_\pi}$.

From datasheet, typical value of f_T = 160MHz at test conditions of I_C = 100mA, V_{EC} = 5V.

From graph of h_{FE} vs. I_C, at 25°C, β = 175. Also,

$$r_\pi = \frac{V_A}{I_C} \Rightarrow \boxed{r_\pi = 2.45K\Omega}$$

$$(C_\pi + C\mu) = \frac{g_m}{2\pi f_T} \Rightarrow \boxed{C_{\text{parasitic}} = 71pF}$$

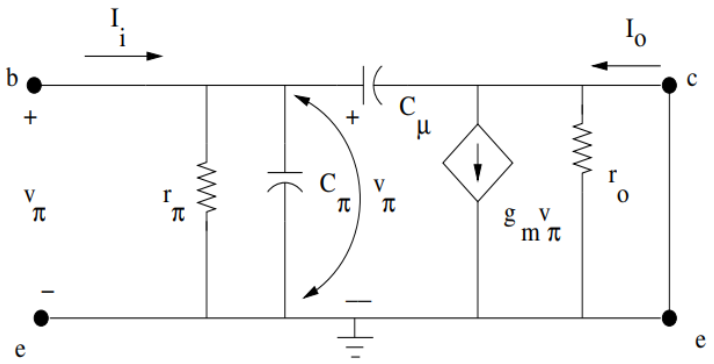

Figure 11: Circuit used for f_T calculation of transistor

4 Device Structure of PNP BJT

Let us review a simplified version of a double polysilicon, self-aligned p-n-p Si BJT. This is the most commonly used, state-of-the-art technique for making BJTs for use in an IC. We will be discussing the essence of each part in detail.

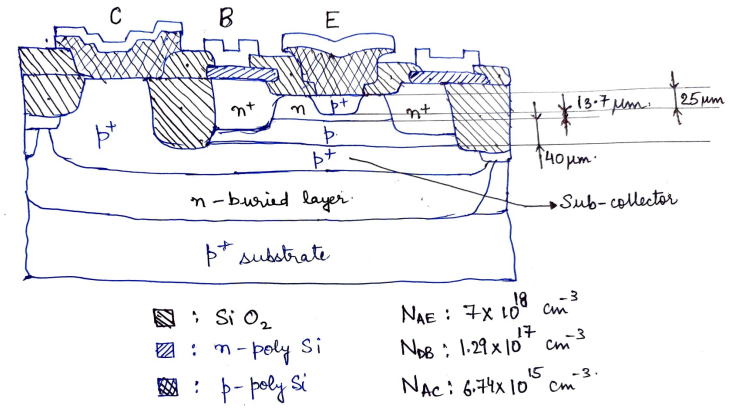

Figure 12: Cross-Sectional View of the proposed PNP BJT

The typical structure of a pnp BJT with a p-substrate and sub-collector might look like this from top to bottom:

1. p^+ **Emitter:** Injects holes into the base.
2. **n Base:** Allows the flow of holes to the collector.
3. **p Collector:** Collects the holes that have passed through the base.
4. p^+ **Sub-Collector:** Located beneath the collector region, providing enhanced collection and support for the collector.

4.1 p^+ Sub-Collector Region

The sub-collector is an additional p^+-type region located beneath the collector region of a pnp BJT. It guarantees a **low collector series resistance path** when it is connected subsequently to the collector ohmic contact.

4.2 Deep n-well Region

This acts as an isolation layer between the sub-collector and the substrate otherwise integration would be difficult as for any substrate, the junction would become forward-biased, and thus, a requirement of n-region is required between them.
With the introduction of Deep n-well, there is a possibility of parasitic PNP bjt where the n-well acts as a base. To tackle that, we would be using a deep n-well region (high base width) that would help in reducing the effect of parasitics.

4.3 P-channel stops

In a typical BJT, the base region and the surrounding collector can experience an electric field (due to the bias) that can induce inversion in the p-type locally into the n-type, creating a conductive path for electrons near the surface, which would act like a **parasitic MOSFET**. This unwanted inversion can lead to leakage currents or even parasitic devices that interfere with the intended operation of the BJT. Heavy doping in the p-channel stop region increases the hole concentration and makes it difficult for an electric field to invert the region, thus preventing the formation of parasitic channels.

4.4 SiO_2

SiO_2 is used as a field oxide to isolate different components of the transistor. This helps to

- Prevent leakage currents between adjacent devices or between different regions within the same device.
- Reduce parasitic capacitances, which would otherwise degrade the speed and performance of high-frequency devices.

SiO_2 also serves as a protective layer against contaminants, such as moisture or dust, which could affect the semiconductor's performance. This protection is critical during both the fabrication process and the operation of the device, ensuring that the sensitive silicon regions remain uncontaminated.

SiO_2 also provides surface passivation to the silicon substrate. The passivation helps stabilize the surface by reducing dangling bonds and defects that could otherwise contribute to unwanted surface recombination and leakage currents.

Thermal Performance: The various regions such as SiO_2 (insulating layer), p-channel stops, and polysilicon layers help to manage the heat dissipation by distributing the thermal load across the device. Efficient power dissipation prevents thermal hotspots and ensures that the junctions remain stable even during heavy current operation which reduces the risk of thermal runaway.

5 Choice of Ohmic Contact

When dealing with dense p^+ and n^+ regions in integrated circuits (ICs), the selection of appropriate ohmic contact materials is essential for optimal device performance. Here's how to choose contacts for both cases:

5.1 p^+ Region

For a dense p^+ region, you want a contact material that forms a low-resistance ohmic contact. Here are some suitable options:

1. **Gold (Au):** Gold is often used for p-type silicon due to its good conductivity and the ability to form low-resistance contacts. However, it can diffuse into the silicon, so it should be used with care.
2. **Nickel (Ni):** Nickel can provide good ohmic contacts to p-type silicon and is commonly used due to its low contact resistance and thermal stability.
3. **Titanium (Ti):** Titanium can serve as a barrier layer to prevent diffusion into the silicon and can also be combined with other materials like Ni or Au for better performance.

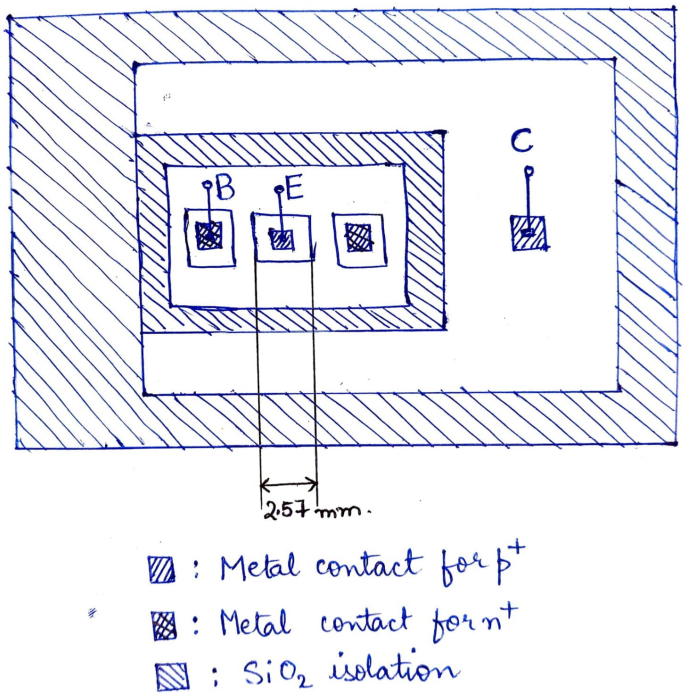

Figure 13: Top view of proposed structure

5.2 n^+ Region

For a dense n^+ region, the contact material should also provide a low-resistance interface. Here are some suitable options:

1. **Aluminum (Al):** Aluminum is widely used for n-type silicon due to its excellent conductivity and ease of deposition. It forms good ohmic contacts when applied to heavily doped n^+ regions.
2. **Titanium (Ti):** Titanium can also be used as an ohmic contact for n-type silicon, often applied as a thin film. It is typically used in combination with other metals.
3. **Platinum (Pt):** Platinum is another option, especially for high-temperature applications, but it is less common than Al or Ti due to cost and deposition complexity.

In the proposed structure, we would be using Nickel in the contacts of the collector and emitter whereas, Aluminium would be the contact of the base region.

6 Basic Circuit using the Device

Consider all calculations at T_{amb} = 25°C.
From h_{FE} vs. I_C plot as shown in figure 8,

$$\boxed{\beta = 175}$$

From $V_{BE(ON)}$ vs. I_C plot, assuming forward active mode of operation

$$V_{EB(ON)} = 0.7V \Rightarrow I_C = 100mA.$$

$$\Rightarrow I_B = \frac{I_C}{\beta} \approx 0.57mA$$

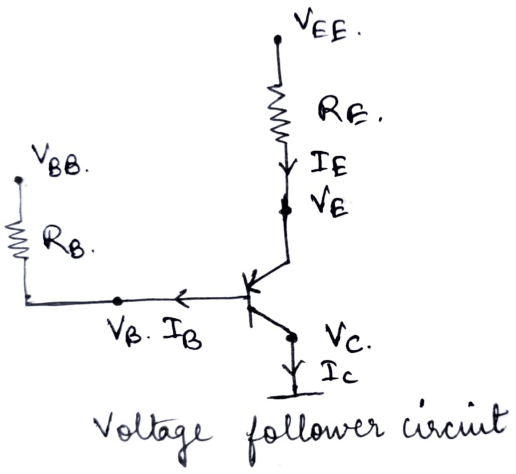

Figure 14: circuit diagram of source follower using PNP BJT

Also, using KCL,

$$I_E = I_C + I_B \approx I_C = 100mA$$
$$\Rightarrow \frac{I_E}{\beta} = \frac{V_{\text{EE}} - V_E}{\beta R_E} = \frac{V_{\text{BB}} - (V_E - V_{EB})}{R_B} = I_B$$

Rearranging terms to get the expression for V_E,

$$V_E = \frac{\beta R_E(V_{\text{BB}} + V_{EB}) - V_{\text{EE}} R_B}{\beta R_E - R_B}$$

Let's say, we wish to obtain V_{CE} = -5V for forward active mode $\Rightarrow V_E = 5V \Rightarrow V_B = 4.3V, V_{EB} = 0.7V$.

Let's choose V_{BB} = 10V.

$$\Rightarrow R_B = \frac{V_{\text{BB}} - V_B}{I_B} = 10k\Omega$$

Similarly, let's choose V_{EE} = 25V.

$$\Rightarrow R_E = \frac{V_{\text{EE}} - V_E}{I_C} = 200\Omega$$

Hence, for the values $\beta = 175, R_E = 0.2k\Omega, R_B = 10k\Omega$,

$$\boxed{V_{\text{CE}} = -5V, I_E = 100mA}$$

This fixes I_B and V_B as well.

References

[1] Datasheet of **2DA1201Y**

[2] Solid state devices by "Ben G. Streetman & Sanjay Kumar Banerjee"

[3] BJT Switching Characteristics, Small Signal Model