Final Report - EE618
2DA1201Y PNP TRANSISTOR

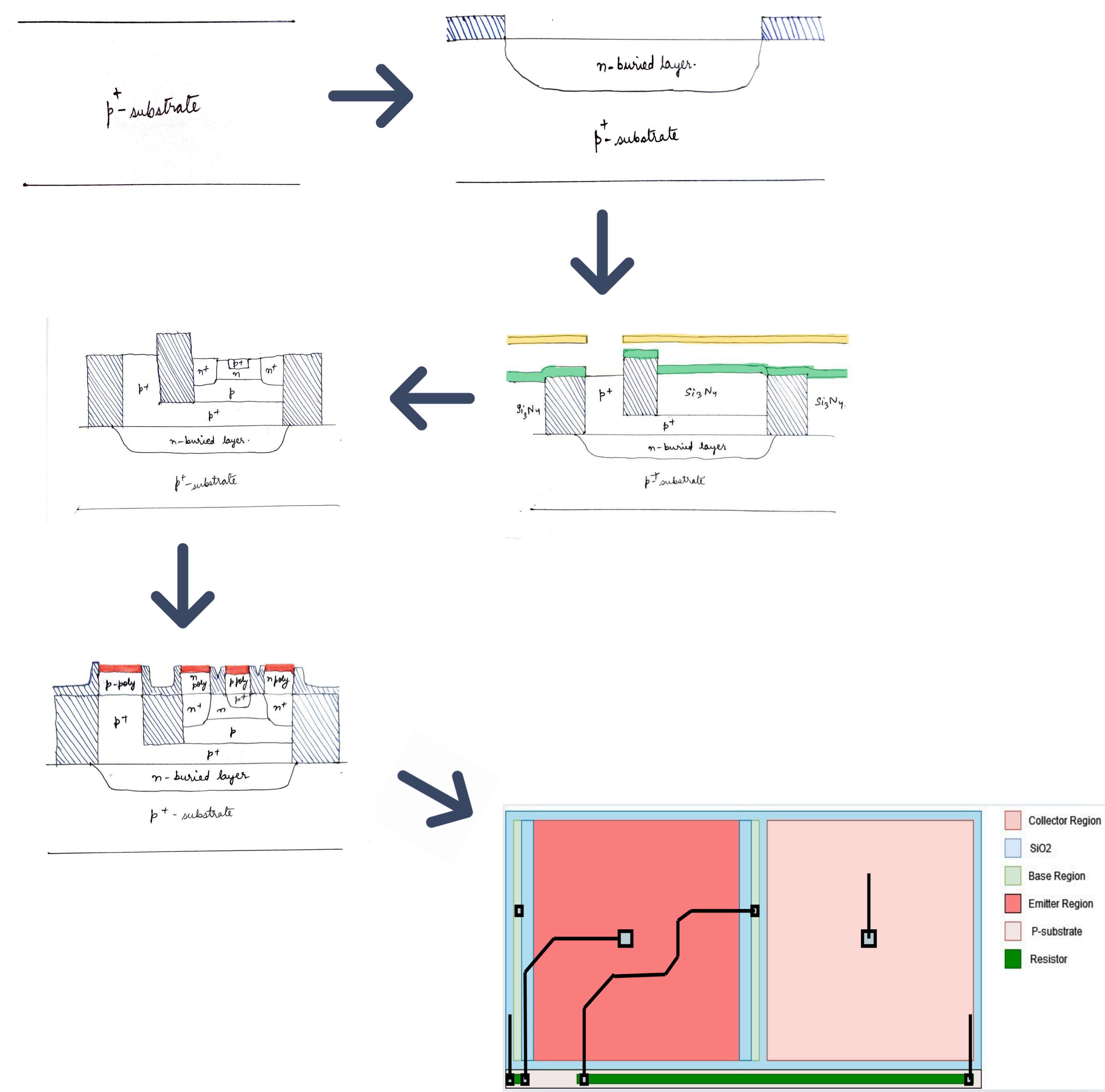
Adrija Bera 210071

Aniket Sen 210134

Devendra Saini 241040608

Pratyush Amrit 210762

1. Fabrication Flow Overview



Description of common processes used

1.1 Photolithography

Photoresist material: **DNQ (**Diazonaphthoquinone**)** with base resin - Novolac. (*reference: Plummer*)
This is a g-line photoresist compatible with a wavelength = *436nm*.

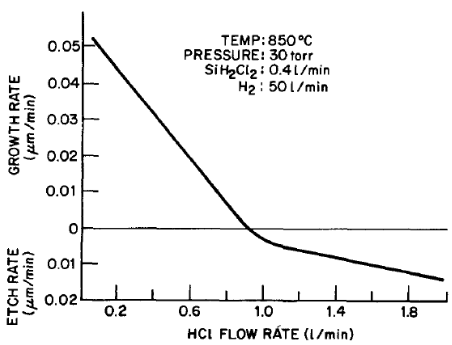
- γ is typically 2-3.
- Q_f value is 100 mJ/cm^2**.**

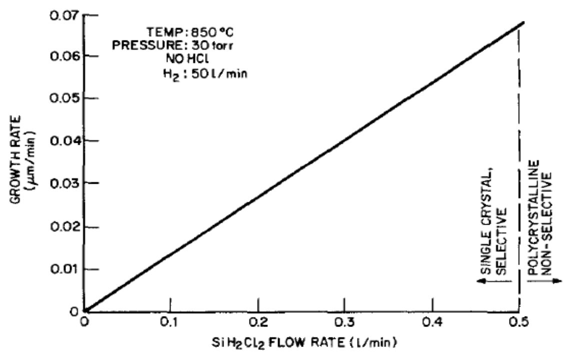
Typical Intensity of Light used: 20 mW/cm^2.
The time taken in each photoresist process is 5 seconds.

1.2 Chemical Vapour Deposition

The most commonly used deposition process in the fabrication of the device is LPCVD.

- A good choice of flow rate of SiH_2Cl_2 used in CVD is *0.4 liter/min*.
- The flow rate of HCl is *0.5 liter/min*.

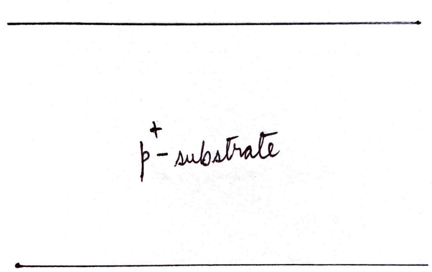


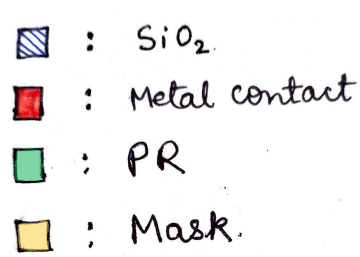


2. Choice of Substrate

The p-substrate should have a moderately high resistivity (25 Ω – 50 Ω) value, which corresponds to a doping level on the order of $10^{15}\ cm^{-3}$. Then the actual device is built on an n-well that is diffused into the surface of the wafer. Typically, the well doping levels are of the order $10^{16} - 10^{17}\ cm^{-3}$ near the wafer surface.

The only other parameter we need to specify in the starting material substrate is the crystal orientation. Modern silicon integrated circuits are typically made with wafers oriented in the (100) crystal direction. This





orientation is preferred because it creates a better Si / SiO_2 interface, with fewer imperfections in atomic bonding when a SiO_2 layer is thermally grown. This improves electrical properties, making (100) orientation the standard for starting wafers.

3. <u>N-buried well Formation</u>

Table 6–2 Rate constants describing (111) silicon oxidation kinetics at 1 Atm total pressure. For the corresponding values for (100) silicon, all C_2 values should be divided by 1.68.

Ambient	B	B/A
Dry O_2	$C_1 = 7.72 \times 10^2\ \mu m^2\ hr^{-1}$	$C_2 = 6.23 \times 10^6\ \mu m\ hr^{-1}$
	$E_1 = 1.23$ eV	$E_2 = 2.0$ eV
Wet O_2	$C_1 = 2.14 \times 10^2\ \mu m^2\ hr^{-1}$	$C_2 = 8.95 \times 10^7\ \mu m\ hr^{-1}$
	$E_1 = 0.71$ eV	$E_2 = 2.05$ eV
H_2O	$C_1 = 3.86 \times 10^2\ \mu m^2\ hr^{-1}$	$C_2 = 1.63 \times 10^8\ \mu m\ hr^{-1}$
	$E_1 = 0.78$ eV	$E_2 = 2.05$ eV

3.1 <u>Thermal oxidation of Si To form SiO_2</u>

The thickness of SiO_2 formed = 1.5 μm, using H_2O.

From Deal-groove's Equation,

$$\frac{x_0^2}{B} + \frac{x_0}{\frac{B}{A}} = t + \tau \; ; \; here,\ \tau = 0,\ B = 0.549 \mu m^2 hr^{-1} \ \& \ \frac{B}{A} = 5.37\ \mu m\ hr^{-1}$$

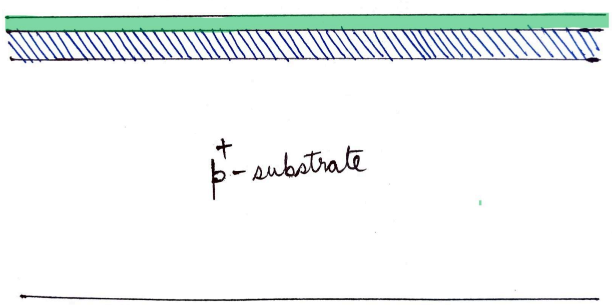
For, (100) Si from the table.

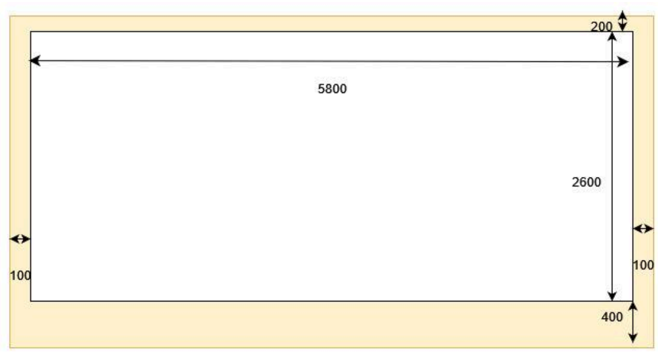
Hence, the time required is 3.01 hours ≈ <u>3 hours</u>.

3.3 <u>Lithography for Forming Mask for Etching of SiO_2</u>

After Applying Photo-resist here.

The time taken is <u>5 seconds</u>.





Mask 1 is used here for photolithography.

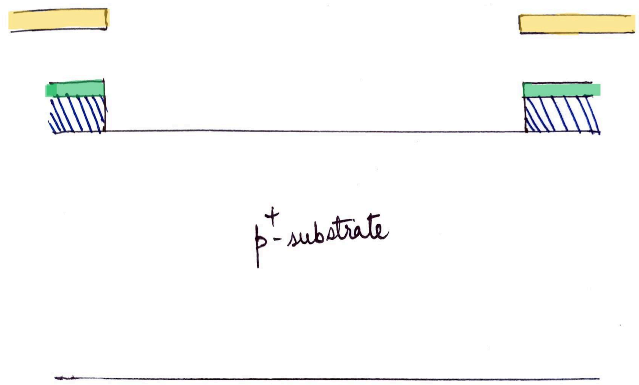
Mask 1

3.4 <u>Etching of SiO_2</u>

The etch rate of SiO_2 using CF_4/H_2 is approximately $0.40\ \mu m\ min^{-1}$.

Therefore, etching will be done for approx 4 min to ensure complete etching.

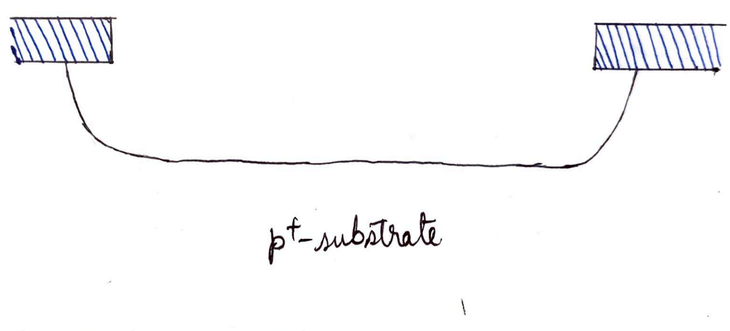
Material	Etchant	Comments
SiO_2	SF_6, NF_3, CF_4/O_2, CF_4	Can be isotropic or near isotropic (significant undercutting); anisotropy better with higher ion energy and lower pressure; poor or no selectivity over Si
	CF_4/H_2, CHF_3/O_2, C_2F_6, C_3F_8	Very anisotropic, selective over Si
	$CHF_3/C_4F_8/CO$	Anisotropic, selective over Si_3N_4



3.6 Etching of Si after removing PR.

Material	Etchant	Comments
Polysilicon	CF_4	Isotropic or near isotropic (significant undercutting); fair to no selectivity over SiO_2
	CF_4/H_2	Very anisotropic, non-selective over SiO_2
	SF_6, CF_4/O_2	Isotropic or near isotropic, good selectivity over SiO_2
	HBr, Cl_2, $Cl_2/HBr/O_2$	Very anisotropic, most selective over SiO_2

Si will be etched using HBr at 8 mt pressure with an energy supply of 1700 W. The Etch rate is Almost $200\ nm/min$. Hence, to remove $30\ um$ Si, we will need 150 mins.



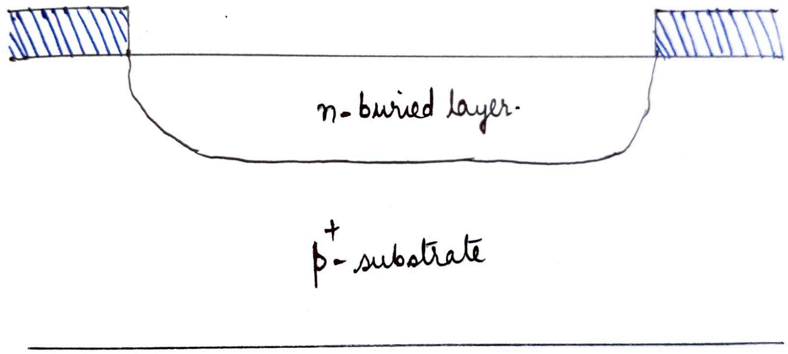
3.7 <u>Formation of the N-buried layer</u>

The n buried region is grown through CVD (along with Arsenic gas impurities such as AsH3) and planarized by CMP on the etched regions.

Concentration of AsH3 = $2 \times 10^{16}\ cm^{-3}$

Temperature = 1000℃
Thickness = 40 um
Growth rate = 0.2 um/min

Time required = _200 minutes_

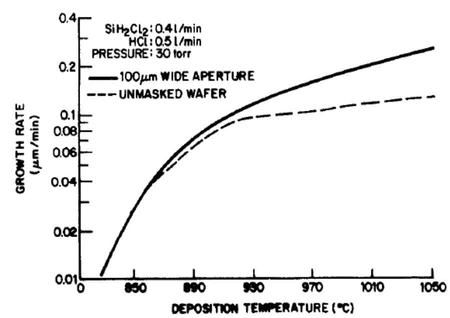


4. Trench Isolation for Isolation Step

4.1 Growth of Si_3N_4 layer

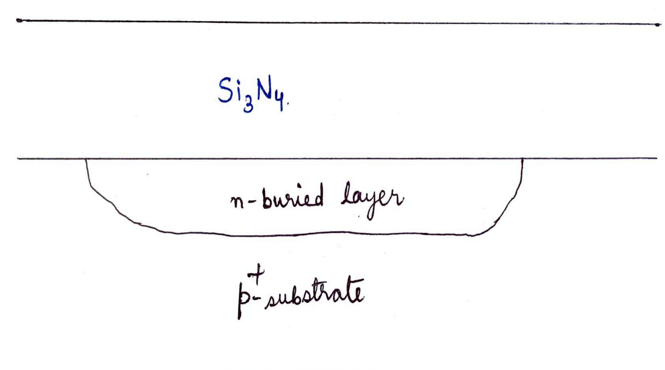
A layer of 75um of **Si_3N_4** is grown on the entire region with the help of CVD. CVD deposits silicon-nitride films in the 650-900℃ range. Low-pressure CVD is frequently used here for good uniformity and high wafer throughput. The source gases are ammonia and either dichlorosilane or silane, following the reactions :

$$3SiH_2Cl_2 + 4NH_3 \rightarrow Si_3N_4 + 6HCl + 6H_2$$
$$3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2$$



Thickness = 108 um
Temperature = 900℃
From the graph, **Growth rate =** 0.08 um/min

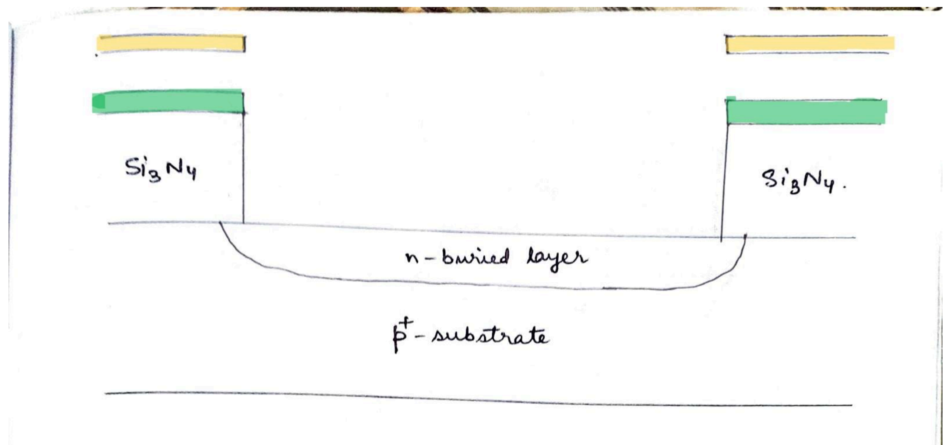
Thus, time taken for the layer formation = Thickness / Growth rate
= 937.5 minutes
≈ 15 hrs 38 minutes



4.2 Etching the desired region

Apply the photoresist layer above the **Si_3N_4** region and then etch the following region with the help of Mask 1 again, as shown above. Using CH_3F with 60% O_2 The power is 250 W and the pressure is 50 mT. (Ref. https://www.sciencedirect.com/science/article/pii/S0167931709003530)

Etching Depth = 108 um.
Etching Rate = 100 nm/min
Time required = *18 hours*.

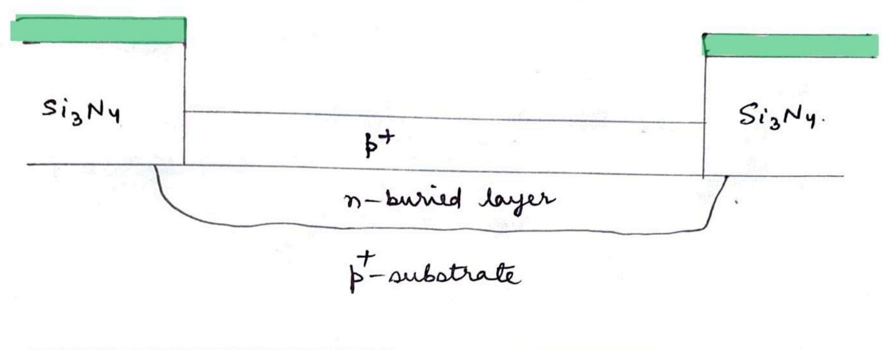


4.3 Growth of p+ sub-collector region

The p+ sub-collector region of 30 um is grown through CVD (along with Boron gas impurities such as BH_3) on the layer of the n-well region.

Concentration of BH_3 impurity = 10^{18} cm^{-3}
Temperature = 850℃
Thickness = 30 um
Growth rate = 0.025 um/min

Time required = *20 hours*

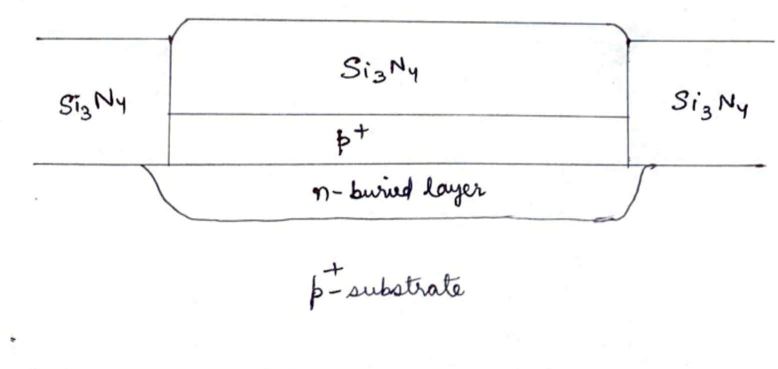


4.4 Growth of the Si_3N_4 layer again and Isolating the active regions

An over-deposition of the **Si_3N_4** layer is performed through CVD.

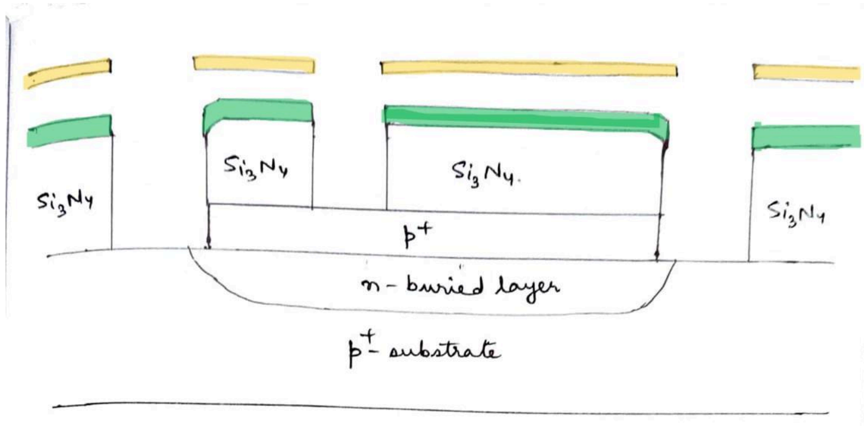
Temperature = 850℃
Thickness = 78 um
Growth Rate = 0.025 um/min

Time required = *52 hours*

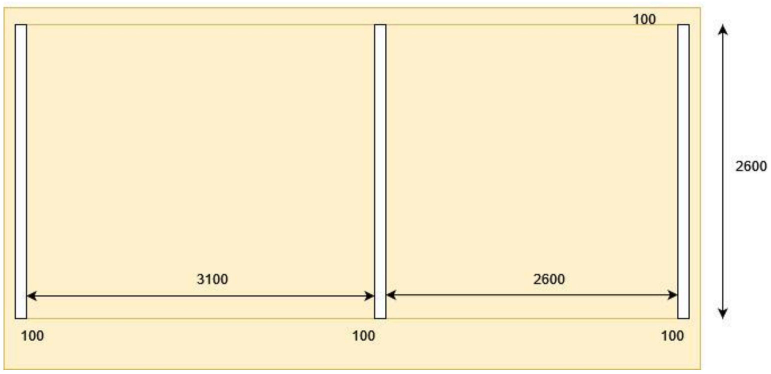


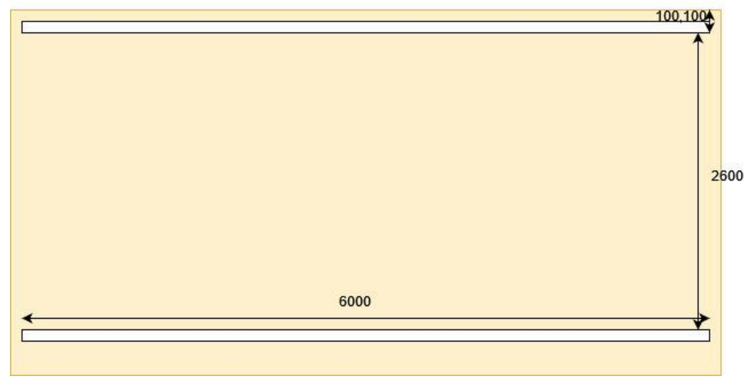
The excess **Si_3N_4** is removed by **CMP** (Chemical-Mechanical Planarization), and the profile is flattened. Now, apply a photoresist again over the top and then etch the following regions with the help of a mask.

Using **Mask No. 2 and 3,** Si_3N_4 is etched using CH_3F with 60% O_2. The power is 250 W and the pressure is 50 mTorr for 78/0.1=780 min ≈ _13 hours_.
Using **Mask No. 3 and 4,** etch for _5 hours_.



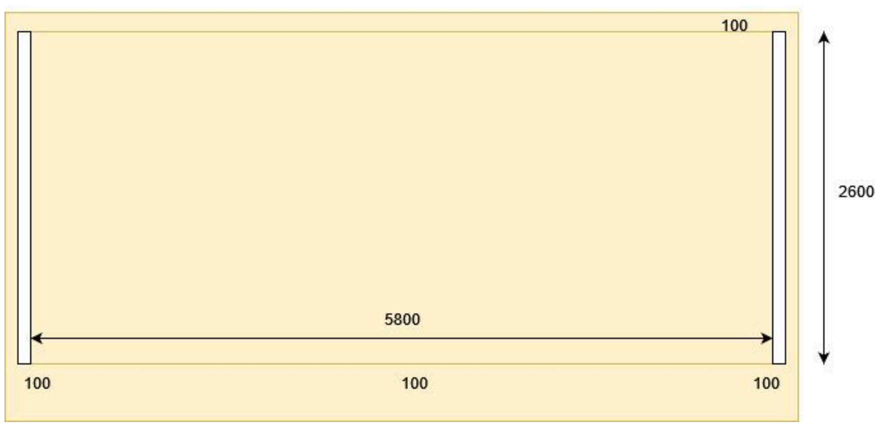
Mask 2





Mask 3

Mask 4

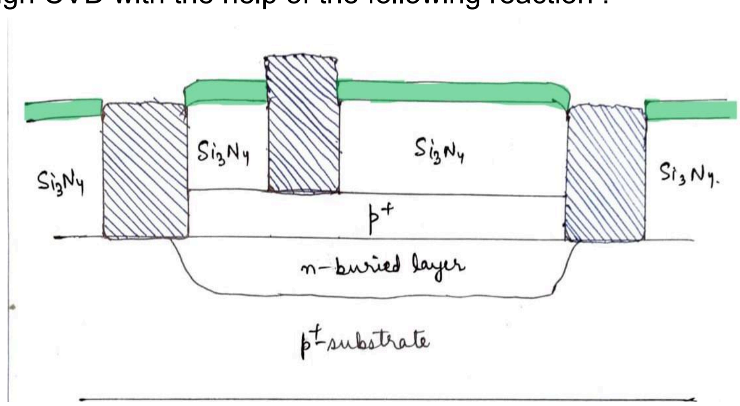


4.5 <u>Growth of SiO_2 Layer in the Trench</u>

Epitaxial Growth of the SiO_2 layer is done through CVD with the help of the following reaction :

$$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2$$

Thickness = 108 um
Temperature = 900℃
Growth rate = 0.08 um/min



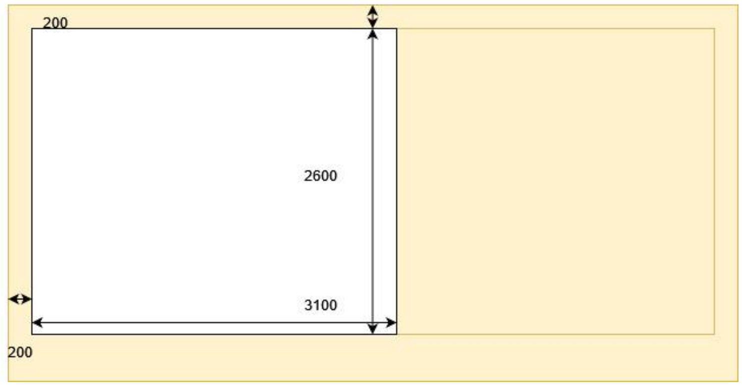
Thus, time taken = *22 hours 30 minutes*

4.6 Etch the Si_3N_4 layer

Apply a photoresist layer of thickness 3 um for masking and expose the Si_3N_4 layer which could be etched out by using **Mask no. 5** using CH_3F with 70% O_2. The power is 250 W and the pressure is 50 m.Torr for 78/0.1=*780 minutes*.

The selectivity over SiO_2 is more than 10.

Mask 5



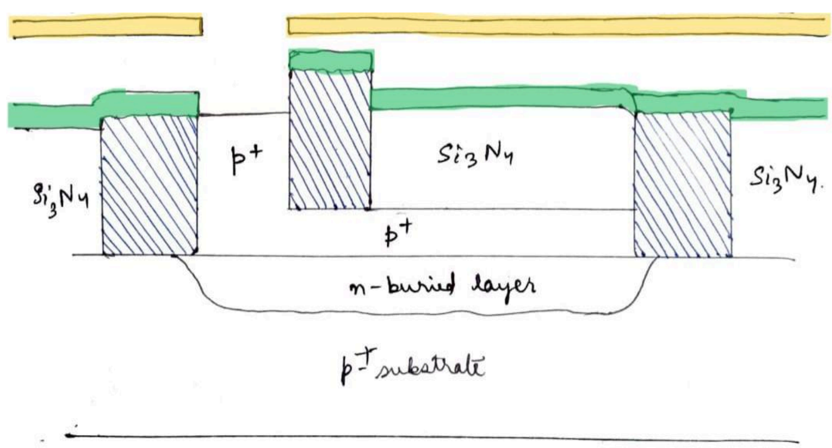
5. Growth of p+ sub-collector region

Photoresist with the help of photolithography is applied to expose the region.

CVD Deposition is performed to form the **p+ sub-collector** region.

Temperature = 900℃
Thickness = 78 um
Growth Rate = 0.08 um/min

Time taken = *16 hours 15 mins*



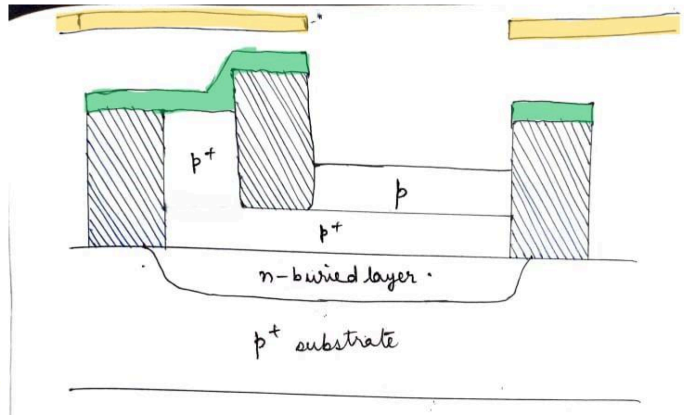
6. Growth of the PNP layer

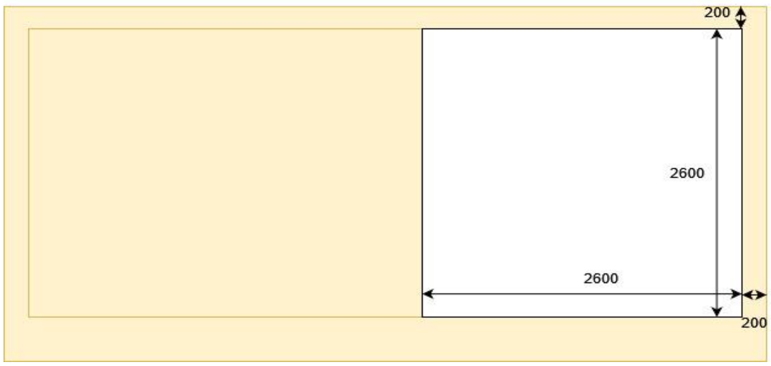
6.1 Collector region formation

Apply a photoresist layer of thickness 3 um for masking and expose the Si_3N_4 layer which could be etched out by using Mask No. 6 is etched using CH_3F with 70% O_2 The power is 250 W and pressure is 50 mT.for 78/0.1=780 min. The selectivity over SiO_2 is more than 10. The collector region of **40 um** is grown through CVD (along with Boron gas impurities such as BH_3) on the layer of the n-well region.

Concentration of BH_3 = 6.7×10^{15} cm^{-3}
Temperature = 850℃
Thickness = 40 um
Growth rate = 0.025 um/min

Time required = *26 hours 40 minutes*





Mask 6

6.2 n+ region formation

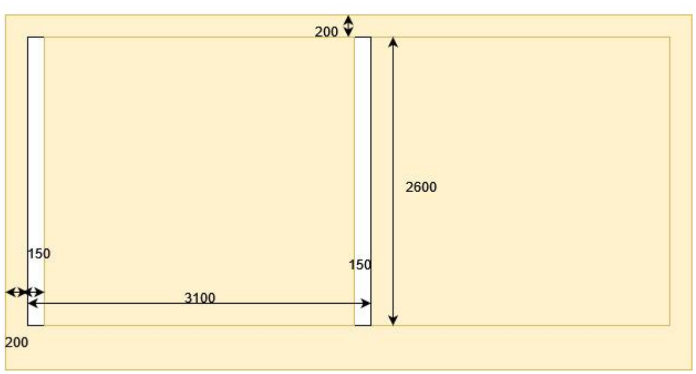
6.2.1 Growth of the Si_3N_4 and Isolating the Active Regions

Deposition of the $\mathbf{Si_3N_4}$ layer is performed through LPCVD.

Temperature = 850℃
Thickness = 39 um
Growth Rate = 0.025 um/min

Time required = *26 hours*

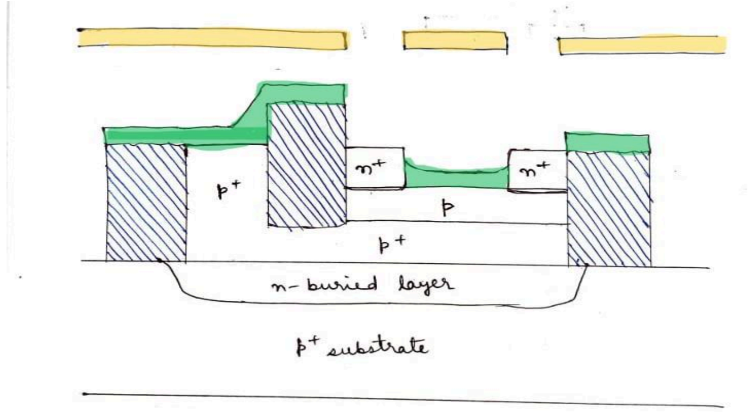
The excess $\mathbf{Si_3N_4}$ is removed by CMP (Chemical-Mechanical Planarization), and the profile is flattened. Now, apply a photoresist again over the top and then etch the following regions with the help of **Mask no. 7** using CH_3F with 70% O_2. The power is 250 W and the pressure is 50 mT for 39/0.1 = *390 minutes*.



Mask 7

6.2.2 Growth of n+ region

The *n+ region* is grown through CVD (along with Arsenic gas impurities such as AsH_3) and planarized by CMP on the etched regions.



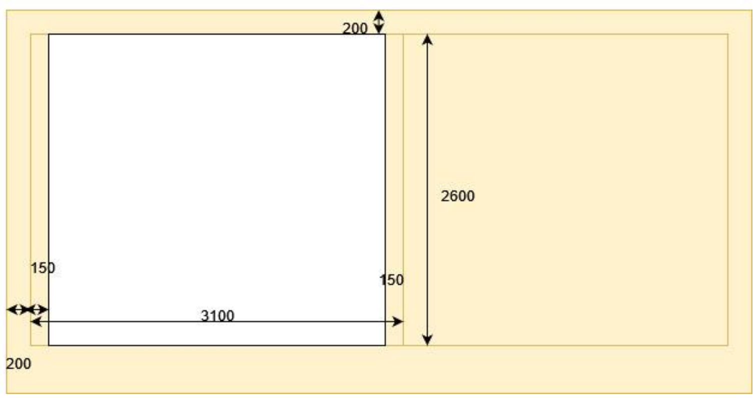
Concentration of AsH_3 = 10^{19} cm^{-3}
Temperature = 850°C
Thickness = 39 um
Growth rate = 0.025 um/min

Time required = *26 hours*

6.2.3 Etch the Si_3N_4 layer

Apply a photoresist layer of thickness 3 um for masking and expose the Si_3N_4 layer which could be etched out by using Mask no 8 is etched using CH_3F with 70% O_2. The power is 250 W and the pressure is 50 m.Torr.
The selectivity over SiO_2 is more than 10.

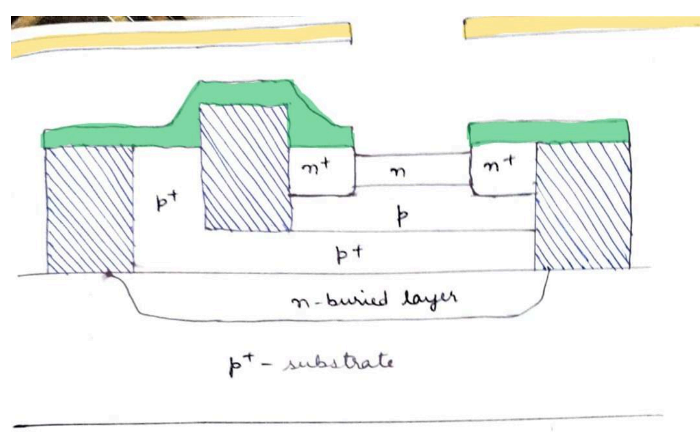
Time required = (78um) / (0.1um/min) = 780 minutes = *13 hours*



Mask 8

6.3 Base Region Formation

The n-doped base region is grown through the LPCVD process.

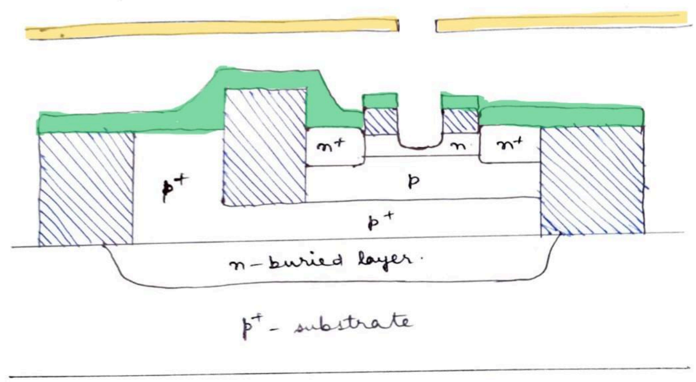


Temperature = 850°C
Thickness = 13.7 um + 25 um = 39 um
Growth Rate = 0.025 um/min

Time required = *26 hours*.

6.4 Emitter Region Formation

Wet oxidation forms a thin layer of SiO_2, and then a photoresist layer is applied. Now, etch the desired region of Si using **Mask 9** (with HBr at 8 m.Torr pressure with an energy supply of 1.7 kW).



Thickness = 25 um

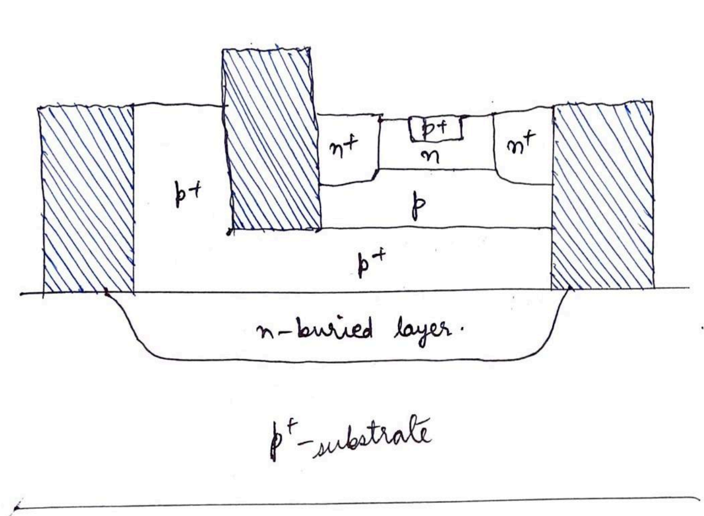
The etch rate is almost 200 nm/min
Etching Time = *125 min*.

After etching, grow the layer of the p+ emitter region

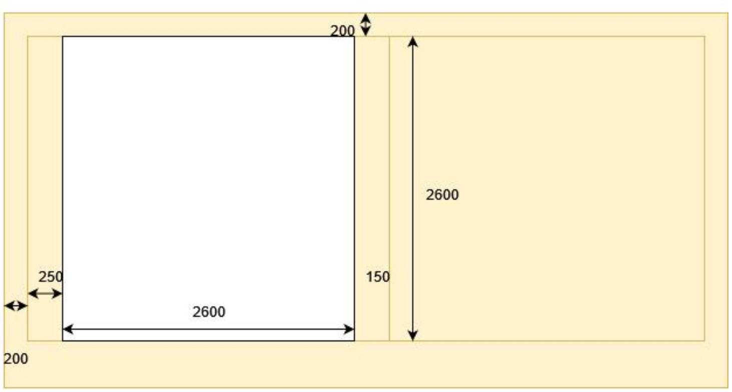
Concentration of BH_3 = 7 x 10^{18} cm^{-3}
Temperature = 850°C
Thickness = 25 um
Growth Rate = 0.025 um/min

Time required = *16 hours 40 minutes*

Then perform CMP to etch out excess SiO_2 for planarizing the surface.

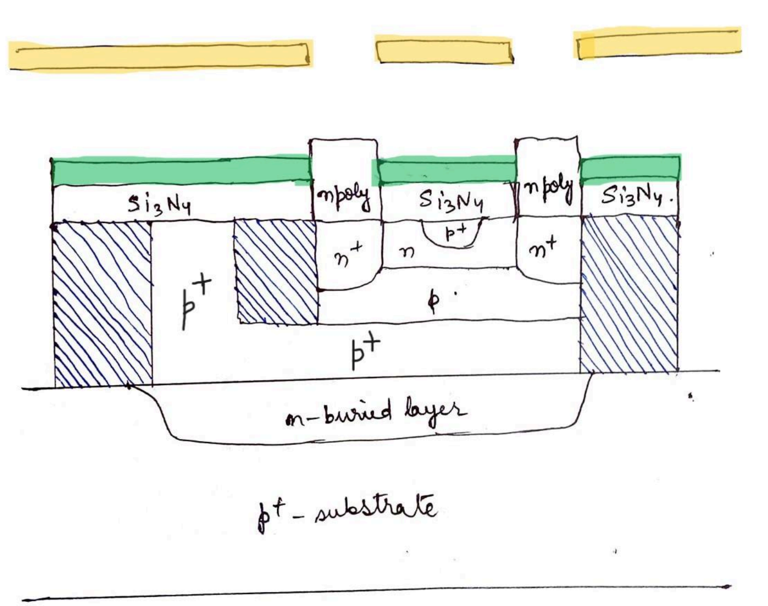


Mask 9



7. Metal-layer Contact Formation

7.1 N-Polysilicon Layer Formation



A layer of Si_3N_4 is deposited epitaxially over the device through CVD.

Thickness = 3 um
Temperature = 850°C
Growth Rate = 0.025 um/min

Time taken = *2 hours*

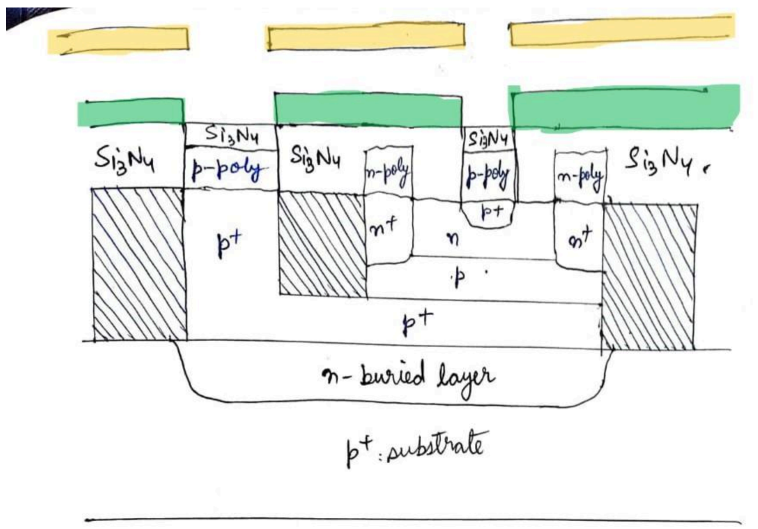
Then apply a photoresist on it and etch the region on which n-polysilicon is to be applied.
Reuse **Mask 8**

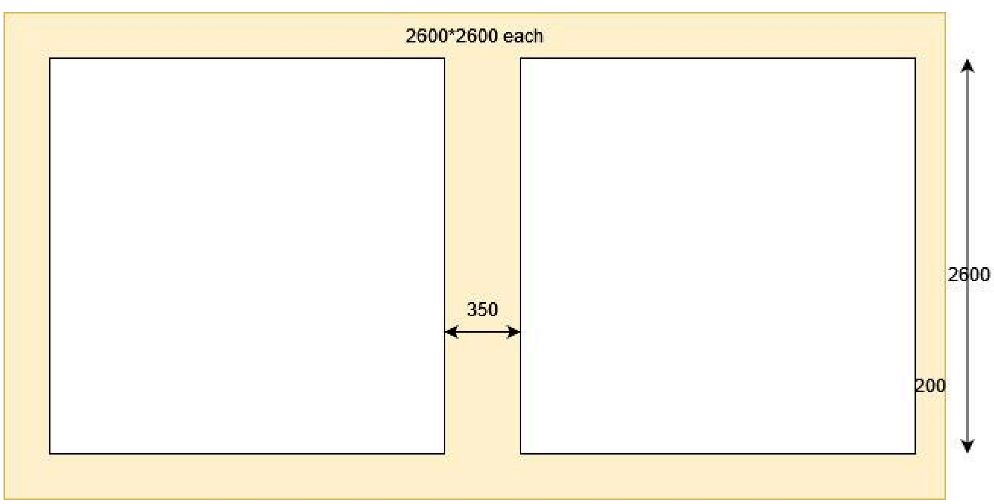
7.2 P-polysilicon Layer Formation

Again grow a layer of Si_3N_4 by LPCVD and apply a layer of photoresist on it and etch away the region on which the p-polysilicon layer is grown using **Mask 10**. After the etching, grow the layer of p-polysilicon through LPCVD.

Thickness = 3 um
Temperature = 850℃
Growth Rate = 0.025 um/min

Time taken = *2 hours*

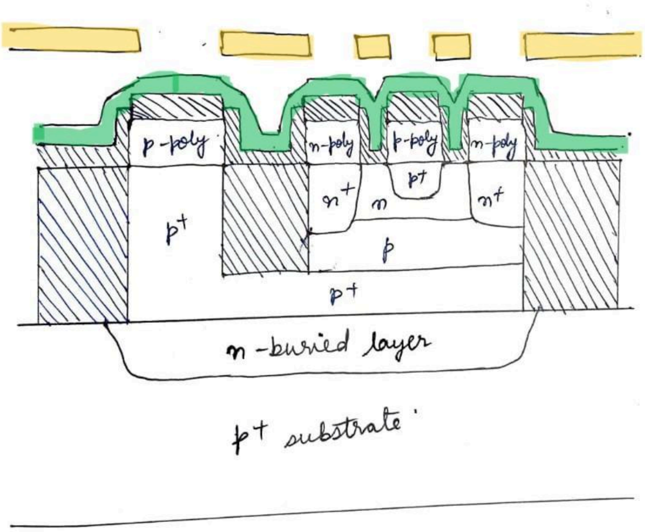




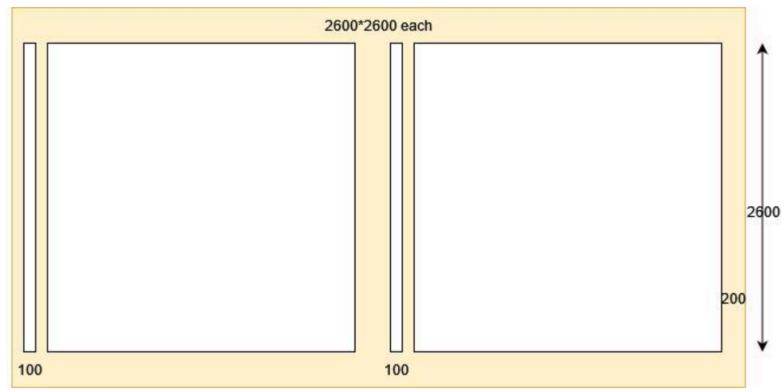
MASK 10

7.3 <u>SiO_2 Mask Formation</u>

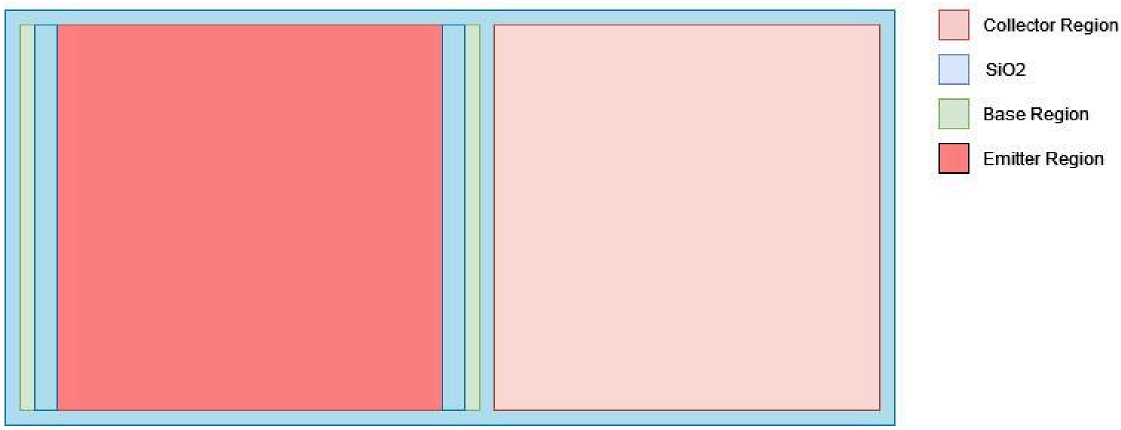
Apply the photoresist and expose the areas where the SiO_2 layer is to be grown. After this, deposit a layer of SiO_2 through CVD, followed by etching of the photoresist layer using **Mask 11**.



Mask 11



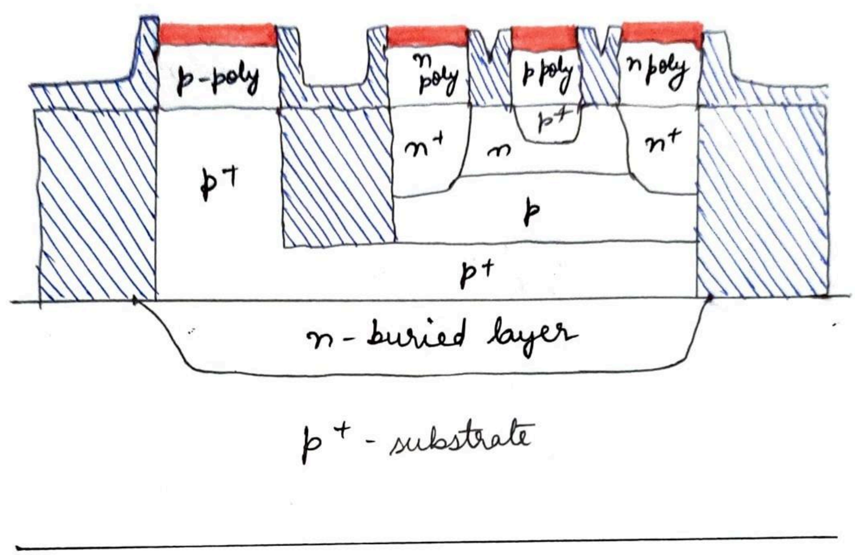
Top View :



7.4 <u>Al Deposition</u>

Aluminum (Al) is the main interconnect material in silicon microelectronics. The technique almost always used is DC magnetron sputter deposition.

Deposition Rate = 1 um/min
Thickness = 15 um
Time required = *<u>15 minutes</u>*



8. Resistor

To fabricate a resistor on a p-type silicon substrate, an n-type region is created with a dopant concentration of $10^{17}\ \mathrm{cm}^{-3}$. This n-type diffusion or implantation forms the resistor, with its cross-sectional area designed as $100\ \mu\mathrm{m} \times 5\ \mu\mathrm{m}$, and a resistivity of $0.1\ \Omega \cdot \mathrm{cm}$. These parameters are critical in determining the resistor's overall resistance.

To calculate the length required for a resistor with target resistances of $200\ \Omega$ and $10,000\ \Omega$ (10 kΩ), we'll use the formula:

$$R = \rho \cdot \frac{L}{A}$$

where:

- R is the target resistance,
- $\rho = 0.1\ \Omega \cdot \mathrm{cm}$ is the resistivity,
- L is the length of the resistor (what we need to find),
- $A = 100\ \mu\mathrm{m} \times 5\ \mu\mathrm{m} = 500\ \mu\mathrm{m}^2 = 5 \times 10^{-6}\ \mathrm{cm}^2$ is the cross-sectional area in cm^2.

Rearranging the formula to solve for L:

$$L = \frac{R \cdot A}{\rho}$$

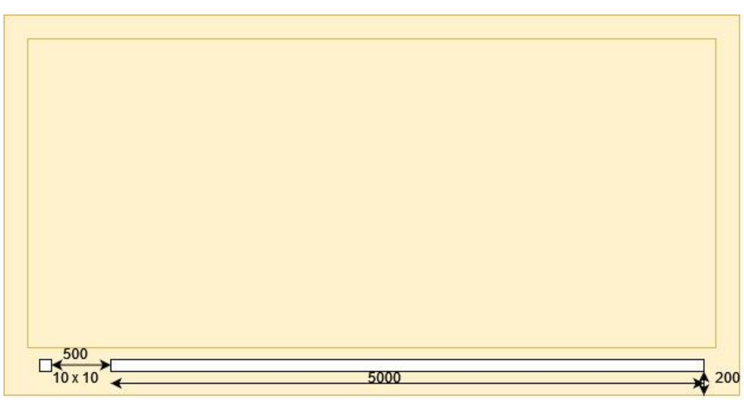
1. **For $R = 200\ \Omega$:**

$$L = \frac{200\ \Omega \cdot 5 \times 10^{-6}\ \mathrm{cm}^2}{0.1\ \Omega \cdot \mathrm{cm}} = \frac{10^{-3}\ \Omega \cdot \mathrm{cm}^2}{0.1\ \Omega \cdot \mathrm{cm}} = 0.01\ \mathrm{cm} = 100\ \mu\mathrm{m}$$

2. **For $R = 10,000\ \Omega$ (10 kΩ):**

$$L = \frac{10,000\ \Omega \cdot 5 \times 10^{-6}\ \mathrm{cm}^2}{0.1\ \Omega \cdot \mathrm{cm}} = \frac{0.05\ \Omega \cdot \mathrm{cm}^2}{0.1\ \Omega \cdot \mathrm{cm}} = 0.5\ \mathrm{cm} = 5000\ \mu\mathrm{m}$$

Mask 12 is used to etch away the SiO2 region followed by the Deposition of N-type material with a resistivity of 0.1 ohms-cm.

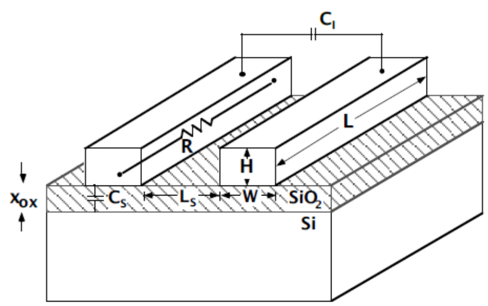


Mask 12 for Resistor formation

9. <u>Interconnects</u>

<u>Ohmic contacts</u> connect an interconnect with active regions or devices in the silicon substrate. A high-resistivity dielectric layer, usually silicon dioxide, separates the active regions from the global interconnect, and electrical contact is made between the interconnect and the active regions in the silicon through openings in that dielectric layer.

Ohmic contacts connect an interconnect with active regions or devices in the silicon substrate. A high resistivity dielectric layer, usually silicon dioxide, separates the active regions from the first level global interconnect, and electrical contact is made between the interconnect and the active regions in the silicon through openings in that dielectric layer.



The line resistance of the interconnect is given by :

$$R = \rho \frac{L}{WH}$$

where ρ is the interconnect resistivity, and L, W, and H are the interconnect length, width, and height, respectively.

The capacitance associated with the line is :

$$C = K_{ox}\varepsilon_o \frac{WL}{X_{ox}} + K_{ox}\varepsilon_o \frac{HL}{L_S}$$

Where x_{ox} and K_{ox} are the oxide thickness and dielectric constant, respectively, and ε_o is the permittivity of free space. The first term represents the line to substrate capacitance, C_s, and the second term is the coupling capacitance between adjacent lines, C_l. It is assumed that the lines are surrounded by oxide on all sides.

The total RC delay associated with the line is thus

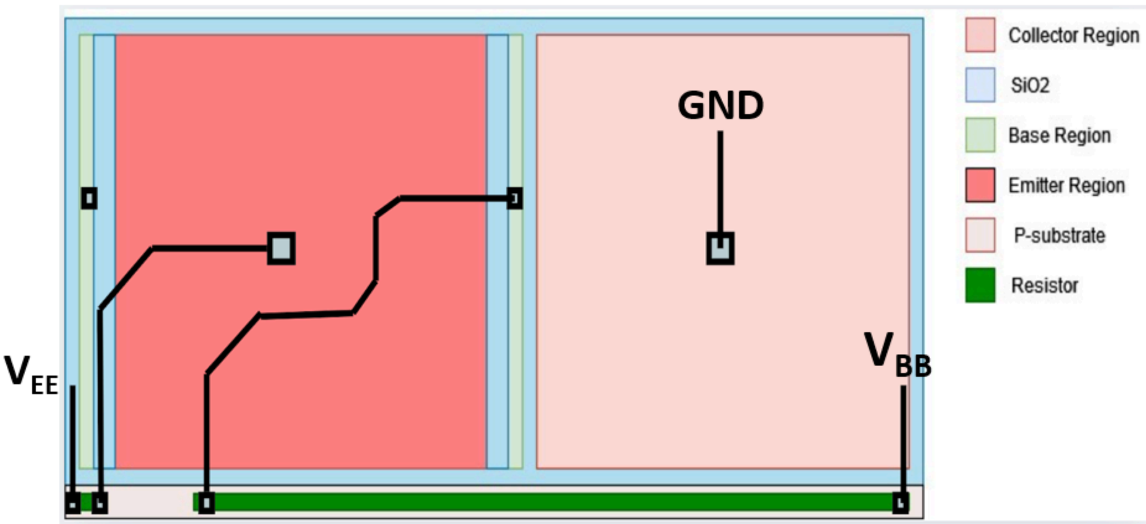
$$\tau_L = 0.89\, K_I K_{ox}\varepsilon_o \rho L^2 \left(\frac{1}{Hx_{ox}} + \frac{1}{WL_S}\right)$$

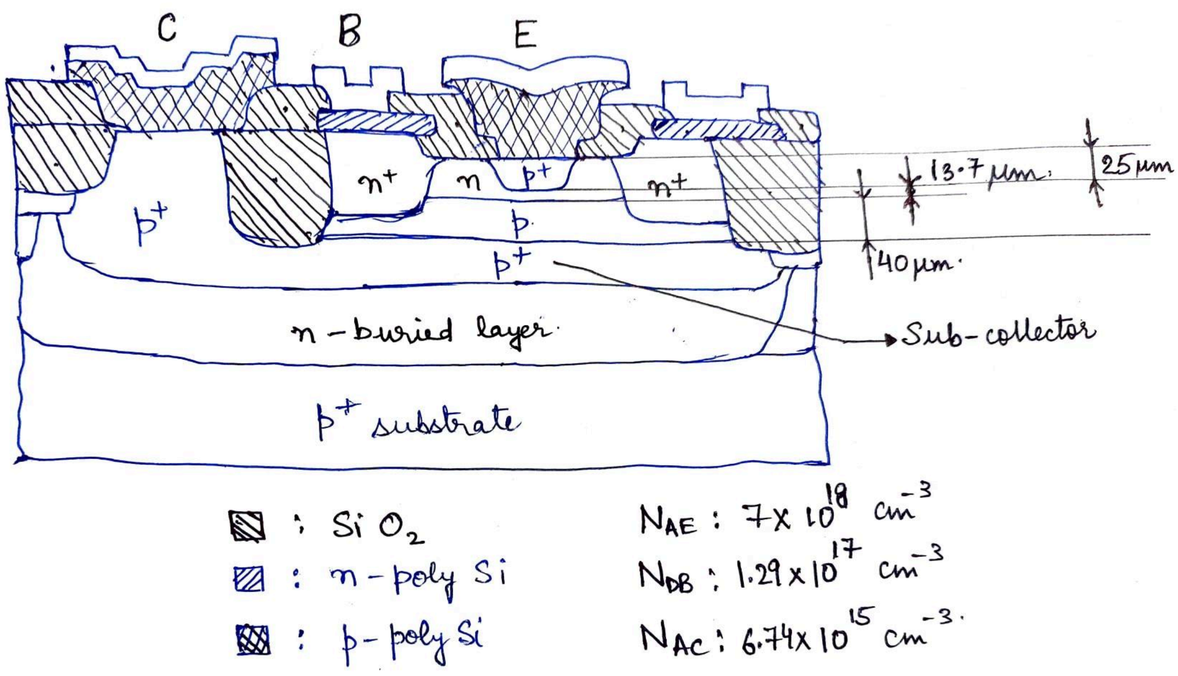
Where, K_l is added to empirically account for fringing fields and other interconnects above and below the line, in multilayer interconnect systems. K_l is often taken to be approximately 2.

In our case, $WL_s >> Hx_{ox}$
So,

$$\tau_L = 0.89K_lK_{ox}\varepsilon_{ox}\rho L^2\left(\frac{1}{Hx_{ox}}\right)$$

<u>Final view of the proposed Fabricated view of the Circuit</u>





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