EE698I: MIXED SIGNAL IC DESIGN

MID-SEM PROJECT

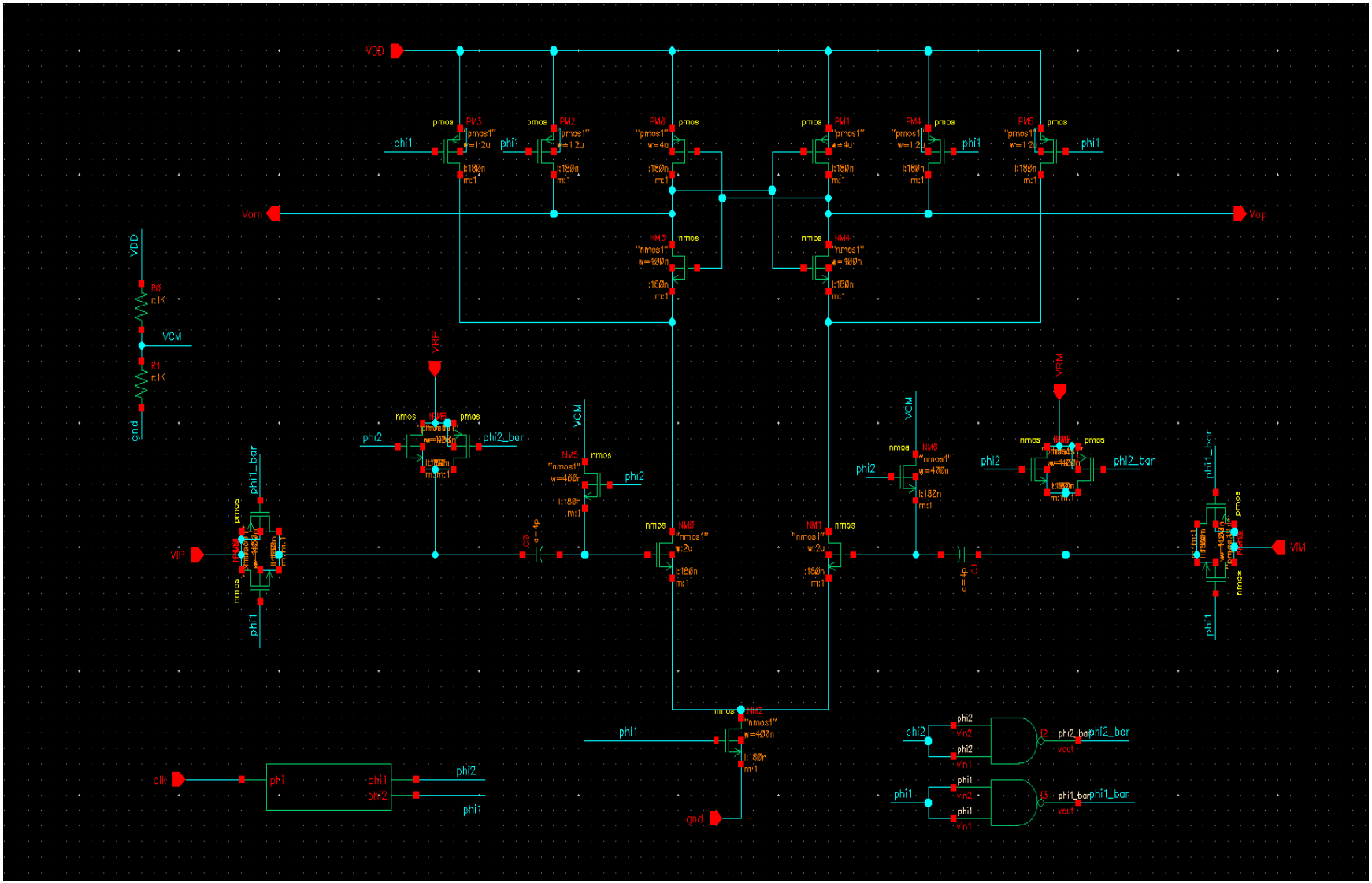
Design of 4-bit FLASH ADC with 2x Time Interpolation

(180 nm PDK)

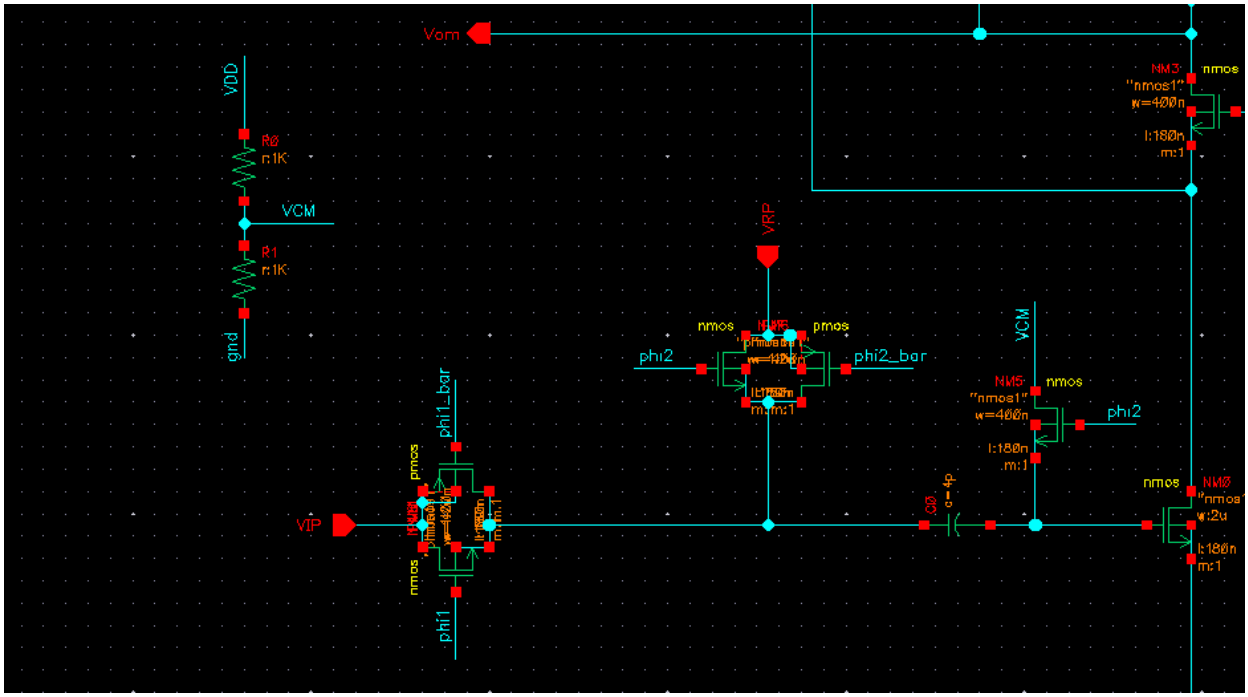
ADRIJA BERA

210071

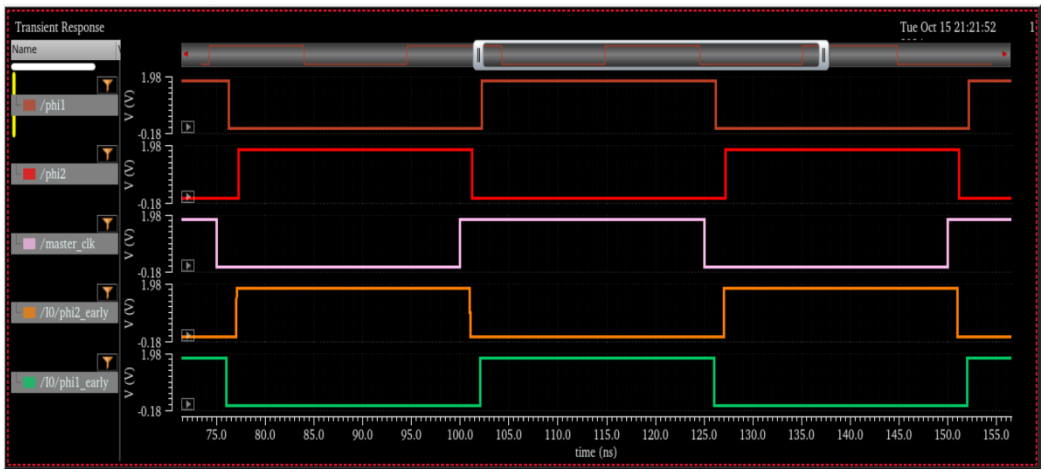
STRONG-ARM LATCH CIRCUIT

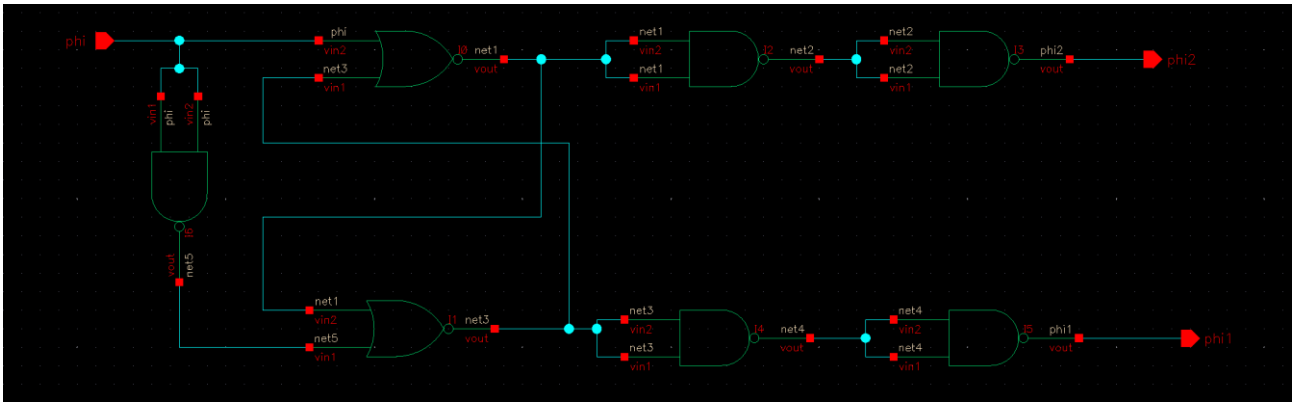

VDD
PM3
PM2
PM0
PM1
PM4
PM5
phi1
Vom
Vop
NM3
NM4
R0
R1
VCM
gnd
VRP
VRM
phi2
phi2_bar
NM5
NM6
NM0
NM1
VIP
VIM
C0
C1
phi1_bar
clk
phi
NM2
phi2
vin2
vin1
vout
phi1_bar

Reference Subtraction Circuit



Clock Phases and circuit (phi2 is 'high' only when phi1 is 'low' with a margin of t_{NOR} = 1ns)





Choice of Switches:

1. Strong-arm latch:

    - The tail node switch (NM2), clocked at phi1 is NMOS. (had to pass ground, 0V)

    - The output resetting switch (PM2, PM3, PM4, PM5), clocked at phi1 are chosen to be PMOS. (had to pass V_{DD})

2. Reference Subtraction Circuit:

    - Switch passing VIP/VIM: CMOS
    Since differential input can vary from 0 to V_{DD}, a CMOS switch can pass full range voltages.

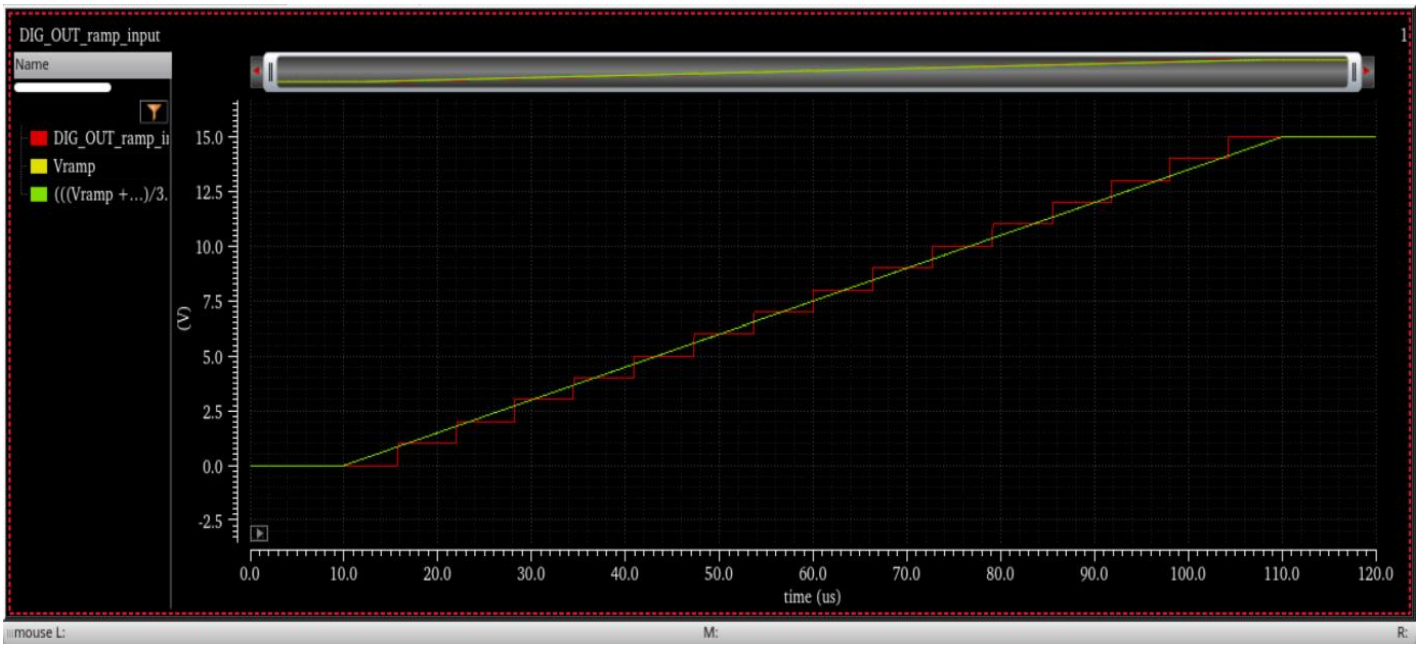
    - Switch passing VRP/VRM: CMOS
    Since $V_{REF,k}^{+}$ and $V_{REF,k}^{-}$ will vary from 0 to V_{DD}, a CMOS switch is used again.

    - Switch passing VCM: NMOS
    Since NMOS can roughly pass voltages until $V_{DD} - V_{TH}$ (which was approx. 1.2 V from simulations), VCM being a “low” signal could be passed by a NMOS switch.

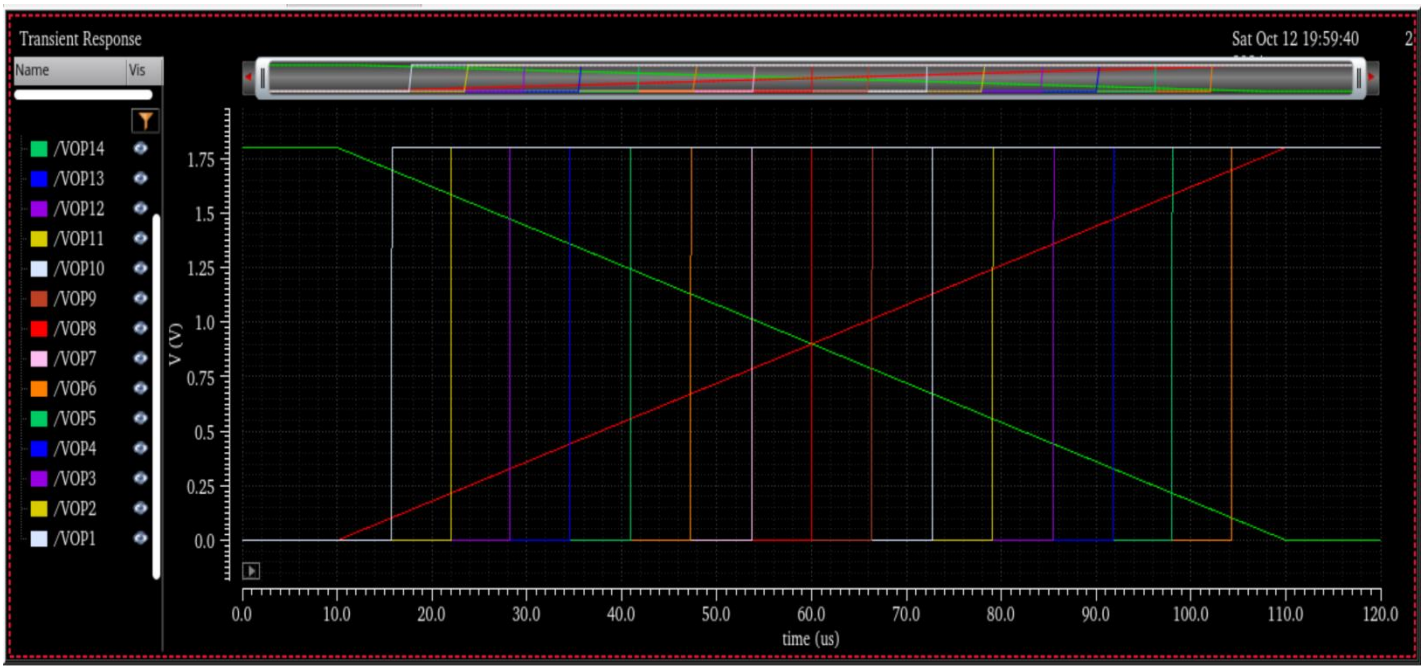
➔ Sizing of CMOS switches was done by calculation of R_{ON}, and choosing for R_{ON}C << T_S / 2.

Input-Output Characteristic (4-bit Flash ADC)

Output for a ramp input:



Differential Inputs and all Output Bits:



Sinusoidal differential Input-Output (4-bit ADC):

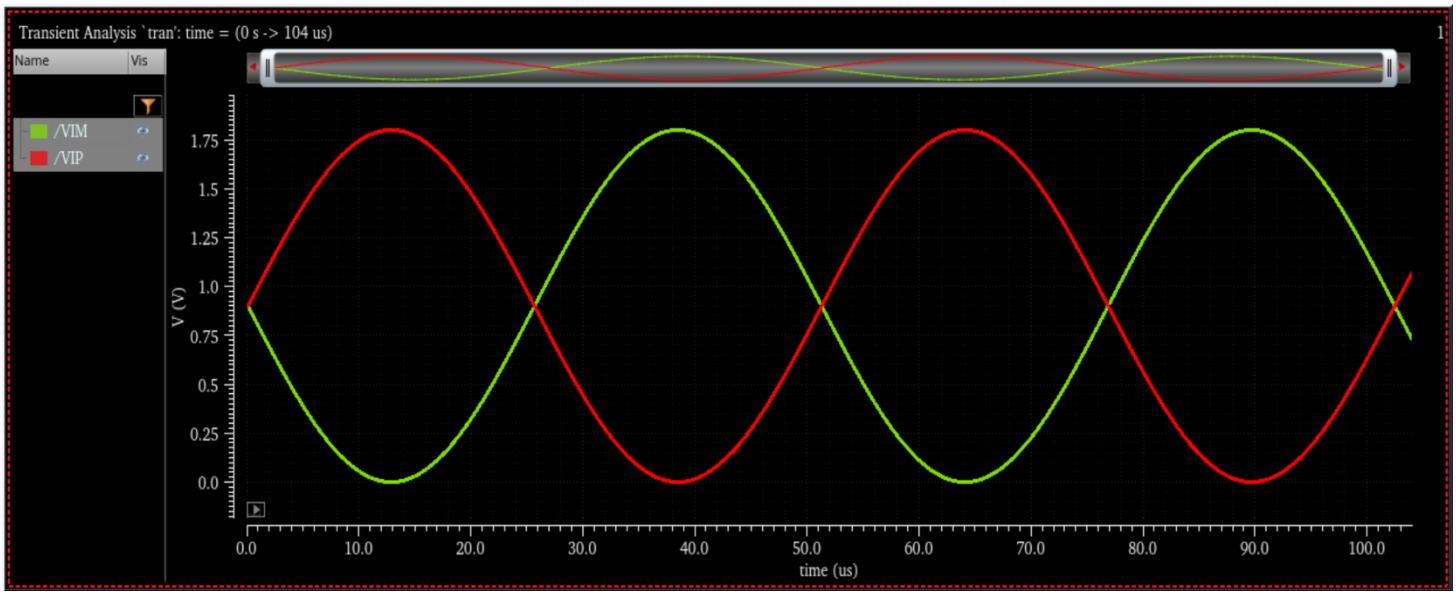
1. Low frequency input

Input frequency (f_{in}) = (1/1024) * 20MHz = 19531.25 Hz

$v_{ip} = 0.9 + 0.9\ \sin(2\pi f_{in} t)$

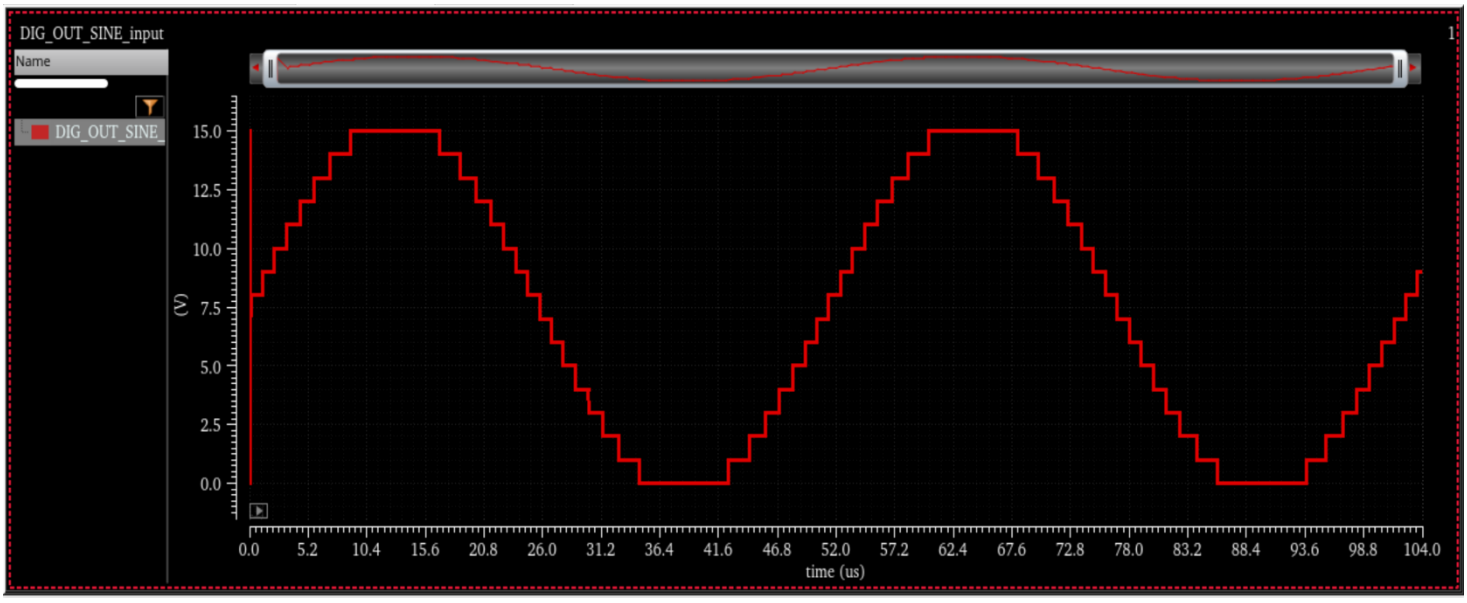
$v_{im} = 0.9 - 0.9\ \sin(2\pi f_{in} t)$

INPUT:



OUTPUT:

2. High frequency input (close to Nyquist frequency, f_s / 2)



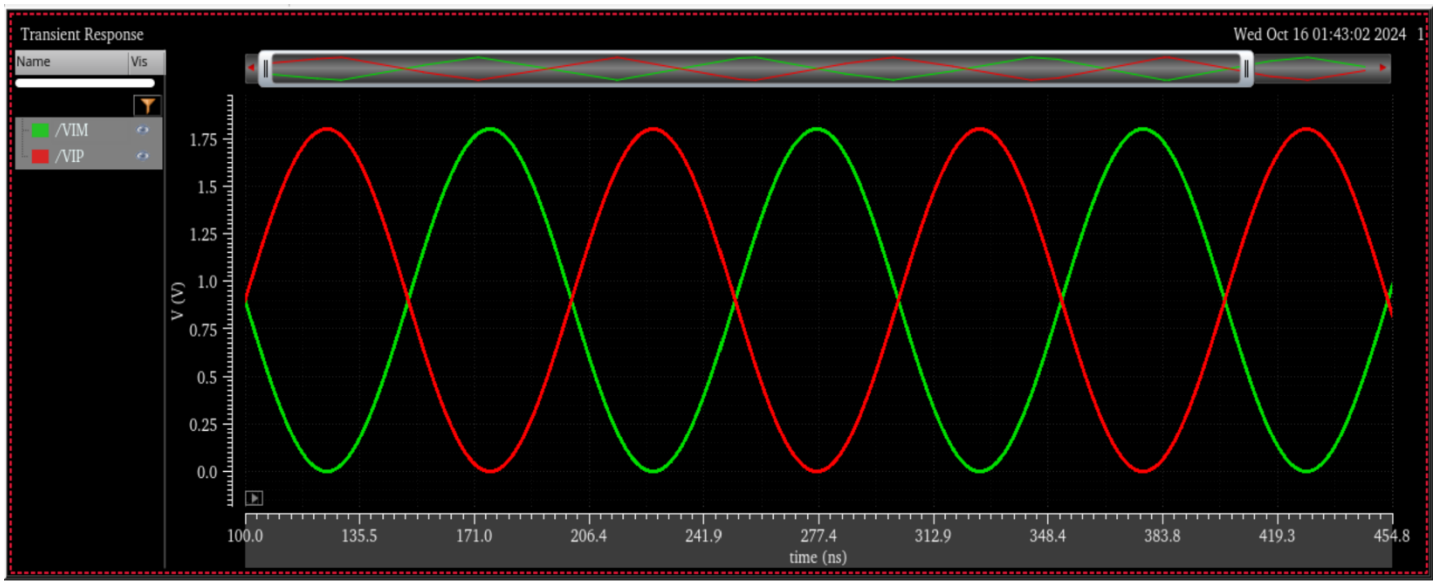
Input frequency (f_{in}) = (507/1024) * 20MHz = 9902343.75 Hz

$v_{ip} = 0.9 + 0.9\ \sin(2\pi f_{in} t)$

$v_{im} = 0.9 - 0.9\ \sin(2\pi f_{in} t)$

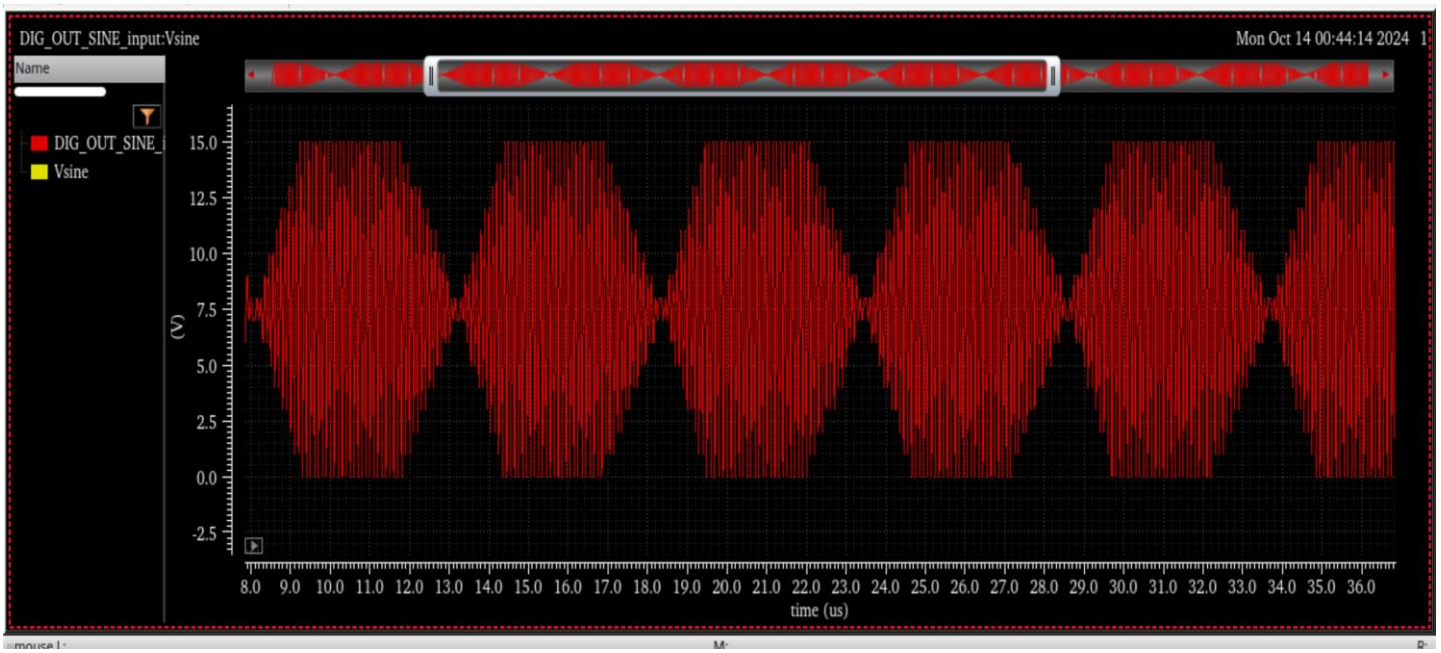
INPUT:

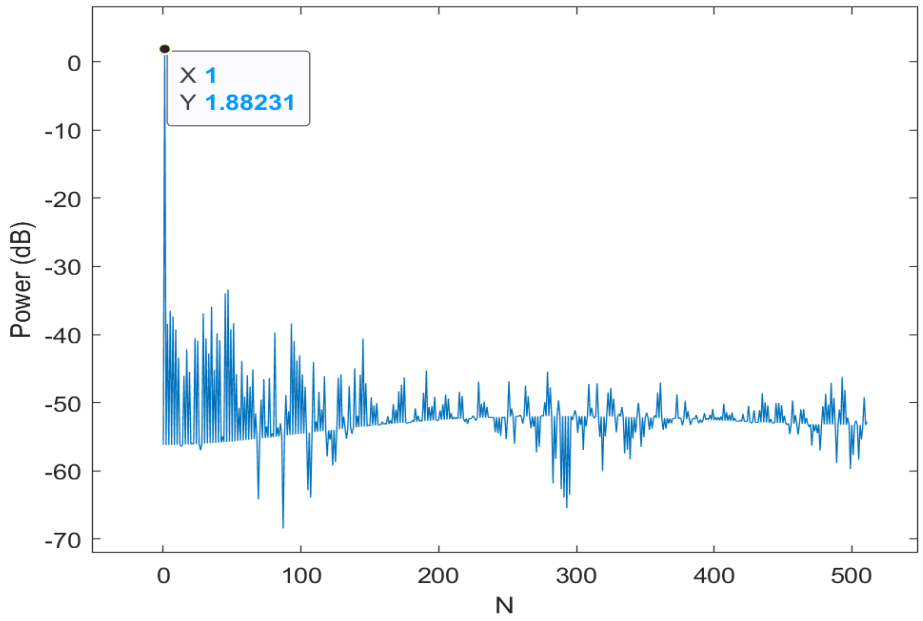
OUTPUT:



SPECTRUMS :

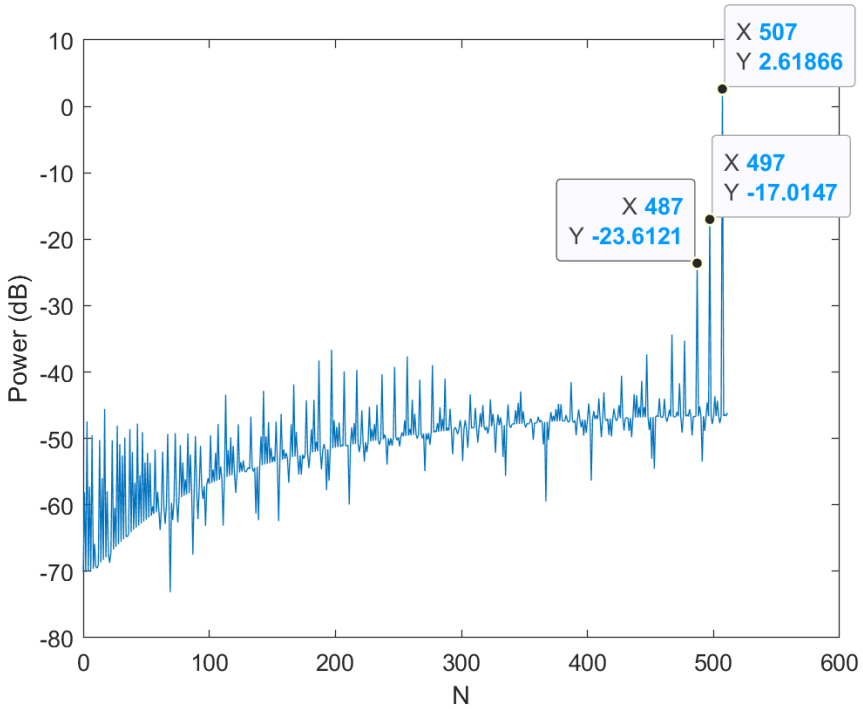
1. 4-bit with low input frequency, bin number = 1





SQNR = 23.6454 dB

2. 4-bit with high input frequency, bin number = 507



SQNR = 17.4441 dB (presence of 3rd and 5th harmonic)
SQNR (improved) = 23.2899 dB (if power in harmonics is also added to signal power)

Method to plot Spectrum and calculate SQNR:

1. Upload the relevant file and define the number of bits, ,

sampling frequency, input amplitude and input frequency.

2. Find the number of the levels and step size from the given number of bits. ($levels = 2^{no.\ of\ bits} - 1$)

3. Read the data from csv file and store them in a matrix.

4. Convert the digital outputs to voltages using mid-rise quantizer rule.

5. Declare the value of “N”, this will decide the number of points in DFT. (in our case N = 1024)

6. Find Fourier transform using FFT and then find the one-sided normalized PSD.

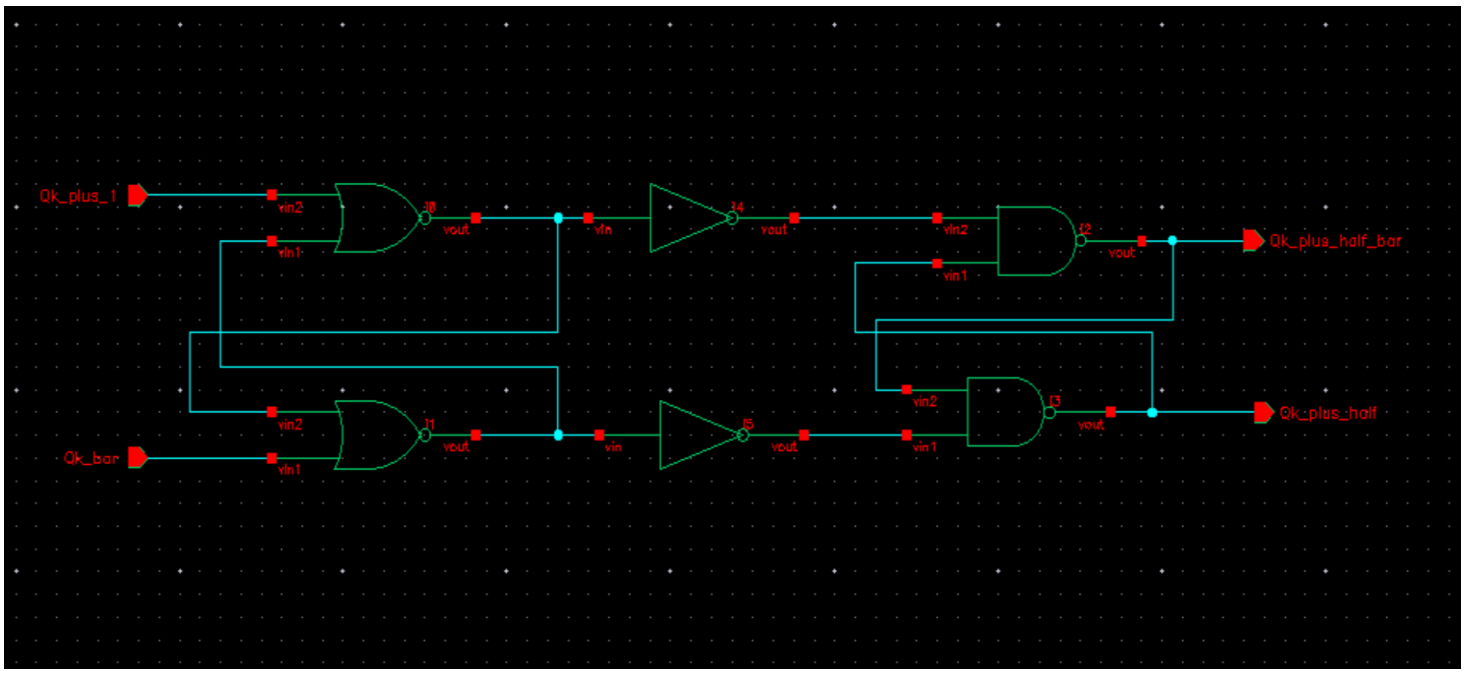
7. Calculate the bin number from N, input and output frequency.

8. For signal power, take the normalized PSD in the input frequency bin.

9. For noise power, add power in all bins and subtract the signal power.

$$SQNR_{dB} = 10 * \log_{10} \frac{signal\ power}{noise\ power}$$

2x Time Interpolation circuit:



1. The above latch was used for doing time-interpolation which is series combination of NOR based SR latch and NAND based SR latch connected through inverters.

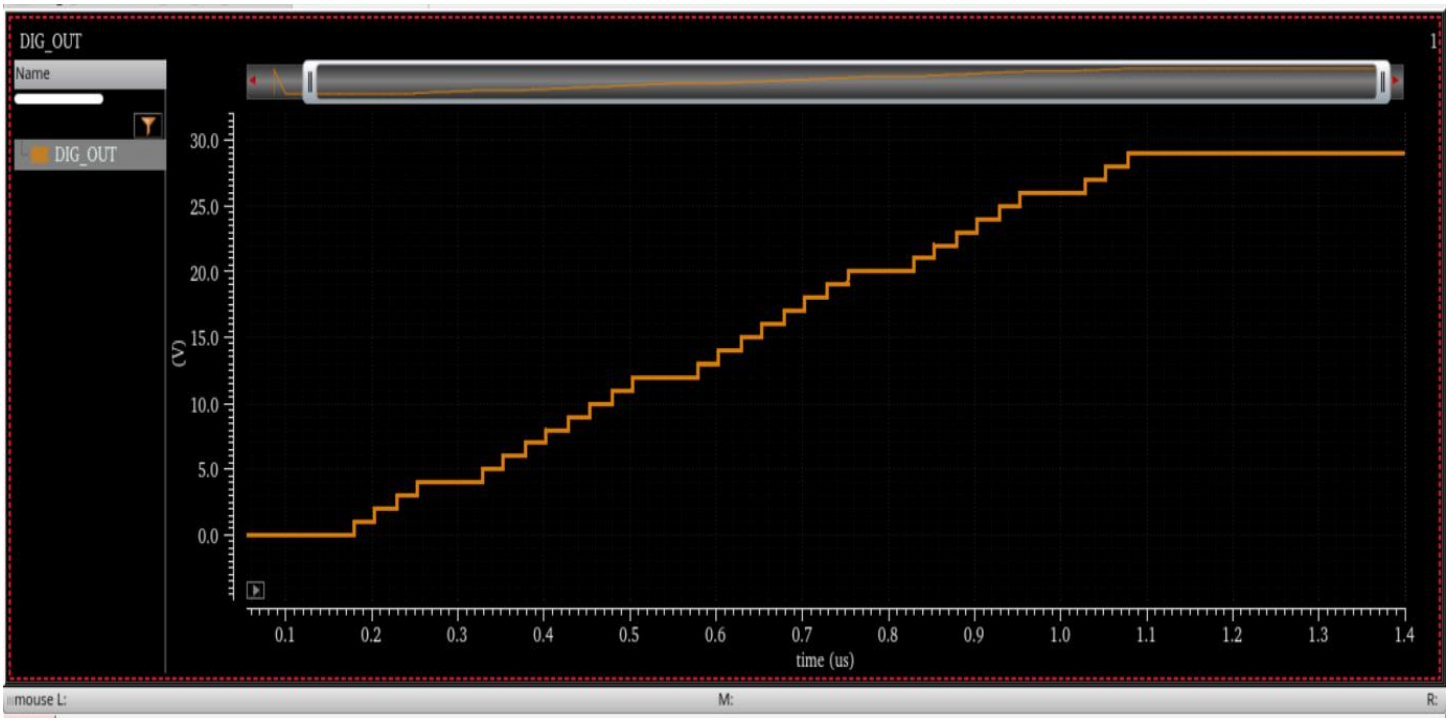
2. The inverters along with NAND based SR latch form a NOR based SR latch; stacking of two NOR based latches was done to handle the scenario when all the outputs are charged to V_{DD}. (since NOR based latch will lose its information in reset phase)

3. The output is Qk_plus_half, which is our time interpolated bit. Using this interpolation, we can get 29 digital bits at max. because first and last comparator outputs cannot be interpolated. Hence, ENOB will always be less than 5 bits.

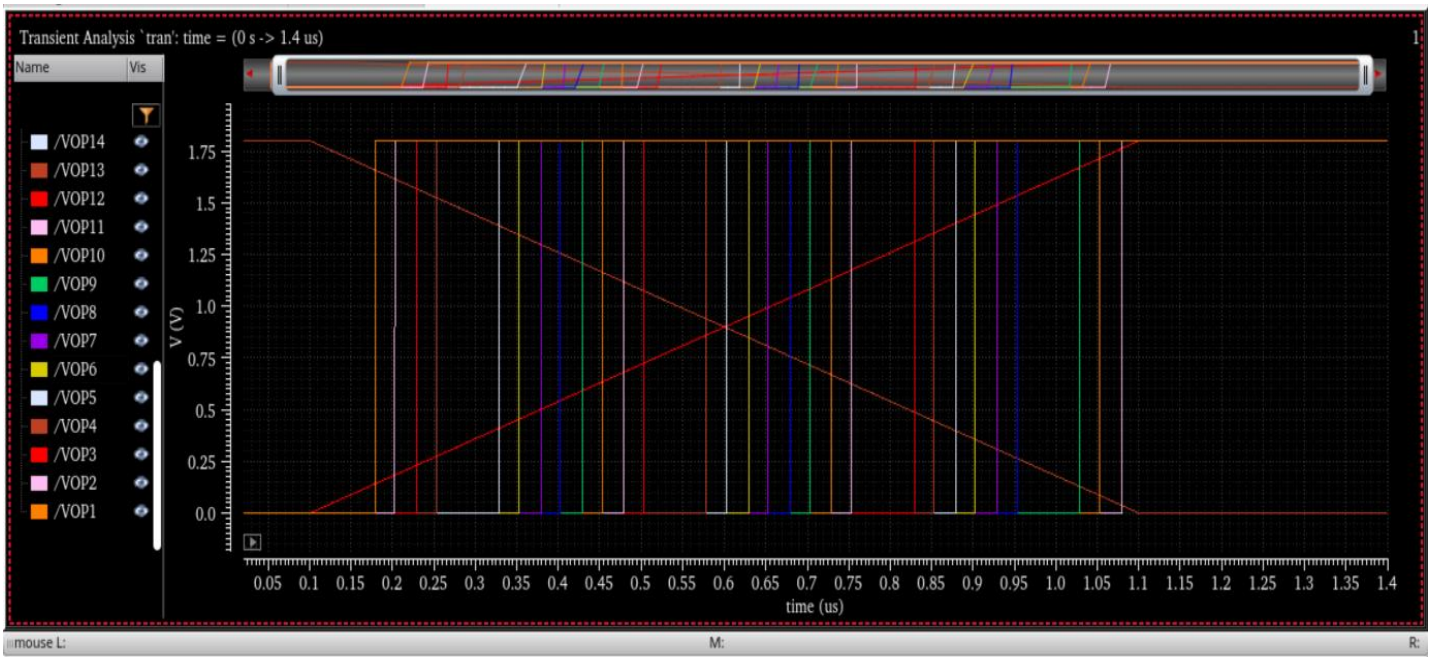
Input-Output Characteristic (2x time interpolated 4-

bit Flash ADC)

Output for a ramp input:



Differential input and all Output Bits: Sinusoidal differential Input-Output (2x interpolation):



1. Low frequency input

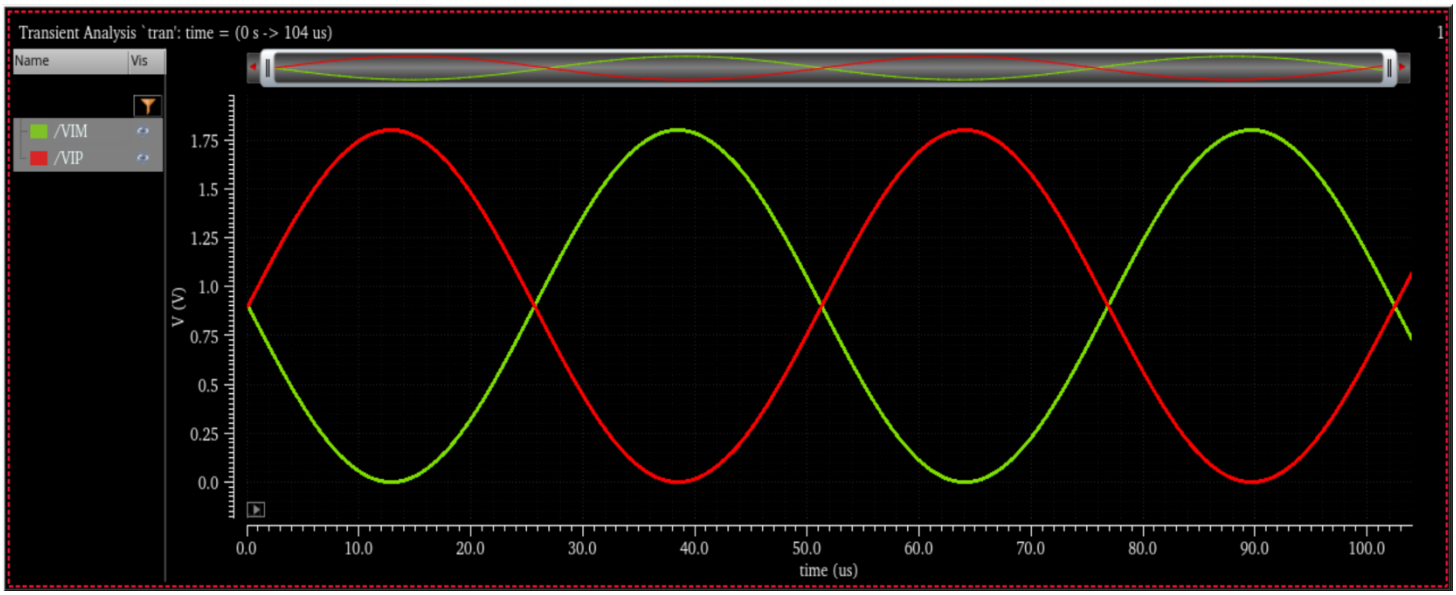
Input frequency (f_{in}) = (1/1024) * 20MHz = 19531.25 Hz

$v_{ip} = 0.9 + 0.9\ \sin(2\pi f_{in} t)$

$v_{im} = 0.9 - 0.9\ \sin(2\pi f_{in} t)$

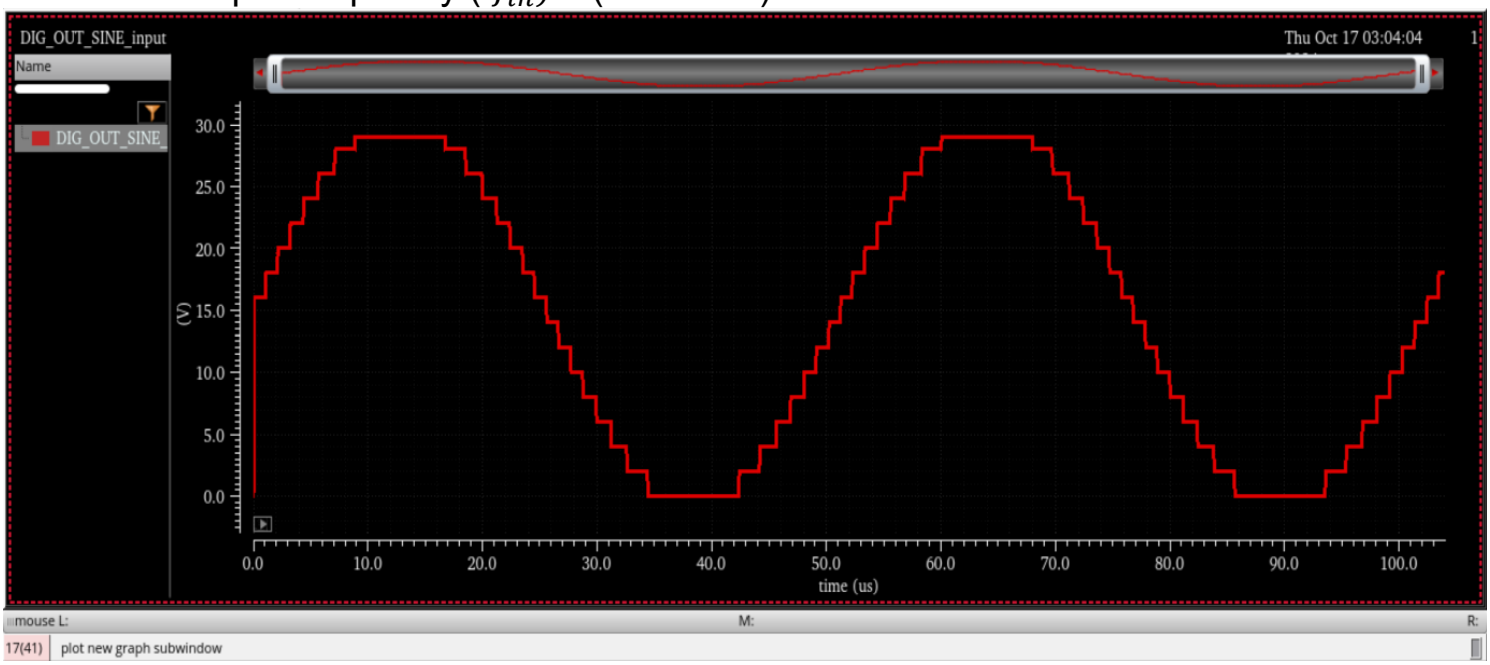
INPUT:

OUTPUT: (we see interpolated bits but with high non-linearity)



2. High frequency input (close to Nyquist frequency, f_s / 2)

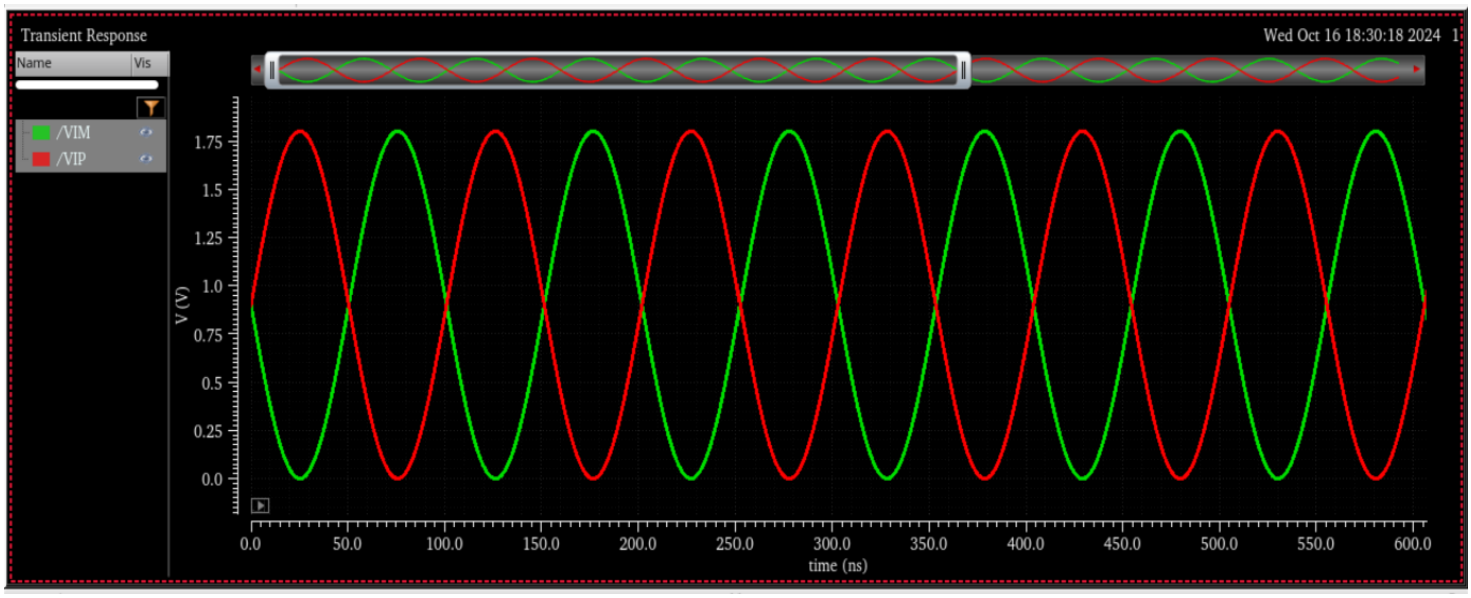
Input frequency (f_{in}) = (507/1024) * 20MHz = 9902343.75 Hz



$$v_{ip} = 0.9 + 0.9\ \sin(2\,\pi f_{in} t)$$
$$v_{im} = 0.9 - 0.9\ \sin(2\,\pi f_{in} t)$$

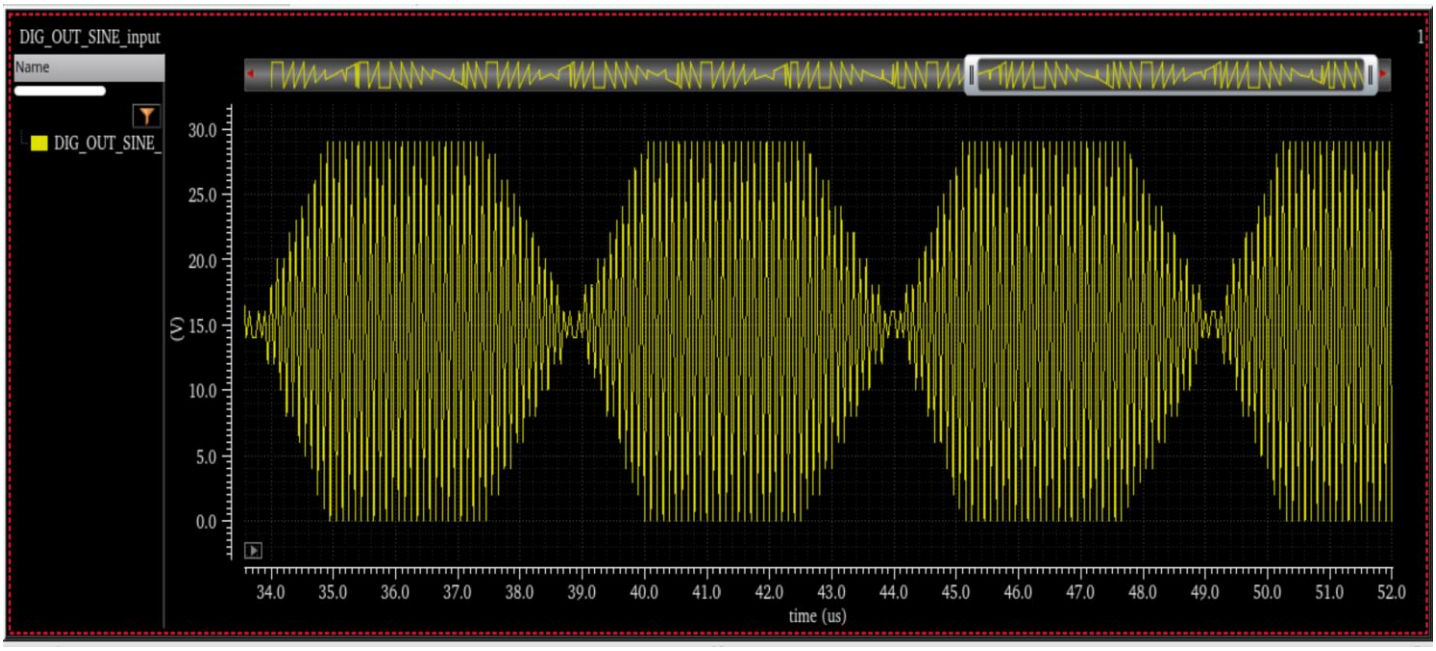
INPUT:

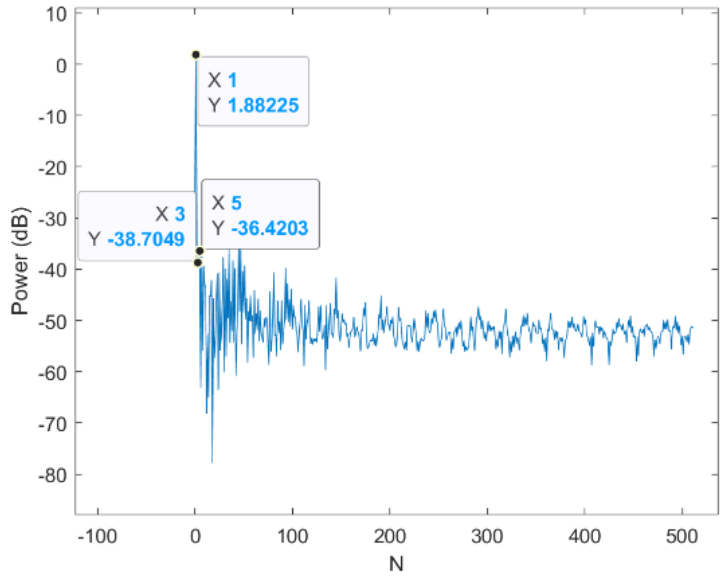
OUTPUT:



SPECTRUMS:

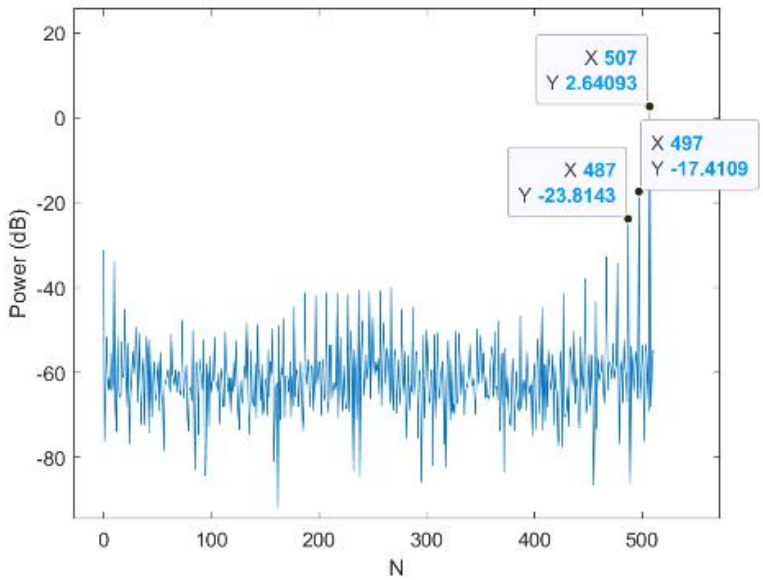
1. 4-bit (2x interpolation) with low input frequency, bin no. = 1



SQNR = 

21.963 dB (due to high quantization noise because of rapid switching of output of interpolator, my circuit could not hold its decision for more than one clock period)

2. 4-bit (2x interpolation) with high input frequency, bin no. = 507

SQNR = 

18.4267 dB
(presence of 3rd and 5th harmonic)
SQNR (improved) = 26.9968 dB (if power in harmonics is also added to signal power)