EE698I: MIXED SIGNAL IC DESIGN

END-SEM PROJECT

Design of 6-BIT SAR ADC

(180 nm PDK)

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Design Choices:

1. Bits for ADC: 6 bits (given by ENOB specification)

2. Switching scheme for DAC: Monotonic switching scheme
   Monotonic switching scheme has least power consumption (discussed in lectures), hence the choice.

3. Input differential pair for SA latch: PMOS input differential pair.
   In monotonic switching scheme, after each comparison, we ground a capacitor in either half. As a result, the input to the SA latch should decrease.
   To verify this intuitive phenomenon, I probed the input nodes after each comparison, and observed the same. Hence, the choice of PMOS input pair.

4. Minimum Unit Capacitor value: 20fF
   For "low" resolutions, we find the minimum sampling capacitor to match the thermal noise requirement, and then find the minimum unit capacitor. The value comes out to be very small when compared to the minimum capacitor value that can be fabricated. So, we keep the minimum unit capacitor to be equal to 20fF so that it is mainly quantization noise limited.

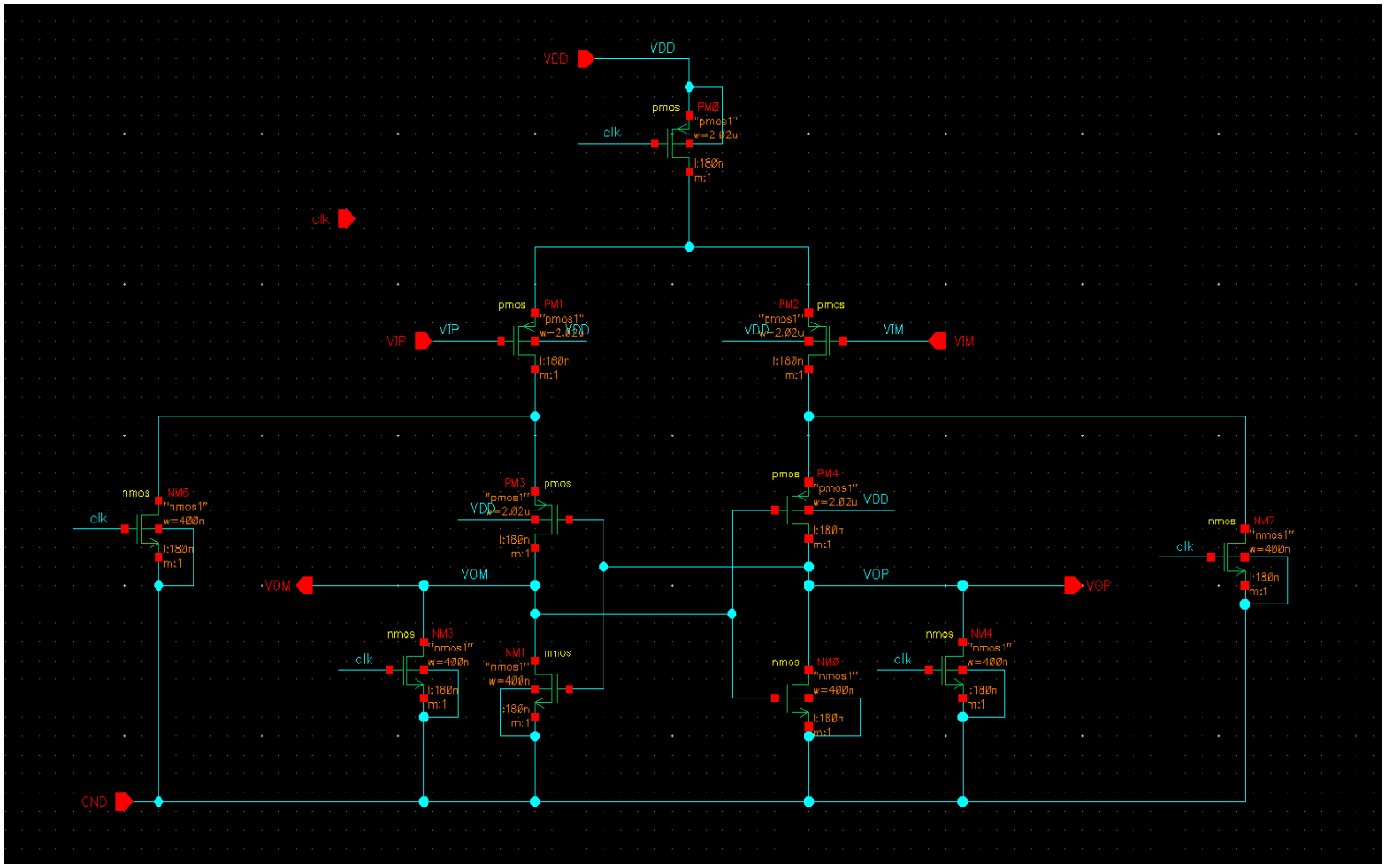
5. Sizing of the CMOS_sampler:
   In the sampler, we need to drive large capacitance with very less delay. So, the width of NMOS was 400nm and PMOS was 2u ($\beta = 5\ for\ t_{pLH} = t_{pHL}$). This is to reduce delay while sampling input and feeding to SA latch for comparison.

6. Delay in reset of SA latch: 8ns (valid signal is delayed by 8ns)
   Basically, comparator should be fired for next cycle only when previous comparison output has settled, phi signals are generated and required capacitors are grounded.
   This gives total delay in comparison as

Total delay = max (delay in phi generation, delay in output registers) + delay of digital logic to switch the caps + comparison delay of SA latch = 150ps + 200ps + comp_delay
Since sampling frequency is quite low, we have ample time for each comparison, hence a choice of 8ns.

7. D flip flop with reset: In in-built digital library, we only have D flip flop without reset. But we need to reset $\varphi_1, \varphi_2, \varphi_3, \varphi_4, \varphi_5, \varphi_6$ to logic 0, so modified the Verilog a code to add a reset pin.

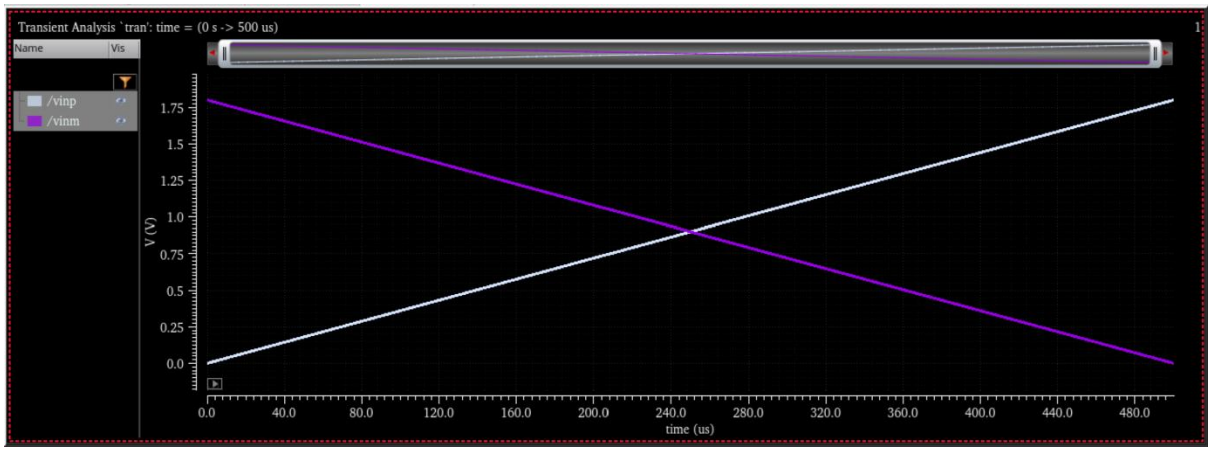
STRONG-ARM LATCH CIRCUIT



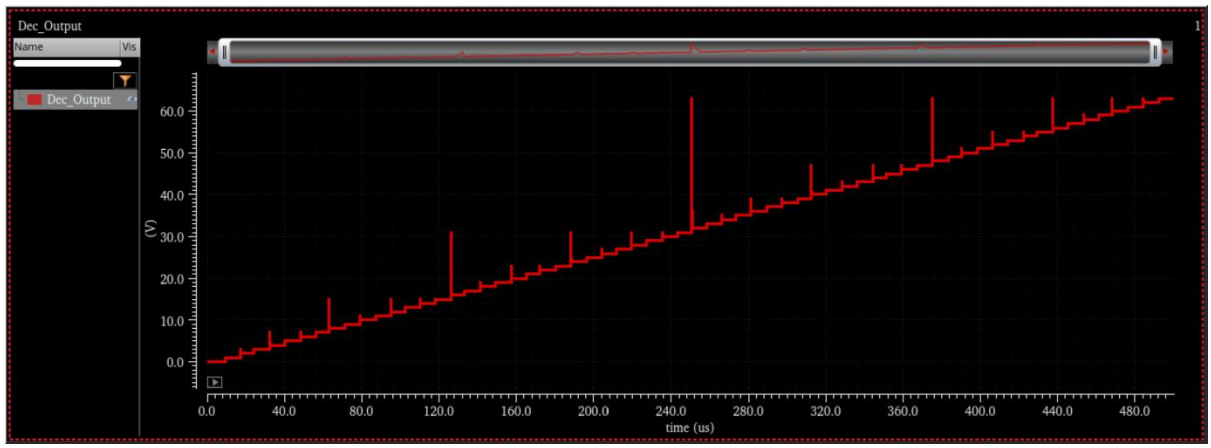
Sizing of transistors follow similar ideology as of CMOS_sampler. NMOS sized at minimum sizes and PMOS made 5x to ensure $t_{pLH} = t_{pHL}$.

Input-Output Characteristics (6-bit SAR ADC)

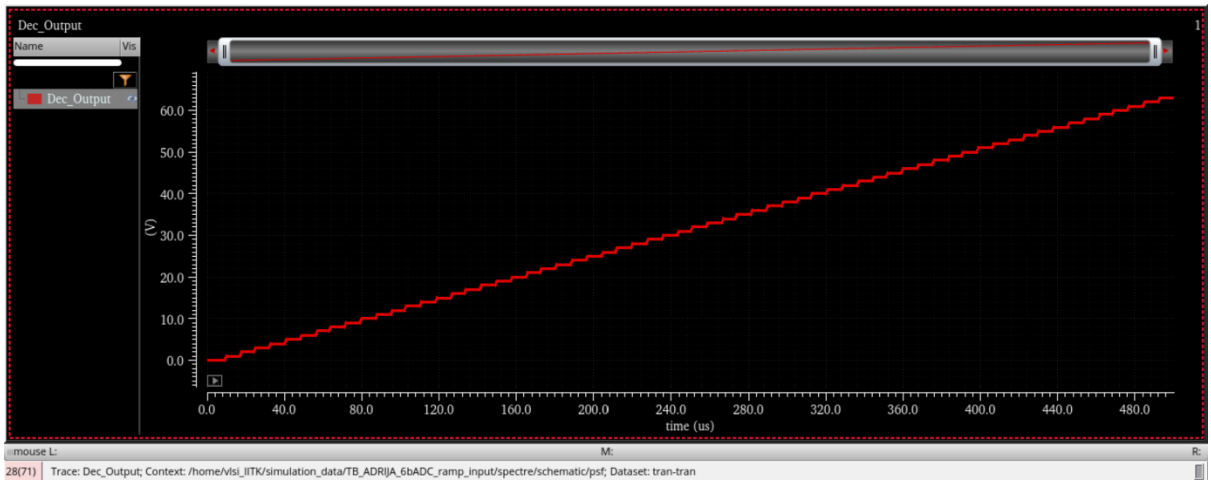
Differential Ramp Input:



Output for a ramp input:



Output for ramp input (after strobing):



Strobing the data removes spurious spikes as we sample at a strobe period = time period of sampling clock = 1us.

Sinusoidal differential Input-Output (6-bit SAR ADC):

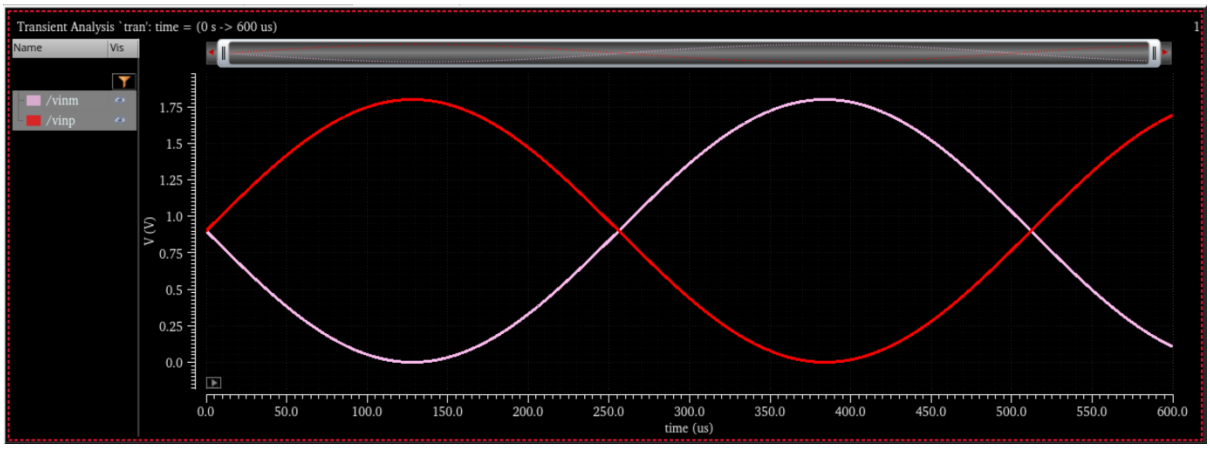
1. Low frequency input

Input frequency (f_{in}) = (9/1024) * 1MHz = 8789.0625 Hz

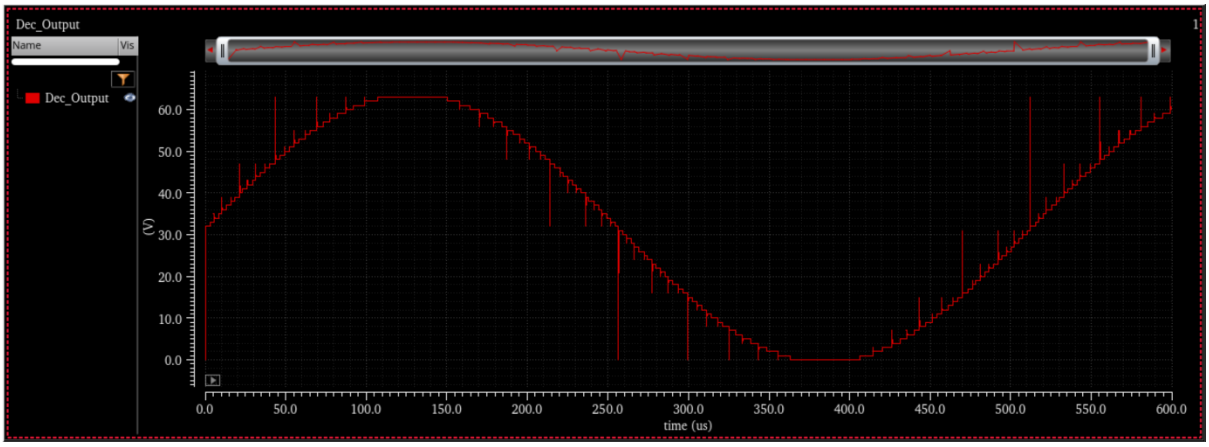
$v_{ip} = 0.9 + 0.9\ \sin(2\pi f_{in} t)$

$v_{im} = 0.9 - 0.9\ \sin(2\pi f_{in} t)$

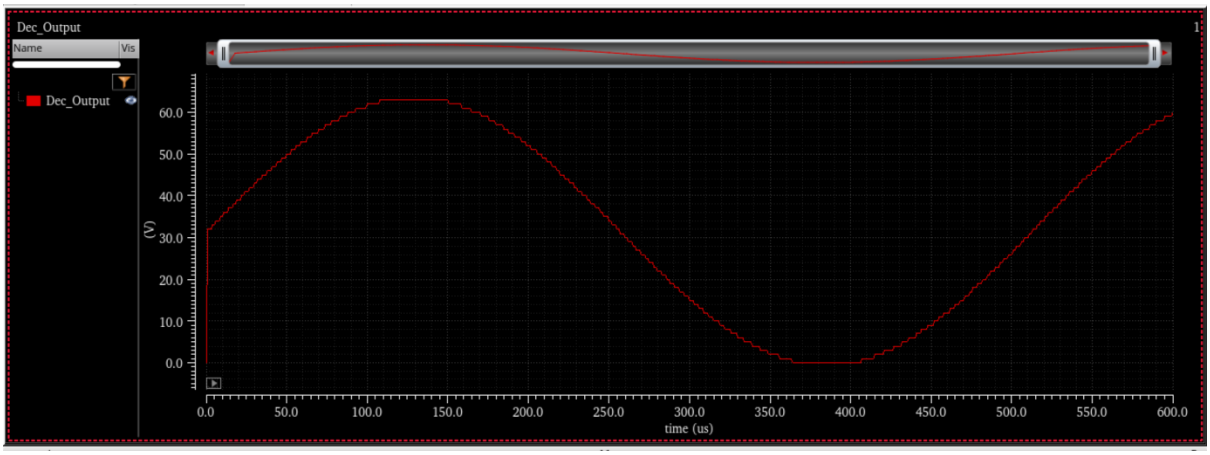
INPUT:



OUTPUT:



OUTPUT (when strobed for refining):



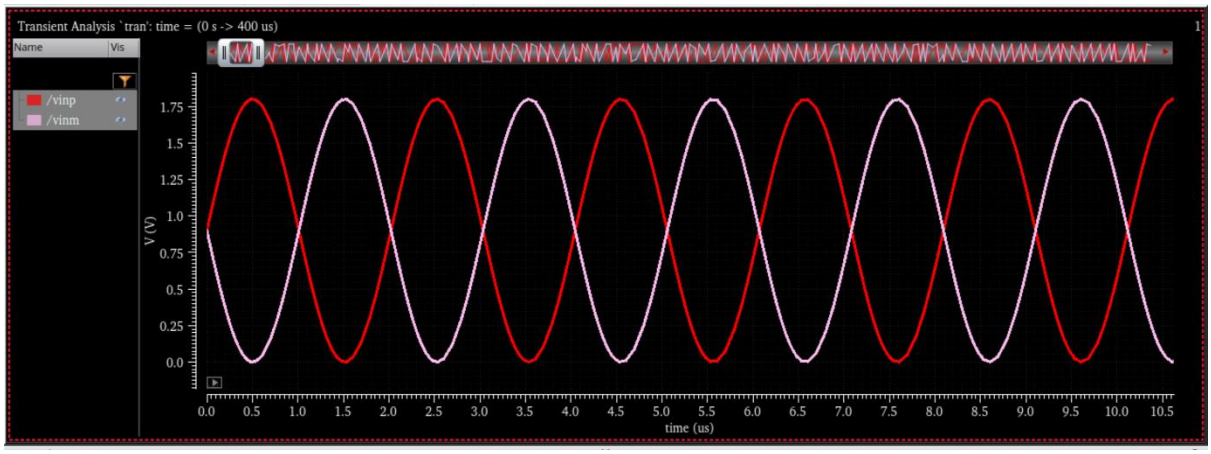
2. High frequency input (close to Nyquist frequency, f_s / 2)

Input frequency (f_{in}) = (503/1024) * 1MHz = 491210.9375 Hz

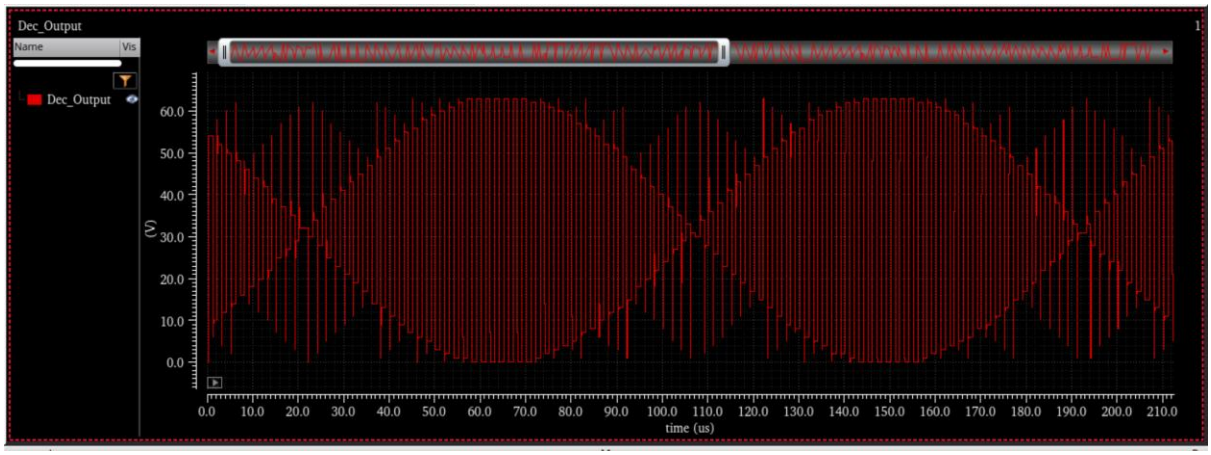
$v_{ip} = 0.9 + 0.9 \sin(2\pi f_{in} t)$

$v_{im} = 0.9 - 0.9 \sin(2\pi f_{in} t)$

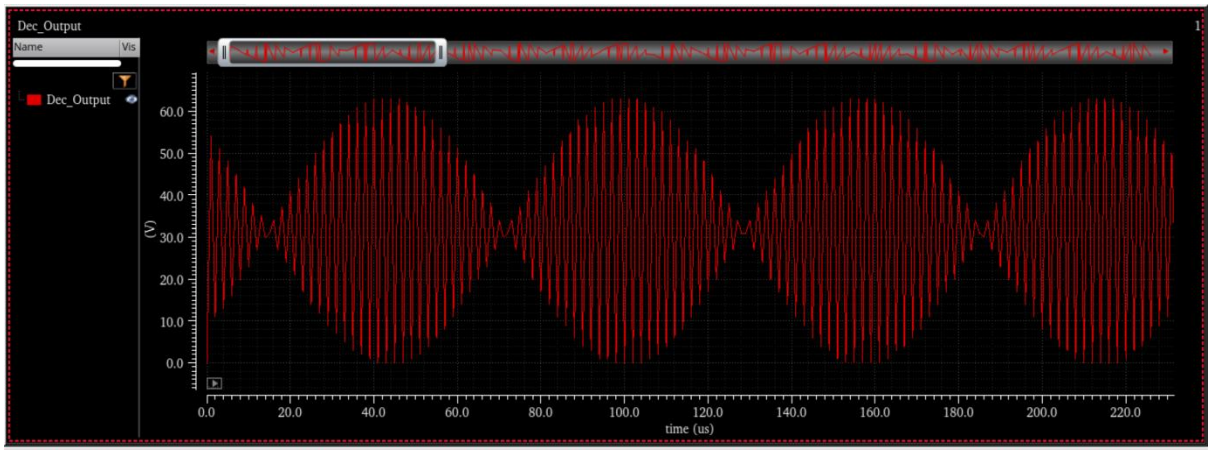
INPUT:



OUTPUT:

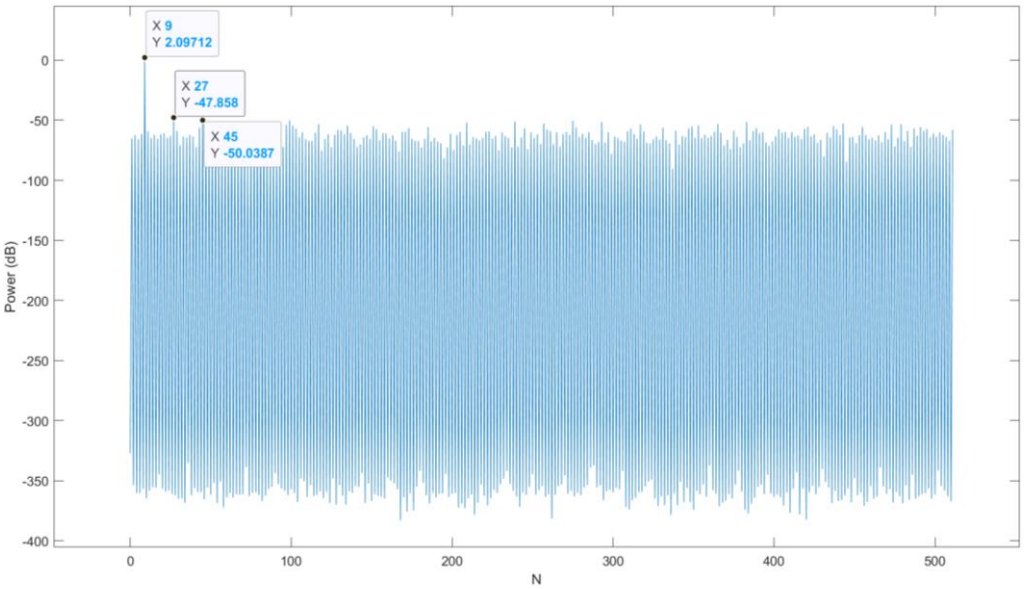


OUTPUT (when strobed for refining):



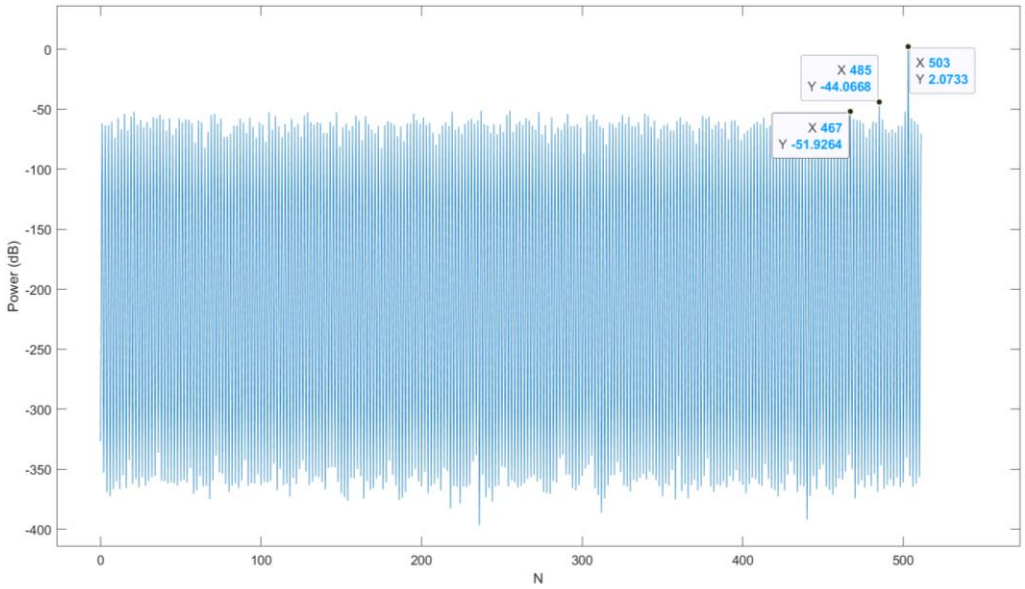
SPECTRUMS (differential sinusoidal input):

1. Low input frequency = (9/1024) *1MHz, bin number = 9



SQNR = 37.445 dB
ENOB = 5.9475

2. High input frequency = (503/1024) *1MHz, bin number = 503



SQNR = 37.3787 dB
ENOB = 5.9365