Project – 1

DLL (Delay Locked Loop) Design

EE698G

Submitted by : ADRIJA BERA

210071

Specifications to be met :

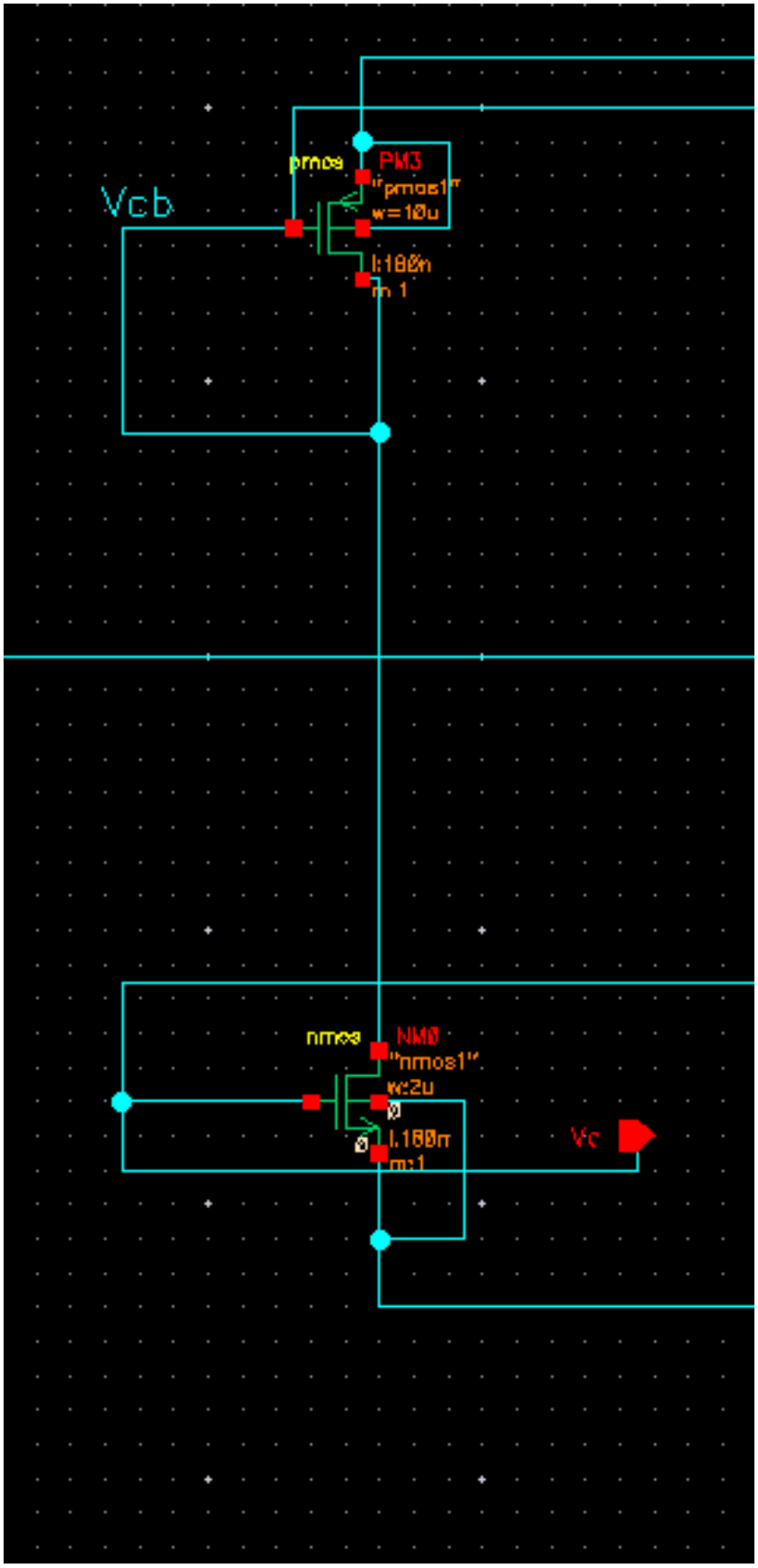
Reference frequency : 600 MHz to 700 MHz

Static phase Offset : ≤ 25ps

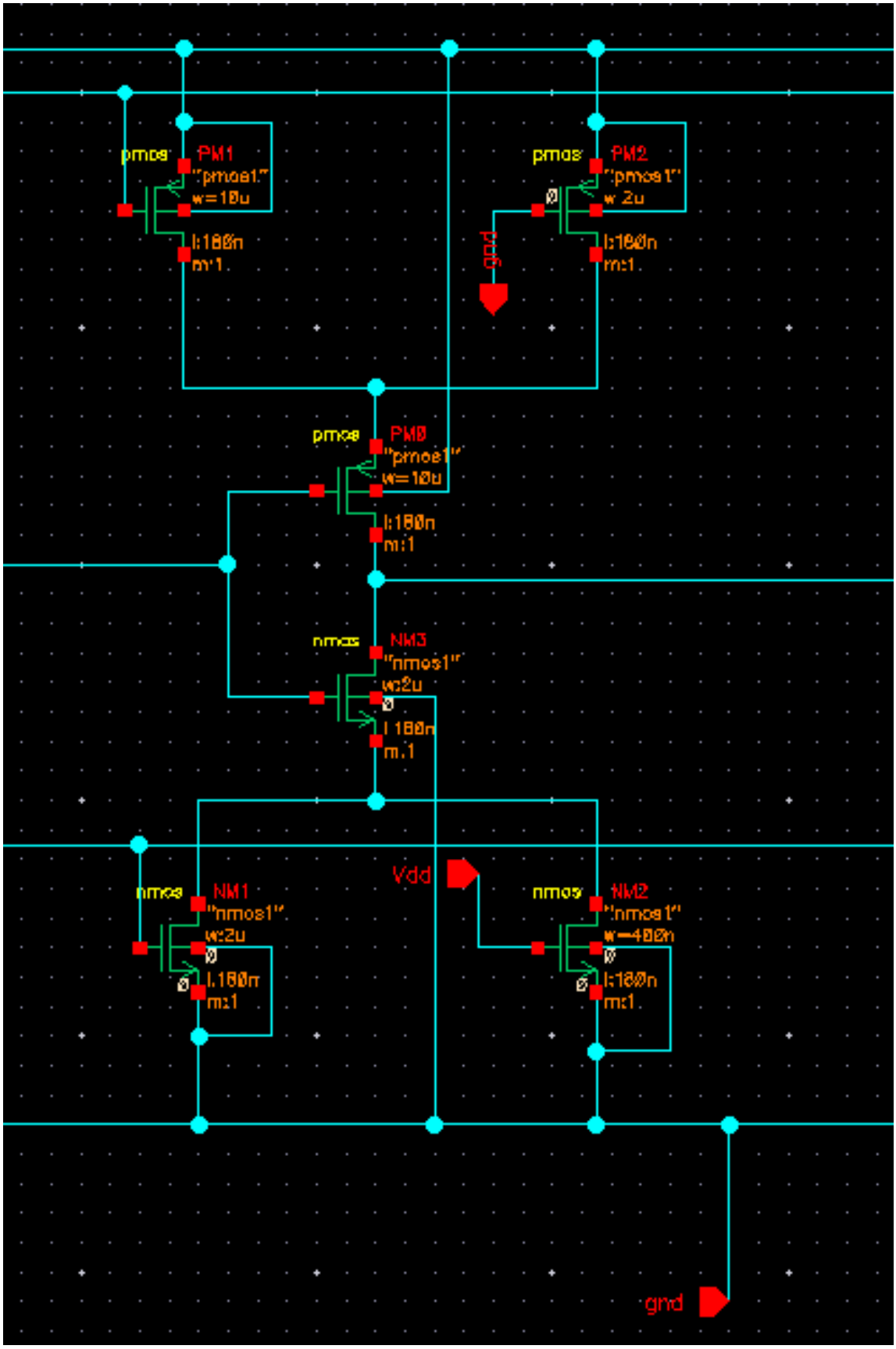
All transistors are used from gpdk180 library , with supply voltage as 1.8V.

SCHEMATICS :

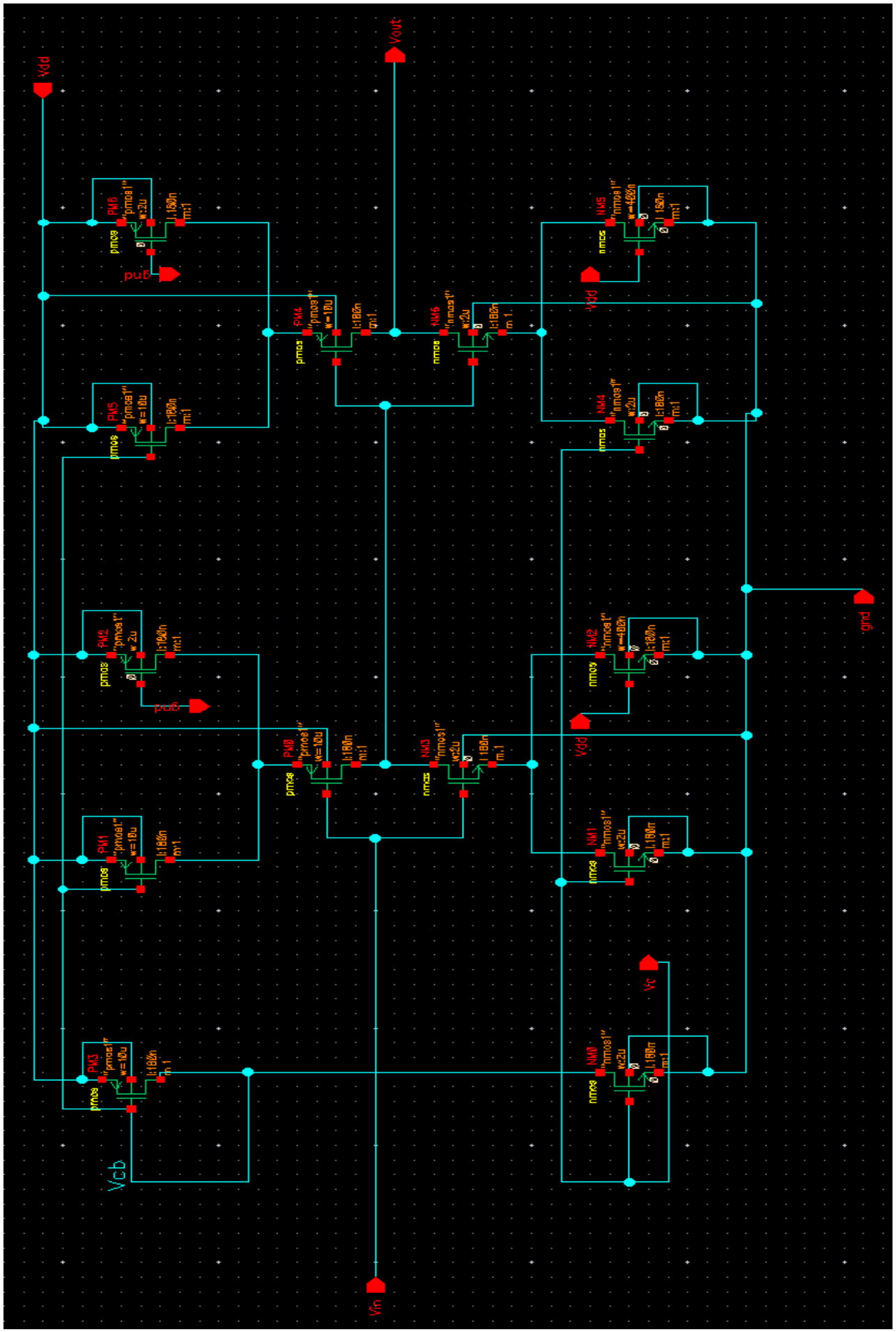
1. Bias Circuit for VCDU :



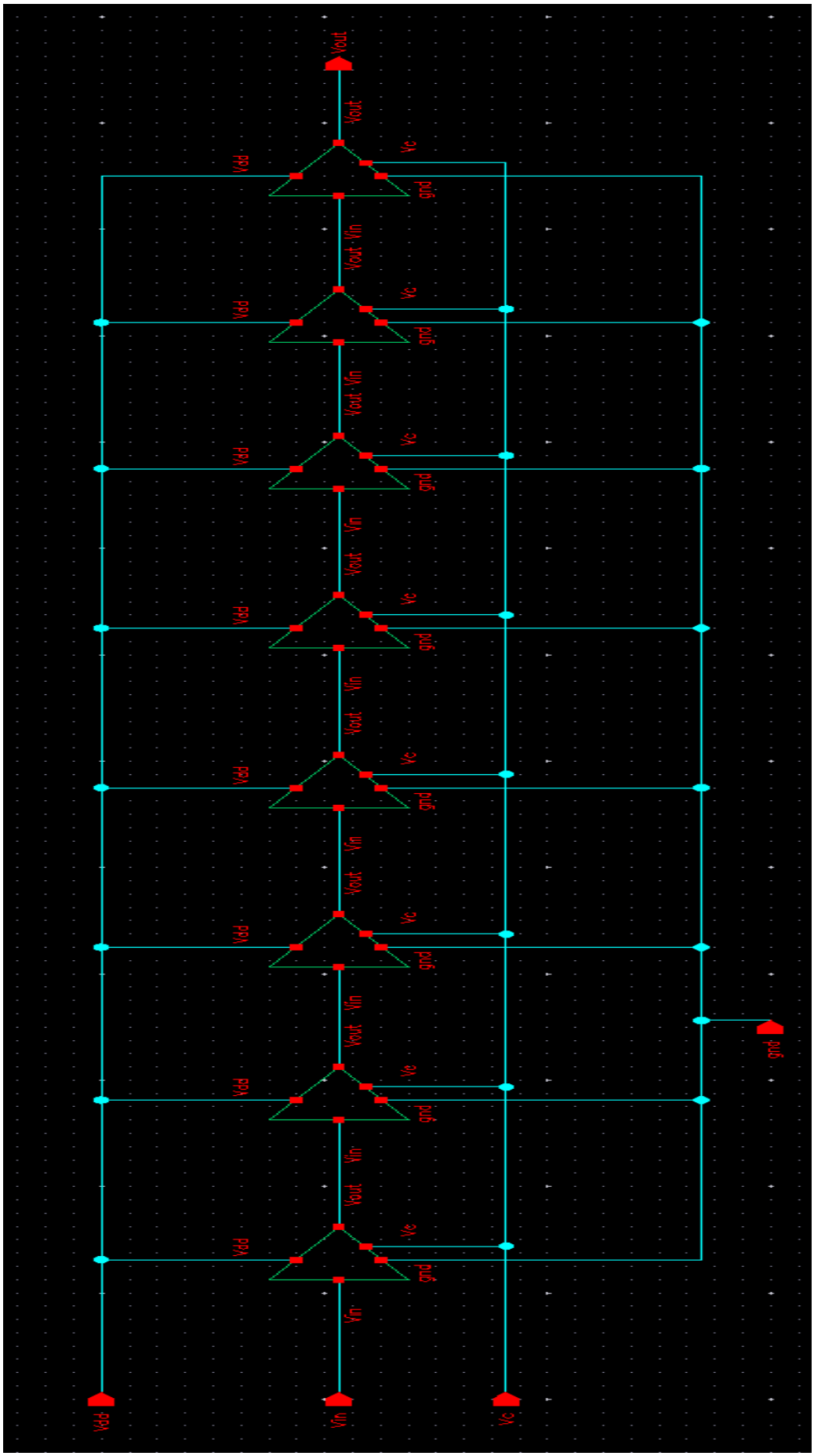
2. Current starved Inverter



3. Buffer (based on above architecture)

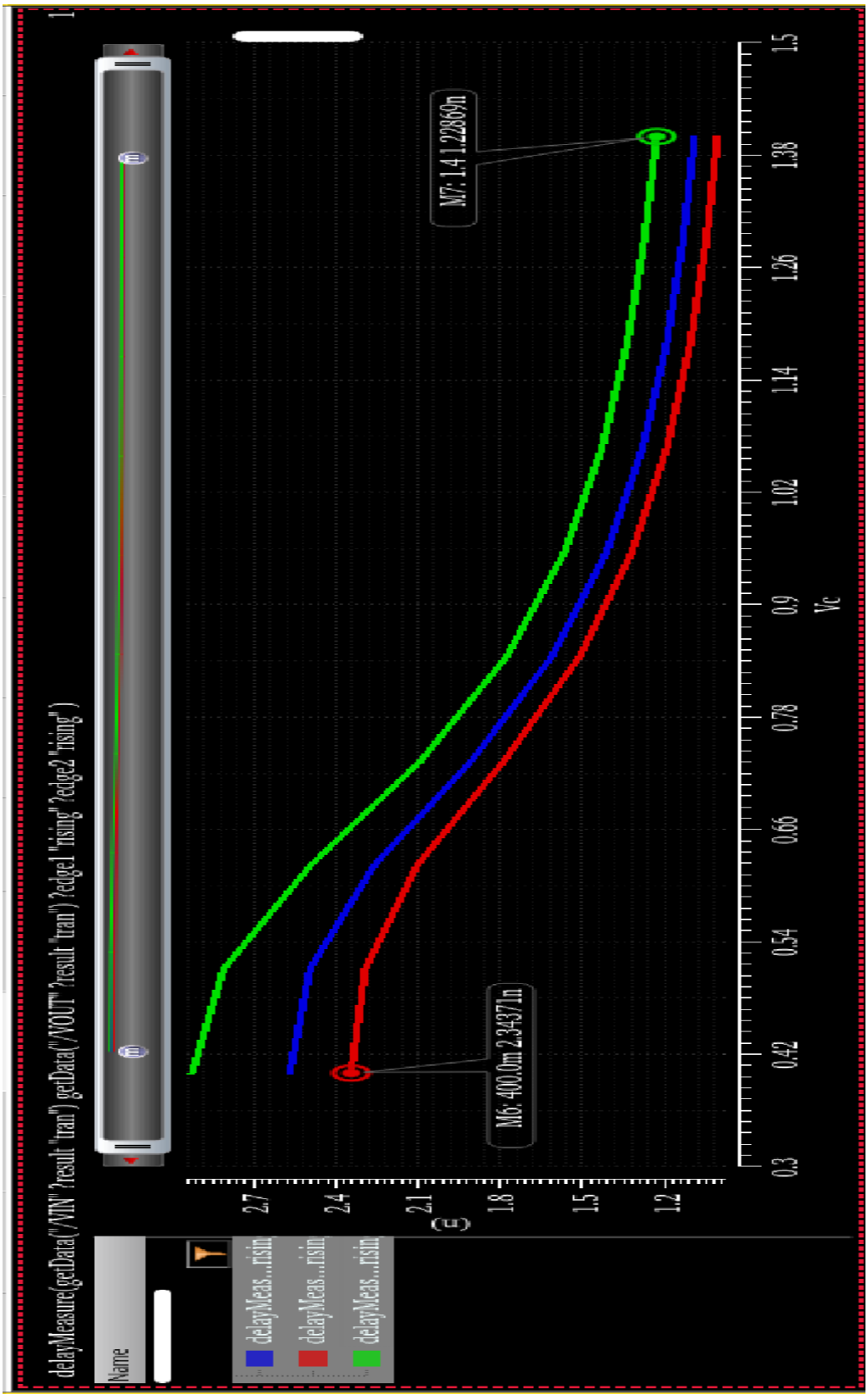


4. Final VCDL symbol view (8 VCDUs are cascaded together)

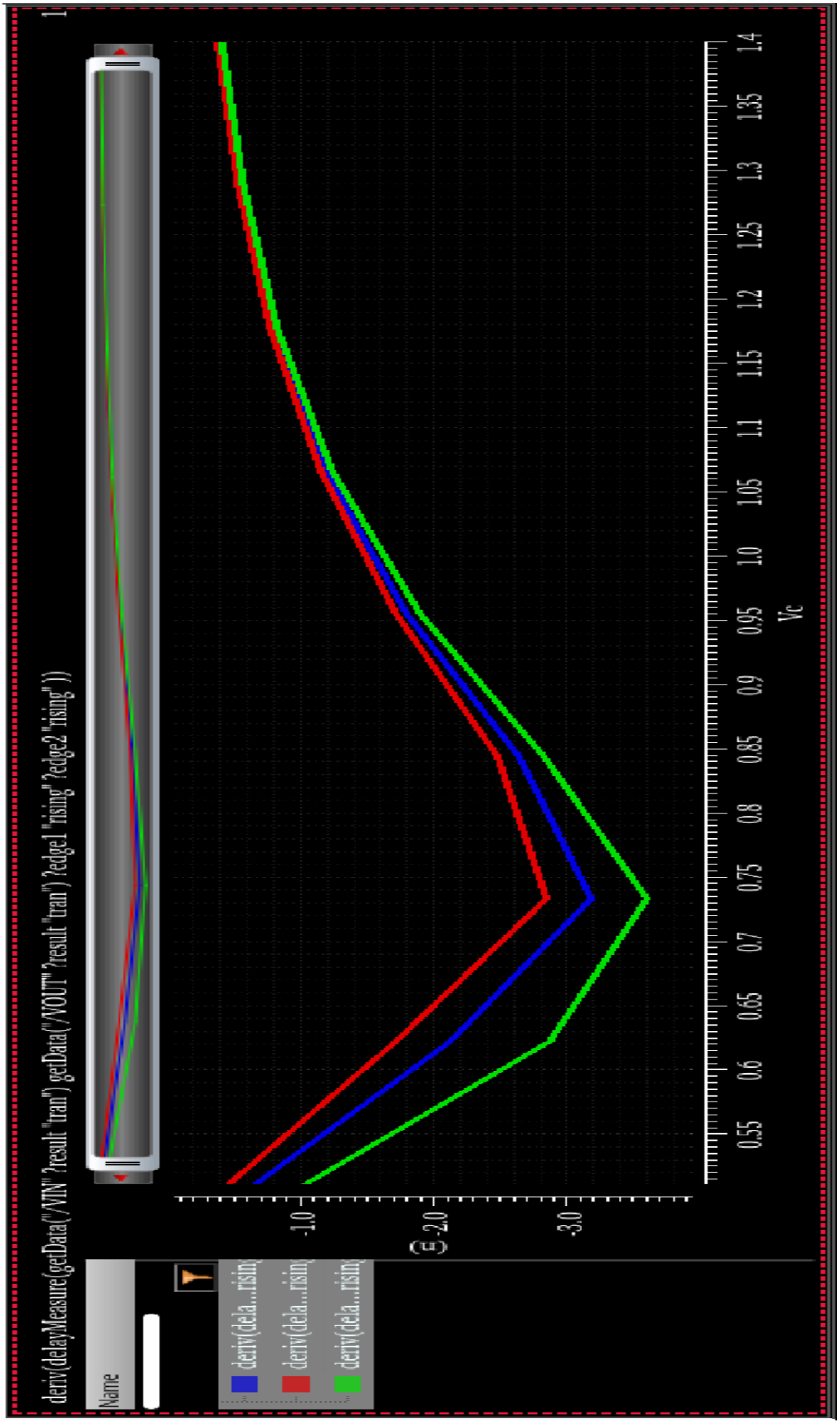


Plot 1 : tp vs Vc plot for all corners
Min frequency = 426.673 MHz
Max frequency = 813.874 MHz

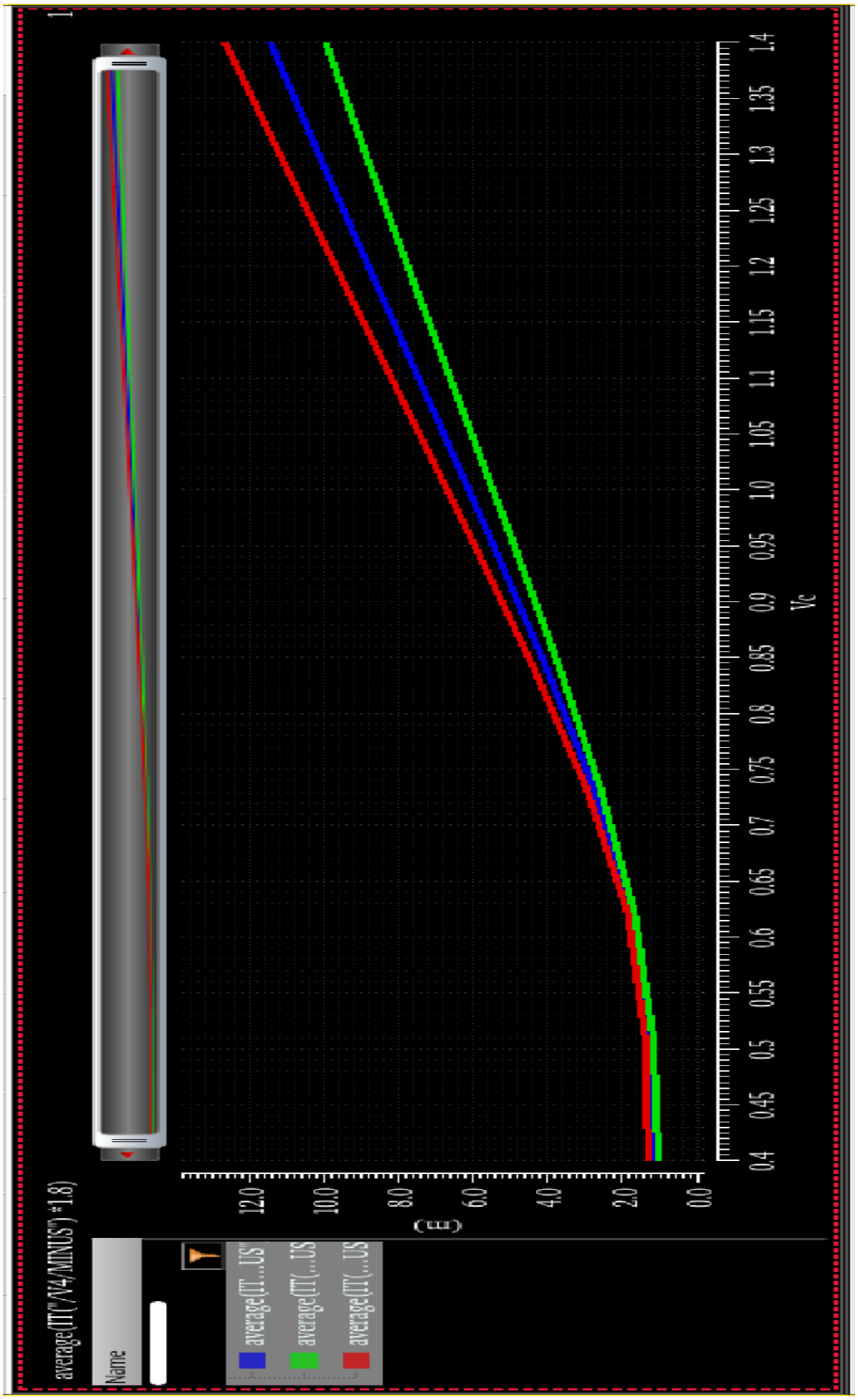
Red : fast **Blue : nominal** **Green : slow**



Plot 2 : Kdl vs Vc for all corners



Plot 3 : Pdl vs Vc for all corners

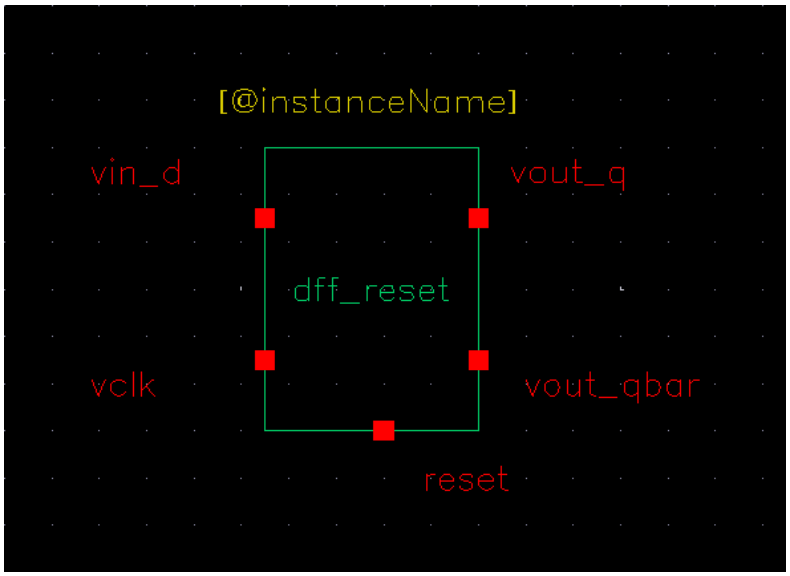


Schematics:

5. D_FF with asynchronous reset :

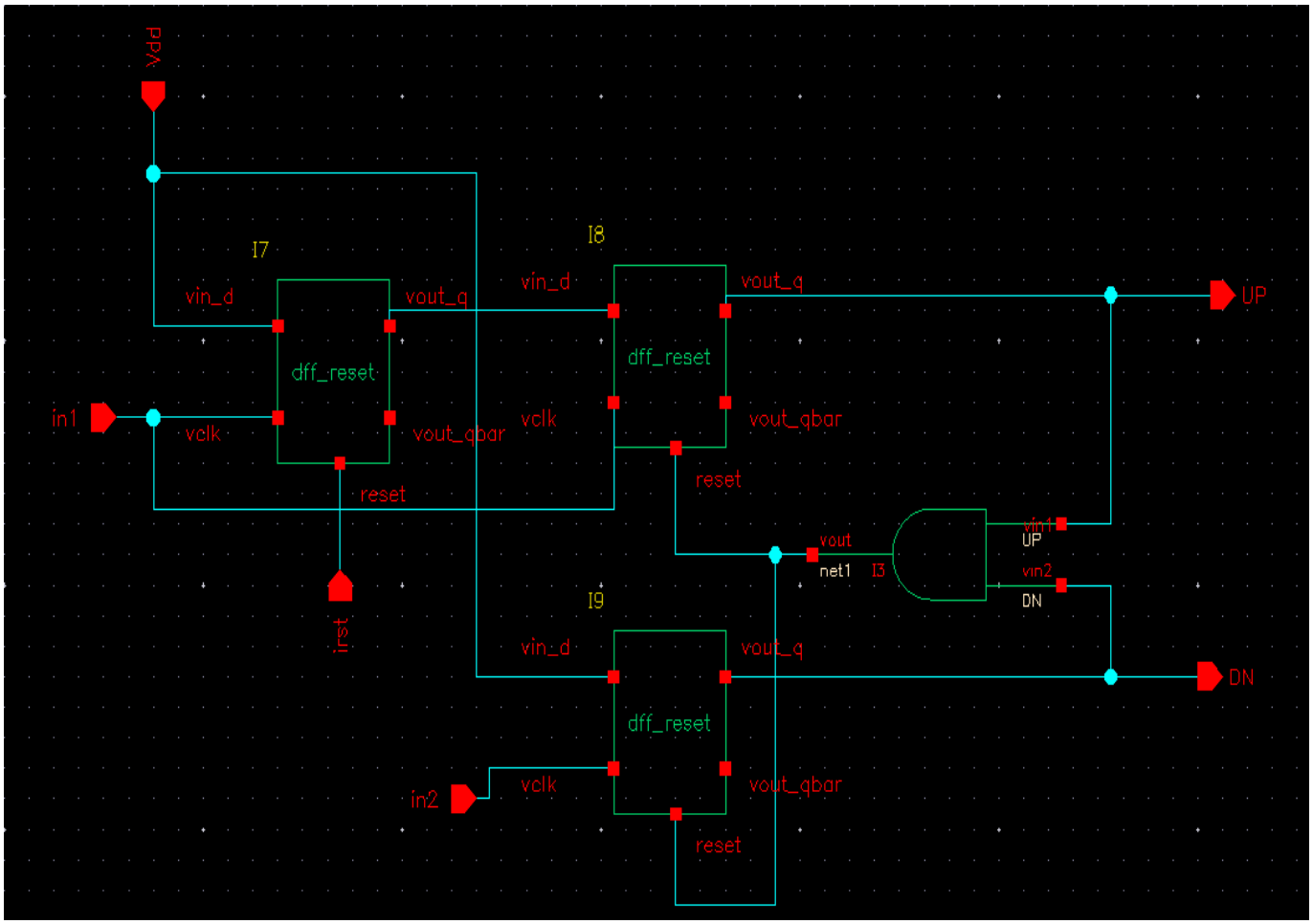
The following modified code was used to obtain D_FF with asynchronous reset option.

```
// VerilogA for dll_design, dff_reset, veriloga

`include "constants.vams"
`include "disciplines.vams"

module dff_reset(vin_d, vclk, vout_q, vout_qbar, reset);
input vclk, vin_d, reset;
output vout_q, vout_qbar;
electrical vout_q, vout_qbar, vclk, vin_d, reset;
parameter real vlogic_high = 5;
parameter real vlogic_low = 0;
parameter real vtrans_clk = 2.5;
parameter real vtrans = 2.5;
parameter real reset_trans = 2.5;
parameter real tdel = 3u from [0:inf);
parameter real trise = 1u from (0:inf);
parameter real tfall = 1u from (0:inf);

   integer x;

   analog begin
      @ (cross( V(vclk) - vtrans_clk, +1 ) or cross(V(reset) - reset_trans, +1))
                if(V(reset) > reset_trans)
                        x = 0;
                else if (V(vin_d) > vtrans)
                        x = 1;
                else
                        x = 0;
         V(vout_q) <+ transition( vlogic_high*x + vlogic_low*!x,
                                  tdel, trise, tfall );
         V(vout_qbar) <+ transition( vlogic_high*!x + vlogic_low*x,
                                    tdel, trise, tfall );
    end
endmodule
```



Symbol for D_FF_reset

6. PFD (Phase Frequency Detector) schematic

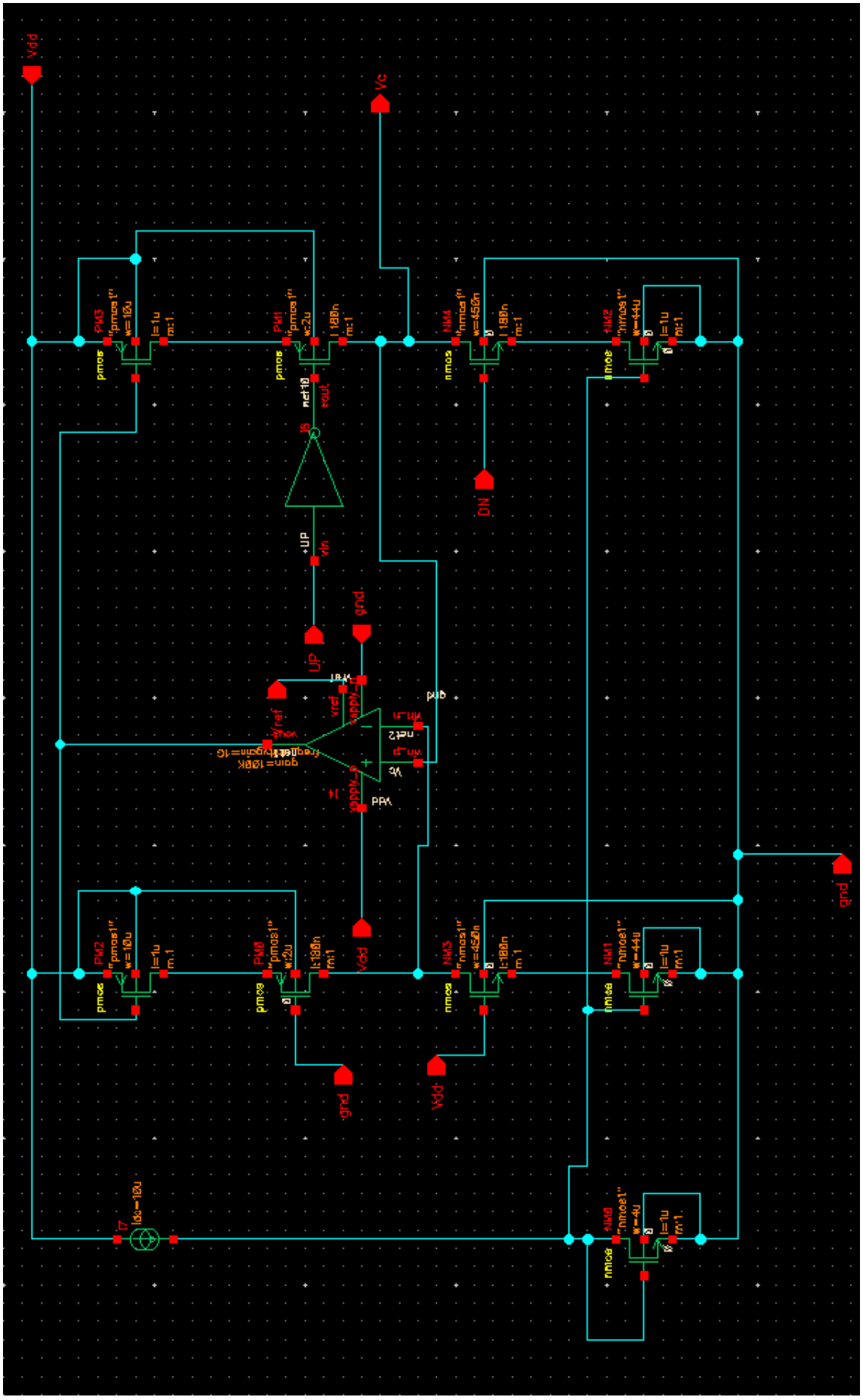


Here, we add trst in AND gate as time taken for it to reset both UP and DN signals.

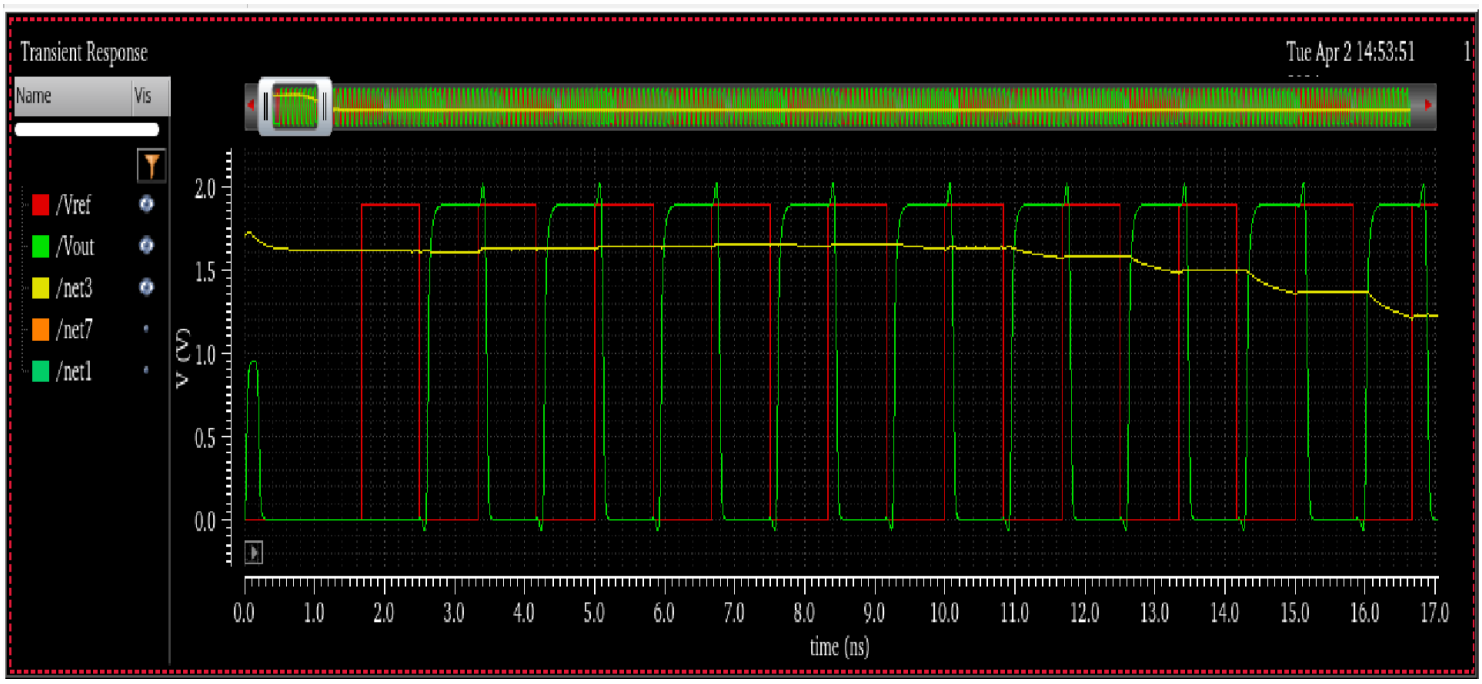
irst is a special reset pin which helps to ignore first edge of the signal. Hence, false locking is avoided.

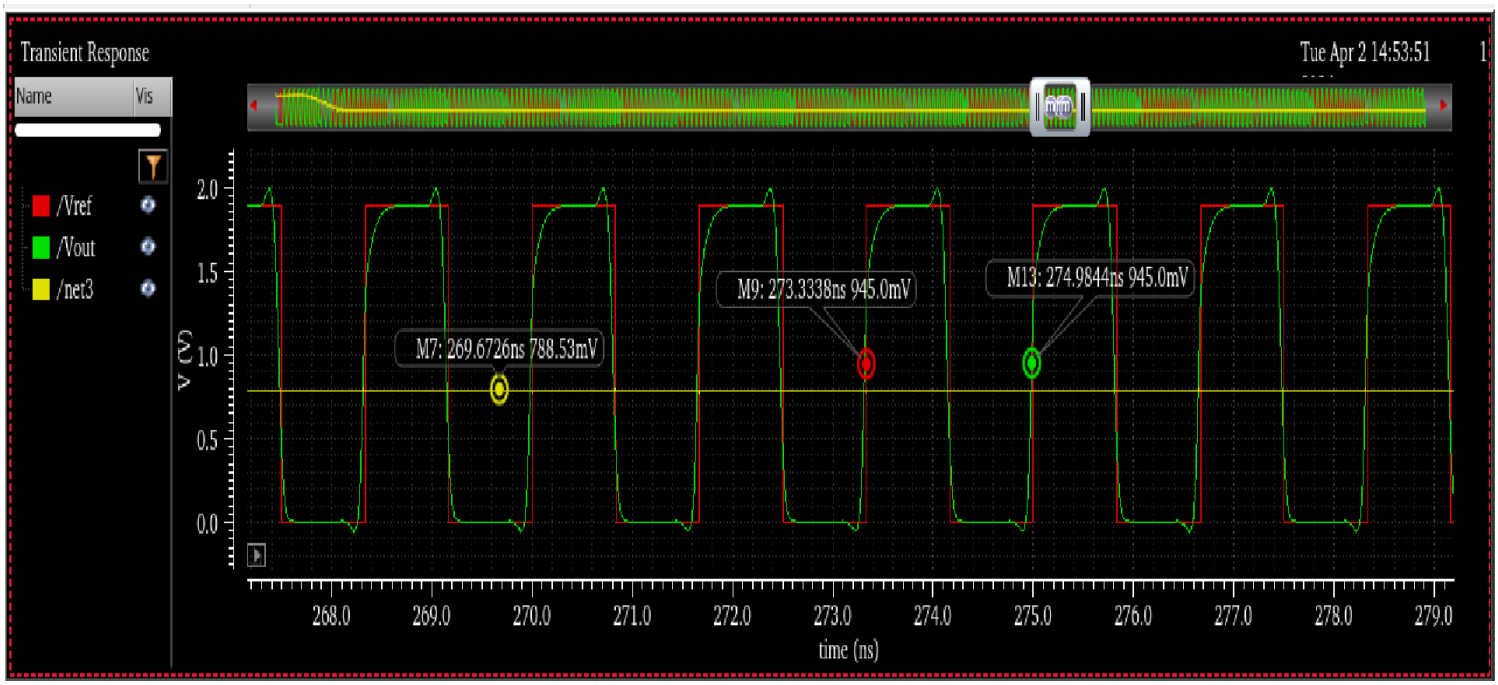
Also for design purposes, we have set trst = 50ps.

7. Charge Pump schematic



Plot 4 : Transient locking behavior of DLL under 'fast' condition



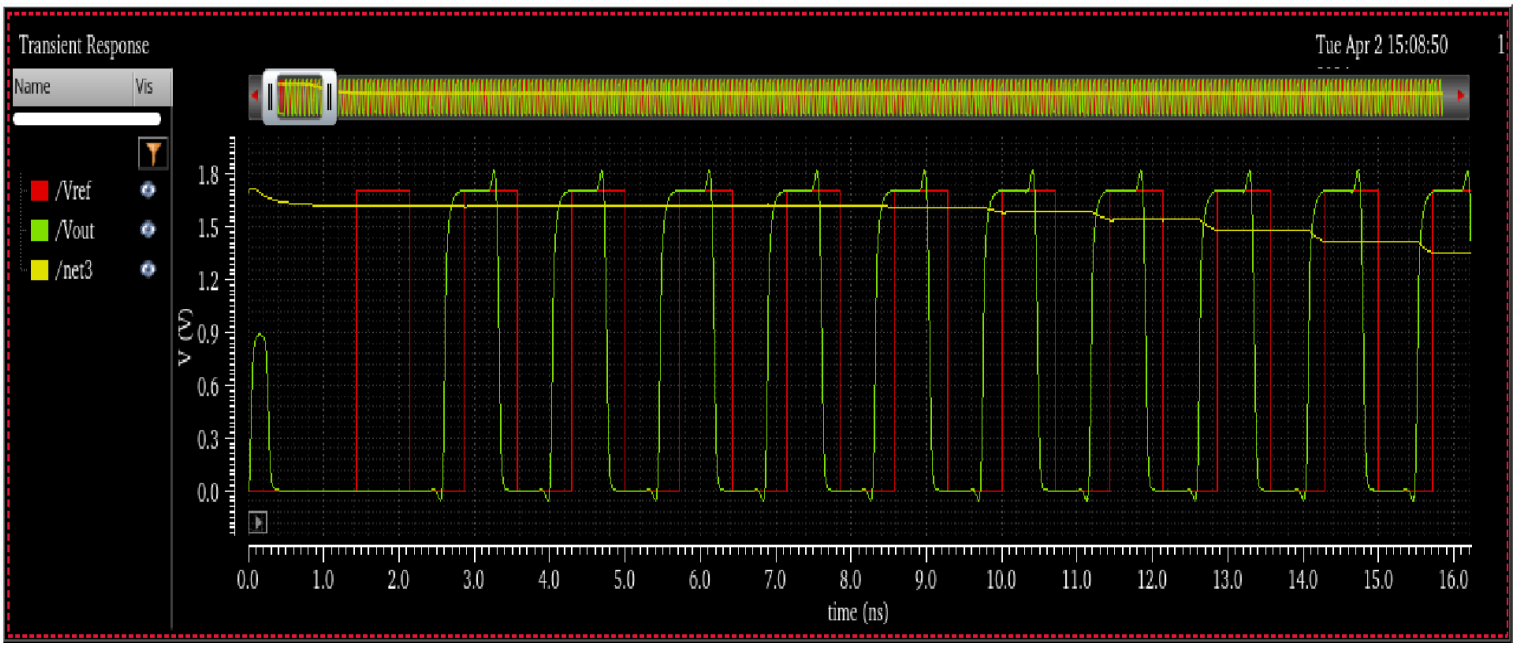


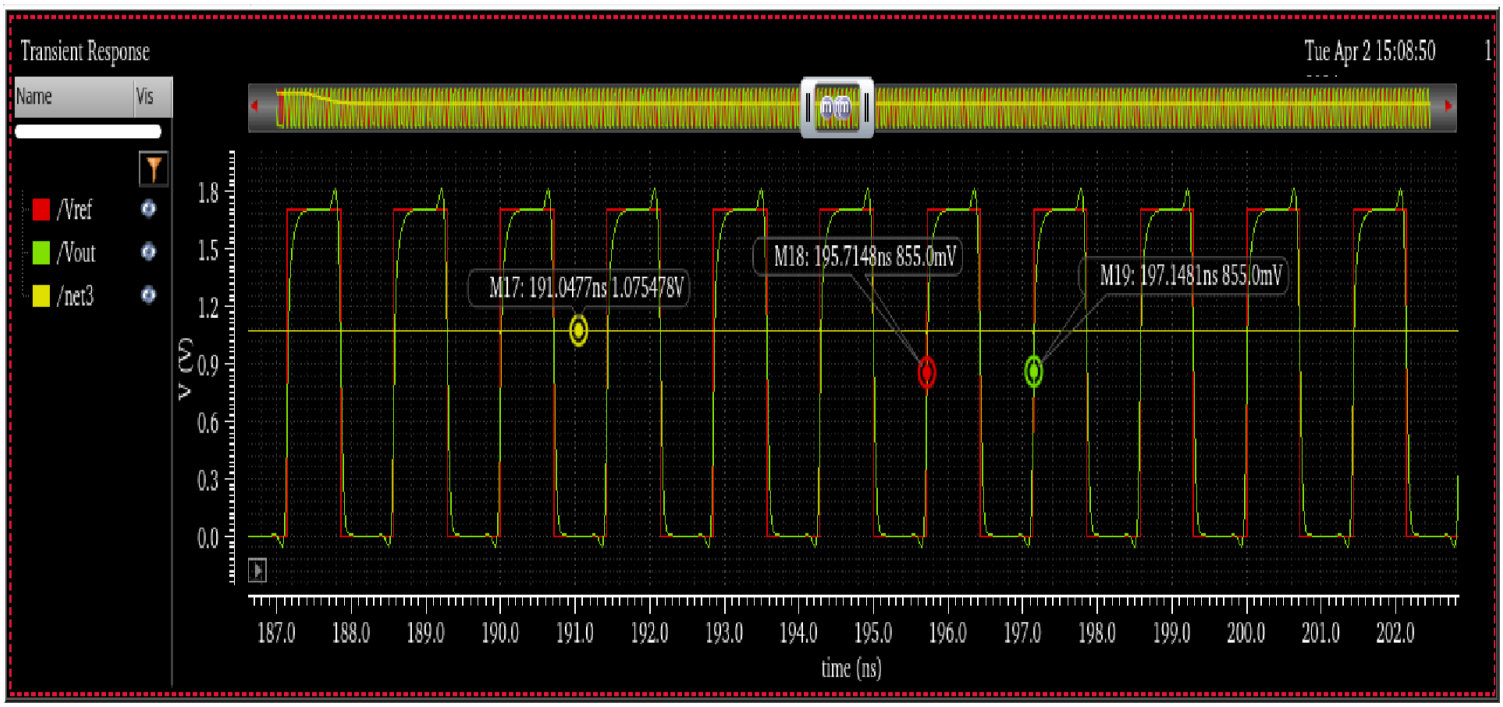
Delay = 274.9844 ns – 273.3338 ns = 1.6506 ns

Static phase offset = Delay – 1/(ref frequency)

= -16.067 ps (≤ 25 ps)

Plot 5 : Transient locking behavior of DLL under 'slow' condition





Delay = 197.1481 ns – 195.7148 ns = 1.4333 ns

Static phase offset = Delay – 1/(ref frequency)

= 4.728 ps (≤ 25 ps)

Table :

Table 1 :

C = 0.5pF

Corner	$\mathbf{f_{ref}}$ **(MHz)**	$V_c\,(V)$	$K_{dl,s}\,(ns\,V^{-1})$	I_{CP} **(µA)**	$\omega_u\,(Mrad\,s^{-1})$
fast	**600MHz**	**788.53 mV**	**-2.6487**	**340**	**1080.66**
slow	**700MHz**	**1.075478 V**	**-1.069514**	**245**	**366.843**

$$\omega_u = \frac{K_{dl,r} * I_{CP}}{2\pi C}$$

$$K_{dl,r} = -K_{dl,s} * 2\pi f_{ref}$$

$$\omega_u = \frac{|K_{dl,s}| * I_{CP} * f_{ref}}{C}$$

Table 2 :

Corner	Power Consumption (mW)
fast	**4.831**
slow	**7.257**

Design Methodology of the DLL design is as follows :

Design Methodology

(1) Design of current starved inverter (and hence VCDU)

As discussed in class, current starved inverter was used with a bias circuit.

Here, I tried to make the t_{plh} and t_{phl} equal. Also, it was ensured that all transistors remain in saturation.

Initially, bias transistor was sized so that it remains just in saturation.

Hence $\left(\frac{W}{L}\right)_b = \left(\frac{24}{180n}\right)$

Now, for current starved inverter, I set $\frac{\left(\frac{W}{L}\right)_p}{\left(\frac{W}{L}\right)_n} = 5$ for $t_{plh} = t_{phl}$. and the transistors which act as weak current sources are sized at minimum sizes. This is because we need to use them as weak sources and C_{eff} will be less for lower size. Now, after the sizes are set; we cascade initially 5 stages and check for the

fast and slow corners to be met.

In order to meet the corners, we tweak number of stages accordingly and at N=8, the corners are met appropriately.

Also, weak current source ensured that for low values of V_c, it does not draw more current.

After cascading 8 units, parametric analysis was run stepping V_c from 0.4V to 1.4V.

Instead of tweaking sizes of transistors to meet corners, no. of VCDUs were tweaked.

2. DFF with asynchronous reset was made by modifying verilog A code for D-FF. The code is attached.

3. PFD

After DFF with reset is made, we make the attached architecture.

In this design, one additional D-FF is added which is used to ignore first rising edge (so that false locking does

not happen). Also trst was a parameter which was added to AND gate.

4. Charge Pump.

Drain switched architecture was chosen for this. Initially a bias current of 10 μA passes through bias transistor with $\left(\frac{W}{L}\right) = \left(\frac{4}{1}\right)$ so that it is just in saturation.

Here we need switches, hence we use minimum sizes of $\left(\frac{W}{L}\right)_n = \left(\frac{450n}{180n}\right)$ and $\left(\frac{W}{L}\right)_p = \left(\frac{2.u}{180n}\right)$.

Now, we assigned some sizes by guess initially and put it in loop. Based on the static phase offset observed in loop, sizes in charge pump are tweaked. We try to match I_{UP} and I_{DN} by adding (almost) ideal OPAMP. This OPAMP has high gain and UGF so that it gives almost convergence.

Now for static phase offset, acc. to specs, it should be less than 25 ps.

$$(I_{UP} - I_{DN})\, t_{rst} = I_{UP}(t_{OS})$$

$$t_{OS} \propto \frac{t_{rst}}{I_{UP}}$$

So, to reduce tos, t_{rst} is kept at 50 ps (constant, let's say).

and I_{up} is increased. Hence, sizing is done by increasing sizes of PMOS and consequently NMOS as well.

Also, saturation for all transistors is maintained.

5. Loop filter.

Initial choice of loop filter was done at 2 pF.

Now, for settling of loop as well, we require that $\frac{\omega_{ref}}{\pi} > \omega_u$.

$$\Rightarrow \frac{\omega_{ref}}{\omega_u} > \pi$$

$$\text{Also } \omega_u = \frac{|K_{dld}| \times I_{cp}}{2\pi C}$$

$$= \frac{|K_{dld}| \times I_{cp} \times t_{ref}}{C}$$

Hence value of loop filter was set accordingly.

6. Initialization of Capacitor voltage

Initially DLL locking happened for fast corner. However due to changes made in charge pump and loop filter, changes in t_p vs V_c characteristics for slow corner happens and harmonic locking takes places.

As a result, instead of starting from $V_c = 0$, V_c is initialized to 1.7 V.

As a result, instead of locking to harmonics of T_{ref}, it locks to T_{ref}. (since V_c is decreased due to offset in UP and DN currents).

Now for both corners, we set ω_u such that $\frac{\omega_{ref}}{\omega_u} > \pi$.

This also gives a rough estimate of loop filter value to be chosen.

The design was made by taking $\frac{\omega_{ref}}{\omega_u} = \pi$. and further tweaked.