An FPGA-based Medical Image Enhancement Super-Resolution System

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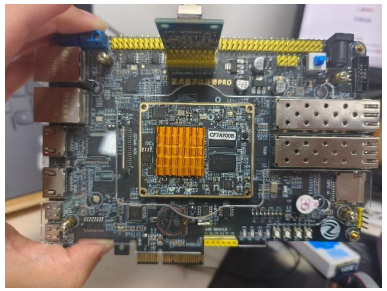
OpenHW2024

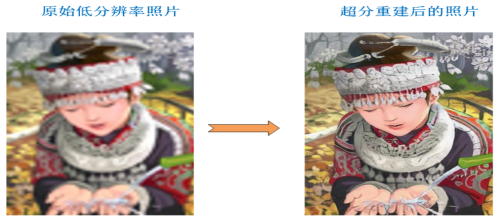
AMD



On board test by AMD A7-100T

INTRODUCTION

The medical image enhancement super-resolution system, based on super-resolution neural networks, can enlarge the details of medical images and improve the accuracy of diagnosis and detection.



Typical application case

Medical imaging often suffers from uneven lighting, noise, and low resolution. Traditional methods improve resolution but result in blurry images, while deep learning-based super-resolution offers high-quality results but lacks real-time performance. This project aims to develop a real-time medical image enhancement system.

Key technical issues addressed:

1. Low resolution: The resolution of the image is enhanced using bicubic interpolation.
2. Low clarity: Design a lightweight neural network to process and enhance blurred images.
3. Real-time processing: Use a fully parallelized approach to avoid frequent read and write operations to the DDR.
4. Performance improvement: Introduce residual structures and perceptual loss.

CREATIVE DESING

System Architecture

DSRNet(Depthwise Separable Residual Network for Super-Resolution):

1. Introduced residual structures to improve the model's generalization ability.;
2. Added perceptual loss function to enhance visual clarity;
3.Compared to SRCNN, the model's parameters were reduced by over 2000.

Advantages of CLAHE and Bicubic Interpolation:

1. CLAHE:Enhances Low-Light Images、Local Contrast Enhancement、Noise Suppression、Adaptability
2. Bicubic:Preserves Details、Smooth and Precise、Efficient Calculation

RESULT

The completed work successfully deployed the lightweight DSRNet super-resolution neural network, capable of scaling images received from the camera to any size. Additionally, CLAHE (Contrast Limited Adaptive Histogram Equalization) was incorporated to enhance images with weak lighting. The system leverages FPGA's logic programmability and convolutional neural network technology, enabling it to meet higher performance demands.

The work designed a lightweight **DSRNet** super-resolution neural network, using **16 3x3 convolution kernels**, **16 1x1 convolution kernels**, and **11 biases**, with **hardware acceleration implemented in Verilog on FPGA**.

Compared to the traditional **SRCNN** (with 64 9x9 kernels and 2080 5x5 kernels), DSRNet reduces parameters by over **2000** and has an inference time of **256μs**. The model's PSNR is **3-4 points higher** than that of **Bicubic interpolation**, demonstrating significant improvements in both image quality and processing speed.