COMPUTER ORGANIZATION AND ARCHITECTURE

Course Code : CSE 2151

Credits : 04

HARDWIRED APPROACH

- Control logic is a clocked sequential circuit.
- So conventional sequential circuit design procedure can be applied to build CU.
- Final circuit is obtained by physically connecting gates and flip flops.
- Cost of control logic increases with system complexity.

10 STEPS FOR HARDWIRED CONTROL

1. Define task to be performed.
2. Propose a trial processing section.
3. Provide a register transfer description algorithm based on processing section outlined.
4. Validate the algorithm by using trial data.
5. Describe the basic characteristics of the hardware elements to be used in the processing section.
6. Complete the design of the processing section by establishing necessary control points.
7. Propose the block diagram of the controller.
8. Specify state diagram of controller.
9. Specify the characteristics of the hardware elements to be used in the controller.
10. Complete the controller design and draw a logic diagram of final circuit.

10 STEPS FOR HARDWIRED CONTROL

Step 1: Task definition.

Design a Booth's multiplier to multiply two 4-bit signed numbers.

Step 2: Trial processing section.

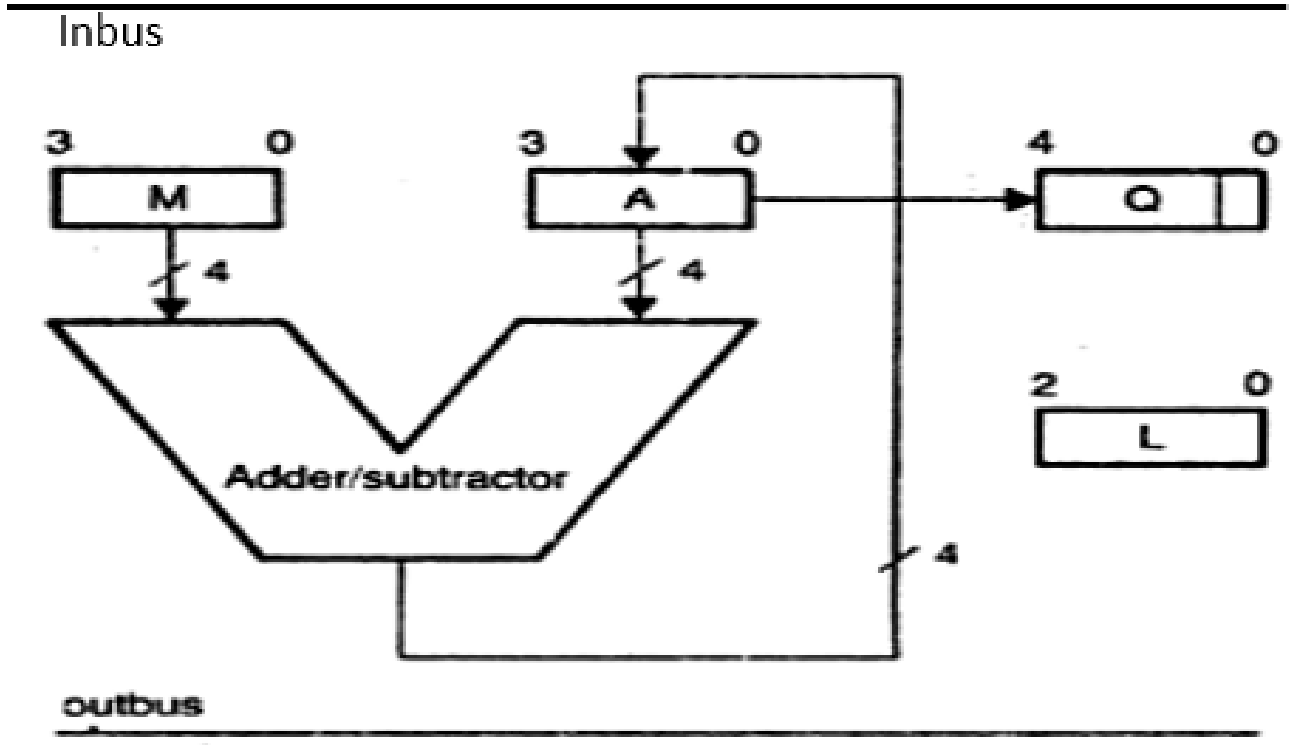
q_1 q_0

0 0→none

0 1→ add M

1 0→sub M

1 1→ None



10 STEPS FOR HARDWIRED CONTROL

Step 3: Register transfer description of Booth's multiplier procedure based on the processing section outlined in the previous step.

	Declare registers A[4], M[4], Q[5], L[3];	
	Declare buses inbus[4], outbus[4];	
Start:	A←0, M←inbus, L←4;	clear A and transfer M
	Q[4:1]←inbus, Q[0]←0;	transfer Q
Loop:	if Q[1:0]= 01, then go to ADD;	
	if Q[1:0]=10, then go to SUB;	
	go to Rshift;	
ADD:	A←A+M;	
	goto Rshift;	
SUB:	A←A-M;	
Rshift:	ASR(A$Q), L←L-1;	
	if L>0, then go to Loop	
	outbus =A;	
	outbus=Q[4:1];	
Halt:	go to Halt	

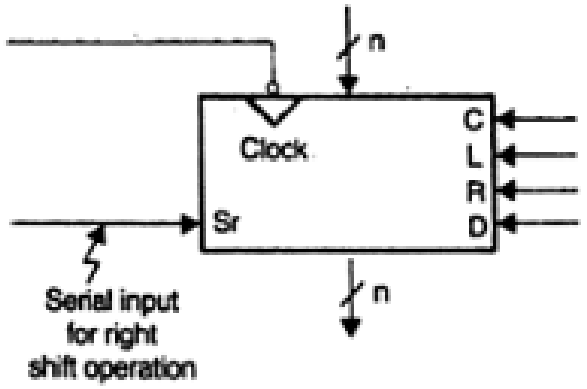
10 STEPS FOR HARDWIRED CONTROL

Step 4: Validate the algorithm by using trial data.

A	Q	Q_{-1}	M		
0000	0011	0	0111	Initial Values	
1001	0011	0	0111	A ← A - M	First Cycle
1100	1001	1	0111	Shift	
1110	0100	1	0111	Shift	Second Cycle
0101	0100	1	0111	A ← A + M	Third Cycle
0010	1010	0	0111	Shift	
0001	0101	0	0111	Shift	Fourth Cycle

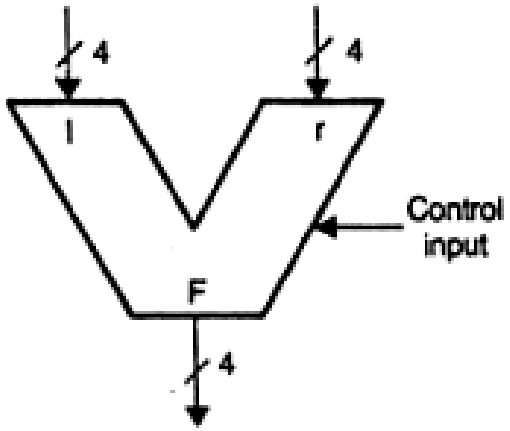
10 STEPS FOR HARDWIRED CONTROL

Step 5: Processing section includes GPRs, 4-bit adder / subtractor, Tristate buffers



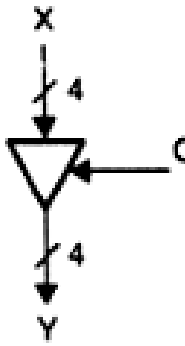
C	L	R	D	Clock	Action
1	0	0	0	↓	Clear
0	1	0	0	↓	Load external data
0	0	1	0	↓	Right shift
0	0	0	1	↓	Decrement by one
0	0	0	0	↓	No change

a. Storage Register



Control input	F
1	I + r
0	I − r

b. Adder-subtractor



Control input	Y
1	X
0	High Z

c. Tri-state Buffer

10 STEPS FOR HARDWIRED CONTROL

Step 6: The complete design of processing section establishing control points.

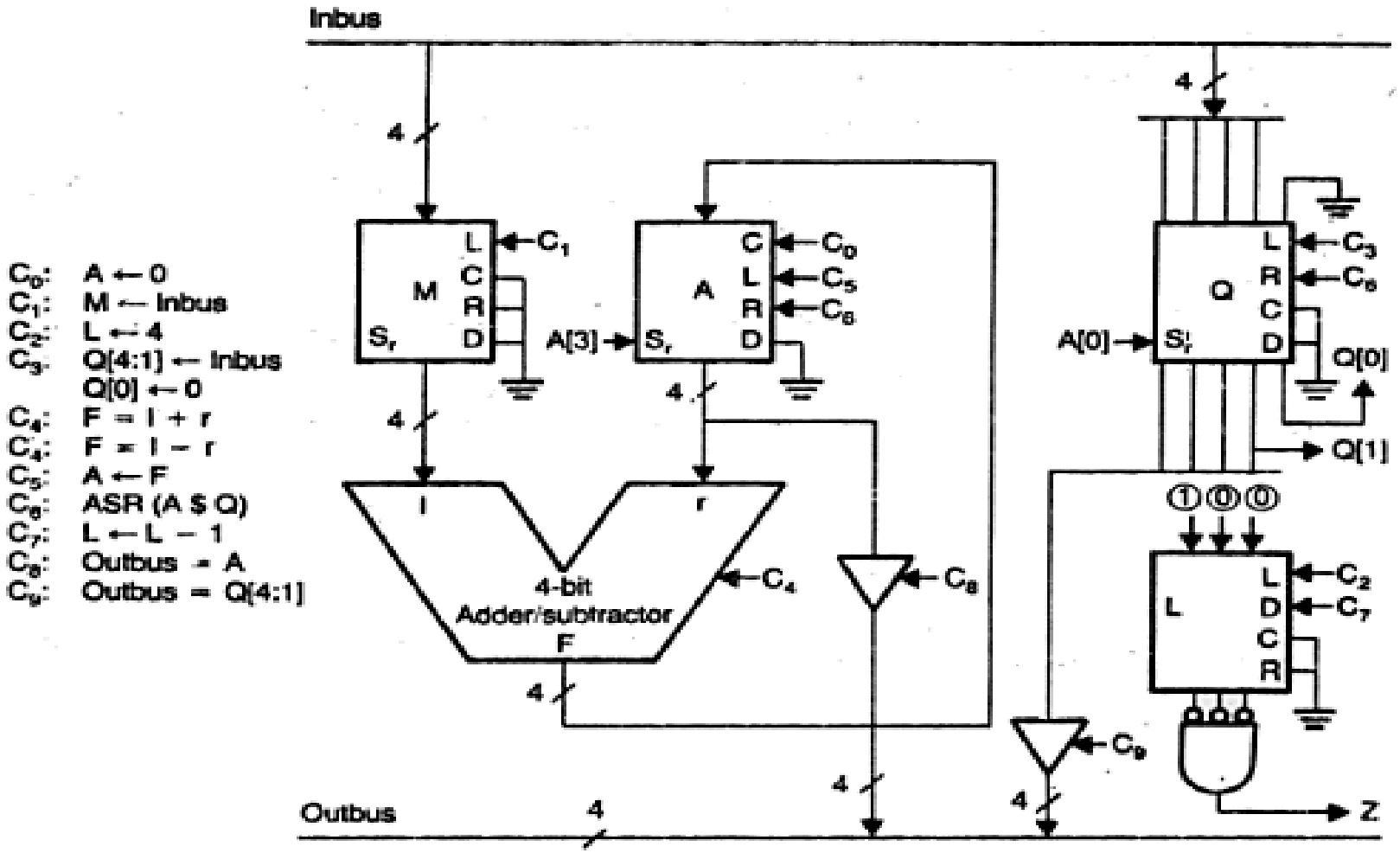


Figure 4.18 Processing Section of the Booth's Multiplier

TOPICS COVERED FROM

- Textbook 3:
  - Chapter 4: 4.2 and 4.3