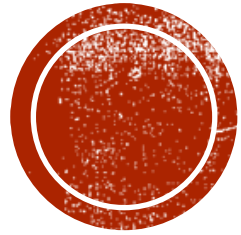


COMPUTER ORGANIZATION AND ARCHITECTURE

Course Code : CSE 2151

Credits : 04





ARITHMETIC AND LOGIC UNIT

MODULE 3

ARITHMETIC AND LOGIC UNIT

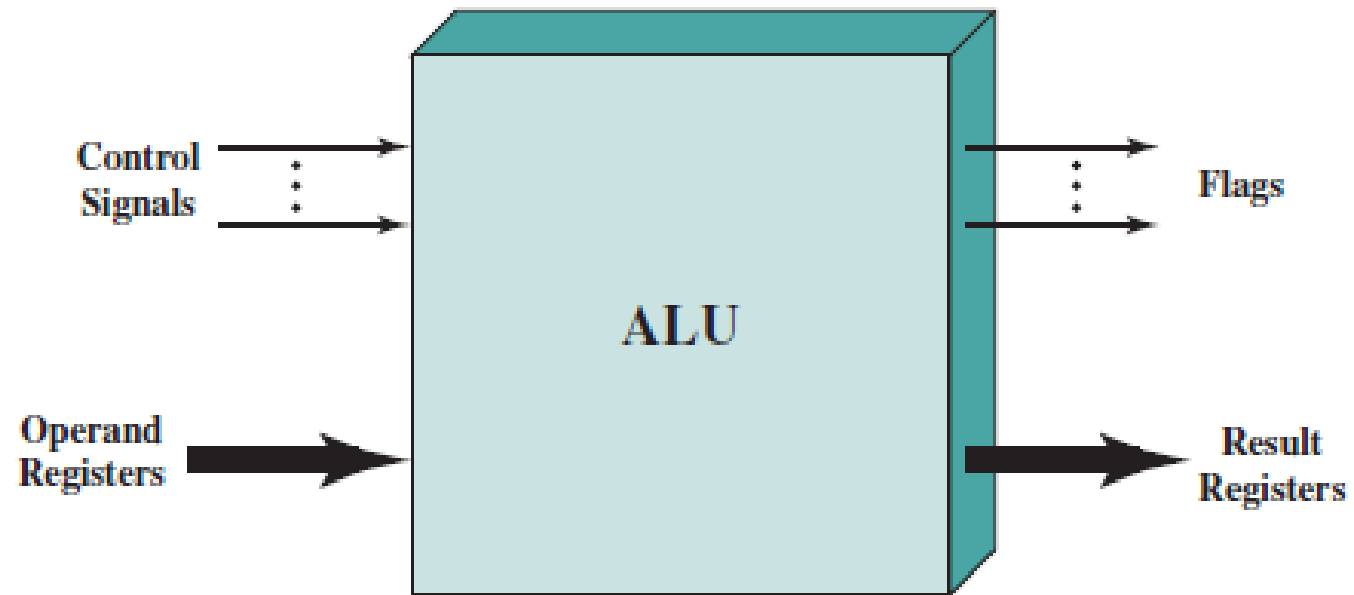


Figure 10.1 ALU Inputs and Outputs

ADDITION AND SUBTRACTION

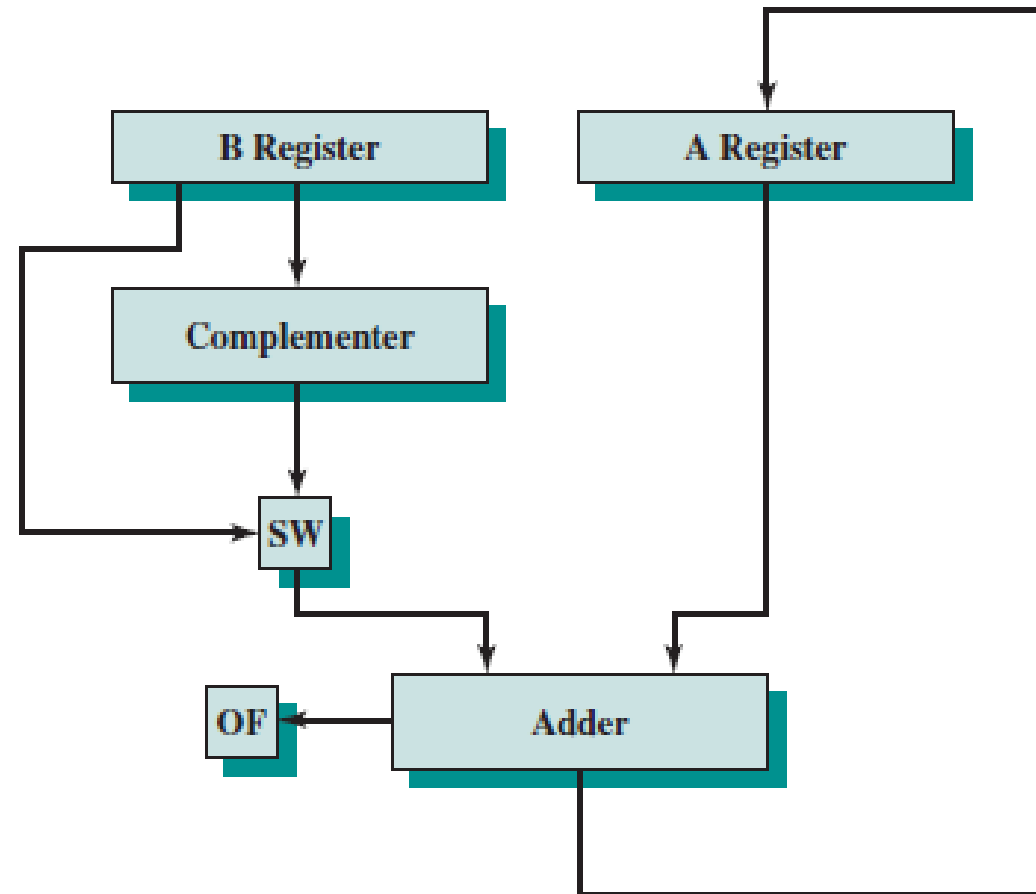
- OVERFLOW RULE:

- If two numbers are added, and they are both positive or both negative, then overflow occurs if and only if the result has the opposite sign.

- SUBTRACTION RULE:

- To subtract one number (subtrahend) from another (minuend), take the twos complement (negation) of the subtrahend and add it to the minuend.

ADDITION AND SUBTRACTION: HARDWARE



OF = Overflow bit
SW = Switch (select addition or subtraction)

Figure 10.6 Block Diagram of Hardware for Addition and Subtraction

MULTIPLICATION: UNSIGNED INTEGERS

1011		Multiplicand (11)
×1101		Multiplier (13)
1011	}	
0000		
1011		Partial products
1011		
10001111		Product (143)

- Perform immediate addition to eliminate the need for additional registers to store the partial products
- Save time:
 - 1 multiplier: add and shift operation
 - 0 multiplier: shift operation

Figure 10.7 Multiplication of Unsigned Binary Integers

MULTIPLICATION: UNSIGNED INTEGERS

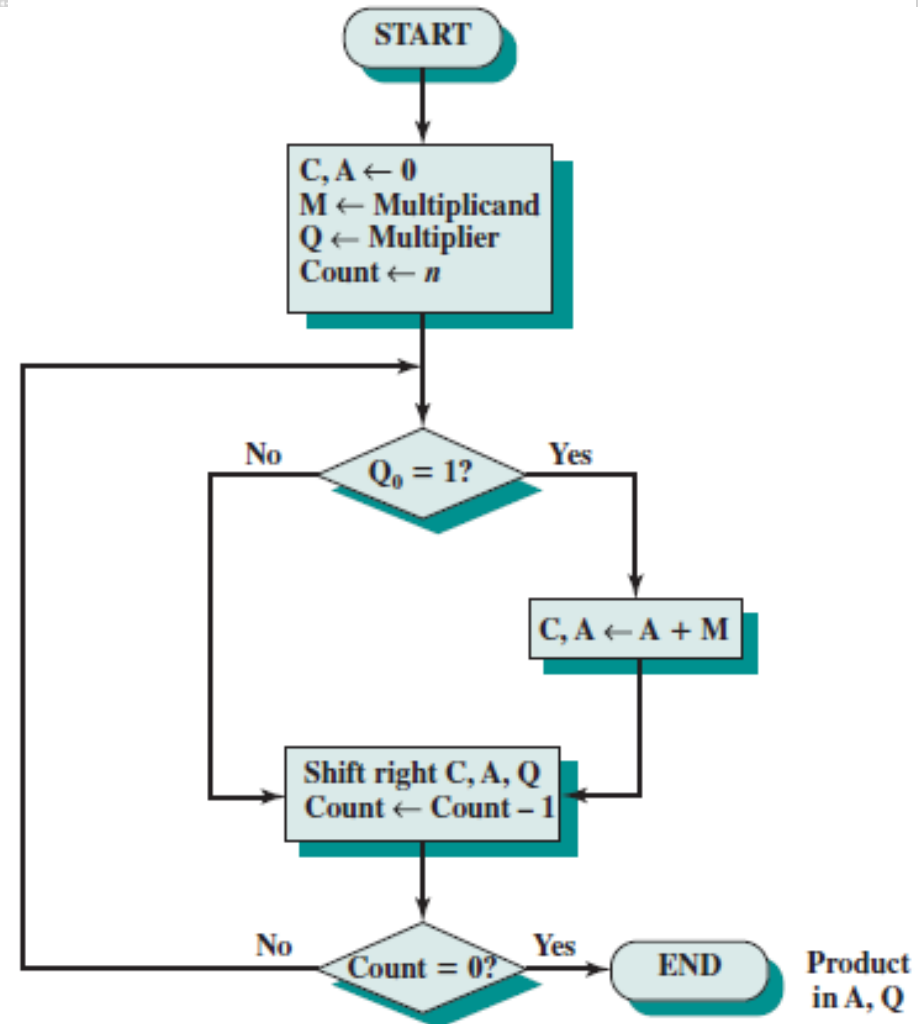
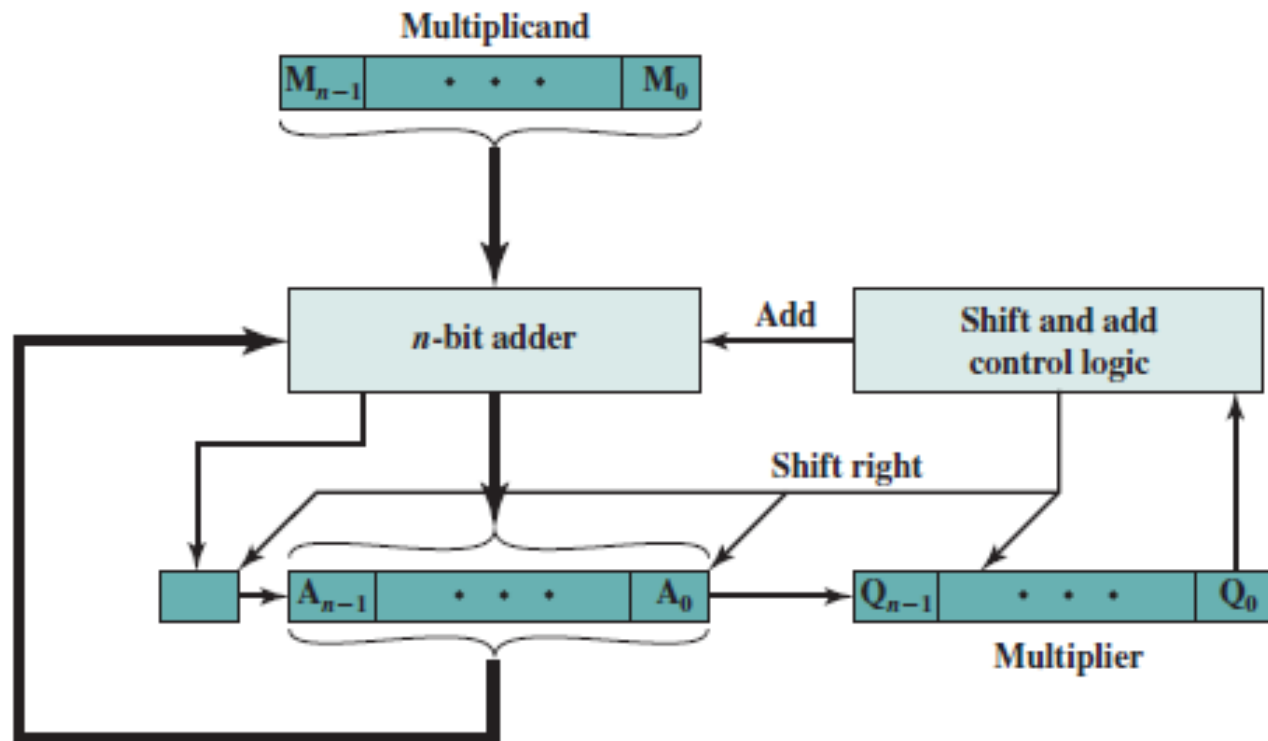


Figure 10.9 Flowchart for Unsigned Binary Multiplication

MULTIPLICATION: UNSIGNED INTEGERS



(a) Block diagram

C	A	Q	M		
0	0000	1101	1011	Initial values	
0	1011	1101	1011	Add	First cycle
0	0101	1110	1011	Shift	
0	0010	1111	1011	Shift	Second cycle
0	1101	1111	1011	Add	
0	0110	1111	1011	Shift	Third cycle
1	0001	1111	1011	Add	
0	1000	1111	1011	Shift	Fourth cycle

(b) Example from Figure 10.7 (product in A, Q)

MULTIPLICATION: UNSIGNED INTEGERS

- 45 (101101) X 33 (100001)=1485

C	A	Q	M	
0	000000 <u>101101</u>	100001	101101	Add First Cycle Shift
0	101101	100001	101101	
0	010110	110000		
0	001011	011000	101101	Shift 2 nd Cycle
0	000101	101100	101101	Shift 3 rd cycle
0	000010	110110	101101	Shift 4 th cycle
0	000001	011011	101101	Shift 5 th cycle
0	<u>101101</u> 101110	011011	101101	Add Shift 6 th cycle
0	010111	001101	101101	
	Product			

MULTIPLICATION: SIGNED INTEGERS- 2'S COMPLEMENT

- $-5 (1011) \times -3 (1101) = -113 (10001111)$

1011	
<u>× 1101</u>	
00001011	$1011 \times 1 \times 2^0$
00000000	$1011 \times 0 \times 2^1$
00101100	$1011 \times 1 \times 2^2$
<u>01011000</u>	$1011 \times 1 \times 2^3$
10001111	

Figure 10.10 Multiplication of Two Unsigned 4-Bit Integers Yielding an 8-Bit Result

MULTIPLICATION: NEGATIVE MULTIPLICAND

- $-13 (10011) \times +11 (01011) = -143 (1101110001)$

Sign extension is shown in blue

						1	0	0	1	1	(-13)
						×	0	1	0	1	(+11)
						<hr/>					
	1	1	1	1	1	1	0	0	1	1	
	1	1	1	1	1	0	0	1	1		
	0	0	0	0	0	0	0	0			
	1	1	1	0	0	1	1				
	0	0	0	0	0	0					
	<hr/>										
	1	1	0	1	1	1	0	0	0	1	(-143)

Figure 9.8 Sign extension of negative multiplicand.

MULTIPLICATION: UNSIGNED V/S SIGNED

$\begin{array}{r} 1001 \quad (9) \\ \times 0011 \quad (3) \\ \hline 00001001 \quad 1001 \times 2^0 \\ 00010010 \quad 1001 \times 2^1 \\ \hline 00011011 \quad (27) \end{array}$	$\begin{array}{r} 1001 \quad (-7) \\ \times 0011 \quad (3) \\ \hline 11111001 \quad (-7) \times 2^0 = (-7) \\ 11110010 \quad (-7) \times 2^1 = (-14) \\ \hline 11101011 \quad (-21) \end{array}$
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(a) Unsigned integers

(b) Twos complement integers

Figure 10.11 Comparison of Multiplication of Unsigned and Twos Complement Integers

READ FROM....

- Go through examples given in Section 2.12 and 2.15 of the Reference Book (textbook 1)

TOPICS COVERED FROM

- Textbook 2:
 - Chapter 10: 10.3