COMPUTER ORGANIZATION AND ARCHITECTURE

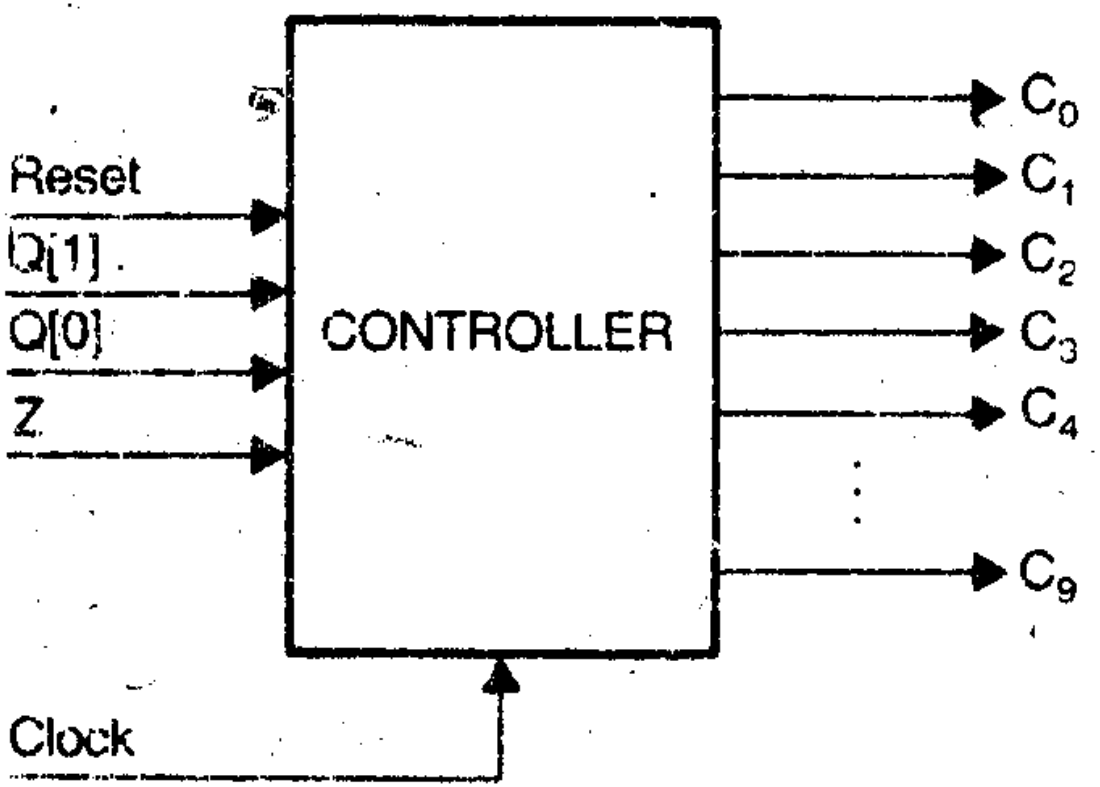
Course Code : CSE 2151

Credits : 04

10 STEPS FOR HARDWIRED CONTROL

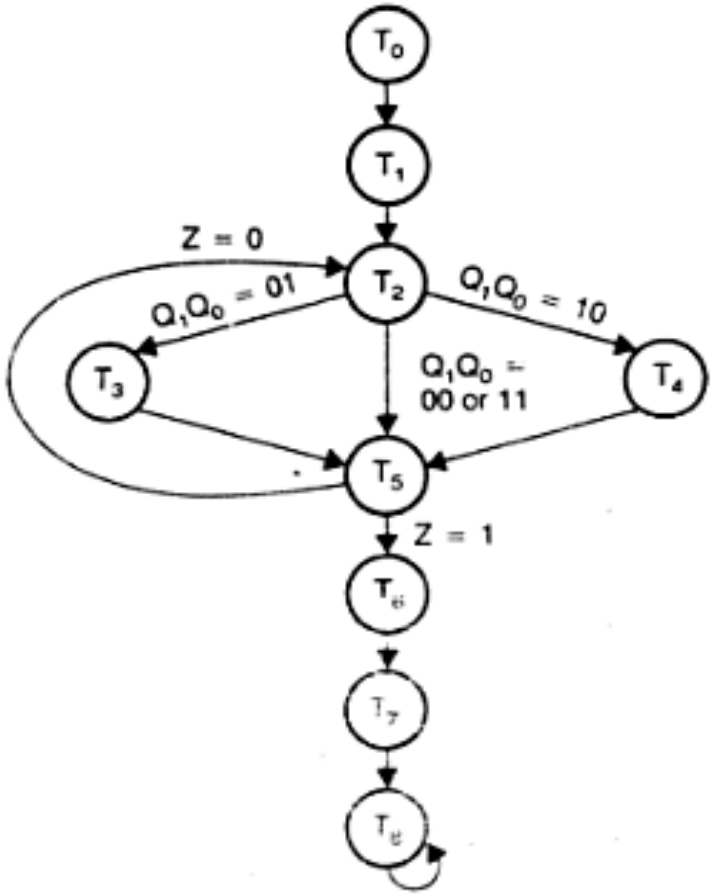
Step 7: Block diagram of controller:

- will have 5 I/Ps and 10 O/Ps.
- RESET i/p is used to reset the controller so a new computation can begin.
- CLK is used to synchronize the controller action for trailing edge of clock pulse.



10 STEPS FOR HARDWIRED CONTROL

Step 8: The state diagram of Booth's multiplier controller



a. State Diagram

CONTROL STATE	OPERATION PERFORMED	CONTROL SIGNALS TO BE ACTIVATED
T_0	A ← 0, L ← 4, M ← Inbus	C_0, C_1, C_2
T_1	Q [4:1] ← Inbus, Q [0] ← 0	C_3
T_2	None	None
T_3	A ← A + M	C_4, C_5
T_4	A ← A − M	C_5 (C_4 = 0)
T_5	ASR (ASQ), L ← L − 1	C_6, C_7
T_6	Outbus = A	C_8
T_7	Outbus = Q [4:1]	C_9
T_8	None	None

b. Controller Action

C_0: A ← 0
C_1: M ← Inbus
C_2: L ← 4
C_3: Q[4:1] ← Inbus
Q[0] ← 0
C_4: F = I + r
C_4: F = I − r
C_5: A ← F
C_6: ASR (A $ Q)
C_7: L ← L − 1
C_8: Outbus = A
C_9: Outbus = Q[4:1]

Figure 4.20 Controller Description

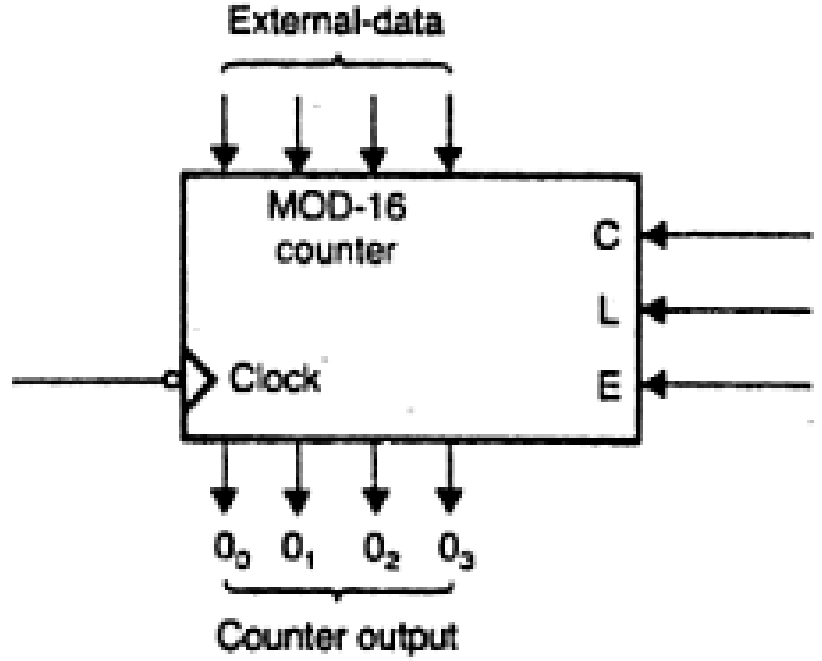
10 STEPS FOR HARDWIRED CONTROL

Step 9: The controller includes a mod -16 counter, a 4: 16 decoder, a sequence controller (SC).

- SC HW, which sequences the controller according to state diagram.

- Hence Truth Table for SC must be derived from the controller's state

C	L	E	Clock	Action
1	X	X	X	Clear
0	1	X	↓	Load external data
0	0	1	↓	Count up
0	0	0	↓	No operation



a. Block Diagram

10 STEPS FOR HARDWIRED CONTROL

Step 10: Logic Diagram of the Booth's multiplier controller

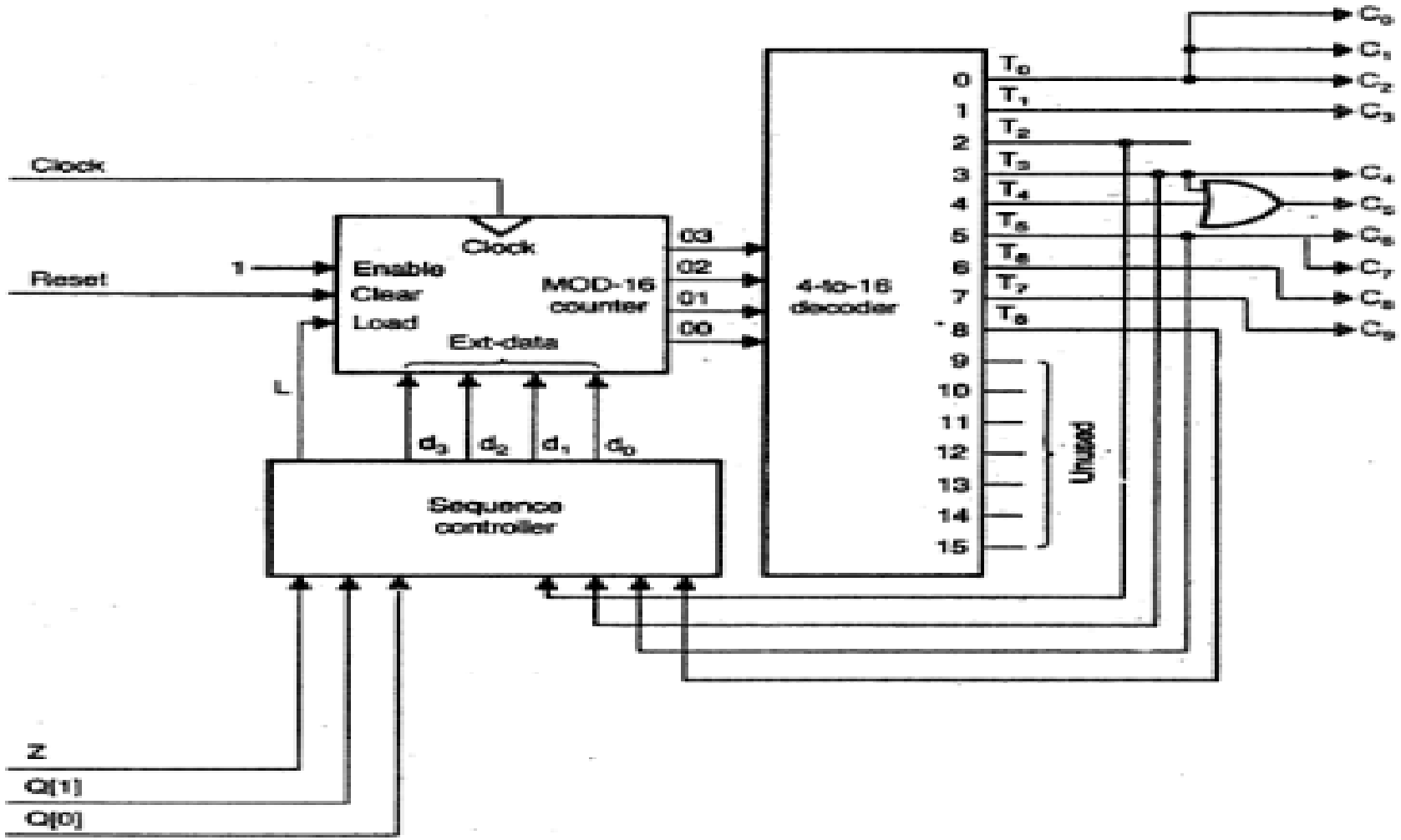


Figure 4.23 Logic Diagram of the Booth's Multiplier Controller

10 STEPS FOR HARDWIRED CONTROL

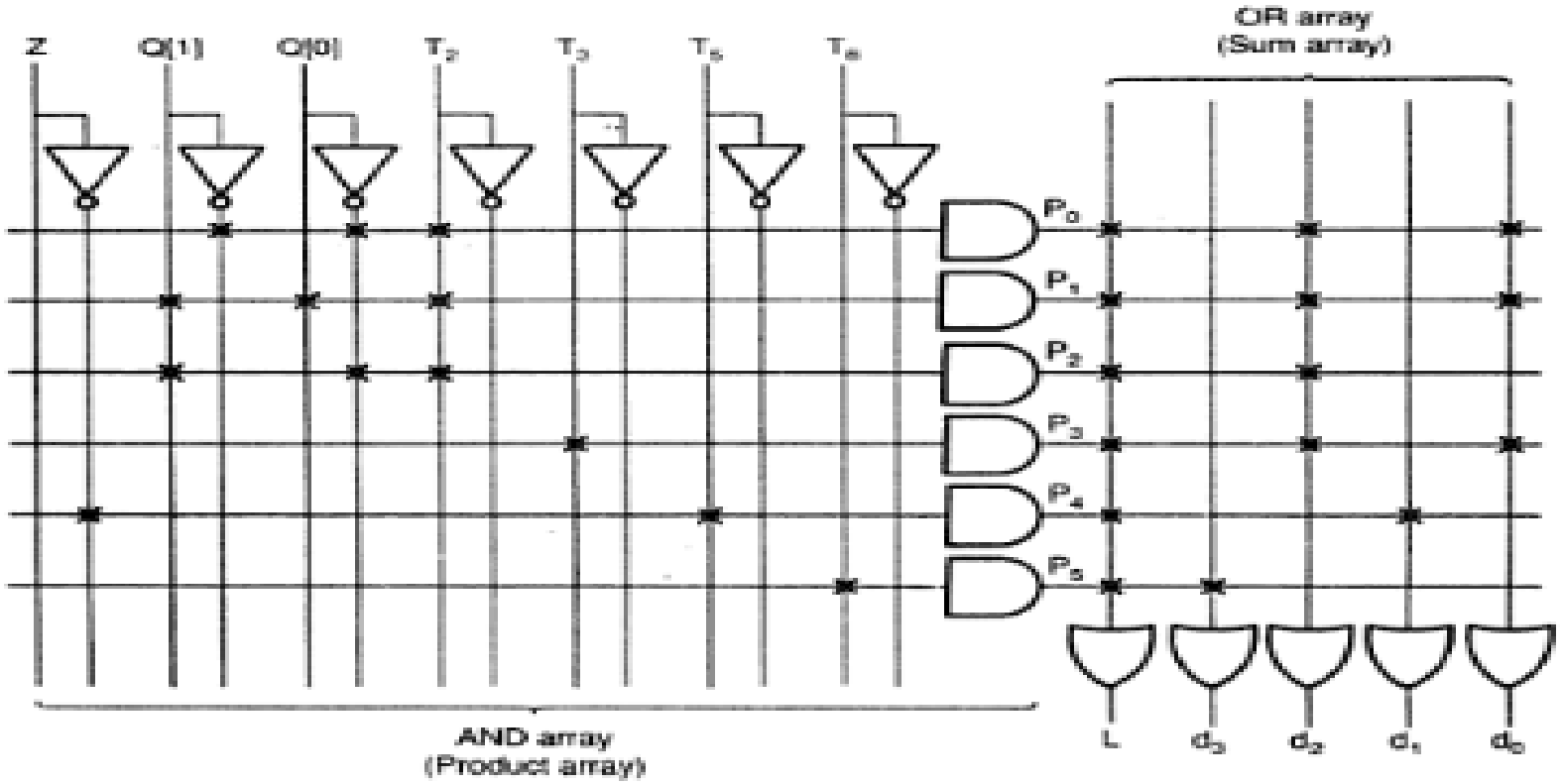
Step 10: Truth Table for SC Design

								External-data			
Z	Q [1]	Q [0]	T_2	T_1	T_0	T_0	L	d3	d2	d1	d0
X	0	0	1	X	X	X	1	0	1	0	1
X	1	1	1	X	X	X	1	0	1	0	1
X	1	0	1	X	X	X	1	0	1	0	0
X	X	X	X	1	X	X	1	0	1	0	1
0	X	X	X	X	1	X	1	0	0	1	0
X	X	X	X	X	X	1	1	1	0	0	0

10 STEPS FOR HARDWIRED CONTROL

Step 10: PLA Design

								External-data			
Z	Q [1]	Q [0]	T_2	T_3	T_5	T_6	L	d3	d2	d1	d0
X	0	0	1	X	X	X	1	0	1	0	1
X	1	1	1	X	X	X	1	0	1	0	1
X	1	0	1	X	X	X	1	0	1	0	0
X	X	X	X	1	X	X	1	0	1	0	1
0	X	X	X	X	1	X	1	0	0	1	0
X	X	X	X	X	X	1	1	1	0	0	0



b. PLA Implementation

Figure 4.24 Sequence Controller Design

10 STEPS FOR HARDWIRED CONTROL

Step 10: PLA Design

Implementing SC using PLA:

$P_0 = Q[1]' Q[0]' T_2$

$P_1 = Q[1] Q[0] T_2$

$P_2 = Q[1] Q[0]' T_2$

$P_3 = T_3$

$P_4 = Z'T_5$

$P_5 = T_8$

- The PLA o/ps are summarized as
- L = P0 + P1 + P2 + P3 + P4 + P5
- d3 = P5
- d2 = P0 + P1 + P2 + P3
- d1 = P4
- d0 = P0 + P1 + P3

- The controller design is completed by relating the control (T0-T8) with control i/ps C0-C9 as below:
- C0 = C1 = C2 = T0
- C3 = T1
- C4 = T3
- C5 = T3 + T4
- C6 = C7 = T5
- C8 =T6
- C9 = T7

TOPICS COVERED FROM

- Textbook 3:
  - Chapter 4: 4.3