

LDA 4000H ; A = 22H
MOV B, A ; B = 22H

LDA 5000H ; A = 33H
STA 4000H ; [4000H] = 33H
MOV A, B ; A = 22H
STA 5000H ; [5000H] = 22H

HLT

5th

DEC (R) IN 8-bit address

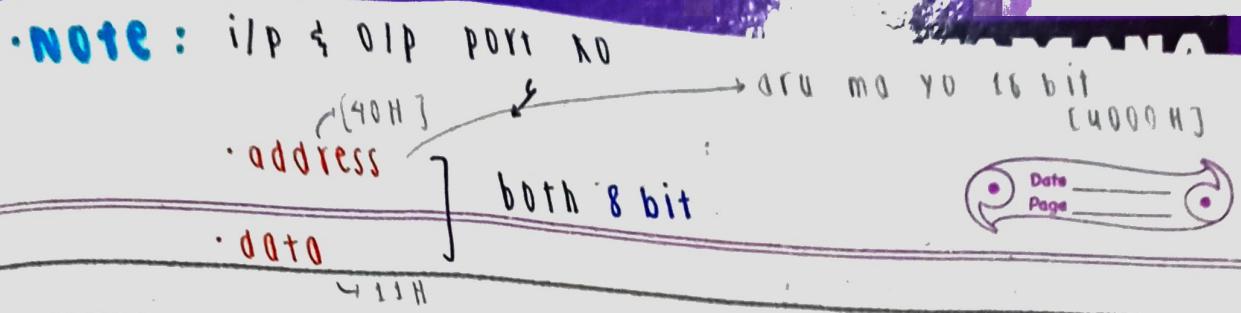
↳ 2 byte instⁿ

↳ Read data from I/O port address specified in 2nd byte & loads data into A.

• EG: IN 40H

↳

A ← [40H]



① OUT 8 bit address

↳ 2 byte instⁿ

↳ copies content of A to O/I port address specified in 2nd byte

• EG: OUT 40H

[40 H] ← A

NOTE : LHLD] ONLY for HI pair
SHLD .]

93 00	11 H
95 01	22 H

② LHLD 16 bit address

(load HI directly)

↳ 3 byte instⁿ

↳ loads content of specified memory location to
l reg

& contents of next higher location

→ H reg

E0: LHLD 9500H

Address	DATA
9500	11H
9501	22H

⑩ SHLD 16 bit address
(store HI directly)

3 byte inst

- ↳ stores content of L reg to specified memory location
- ↳ content of H reg to next higher memory location.

E0:

SHLD 8500H

[8500] ← L

[8501] ← H

22H

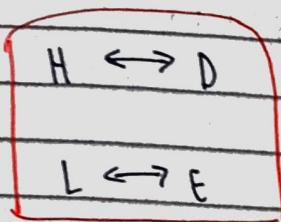
only for • HL
• DE] pairs



② XCHG (Exchange)

↳ 1 byte instⁿ

↳ exchanges DE w. HI pair



Ex:

LXI H, 7500H

; H = 75, L = 00

LXI D, 9532H

; D = 95, E = 32

XCHG

; H = 95H, L = 32H, D = 75H, E = 00H

HLT

→ asked !!

Addressing mode

- ↳ various format of specifying operands
source only
destination only
or both

↳ 5 addressing mode

① Direct addressing mode

- ↳ can be 2 or 3 bytes
 - ↳ 1st byte = op code
 - ↳ 2nd & 3rd byte = address of data

- ↳ specifies effective address as part of instruction.

- ↳ also called absolute addressing.

• Eg:

LDA 8500H

IN 80H



direct address XA



(6) Reg direct addressing mode

↳ specifies reg or reg pair that contains data

• Eg:

MOV A, B

ADD C ; A \leftarrow A+C ; XCHG (not sure)

(7) Reg indirect addressing mode

↳
subai m rando instⁿ
; STAX, LDAX

↳ Address part of instⁿ specifies the memory whose contents are address of operands.

• Eg: MOV R, M

MOV M, R

STAX

LDAX

I alone inst"

① Immediate addressing mode
↳ operand specifies immediate data.

↳ • 8-bit data = 2 bytes

• 16-bit data $\xrightarrow{\text{instn size}}$ 3 bytes

• Eg: MVI A, 32H
LXI I, B, 4567 H

② Implied / Inherent addressing mode

↳ no operands

• Eg:

NOP : NO operation

HLT : Hold

EI : Enable Interrupt

DI : Disable Interrupt

↳ sometimes XCHG

J
Don't write

- (a) Immediate
- (b) Reg indirect
- (c) Reg indirect

- (d) Direct
- (e) Indirect reg

- (f) Reg direct
- (g) Direct
- (h) Direct

Date _____
Page _____

Instructions

Addressing mode Reg · Direct

- ii) MOV Rd, Rs
- iii) MVI R, 8 bit data
- iv) MOV m, R
- v) MOV R, m
- vi) LXI Rp, 2 bytes data
- vii) MVI m, data
- viii) LDA 16-bit address
- ix) LDAX Rp
- x) STA 16-bit address
- xi) STAX Rp
- xii) IN 8-bit address
- xiii) OUT 8-bit address
- xiv) LHLD 16-bit address
- xv) SHLD 16-bit address
- xvi) XCHG

I. STORE 22H IN 3000H
ii) USING HI pair
LXI H, 3000H
MOV H, 22H
HLT

iii) USING A

MOV A, 22H
STA 3000H
HLT

A \neq as memory location

ma already data
nuna parra

iii) USING DE pair

LXI D, 3000H
MOV A, 22H
STAX D
HLT

of location \rightarrow (copy this data)

[200AH] in D reg

data

LDA 200AH ; A \leftarrow [200AH]

MOV D, A

HLT)

8

77H

D \leftarrow A

already [200AH] ma data

vayera use garna milyo.

- USING HI pair

LXI H, 200AH

MOV D, M

HLT

3. Reg I contains data 95H transfer data to location 3000H

MOV A, L ; A \leftarrow L

STA 3000H ; [3000H] \leftarrow A

HLT

- USING HI pair

MOV B, I ; B \leftarrow L

LXI H, 3000H ; H = 30H, L = 00H

MOV M, B ; [3000H] \leftarrow B

HLT

1000 reg pairs B & D w. data 1122H & 3344H
WAP to exchange content of reg pairs BC & DE

ii) USING MOV instn

LXI B, 1122H ; B = 11H C = 22H

LXI D, 3344H ; D = 33H E = 44H

iii) USING XCHG instn