me bismikklidie bleg & abblication of Soke - Rapiesh Gaoghar CA 91 -1 23 th NOV · Bit " binary digit 4041 8 bit = 1 byte 9 bit = 1 mibble 1024 byte = 1 KB 1024 KB = 1 MB 1024 VB = 1TB . 1024 TB = 1 PB -System Bus Brown of lines 80 86 8085 that reansfers 20.611 16bit - Address Bus MOI+ DIEL 16 611 s bit - Data Bus gorice to destination CONTROL BUS memory capacity more efficient add iines bytes . 8086 8085 220 64166 2 26 bytes = 1 M B = 64 KB

denotes Hexadecimal No. 16 bit 2050 (H theret fried MICTO PLOCE SS OF 4 multipurpose 7 full sentence!! · progra mmable · civer driver · register based electronic derice that Exam maFUII sentance leepung; · (Teads) binary data from memory . accepts binary data as ilp. . 4 process data acc. to instructio-20 · 4 provides results as old Micro processor IIP aı 010 CPU memory Fig General Block Diagram of computer

	. 10 46: W.b. to atual interval we work undaina.
	for remporary storage
1	10, memory ko interfacing garna
1 1	parxa.
+	
-	micro controller
	4 For a specific purpose.
	The second secon
1	MPU
-	
	Memory 110
	Peripheral Devices
4	AID CONVETTET
4	· sesion and their of a plantage of
1	e marks toi souther to the same
	micro processor micro controller
0	for general purpose a specific purpose
	to washing machine,
	Angetick light.
0	wore expensive @ less expensive
	more versotile. III Less versotile
	N N



based system microprocessor Mp

micro processor

ALU REGISTET INPUT OUTPUT

ATTOY

CONTION UNIT

Fig: Microprocessor based system

memory

RAMIROM

Performs anishmetic & logical calculations

14- * 11 (AND. DR. ...)

Register Array
L Temporary storage during execution of program.

a occessipic to mich

inpails sold piez As xaitai + A w accumulator B, C, D, E, H, L in 8085 8086 7 4 foi descare gains · control unit provides necessary timing 4 control signals to 270107990 110 " controls data flow bet" up, memory & peripherals Input | purput devices - also colled peripheral devices memory croses data & instructions memory RAM Ram - Rondom Access Memory 4 REGO ONLY memory Read & Write dubai DDIY TEOD



BUS

system Bus communication channel bet up & peripheral group of wives to corry bits

Metaya BUI (control OBOGIESS BUS

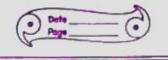
a nadress bus used to designate source & destination of data on data bus

101 DIO PUL

petermines memory copacity of processor W.C. = 50

n= no. of address lines

Dara Bus system modules. moving data beta



C CONTROL BUS ILINES

L USED to CONTROL ACCESS & the use of data & addre
SS lines

Interrupt request, Interrupt acknowledge

TIGNOIL NOID

Auto mated Calculator

A EXCUSIO POLY WO 18 WILLS)