

18th

Dec

Instructions instn

\downarrow
XCHG
SREG

Addressing mode X
Immediate X

reg dir

(ix) SBB R/M (sub w. BORROW)

\downarrow
1 byte instn

- ↳ sub contents of reg or memory
- ↳ & borrow from contents of accumulator & stores result in accumulator.

• Eg:

SBB D

$$A = A - D - \text{BORROW}$$

(x) SBT 8 bit data (sub. w. Borrow immediate)

\downarrow
2 byte instn

- ↳ subtracts 8-bit immediate data & borrow from content of A & stores result in accumulator

• Eg:

SBT 7DH

$$A \leftarrow A - 7D - \text{BORROW}$$

reg indirect

(ii) DAD RP (double addition)

↳ 1 byte instⁿ↳ adds reg pair w. HL pair↳ store 16 bit
result in HL pair

• EG:

LXI H, 7320H

LXI B, 4220H

DAD B

↓

$$HL = HL + BC$$

$$(7320 + 4220 = B540H)$$

(xi)

DAA → asked → implied

(decimal adjustment Accumulator)

↳ used only after addition

↳ 1 byte instⁿ↳ content of A is changed frombinary $\xrightarrow{+0}$ 3 4-bit BCD
digits

Eg: MVI A, 78H ; A = 78H
MVI B, 42H ; B = 42H
ADD B ; A = A + B
DAA

$(78H + 42H) \Rightarrow 1BAH$

↓
 $A = 20, CY = 1$

• BCD addition

↓
not
asked

L Any no. larger than 9 (A to F)
is invalid.

↓ needs to be adjusted by
adding in binary

6

Eg: ADD 77 48

$$\begin{array}{r} 77 = 0111\ 0111 \\ + 48 = 0100\ 1000 \\ \hline 125 \end{array}$$

79 ↙ 1011 ↘ 79
+ 0110
10101

$$\begin{array}{r}
 1011 \\
 + 0110 \\
 \hline
 10101
 \end{array}$$



+ 0110

$CY = 1 \quad 0010\ 0101$

[25 BCD]

• SUBTRACTION

→ Using 2's complement

→ complement carry flag

L MVI A, 97 H

MVI B, 65 H

SUB B

HLT

$$97 = 10010111$$

$$65 = 01100101$$

↙

2's complement

1's complement

$$\begin{array}{r}
 10011010 \\
 + 1 \\
 \hline
 10011011
 \end{array}$$

2's complement

$$\begin{array}{r}
 10011010 \\
 + 1 \\
 \hline
 10011011
 \end{array}$$

$$10011011$$

$$97 - 65$$

$$\Rightarrow 97 + (-65)$$

$$\begin{array}{r}
 \begin{array}{r}
 10010111 \\
 + 10011011 \\
 \hline
 100110010
 \end{array} \\
 \begin{array}{r}
 10101010 \\
 \text{complement for carry flag}
 \end{array}
 \end{array}$$

$$\therefore CY = 0, 32H$$

(2) MVI A, 65H

MVI B, 97H

SUB B

HIT

$$\hookrightarrow 65 - 97$$

$$65 = 01100101$$

$$97 = 10010111$$

$$\begin{array}{l}
 \hookrightarrow 1's \text{ complement} \\
 = 01101000
 \end{array}$$

• 2's complement

$$\Rightarrow 01101001$$

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Then,

$$65 + (-97)$$

$$\begin{array}{r} 011000101 \\ + 01101001 \\ \hline 11001110 \end{array}$$

yes 2's complement

negative ans



• 1's complement

$$00110001$$

• 2's complement

$$00110001$$

$$+ 1$$

$$\begin{array}{r} 000110010 \\ \hline \end{array}$$

↓ 13 → 2

complement for carry flag

1

$$\therefore CY = 1$$

32H

logical group inst^d

↳ implicitly assume that A is one of the operands

↳ All reset carry flag

↓ except

for complement where
flag is unchanged

↳ modify • Z
 • P] acc. to data condn
 • S of results

↳ place result in R.

↳ DO NOT affect contents of operand register.

AND

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

OR

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

NOT

A	Y
0	1
1	0
0	1
1	0

NOR

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

NAND

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

X-NOR

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

X-OR

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

• Eg: ANA R ; A \leftarrow Adf R

ANA M ; A \leftarrow Adf [M]

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i) ANA R/M

- ↳ logically AND contents of register M.
- w. contents of accumulator.

I WRAP TO AND CONTENT OF B & F & DISPLAY O/P
AT PORT 45H

MVI B, 56H

56 = 010101100

MVI E, 95H

95 = 1001010101100

MOV A, B

00010100

ANA F

↓

OUT 45H

14H AND
GND

HLT

ii) ANI 8 bit data

- ↳ 2 byte instn

↳ logically AND 8 bit immediate
data w. content of A.

Eg:

A \leftarrow A & 8 bit data

ANI 22H ; A \leftarrow A AND 22H

iii) ORA RIM

↳ logically OR the content of A w. content of
reg / mem

[.CY]
[&] is reset
[.AC]

& other as per result.

iv) ORI 8 bit data

↳ logically OR 8 bit immediate data w.
contents of ACCUMULATOR.

[.CY]
[&] is reset
[.AC]

& other as per result.

ED: MVI A, 42H

MVI B, 85H

DRA B

HIT