

# INSTRUMENTATION II (III/I)

Course Code: EX-602  
(Module#4)

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# CHAPTER #4

## INTERFACING A/D AND D/A CONVERTERS

### ✓ Class Outline

- ① Introduction to DAC/ADC Converter
- ② General terms in ADC and DAC
- ③ Examples of ADC and DAC Interface
- ④ Selection Criteria based on Design Requirements

# Introduction to DAC/ADC Converter

## Need of ADC and DAC

- Real world signals are analog, but processing units take and process the signal in digital form.
- Signal storage in analog form is difficult, so requiring digital conversion.
- as a solution, there exists analog to digital converter specifying resolution – inverse of information loss probability.

## Analog to Digital Converter

- A/D conversion involves sampling/discretization, and quantization with some error or information loss - higher the difference between two succeeding samples higher the loss is.

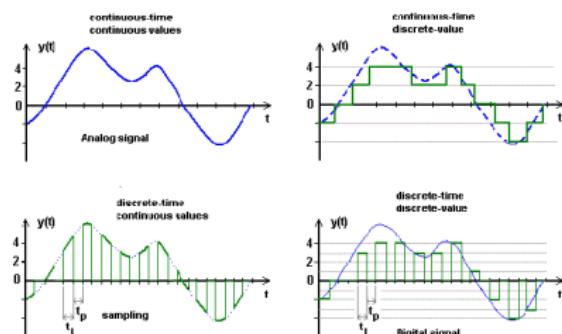
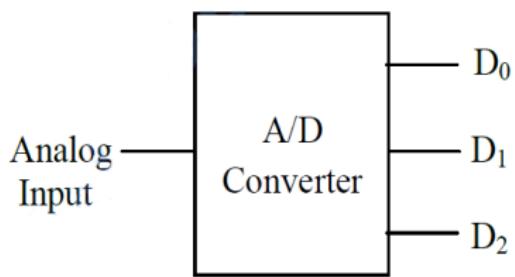
# Introduction

## Analog to Digital Converter....

- A/D conversion can be classified into two group:
  - ① Analog signal is compared with equivalent signal generated without discretization of target signal – it includes:
    - ✓ successive approximation, ✓ counter and ✓ flash type
  - ② Changing an analog signal into time or frequency and comparing new parameters to known value – it includes:
    - ✓ integrator converter, and ✓ voltage to frequency converter.
- Generally, successive approximation and flash type converters are faster with some information loss or lesser accuracy than integrator and voltage to frequency converters.
- Flash type converters are expensive and difficult or complex in design for higher accuracy.

# Introduction

## Analog to Digital Converter....



**Fig. 1** 3-bit ADC Block Diagram

**Fig. 2** sampling and discretization

- Above mentioned A/D converter can convert an analog signal into equivalent 8 ( $2^3$ ) states from '000' to '111'.
- if analog signal has max voltage level ' $a$ ' v then resolution is  $\frac{a}{8}$  v each state equivalent to  $\frac{1}{8}$  of  $a$ .

# General terms in ADC and DAC

## Characteristics of A/D Converters

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- ① Resolution : is the smallest change that can be represented distinguishably in digital form.

$$\text{Resolution} = \frac{\text{Full Scale Range}}{2^n}$$

- ② Conversion time : time required to convert an analog signal into digital output.
- ③ Accuracy : comparison of actual output and the expected output.
- ④ Linearity : output should be linear function of input.
- ⑤ Full scale output value : is max bit output achieved from the respective input.

# Different types of A/D Converters

## # 1. Successive Approximation A/D Converter

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- Common most A/D converter.
- Faster conversion time compared dual slope, but slower than flash type; it has fixed conversion time.
- It requires digital to analog converter.
- successive approximation register generates series of bit and D/A converter converts bits to analog which is compared with analog signal to be digitized.
- $V_{ref}$  signifies the maximum voltage D/A converter (in Successive Approximation) can convert to analog voltage.

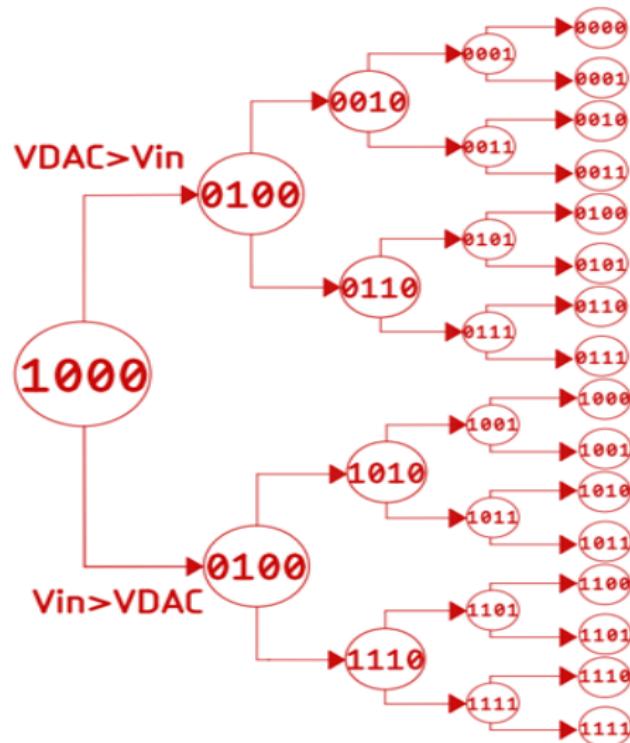
# Different types of A/D Converters

## Example of 4-bit Successive Approximation A/D converter:

- ✓ Successive Approximation generator/register generates 1000 and its analog value is compared with target signal;
- ✓ if converted analog signal is greater, 1 is flipped to 0.
- ✓ in next clock, second bit is changed to 1 if converted value is smaller and the process continues up to LSB.

# Different types of A/D Converters

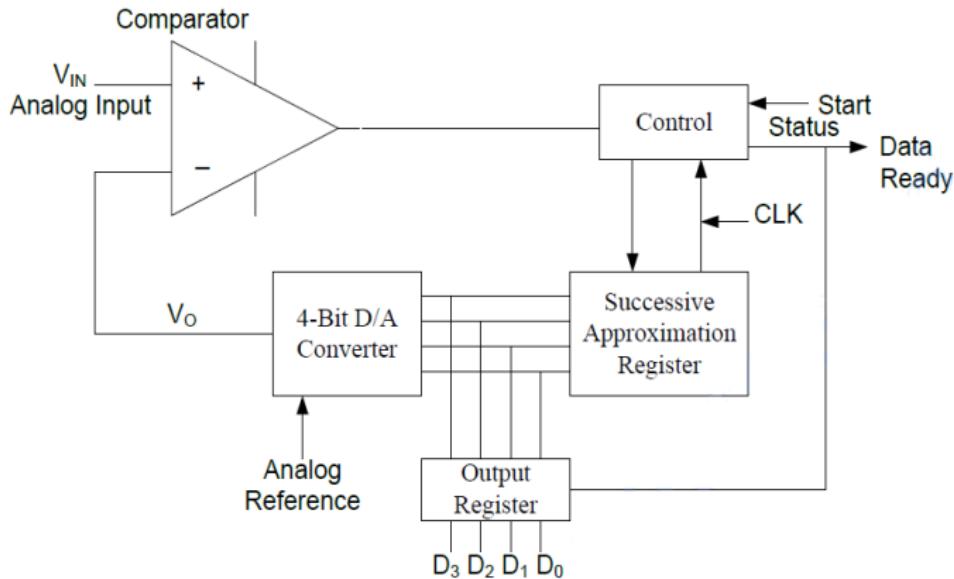
## # 1. Successive Approximation A/D Converter...



Successive Approximation ADC method

# Different types of A/D Converters

## # 1. Successive Approximation A/D Converter...



**Fig. 3** Block Diagram for Successive Approximation A/D Converter

# Different types of A/D Converters

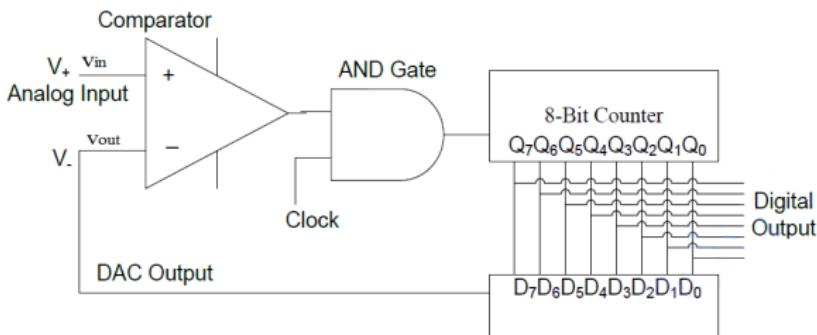
## Major Components in Successive Approx A/D Converter

- ① D/A Converter
- ② Successive Approximation generator register
- ③ Comparator.

When D/A Converter value matches to input signal to be converted, corresponding digital signal generated at Successive Approximation Register is equivalent digital value.

# Different types of A/D Converters

## # 2. The Counter type A/D Converter

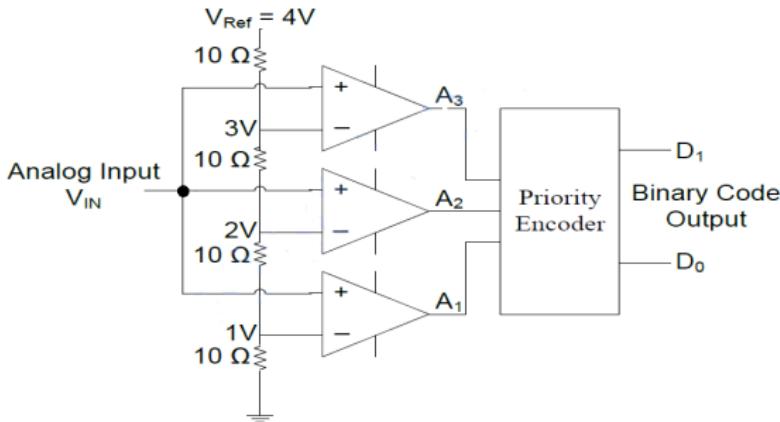


**Fig. 4** Block Diagram for 8bit Counter Type A/D Converter

- as long as  $v_{in}$  is greater than DAC output, counter o/p  $v_{out}$  is converted to analog and compared with  $v_{in}$
- counter counts up till the DAC output matches input signal  $v_{in}$
- once DAC output  $v_{out}$  and  $v_{in}$  equals, the AND out is low and counter stops to count.
- the corresponding digital output of the counter is equivalent digital value to  $v_{in}$

# Different types of A/D Converters

## # 3. The Flash type ADC (Parallel Comparator)



**Fig. 5** Block Diagram for Flash Type 2bit A/D Converter

- Fastest ADC with comparator to compare reference voltage with input analog voltage.
- output of the comparator is converted to equivalent binary with priority encoder.

# Different types of A/D Converters

## # 3. The Flash type ADC (Parallel Comparator)...

- for  $n$  bit ADC  $2^n - 1$  comparator is needed.
- It can be used for video signal digitization because of less conversion time.
- voltage dividers set reference voltage on the inverting inputs of each comparator.
- voltage at the top of the divider chain represents full scale value for ADC.
- voltage to be digitized is applied to non-inverting input of each comparator.

# Different types of A/D Converters

## # 3. The Flash type ADC (Parallel Comparator)...

- if the voltage to non-inverting input is greater than reference voltage(input to inverting), comparator output goes high.
- the output of the comparators gives the digital representation of the input voltage level.
- **Advantage:** very fast, clock is not required.
- **Disadvantage:** expensive, high power, complexity doubles for each additional bit.

# Different types of A/D Converters

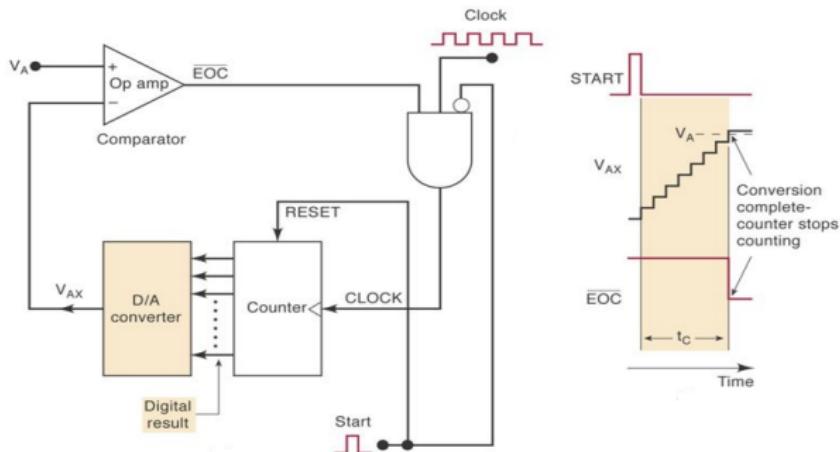
## # 3. The Flash type ADC (Parallel Comparator...)

$V_{in}$	$A_3$	$A_2$	$A_1$	$D_1$	$D_2$
$0 \leq V_{in} \leq 1$	0	0	0	0	0
$1 \leq V_{in} \leq 2$	0	0	1	0	1
$2 \leq V_{in} \leq 3$	0	1	1	1	0
$3 \leq V_{in} \leq 4$	1	1	1	1	1

- For instance, let say input voltage 2.6 v.
- output of comparators  $A_1$  and  $A_2$  will be high.
- Priority Encoder produces a binary output corresponding to the input having the highest priority.

# Different types of A/D Converters

## # 4. Ramp (staircase) ADC/ Dual Slope Ramp ADC

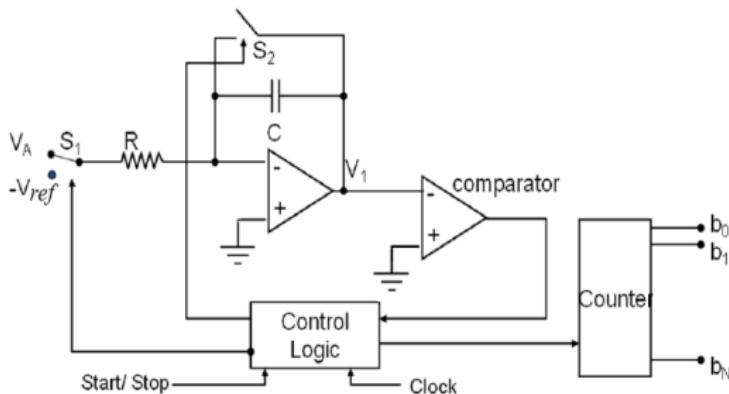


**Fig. 6** Block Diagram for Ramp/staircase A/D Converter

- it is counter type ADC.
- when DAC output increases to exceed  $V_A$  at some point comparator output triggers to stop binary counter.
- corresponding binary value is required binary equivalent of  $V_A$ .

# Different types of A/D Converters

## # 4. Ramp (staircase) ADC/ Dual Slope Ramp ADC...

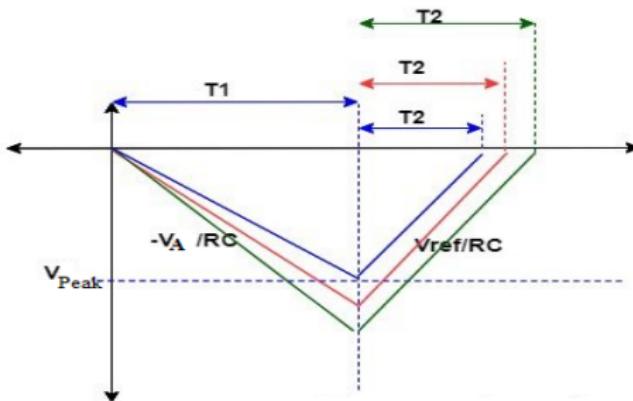


**Fig. 7** Block Diagram for Dual Slope Ramp A/D Converter

- ADC generates dual slope; one with  $V_A$  and another with  $-V_{ref}$
- initially, counter is set to  $0_n 0_{n-1}..0$ ; integrator output is 0v
- the input  $V_A$  is integrated by inverting integrator, so the negative ramp output, positive O/P from comparator triggers the count to time  $T_1$ .

# Different types of A/D Converters

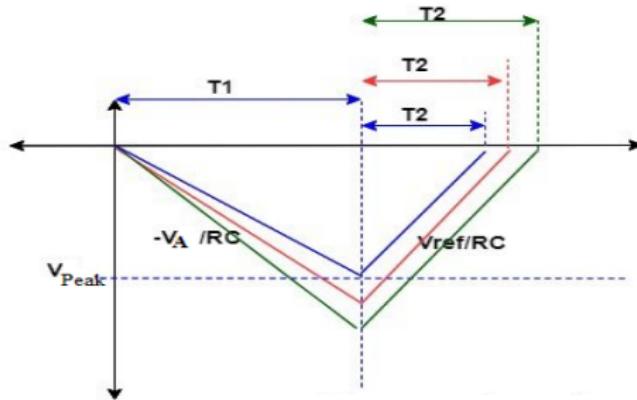
## # 4. Ramp (staircase) ADC/ Dual Slope Ramp ADC...



- At the end of time  $T_1$ , ramp O/P is  $V_s = -\frac{V_A}{RC} \times T_1 [= V_{Peak}]$ .
- At time  $T_1$  counter reset to 0, integrator I/P flipped to  $-V_{ref}$ .
- The counter starts counting for  $T_2$  until  $-V_{Peak}$  reached to 0v.
- Conversion cycle is completed at this point; positive ramp voltage is given by  $V_s = \frac{V_{ref}}{RC} \times T_2$

# Different types of A/D Converters

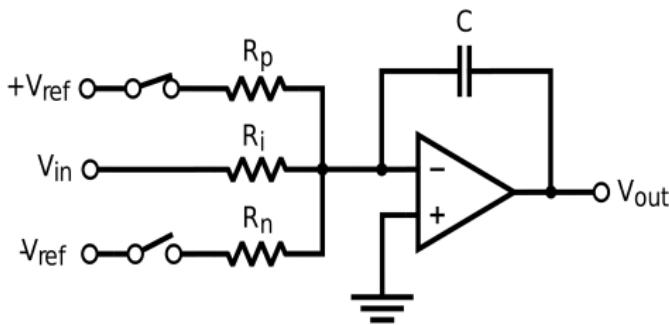
## # 4. Ramp (staircase) ADC/ Dual Slope Ramp ADC...



- being ramp voltage start from 0 to  $-V_S$  and return to 0,  
 $\frac{V_{ref}}{RC} \times T_2 = -\frac{V_A}{RC} \times T_1 \Rightarrow V_A = -V_{ref} \times \frac{T_2}{T_1}$
- binary counter value during time  $T_2$  is the equivalent digital value for  $V_A$ .

# Different types of A/D Converters

## # 4. Ramp (staircase) ADC/ Dual Slope Ramp ADC...

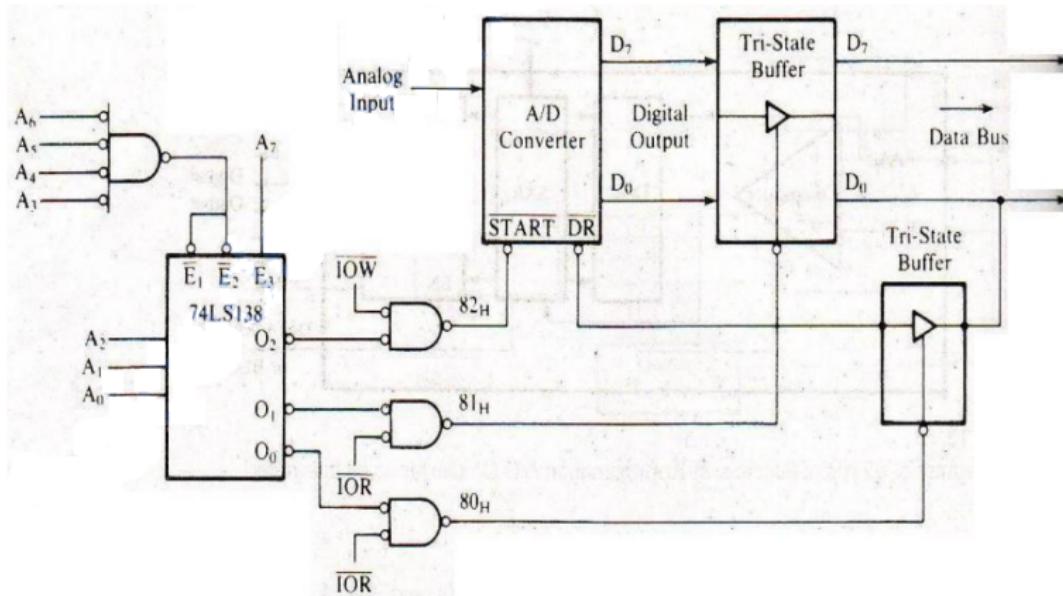


**Fig. 8** Integrator circuit for multi-slope run-down

- this kind of ADC is generally used in voltmeter, because of slower speed;  $T_1 + T_2$  time for analog to digital conversion.
- but the resolution can be increased with increased clock frequency to control logic.

# Examples of ADC and DAC Interface

## Interfacing 8-bit ADC using status check



**Fig. 9** Interfacing an ADC using status Check

# Examples of ADC and DAC Interface

## Interfacing 8-bit ADC using status check

- ADC has one analog input and 8bit output line for converted digital output signal.
- Typically, analog signal ranges from 0 to 10 v or 0 to  $\pm 5$ v.
- when active low to  $\overline{START}$ ,  $\overline{DR}$  goes high and O/P line goes into high impedance state.
- when conversion completes,  $\overline{DR}$  goes low and data are made available at output port or output line from where processor reads the digital signal.
- while interfacing ADC, there is need of one output line ( $\overline{IOW}$ ), and two input line  $\overline{IOR}$  – one to read status of  $\overline{DR}$  while another to read data (converter output).

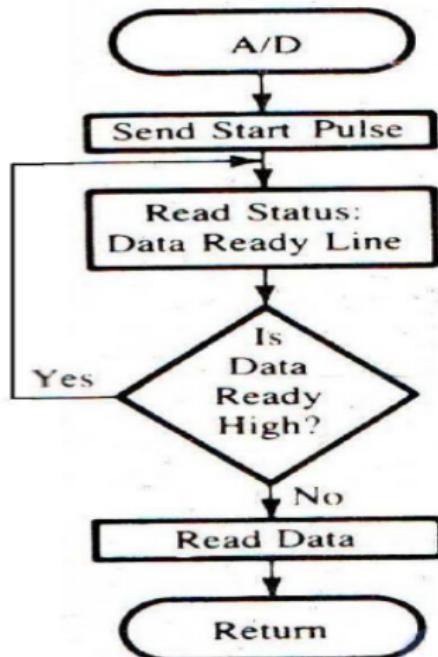
# Examples of ADC and DAC Interface

## Interfacing 8-bit ADC using status check

- Output port 82H of decoder is used to send start pulse with OUT instruction.
- when conversion begins,  $\overline{DR}$ (Data Ready) goes high and stay high till conversion completes.
- the status of  $\overline{DR}$  line is monitored by connecting  $\overline{DR}$  line to bit  $D_0$  through tri-state buffer with input port 80H
- when  $\overline{DR}$  goes low, data are available on output line; this can be done by reading port 81H.

# Examples of ADC and DAC Interface

## Interfacing 8-bit ADC using status check



**OUT 82H** : start conversion

**TEST:**

**IN 80H** : read data ready status

**RAR** : rotate  $D_0$  into carry

**JC TEST** : if  $D_0 = 1$ , conversion is not completed yet

**IN 81H** : Read Output and save it in Acc

**RET** : Return.

## Flow chart of ADC Process

# Examples of ADC and DAC Interface

## Integrating 8-bit ADC using Interrupt

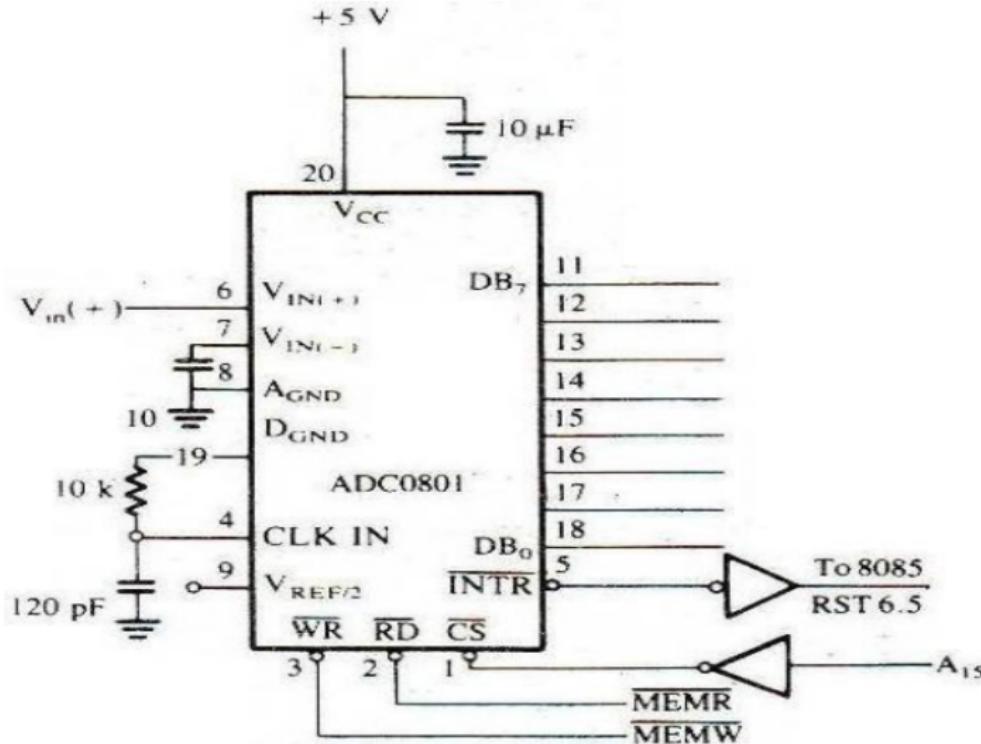


Fig. 10 Interfacing an ADC using Interrupt

# Examples of ADC and DAC Interface

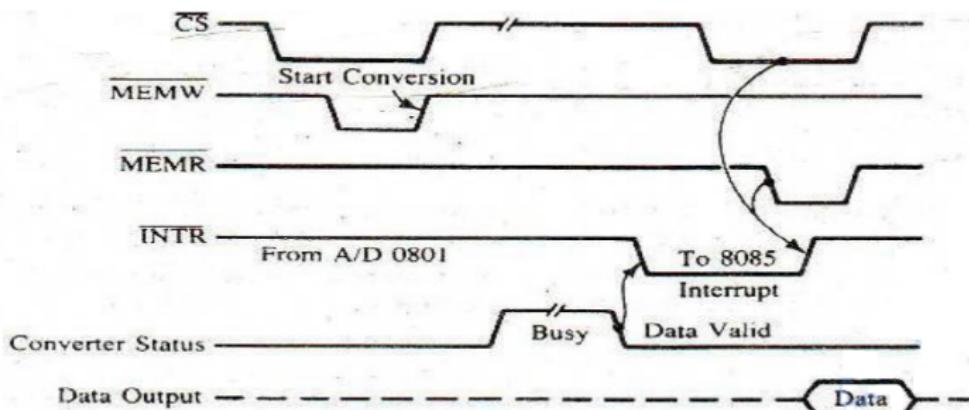
## Integrating 8-bit ADC using Interrupt

- ADC0801 is Successive Approximation type ADC with 20 pins.
- Converter requires clock, so CLK IN (pin-4) as shown; it ranges from 100KHz to 200KHz.
- Fig. 10 shows the use of internal clock connecting pin 19 with resister and pin 4 with capacitor.
- Frequency is evaluated as  $F = \frac{1}{1.1 \times RC}$
- When  $\overline{CS}$  and  $\overline{WR}$  go low, conversion starts.
- $\overline{WR}$  low resets internal Successive Approximation Register (SAR) and output line goes into high impedance state.
- Transition of  $\overline{WR}$  from low to high signifies conversion started.
- Once conversion is completed,  $\overline{INTR}$  is asserted low placing data at output line;  $\overline{INTR}$  signal to the processor for data reading.

# Examples of ADC and DAC Interface

## Integrating 8-bit ADC using Interrupt

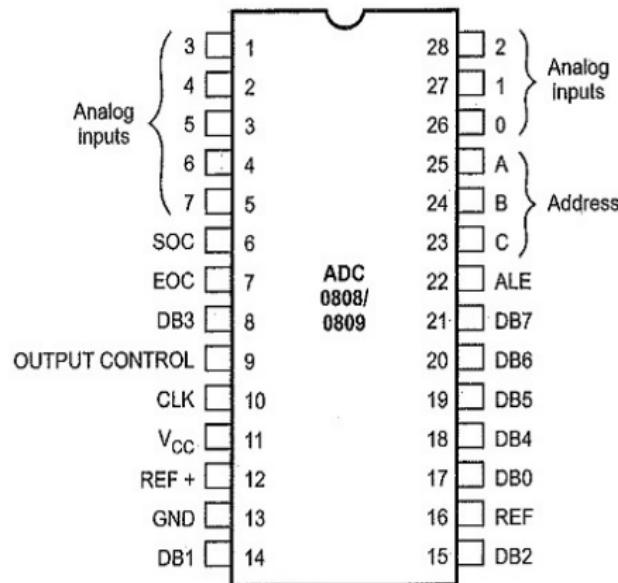
- Processor reads the data by asserting  $\overline{RD}$  and  $\overline{INTR}$  is set when read is complete.
- when  $V_{cc}$  is +5v, the input can range from 0v to 5v and corresponding output from 00H to FFH.
- pin 9 can be used to limit the full-scale output lower than 5v.



**Fig. 11** Timing Diagram for Reading Data from ADC

# Examples of ADC and DAC Interface

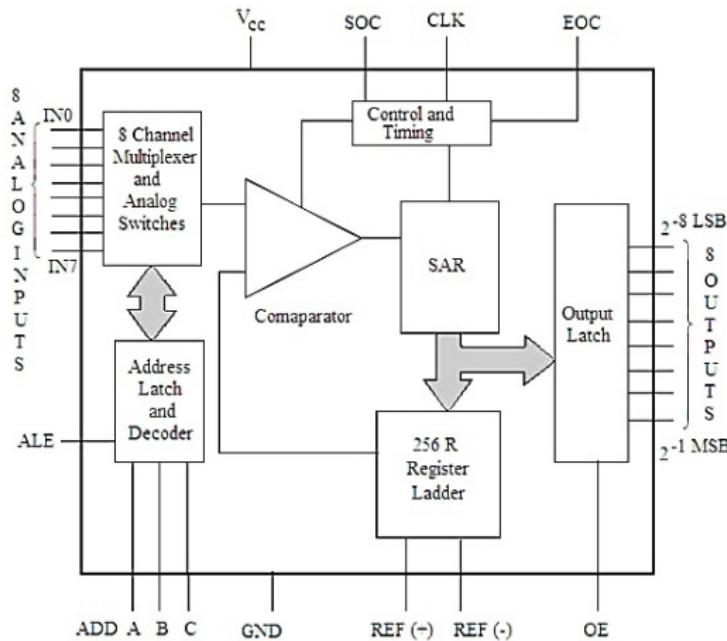
Integrating 8-bit/ 8-channel (0808/0809) ADC using status check



**Fig. 12** Pin Diagram of ADC (0808/0809)

# Examples of ADC and DAC Interface

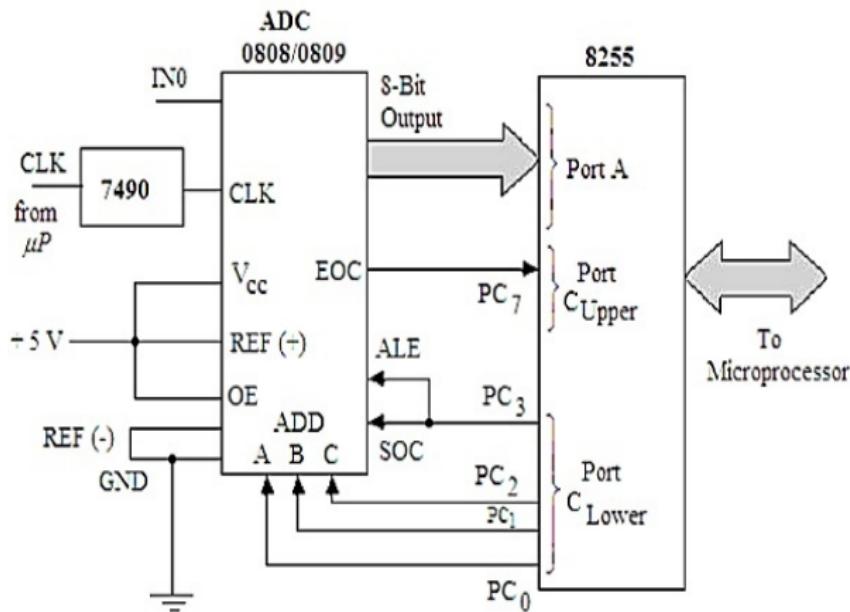
## Integrating 8-bit/ 8-channel (0808/0809) ADC using status check



**Fig. 13** Detail Internal Block Diagram of ADC (0808/0809)

# Examples of ADC and DAC Interface

## Integrating 8-bit/ 8-channel (0808/0809) ADC using status check



**Fig. 14** Interfacing ADC(0808/0809) using 8255 PPI (base address 00H)

# Examples of ADC and DAC Interface

## Integrating 8-bit/ 8-channel (0808/0809) ADC using status check

**MOV A, 89H** : Port A/Port B (input), PCu(input)

**OUT 83H** : Control word to Control Reg.

### START\_CONVERSION:

**MVI A, 00H** : Channel 0 address (A=0, B=0, C=0)

**OUT 82H** : Output to Port C lower bits to select channel

**MVI A, 08H** : Set ALE (PC3) high to latch the address

**OUT 82H** : Output to Port C to latch the address

**NOP** : Small delay to ensure ALE is high

**MVI A, 00H** : Set ALE/START(PC3) low

**OUT 82H** : Output to Port C to start the conversion

# Examples of ADC and DAC Interface

## Integrating 8-bit/ 8-channel (0808/0809) ADC using status check

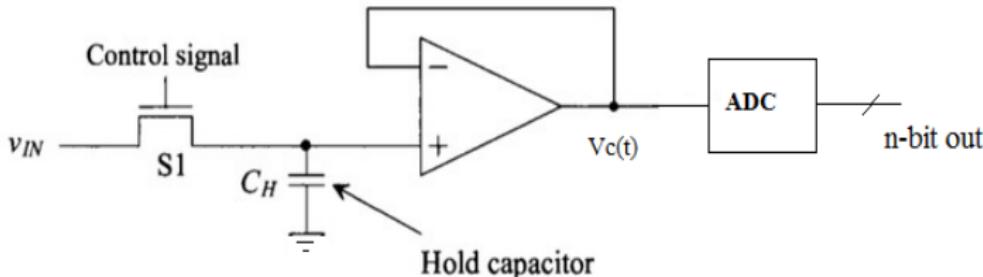
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**WAIT\_EOC:**

- IN 82H** : Read from Port C (EOC)
- ANI 80H** : Mask all but the EOC bit (PC7)
- JZ WAIT\_EOC** : Wait until EOC is high
- IN 80H** : Read from Port A (data lines)
- HLT** : Halt the processor

# Sample and Hold Circuit

## Sample and Hold Circuit



**Fig. 15** Sample and Hold Circuit

- Sample and hold circuit is used to sample and hold the sample voltage to be fed to ADC keeping sample voltage constant with hold capacitor during conversion time.
- Sampling process can be equivalently represented with multiplication of input signal by train pulse.
- To hold the sampled voltage, switch is opened; voltage follower cause capacitor to hold voltage with high input impedance.

# Sample and Hold Circuit

## Quantization

- Process of converting sampled value to a discrete value which is suitable to digitize.

## Binary Coding

- Method to assign binary equivalent to discrete level quantized.

## Sampling Rate

- the sampling rate is the frequency to take the sample of input continuous signal.
- Because of quantization error, there is probability of information loss when digital signal is converted back to continuous signal.

# Sample and Hold Circuit

## Nyquist Sampling Criteria

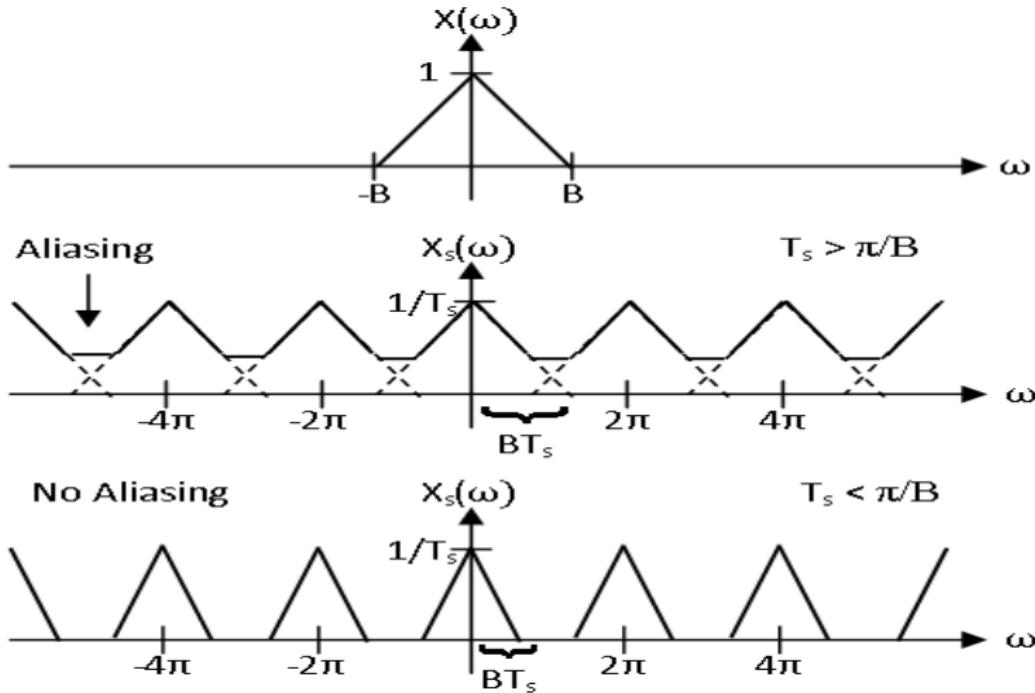
- Lowest possible sampling rate is twice that of highest frequency (components with significant amplitude) of input signal,  
 $f_s \geq 2B$ ;  $B$  is Nyquist frequency.
- sample and hold circuit must hold the value to be converted till conversion time.

## Aliasing

- when sampling frequency is smaller than max frequency content of input signal, there could be over-lapping of side bands (not exact replica) in frequency domain when the signal is recreated from digital signal to analog signal.
- to avoid this effect either sampling frequency can be increased or some bands of insignificant amplitude can be filtered out using anti-aliasing filter.

# Sample and Hold Circuit

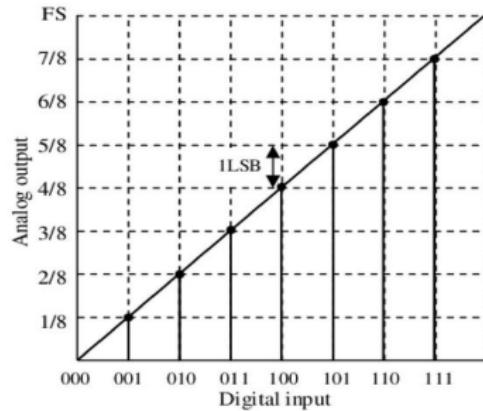
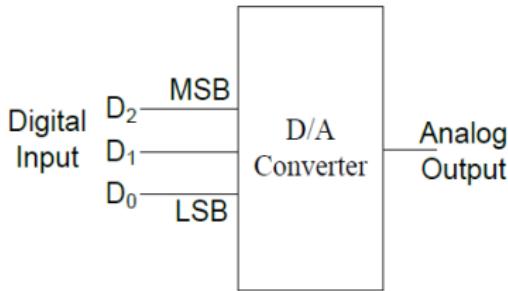
## Aliasing ...



**Fig. 16** Aliasing phenomena

# Digital to Analog Conversion (DAC)

- DAC generates analog equivalent of digital value; information can be integrated into either voltage or current.
- Voltage output DAC is comparatively slower than current output DAC – taking time while converting current into voltage.



**Fig. 17** Simple block diagram for DAC and conversion graph

# Digital to Analog Conversion (DAC)

## Characteristics of DAC

### Resolution

- input binary bit determines the resolution of DAC; 12-bit converter has resolution of 1 part in  $2^{12}$

### Full scale output voltage/current

- maximum voltage/current output for all input bits are high plus 1 LSB value is Full scale output.

### Accuracy

- the accuracy is the measure of difference between actual output and expected output.
- DAC with  $\pm 0.2\%$  error and full scale output 10v will produce maximum error of 20mv

$$\frac{0.2}{100} * 10v = 20mv$$

# Digital to Analog Conversion (DAC)

## Characteristics of DAC...

### Linearity

- theoretically, DAC should be linear; output voltage should be linear function of input binary function.
- deviation from linearity in DAC are due to non-exact value of resistors, non-ideal switches.
- non-linearity is amount by which actual output is deviated from expected one.

### Temperature Coefficient

- it is the degree of inaccuracy that the temperature change can cause to any of the parameters of the DAC.

# Digital to Analog Conversion (DAC)

## Characteristics of DAC...

### Monotonicity

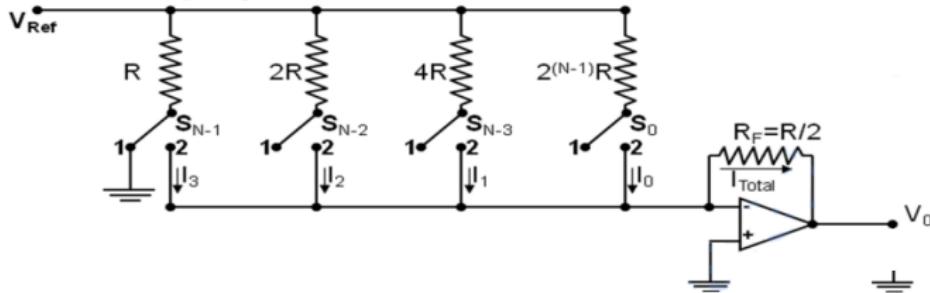
- when DAC analog output follows direction of the digital input then DAC is monotonic.
- that is, analog output is consistently increases as input increases, and decreases as input decreases.

### settling time

- Generally, output overshoot when input changes from one value to another and may oscillate around the new value.
- settling time is time interval between instances of fluctuating analog value to specified error band about its final value.

# Digital to Analog Converters

## DAC with Binary Weighted Resistor Networks(WRN)



**Fig. 18** DAC with Binary Weighted Register Network

$$I_{Total} = \frac{V_{ref}}{R} S_{N-1} + \frac{V_{ref}}{2R} S_{N-2} + \dots + \frac{V_{ref}}{2^{N-1}R} S_0$$

$$I_{Total} = \frac{2V_{ref}}{R} \left( \frac{S_{N-1}}{2^1} + \frac{S_{N-2}}{2^2} + \dots + \frac{S_0}{2^N} \right) = \frac{2V_{ref}}{2^N R} D$$

$$V_0 = -I_{Total} R_F = -\frac{V_{Ref}}{2^N} D$$

# Digital to Analog Converters

## DAC with Binary Weighted Resistor Networks(WRN) ..

- Accuracy of WRN is determined by  
⇒ Accuracy of  $V_{Ref}$ , precision of Binary weighted registers, and perfection of switches.
- Drawbacks of Binary Weighted DAC  
⇒ for higher bit, smallest and largest resistor has larger gap, precise resistor value is unavailable, not practical for larger number of bits.

# Digital to Analog Converters

## R-2R Ladder Networks

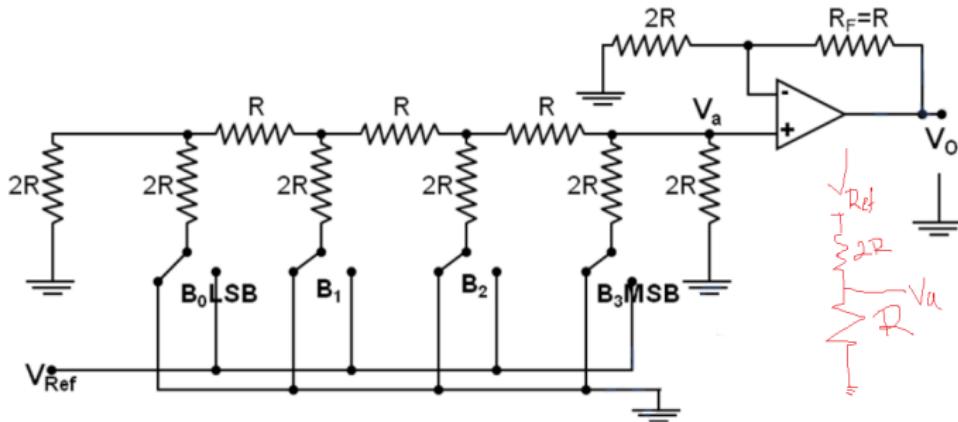


Fig. 19 R-2R Ladder Network

For MSB high:  $I = \frac{V_{Ref}}{(2R||2R)+2R} = \frac{V_{Ref}}{3R} \Rightarrow V_a = IR = \frac{V_{Ref}}{3}$

$$V_0 = \left(1 + \frac{R}{2R}\right)V_a = \frac{V_{Ref}}{2}$$

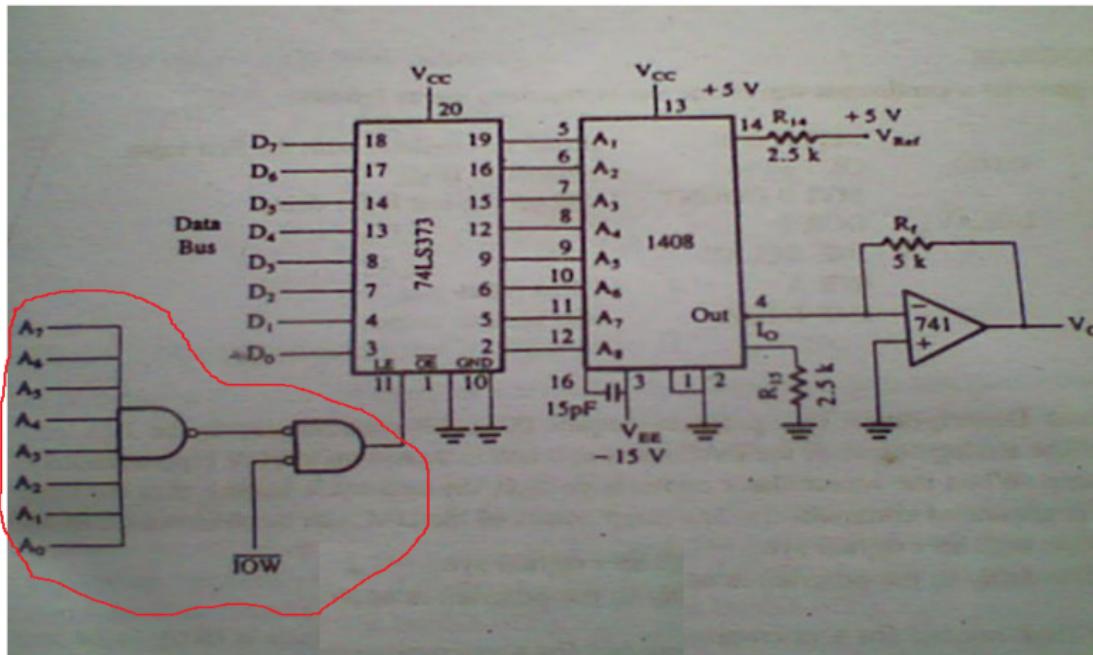
For Next to MSB bit high:  $V_0 = \frac{V_{Ref}}{2^2}$

For LSB bit high:  $V_0 = \frac{V_{Ref}}{2^n}$

# Interfacing 8-bit DAC with 8085

Design Problem: | DAC1408 sometime known as DAC0808

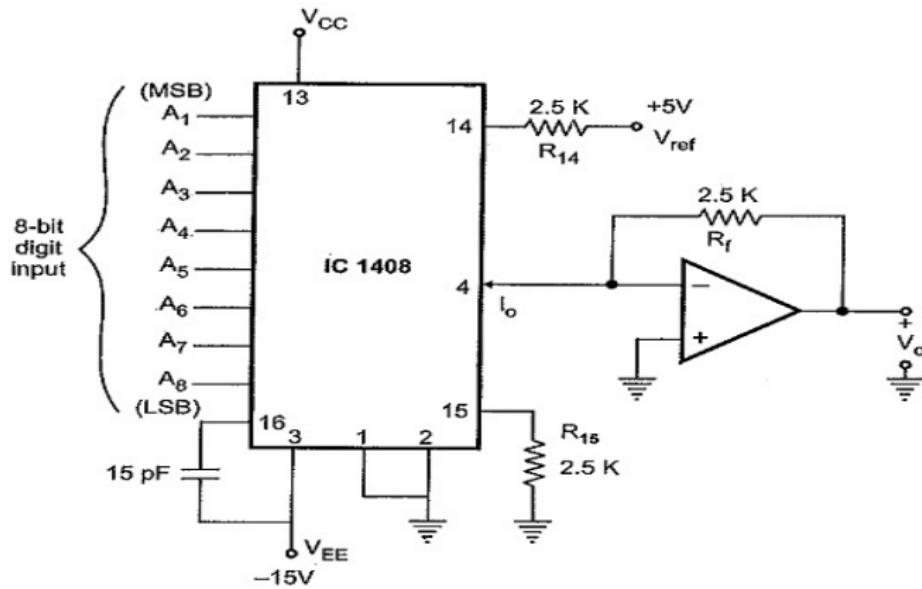
Interface 1408 (R-2R) calibrated 0 to 10v range with port FFH.



**Fig. 20** Interfacing 1408 DAC in unipolar Range

# Interfacing 8-bit DAC with 8085

1408 DAC interfacing for Uni-Polar output:



Interfacing 1408 DAC in unipolar range

# Interfacing 8-bit DAC with 8085

## Design Problem:

- Fig. 20 demonstrates simple interfacing to DAC 1408.
- Being address FFH, 8-input NAND gate and NOR equivalent gate (logic inside red segment) is used as interface logic.
- addressing from microprocessor as FFH enables Latch (74LS373) to place data bits to DAC 1408.
- Generally,  $R_{14}$  equals  $R_{15}$  to match input impedance of  $V_{Ref}$
- $R_f$  should be selected such that  $V_0$  is comparable to 10v for input bit all high.

$$I_0 = \frac{V_{Ref}}{R_{14}} \left( \frac{A_1}{2^1} + \frac{A_2}{2^2} + \dots + \frac{A_8}{2^8} \right)$$

For full scale input (all bit high):

$$I_0 = \frac{5v}{2.5K} \Rightarrow I_0 = 2mA \left( \frac{255}{256} \right) = 1.992mA$$

$$V_0 = I_0 \times R_f \Rightarrow V_0 = 9.961V$$

# Interfacing 8-bit DAC with 8085

1408 DAC interfacing for Bipolar output:

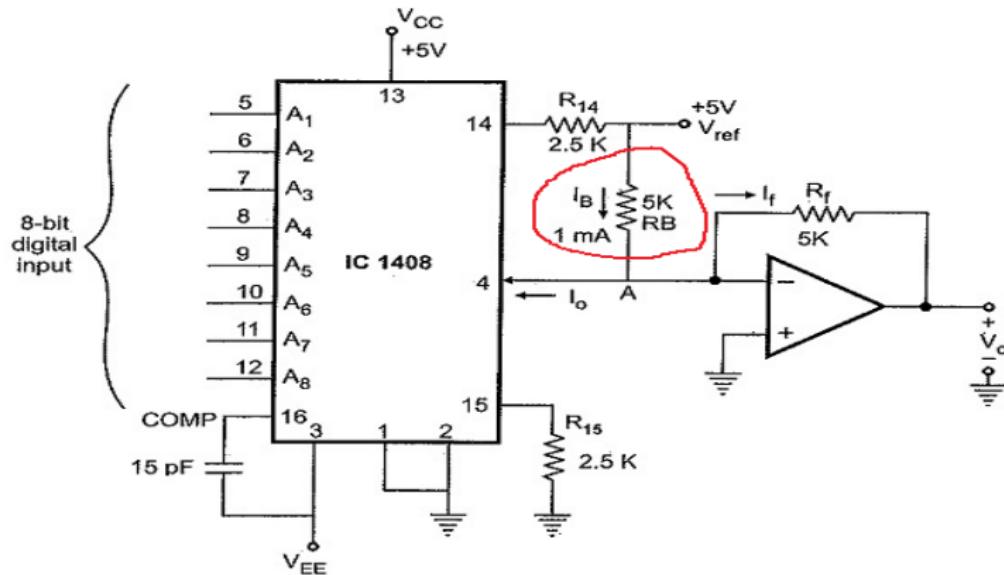


Fig. 21 1408 DAC configuration for bipolar output

# Interfacing 8-bit DAC with 8085

## Bipolar output:

- Fig. 21 demonstrates simple DAC 1408 to work as bipolar with additional resistor  $R_B$ .
- output voltage ranges from +5v to -5v;  $R_B$  supplies current towards output  $\Rightarrow I_f = I_0 - \frac{V_{ref}}{R_B}$

### When input is zero:

$$V_0 = I_f \times R_f$$

$$V_0 = \left( I_0 - \frac{V_{ref}}{R_B} \right) \times R_f \quad \Rightarrow V_0 = -5V$$

### When input is 1000 0000:

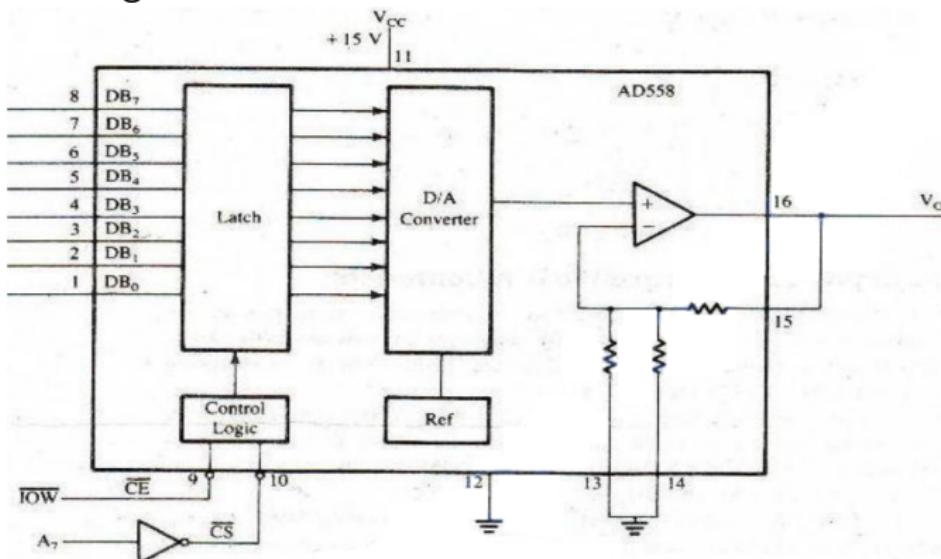
$$V_0 = I_f \times R_f$$

$$V_0 = \left( \frac{V_{ref}}{R_{14}} \times \frac{A_1}{2} - \frac{V_{ref}}{R_B} \right) \times R_f \quad (\rightarrow A_1 = 1) \quad \Rightarrow V_0 = 0V$$

# Interfacing 8-bit DAC with 8085

## Microprocessor Compatible DAC

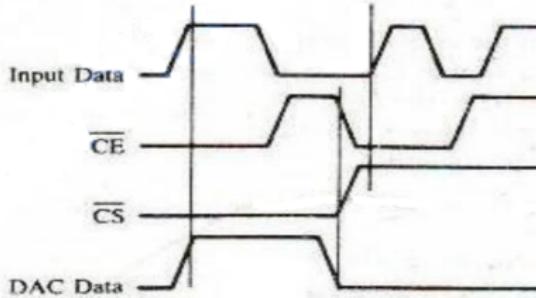
- simply because of growing need of DAC to interface microprocessor, external latch is included inside the DAC eliminating external need.



**Fig. 22** DAC Device with latch and Op-Amp internal to chip

# Interfacing 8-bit DAC with 8085

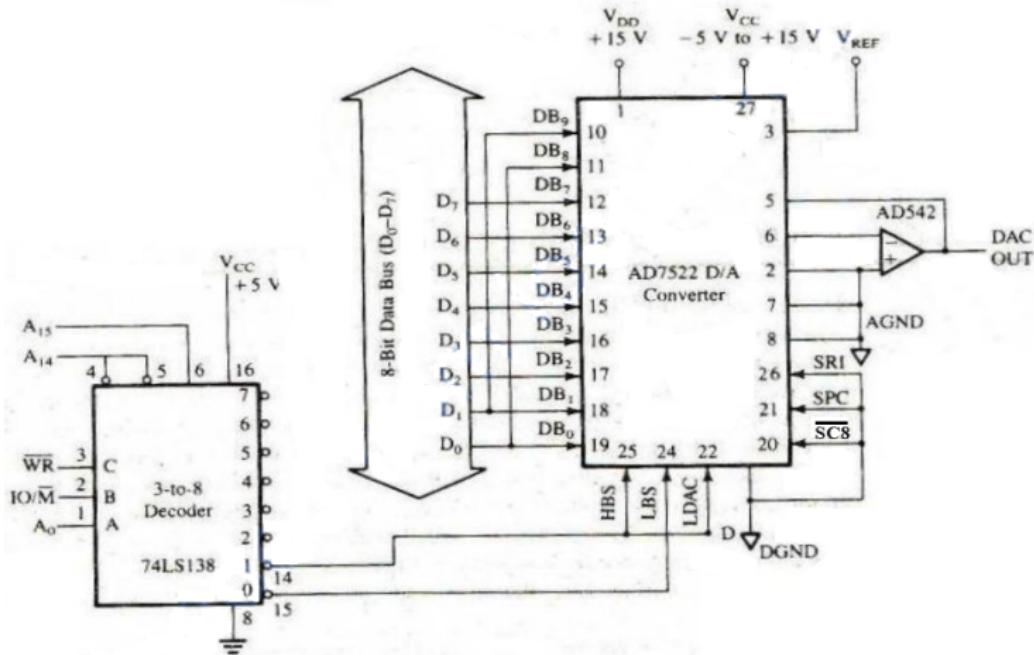
## Microprocessor Compatible DAC



**Fig. 23** Timing Diagram for Control Signals and Data transfer

- Two signals chip select ( $\overline{CS}$ ) and chip enable ( $\overline{CE}$ ) are used.
- As shown in Fig. 22  $A_7$ , is used for chip select through inverter and port address 80H assuming other address line low.
- when both the ( $\overline{CS}$ ) and ( $\overline{CE}$ ) are logic low, data is transferred to DAC otherwise transferred only to latch.

# Interfacing 10 bit DAC with 8085



**Fig. 24** Interfacing 10 bit DAC with 8085

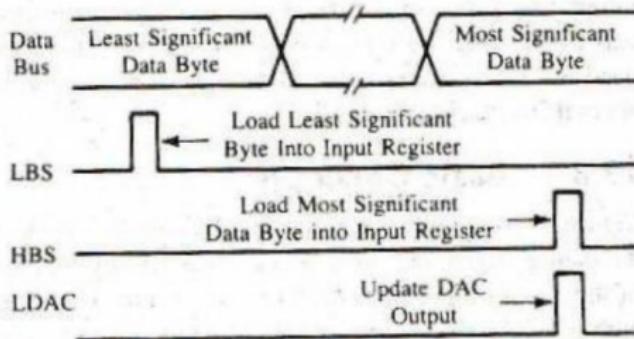
# Interfacing 10 bit DAC with 8085

- Generally, microprocessor are of 8 bit data line.
- When there is need of 10/12 bit data line, time shared method of transmission can be implemented.
- at first slot, 8 bit data, and other 2 bit at second slot.
- AD7522 is a CMOS 8/10 bit DAC with input buffer and holding register allowing direct interface with microprocessor.
- When pin 20 ( $\overline{SC8}$ /8bit Short Cycle Control) is held to logic “0” least two significant bits in buffer are ignored.
- When pin 21 (SPC/Serial-parallel control) is logic low, it accepts parallel input data (DB0-DB9); Pin 23 is no connection.
- While SPC is high, it accepts serial data from SRI (pin 26).

# Interfacing 10 bit DAC with 8085

- When control line LBS (Low Byte Strobe) is selected, lower 8 bits are loaded into input buffer;
- While rest 2 bits are loaded for HBS (High Byte Strobe) line select (provided SPC has log logic input).
- Then 10 bits are latched to holding register for conversion enabling LDAC (Load DAC) line.
- When data byte are sent to port 8000H with memory mapped I/O, with  $\overline{WR}$  and  $\overline{IO/M}$  signal goes low, LBS is enabled.
- Address port 8001H enables HBS and LDAC line to transfer data from input buffer to holding register.

# Interfacing 10 bit DAC with 8085



**Fig. 25** Timing Diagram for 10bit Digital to analog conversion

- LXI B, 03FFH : Load 10 bit at logic 1 in BC register
- LXI H, 8000H : Load HL with port address for lower 8 bits
- MOV M, C : Load 8 bit  $D_7 - D_0$  in the DAC
- INX H : Point to port address 8001H
- MOV M, B : Load bits  $D_9, D_8$ ; switch all 10 bits for conversion.
- RET : Return the routine

# Interfacing 12 bit DAC with 8085

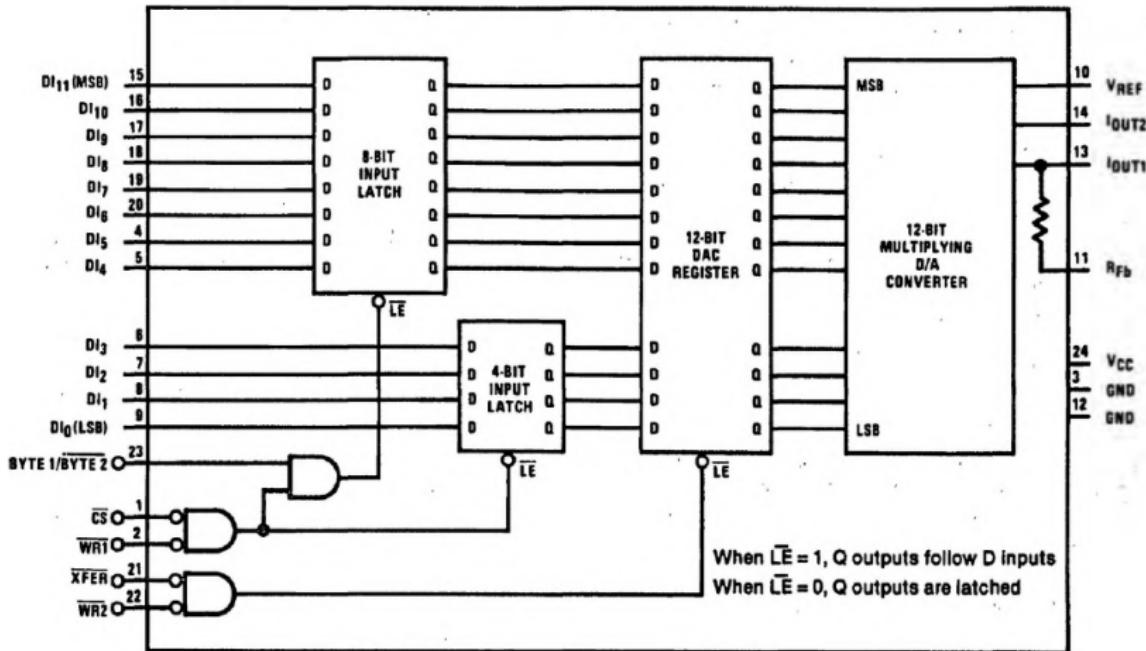


Fig. 26 Interfacing 12 bit DAC(1208/1209/1210) with 8085

# Interfacing 12 bit DAC with 8085

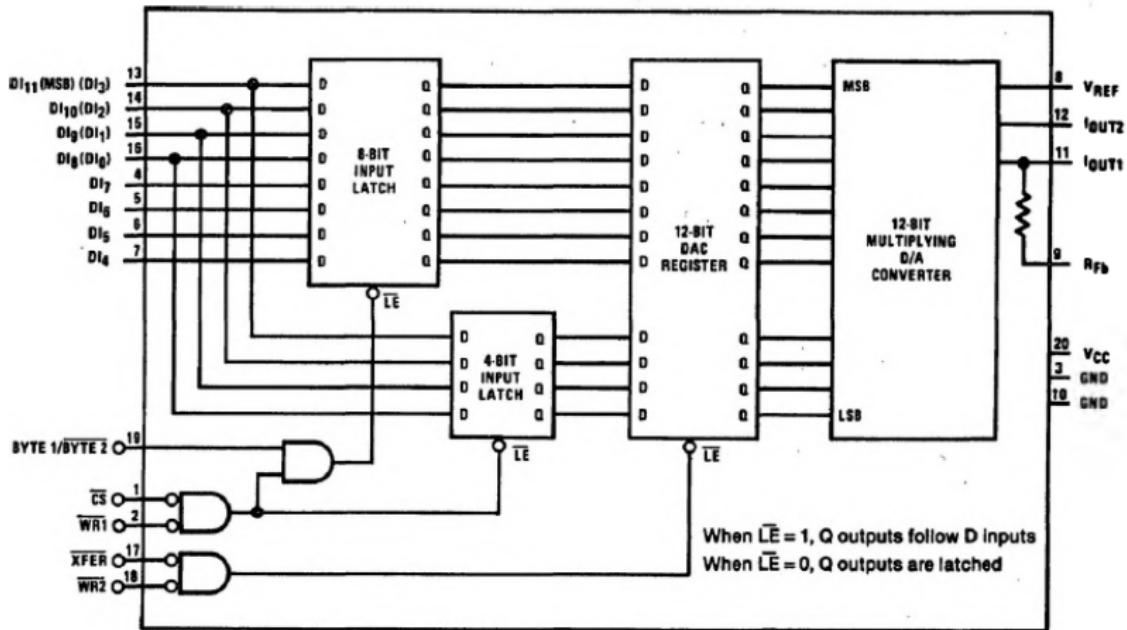


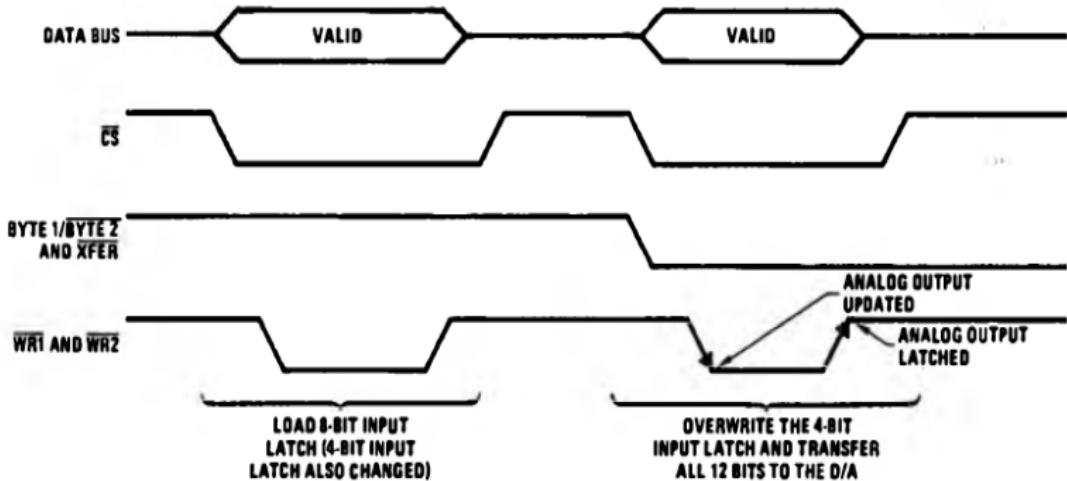
Fig. 27 Interfacing 12 bit DAC(1230/1231/1232) with 8085

# Interfacing 10 bit DAC with 8085

- At first cycle, when  $\overline{\text{BYTE1}}/\overline{\text{BYTE2}}$  is high and  $\overline{CS}$  and  $\overline{WR1}$  is low, 8 Most Significant bits are latched;
- At second cycle,  $\overline{\text{BYTE1}}/\overline{\text{BYTE2}}$  goes low and  $\overline{WR1}$  goes high and 4 Least Significant bits are latched;
- Once all 12 bits are latched;  $\overline{XFER}$  and  $\overline{WR2}$  go low to latch the input into 12bit DAC latch and conversion starts.
- Output  $I_{OUT1}$  is used for unipolar output while  $I_{OUT1}$  and  $I_{OUT2}$  are used for bipolar output.

# Interfacing 10 bit DAC with 8085

- DAC is double buffered to allow 12bit format internally.
- These DAC can be mapped as two byte stack in memory.

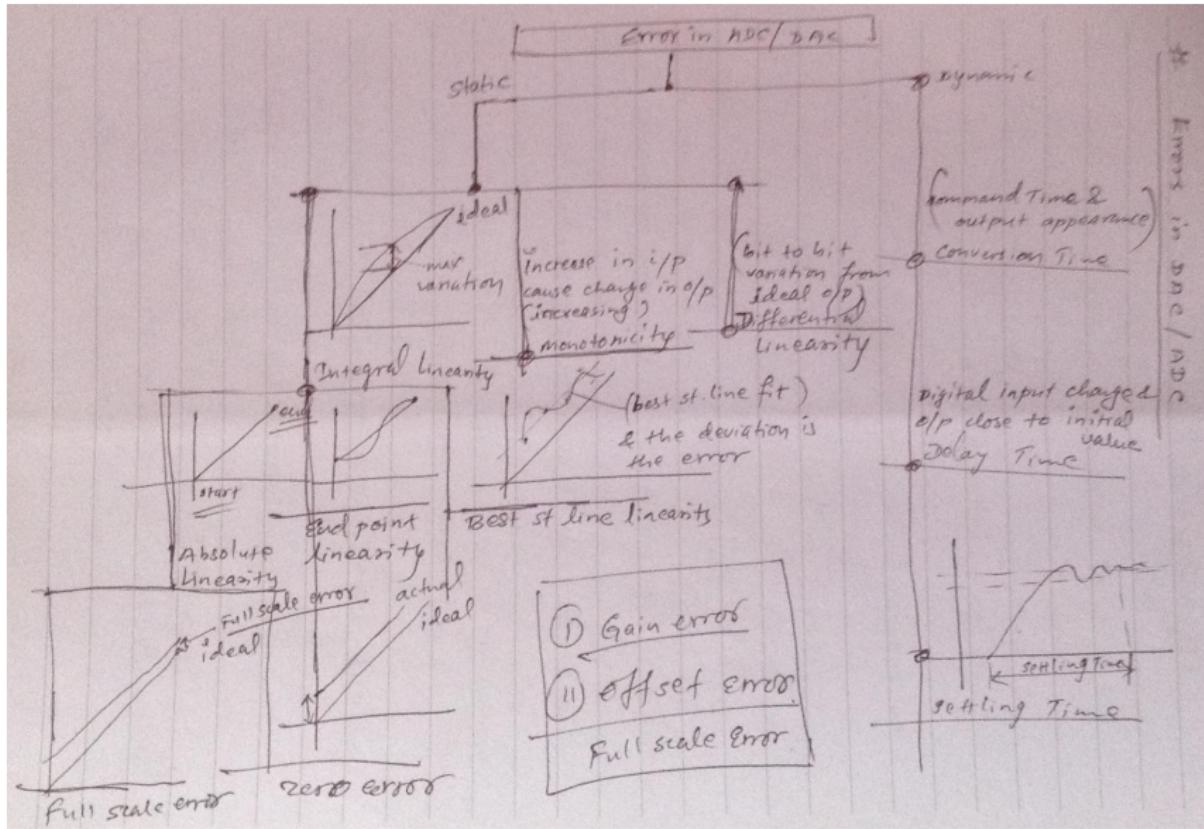


**Fig. 28** Timing Diagram for 12bit Digital to analog conversion

# Selection Criteria based on Design Requirements

- ① Resolution
- ② Linearity
- ③ DAC settling time
- ④ ADC conversion time
- ⑤ Accuracy
- ⑥ Codes used
- ⑦ Cost

# Errors in ADC and DAC ⇐ Self-Study



# As you go Assignment

Assignment Module#4 is available at MS-Team.

Deadline for submission: 13th June 2024 (*Before 3:00 PM*)