Kathmandu Engineering College
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Lab Report on
Instrumentation II

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Introducing 8255 PPI with 8085 (mode 0)

Objective

* To configure 8255 PPI in mode 0 and observe it's application.

Theory

PPI 8255 is general purpose programmable I/O interfacing device. It has 24 pins categorized as groups of 8 pins namely Port A, Port B and Port C. Port C can be further grouped as C upper and C lower but also, it can be used as an individual pin.

The functions of these ports are efined with control word in control register.

8255 can function in two different modes
1) Bit Set/Reset mode (BSR mode)
2) I/O mode

Mode 0 (basic I/O)
There is a simple I/O configuration for all ports (A, B, C) There is no handshaking in this mode. The outputs are latched but inputs are not. It consists of two 8 bit-ports, A and B and two 4 bit Ports, C-upper and C-lower. Any of these ports can be configured as input or output.

Q1) Configure 8255A as Port A in mode 0 as output, and Port B in mode 0 as input.

Mnemonics	Op Code	Address
MVI A, 82H	3EH	8000H
	82H	8001H
OUT 83H	D3H	8002H
	83H	8003H
IN 81H	DBH	8004H
	81H	8005H
OUT 80H	D3H	8006H
	80H	8007H
RST 5	EFH	8008H

Output
Port A : 01110111
Port B: 01110111

Discussion:

Port “A” was configured in mode 0 as an output port and port “B” as in the input port, also in mode 0. To do this, control word 82H was stored in control Register. The input provided in Port “B” was observed as output in Port “A”.

Q2) Configure 8255A as Port A mode 0, output, and Port B as mode 0 and output as well.

Mnemonics	Op Code	Address
MVI A, 80H	3EH	8000H
	80H	8001H
OUT 83H	D3H	8002H
	83H	8003H
MVI A, 07H	3EH	8004H
	D7H	8005H
OUT 81H	D3H	8006H
	82H	8007H
OUT 80H	D3H	8008H
	80H	8009H
RST 5	EFH	800AH

Output:
Port A: 11010111
Port B: 11010111

Discussion: In this D7H was providing by both part A and port B as output D7H in binary is 11010111 and from LED’s we observed the MSB and LSB of Port A and Port B.

Q3) Configure 8255 PPI as Port A (mode0, input) and Port B (mode 1, output)

Mnemonics	Op Code	Address
MVI A, 90H	3EH	8000H
	90H	8001H
OUT 83H	D3H	8002H
	83H	8003H
IN 80H	DBH	8004H
	80H	8005H

OUT 81H	D3H	8006H
	81H	8007H
STA 8FF1H	32H	8008H
	F1H	8009H
	81H	800AH
CALL 044CH	CDH	800BH
	4CH	800CH
	04H	800DH
HLT	76H	800EH

Q4) WAP to send port C pins and Port C pins associated to switched as top of the given 8155 PPI module.

Mnemonics	Op Code	Address	Output
MVI A, 90H	3EH	8000H	PC0, 01H, LED1 on
	90H	8001H	PC1, 03H, LED2 on
OUT 83H	D3H	8002H	PC2, 05H, no LED on
	83H	8003H	PC3, 07H, LED3 on
MVI A, 01H	3EH	8004H	PC4, 09H, no LED on
	01H	8005H	PC5, 0BH, LED4 on
OUT 83H	D3H	8006H	PC6, 0DH, no LED on
	83H	8007H	PC7, 0FH, LED5 on
RST5	EFH	8008H	

Discussion:

Depending upon the input provided at 8055H address for PC0, PC1, PC7 we could observe the port C pins associated to switched in PPI

Conclusion

Hence 8255A PPI was interfaced with 8085 microprocessor in Mode 0 for input and output.