Module#2 (LogBook–Contents)

submission deadline: May 25, 2024 (*Before 3:00 PM*)

1. Explain the different schemes of parallel data transfer with suitable timing diagram. Explain the functional block diagram of 8255A PPI with neat diagram. **[2074 Chaitra]**
2. List out the technical benefit of using 8255 PPI in MBI system. Explain PCI bus in brief. Explain how the base address of 8255A is changed with change in address lines of 8085 connection with 8255A? **[2073 Chiatra]**
3. With a neat timing diagram and an appropriate example, explain the operation of 8255 PPI in mode-2. You should clearly show the necessary control signals and an interfacing circuit to connect 8255 PPI to 8085 microprocessor. Also write the necessary control words to configure the 8255 in this fashion. **[2072 Chaitra]**
4. List out the control signals used by the ISA bus. Provide convincing arguments to justify the replacement of the ISA bus by the PCI bus. Calculate the bandwidth of 64 bit PCI bus operating at 66 MHz. **[2072 Kartik]**
5. Write a short note on PCI Bus. Interface a keyboard and a printer in mode-1. Port-A is designed as input for keyboard with interrupt I/O port-B is designed as output for printer with status check I/O. Draw the mapping circuit and write the control word and address map. **[2071 Chaitra]**