

a)

b) $f = 50 \text{ E}6$

$0.02 \times 50 \text{ E}6 = 1 \text{ E}6$ CLK cycles in 0.02s.

c) $1 \text{ E}6 = [1111\ 0100\ 0010\ 0100\ 0000]_{\text{BIN}}$

↑
20 bits

d) Universal Shift Register;

Can load/receive data either serially or in parallel

i.e.

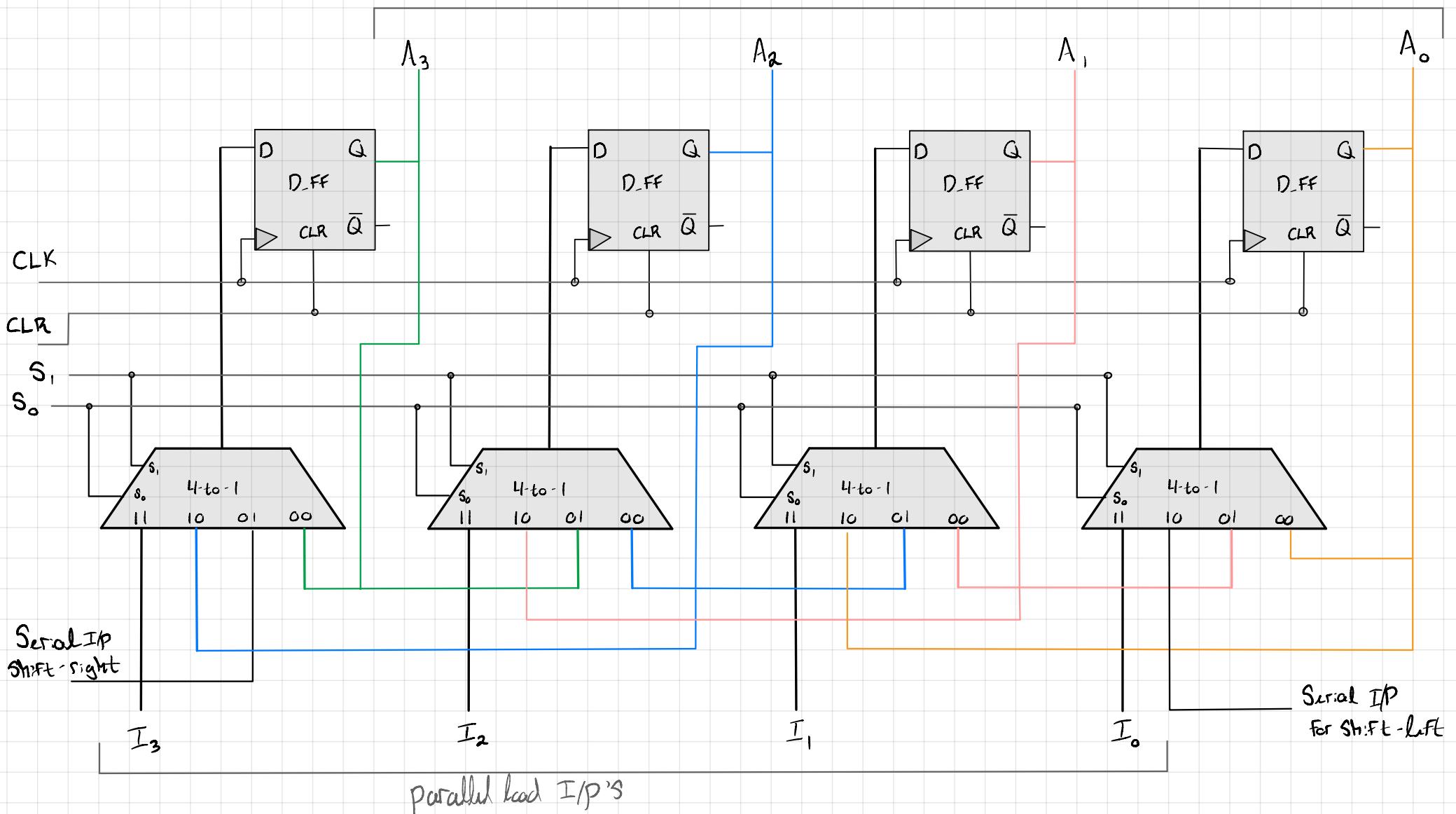
Serially : it is bidirectional (shift-left or shift-right)

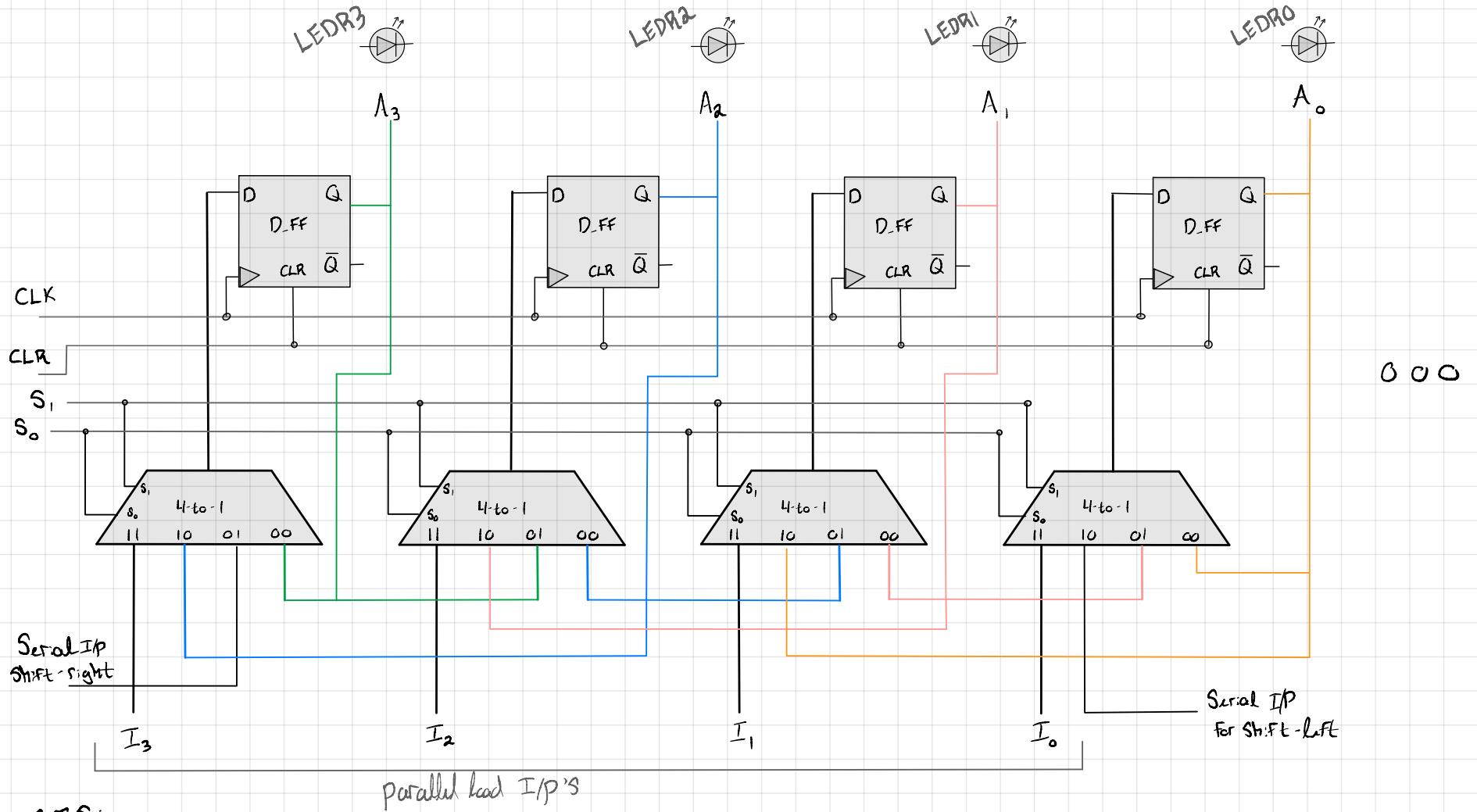
Parallel (load data into flip-flops instantaneously)

Modes:	$S_1 S_0$	Load w/	Output
SISO		→ Shift Right/Left	Shift Right/Left
SIPO		→ Shift Right/Left	data at all flip-flops
PISO		→ simultaneous load	Shift Right/Left
PIPO		→ simultaneous load	data at all flip-flops

Circuit Diagram for Univ. Shift. Reg.

Parallel Outputs





Edge cases:

For 1st MUX:

I/P '01' \Leftarrow Serial I/P
(shift-right)

For ALL MUX:

for MUX-n:

For all other MUX:

for MUX-n:

For last MUX:

I/P '11' \Leftarrow Parallel load I_n

I/P '10' \Leftarrow Serial I/P
(shift-left)

I/P '00' \Leftarrow Q_n

I/P '10' \Leftarrow Q_{n+1}

I/P '01' \Leftarrow Q_{n-1}

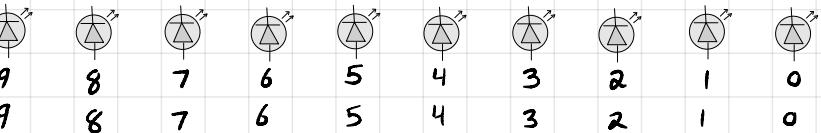
FPGA board DE1-SoC has 10 LED's

For sweeping LED effect we'll need 3 states

S0: LOAD

S1: Shift-right

S2: Shift-left



- Need a way to control Shift right or left

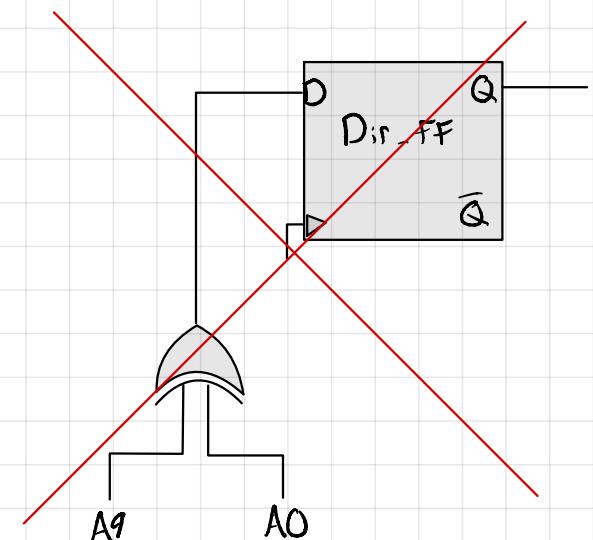
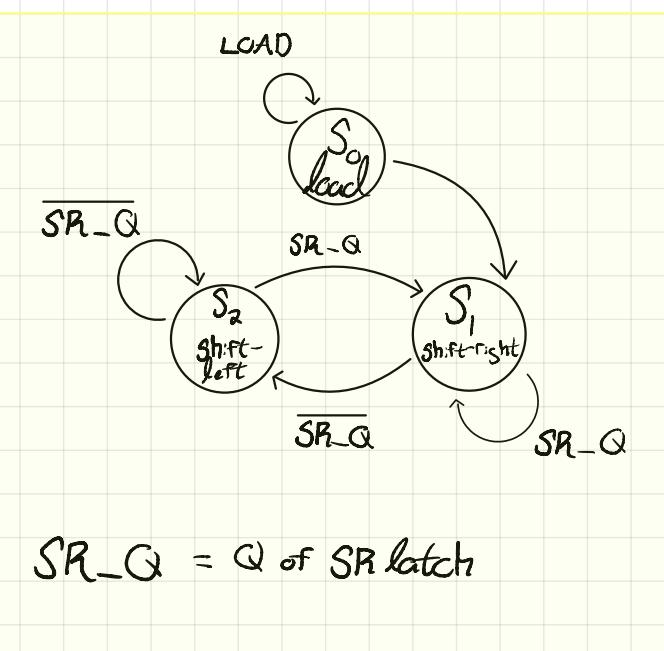
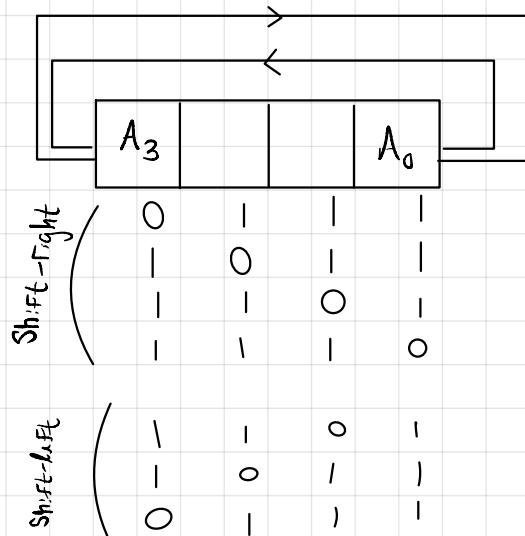
use FF to store direction of shift

↳ FF should only change when LED9 or LED0 get '0' (active low)

~~Let this FF be 'Dir-FF', where: if $Q = \text{Shift-right} \rightarrow \bar{Q} = \text{Shift-left}$~~

$$\text{i.e. } D = A_9 \oplus A_0$$

~~we'll assume initial condition is $A_9 = 0$, thus Shift-right.~~



KITT design (rework)

S_1, S_0
MD (mode)

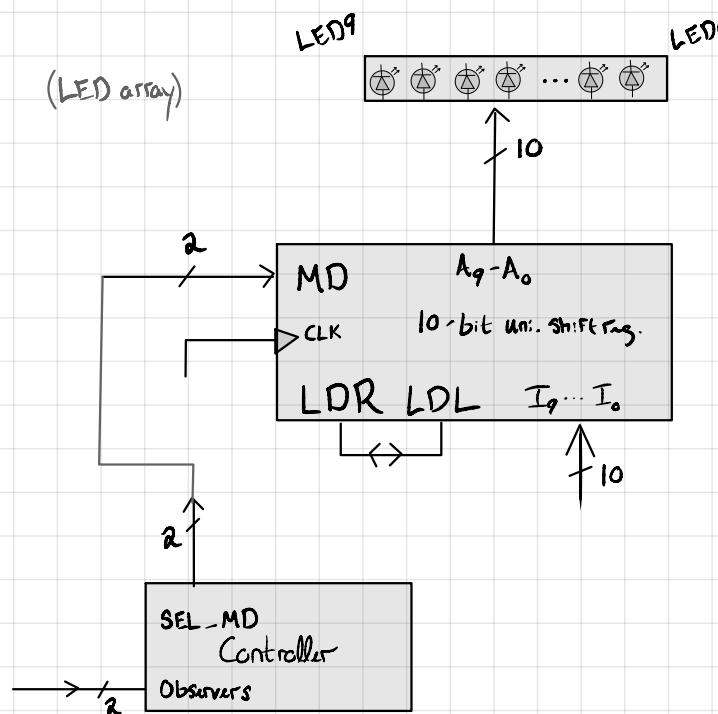
- 0 0 Hold
- 0 1 Shift-right
- 1 0 Shift-left
- 1 1 Parallel load

LDR Load bit (right-shift)

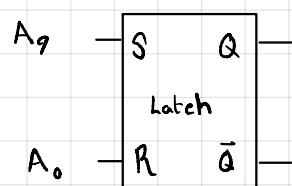
LDL Load bit (left-shift)

$I_9 - I_0$ Inputs (Parallel)

$A_9 - A_0$ Outputs

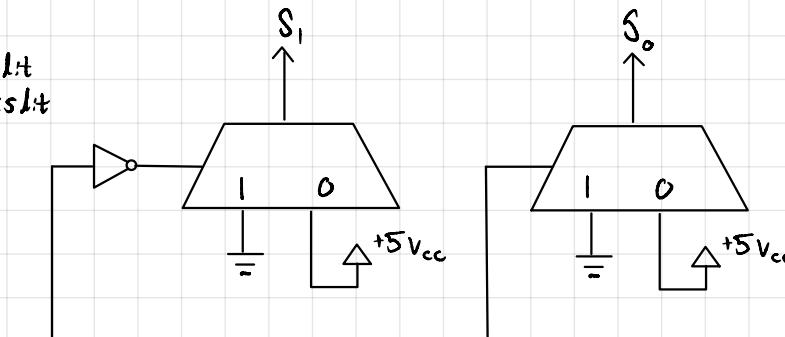


Controller



$S = 1$ indicates Left-most LED is lit
 $R = 1$ indicates Right-most LED is lit

when $Q = 1 \rightarrow$ Shift Right
when $Q = 0 \rightarrow$ Shift Left



Characteristic table

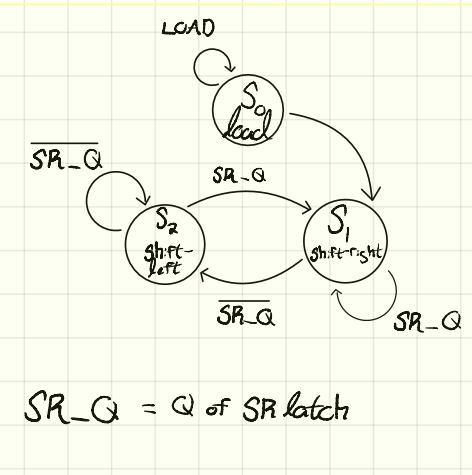
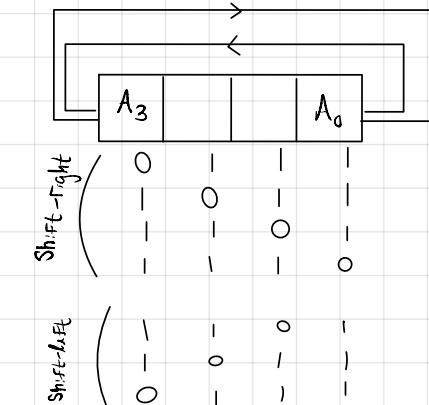
S	R	Q_{out}	Comment
0	0	0	Hold
0	1	0	Reset
1	0	1	Set
1	1	X	Metastable

Excitation table

S	R	Q_{out}	Q_{out}
0	0	0	0
0	1	0	1
1	0	1	0
1	1	X	0

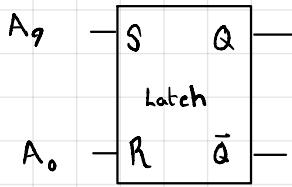
For Controller:

S	R	Q	S_1	S_0
0	0	0	1	0
0	1	0	1	0
1	0	1	0	1



$$SR-Q = Q \text{ of SR latch}$$

Controller



$S = 1$ indicates Left-most LED is lit
 $R = 1$ indicates Right-most LED is lit
 when $Q = 1 \rightarrow$ Shift right
 when $Q = 0 \rightarrow$ Shift left

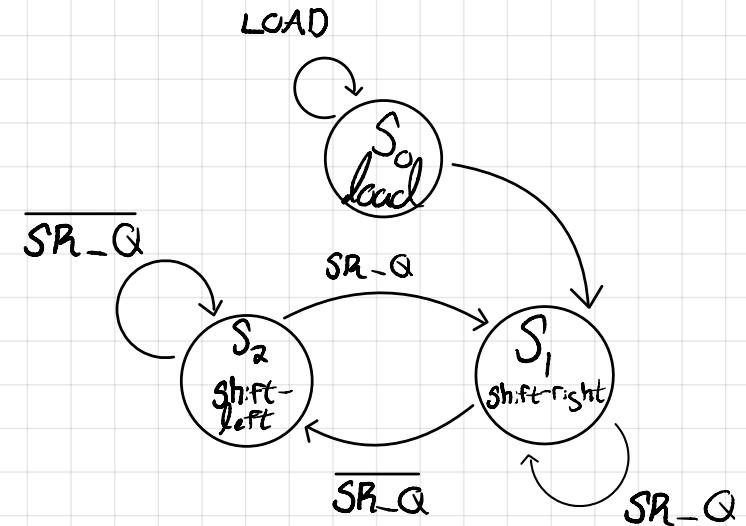
Characteristic table

S	R	Q_{next}	Comment	S	R	Q_{next}	Comment
0	0	0	Hold	0	0	0	X
0	1	0	Pulse	0	1	1	0
1	0	1	Sat	1	0	0	1
1	1	X	Metastable	1	1	X	0

Excitation table

For Controller:

S	R	Q	S_1	S_0
0	0	0	1	0
0	1	0	0	1
1	0	1	1	0



$SR_Q = Q$ of SR latch

(Parallel load)

LOAD corresponds to $S, S_0 = 11$

this occurs when A_9 through A_0 are all logic low (i.e. no LEDs are lit)

