Faculty of Engineering and Applied Science
Department of Electrical and Computer Engineering
ECE 5500 – Digital Systems

Instructions

1. Full participation in all labs in the course is compulsory for all students. Failure to participate in all labs and complete all laboratory tasks will result in an INCOMPLETE grade.

2. TA will be available from 09:00 AM to 12:00 noon via D2L Online room on each scheduled lab dates.

3. Student are required to attend these online support rooms and get assistance from TAs to complete their labs. TAs and course instructor will NOT answer lab-related questions outside the specified time slots (09:00 am - 12:00 noon)

4. Labs include prelabs which are to be completed prior to the lab session. Each student must complete their own prelab individually and attached it with the lab report.

5. Each experiment will be undertaken in groups of 2 students. Only one report per experiment is expected from each group but both students are required to contribute equally to every report and lab activities.

6. Lab submission must contain prelabs of both students, lab report, a set of lab demo videos, and a compressed project folder which include all VHDL codes and simulation testbenches. If project folder is not included, or the submitted files are not running, then the submission will not be graded, and the student group will receive zero grade. Additionally, if lab demo videos are not provided, the lab group will receive zero points for lab demonstration component.

7. Submit above components to the corresponding assignment submission folder in D2L. Submitting to a wrong submission folder or submitting in any other way (e-mailed) will be discarded.

8. It is required to create a single PDF file, including lab report and prelabs of both students before submitting to the D2L assignment submission folder.

9. Lab reports and simulation folders submission are due at 8:00 AM on the subsequent lab date, which includes the time for scanning and creating digital file of any hardcopy reports. No extra time is allowed for converting reports, or prelabs into digital format.

10. Late submission is penalized by 1% per each 15 minutes, i.e., if a lab submission is late for one day, it will be penalized by 96%.

11. The lab report must include a cover page identical to the sample cover page shown in the next page.

12. Lab report without “Declaration of Academic Honesty” followed by student signature will not be graded and the student group will receive zero grade.

ECE 5500 – Digital Systems

Experiment #: .....
Declaration of Academic Honesty

Academic honesty or academic integrity is a very important virtue that all students should always uphold.

We declare that this lab submission is our own work, is not copied from any other person's work (published or unpublished) and has not assisted by others. And also, we confirm that we have read and understood the

Faculty of Engineering and Applied Science Student Code of Conduct (`http://www.mun.ca/engineering/undergrad/academicintegrity.php`),

Memorial University's Code of Student Conduct (`https://www.mun.ca/regoff/calendar/sectionNo=GENINFO-2504`), and

Memorial University's Regulations of Academic Misconduct (`https://www.mun.ca/regoff/calendar/sectionNo=REGS-0748`).

We understand that issuing a false declaration can result in severe penalties and we are willing to be penalized if any form of academic misconduct found valid.

	Student 1	Student 2
Name		
Student ID#		
Signature		
Date		

1 Introduction

In this lab we will be implementing a cool LED light display that uses the red LEDs on the DE1-SoC board to generate a pattern that sweeps back and forth. (Think the robotic Cylons from *Battlestar Galactica*, or the front of K.I.T.T. if anyone remembers *Knight Rider*.)

To accomplish this, we must now start considering time—i.e. sequential design.

2 Prelab

Read the rest of the lab description and then answer the following questions and complete the listed tasks for the prelab:

(a) What signals do we need to add to the top-level VHDL file to interface with the new features we are using?

(b) If we use a clock of 50 MHz, how many clock cycles make up a delay of 0.02 seconds?

(c) What is the smallest number of bits a counter would need to be able to count to the amount above in part (b)?

(d) Describe what a universal shift register does and list its different modes of operation.

(e) Draw a circuit diagram showing your top level design and how you plan to put the components together. You can use a black box to represent any state machines/control logic.

(f) Provide a complete state diagram of your design and explain its functionality (operation).

3 Demo Display

You must design a sequential circuit running off the DE1-SoC's 50 MHz clock that oscillates a single illuminated red LED back and forth across all 10 red LEDs on the board at a rate of 50 shifts per second (i.e. every 0.02 seconds). When the illuminated LED reaches the end of the row, it changes direction and starts shifting back the other way.

Your design will likely require:

- a 10-bit universal shift register,
- one or more counters,
- a state machine for control.

Because I have asked for a specific rate of shift, you cannot just shift the LED on every clock cycle—a clock running at 50 MHz would oscillate the LED too fast for the human eye to detect, and it would just look like they were all constantly on. Thus, your design should be based around a counter that runs off the 50 MHz clock and counts the necessary number of cycles to reach 0.02 seconds. The output of the counter can be used to generate control signals for the shift register and state machine different modes.

You will need to add the signal `CLOCK_50` and the `KEY(3 downto 0)` vector as inputs to your top-level VHDL file so that the DE1-SoC pin assignments will work correctly. You should also use KEY(0) (one of the DE1-SoC's four pushbuttons) as an asynchronous active-low reset for the entire system, which resets the LEDs so that LEDR(0) is the one that is lit. Apart from the asynchronous reset, you may also need a synchronous clear for the counter.

For the state machine, you are free to use either a Moore or Mealy machine as you see fit. Your state machine must respond to the reset signal, hold values in the shift register when appropriate, and shift them left or right at the appropriate times.

3.1 Simulation

Simulation of this design will be tricky since we are dealing with longer time scales—shifting every 0.02 seconds means we must simulate 1 million clock cycles before we see anything happen in the output!

As such, I strongly recommend:

1. Simulating any component parts first to ensure they are working correctly.
2. During simulation, using a much lower count in your VHDL for the counter. (For example, instead of shifting every 1 million clock cycles, shift every 5 clock cycles.) When you are convinced the design works, change the VHDL code back to the original "real-time" counts before synthesis.

4 Deliverables

Your lab submission must include three main components (three files):

- Lab report: This is a single pdf file that include pre-lab, simulation results and all VHDL codes. All following items must be presented on the lab report
  - Pre-lab:
    - Answer all the questions in section 2.
    - Provide all circuit diagrams, state machine diagrams, and design notes.
  - Simulation results:
    - Provide simulation waveform results showing the correct operation of your design. Be sure to modify the counters to use shortened timescales for simulation.

  - Provide the VHDL code for your testbench, top-level design, and all components.

- Lab demo videos: Record and submit a video showing all the functionalities of the demo display.

- A compressed (.zip) folder that contains your entire project.

Therefore, your final submission contains three files, a pdf file, a video file, and a compressed folder.

Reference

This lab manual extracted from the Lab-4 of the former ENGI 5865, designed by Dr. Andrew House.