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Van Wickle Wafers Lab Report

Introduction

Van Wickle Wafers is a company created out of ENGN 1590, comprised of 5 students at Brown University. Over the 2025 spring semester, our company worked to create working diodes meeting the specifications of Professor Zaslavsky. The fabrication process involved hands-on manufacturing in the Engineering Research Center's clean room with steps ranging from photolithography, etching, dopant diffusion, and electronic testing.

The goal was to create market-ready diodes with the following specifications: a current rectification ratio of at least 10^3 at V = ± 1.2 Volts and a forward bias of at least 1mA at 1.2 Volts. To achieve this, our team designed various diode geometries using KLayout and implemented a junction-isolated fabrication method using a pre-coated p-type silicon wafer. During the fabrication process, Van Wickle Wafers followed the standard semiconductor and clean room protocols while aiming to optimize each fabrication step to minimize defects and ensure reliable performance.

In the following report, we detail the fabrication steps, test results, and the economic analysis of our diode production, showing that our diodes not only achieved, but exceeded the required performance targets.

Fabrication Procedure

To fabricate working diodes, the Van Wickle Wafers Company created junction-isolated diodes on a p-doped substrate, driving in a Phosphorus dopant to create the n-doped layer. The general procedure is as follows and will be described in more detail in the subsequent paragraphs. In the first lab session, we spun on photoresist, used lithography to expose the SiO_2 to be etched, and then etched through the SiO_2 with hydrofluoric acid (HF). In the second lab session, we spun on the Phosphorus dopant, annealed the wafer to drive in the dopant, and removed the dopant with hydrofluoric acid. In the third and final fabrication session, we spun on

more photoresist, lithographically defined metal contacts, and applied metal. Then, we removed the metal not on top of the diodes using hydrofluoric acid.

The production began with a pre-coated 2" p-Si wafer (1-10 Ωcm) with 1 μm wet SiO_2 deposited from the factory, chosen based on the pre-coating's convenience. To proceed, the wafer was cleaned using a Trichloroethylene solution, Acetone, Methanol, and DI water for 5 minutes each, and dried with N_2 gas. The next step was to apply photoresist (AZ 5214e) at 4000 RPM, which coated the wafer and was immediately cooked on a hot plate for 2 minutes. Note that the hot plate should've been preheated to 113 Celsius.

Next, lithography was developed using the maskless aligner, which utilizes UV radiation to dissolve the photoresist and clear patterns on the wafer. Using KLayout, hundreds of diodes were developed from 400, 600, 800, and 1000 micrometers. The layout is a three-layer setup composed of a wafer, oxide, and metal. In addition to the normal diodes, we added some testing mechanisms to diagnose the root of any issue with our diodes if they weren't up to spec. Metal was added to some diodes on two opposite sides of the n-doped region. The purpose of this was to allow us to test the resistivity of this region and thus determine the doping of the supposedly n-doped region. Luckily, these were not needed. The design is shown in Figure 1. Loading the wafer into the maskless aligner requires a calibration process, and then our pattern was uploaded and exposed to the wafer. We were mindful not to look into the device without wearing protective eye equipment.

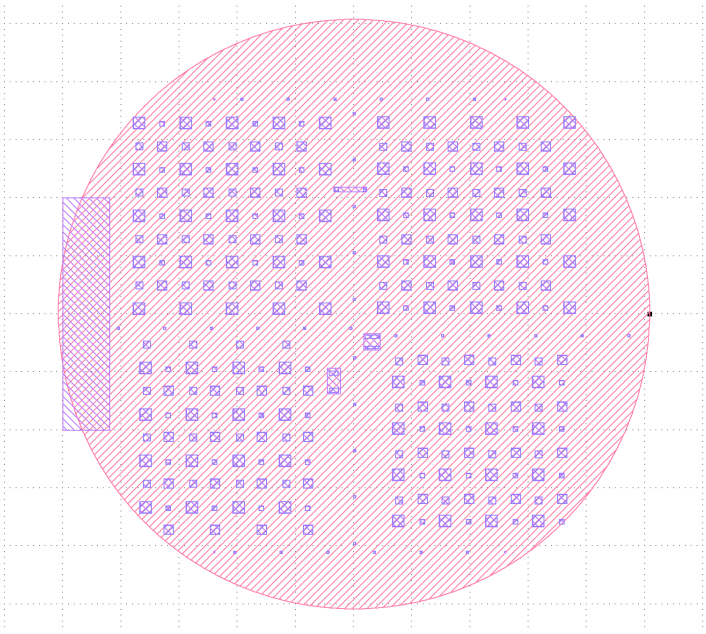

Figure 1: KLayout Diode Patterns for Lithography

After the maskless aligner finalized the lithography, we removed the excess SiO_2 using hydrofluoric acid. For this, we wore the appropriate equipment to pour a couple of mL of acid in a beaker, which means wearing an additional layer of body protection, gloves, and a face mask.

The wafer was placed into a holder, dipped completely into the acid, and swirled around constantly. The etching process took around 20 minutes in the acid and was checked every few minutes. Visually, there's a noticeable distinction in the wafer's light reflection, which should allow the squares to reflect light while the rest obtains a different tone. We cleaned the wafer by pouring deionized (DI) water into it and drying it with the N_2 gun so there are no water droplets on either side of the wafer. We removed the acid by pouring it into a hazardous chemicals container for disposal, and cleaned the lab equipment with DI water. Finally, utilizing Acetone and Isopropyl alcohol, the photoresist was removed. This leaves a wafer where the areas intended to be diodes are exposed, such that the dopant can be driven in and the rest of the wafer is still covered in SiO_2. This can be seen clearly in the Dektak measurement of one of the areas where the SiO_2 was etched through in Figure 2.

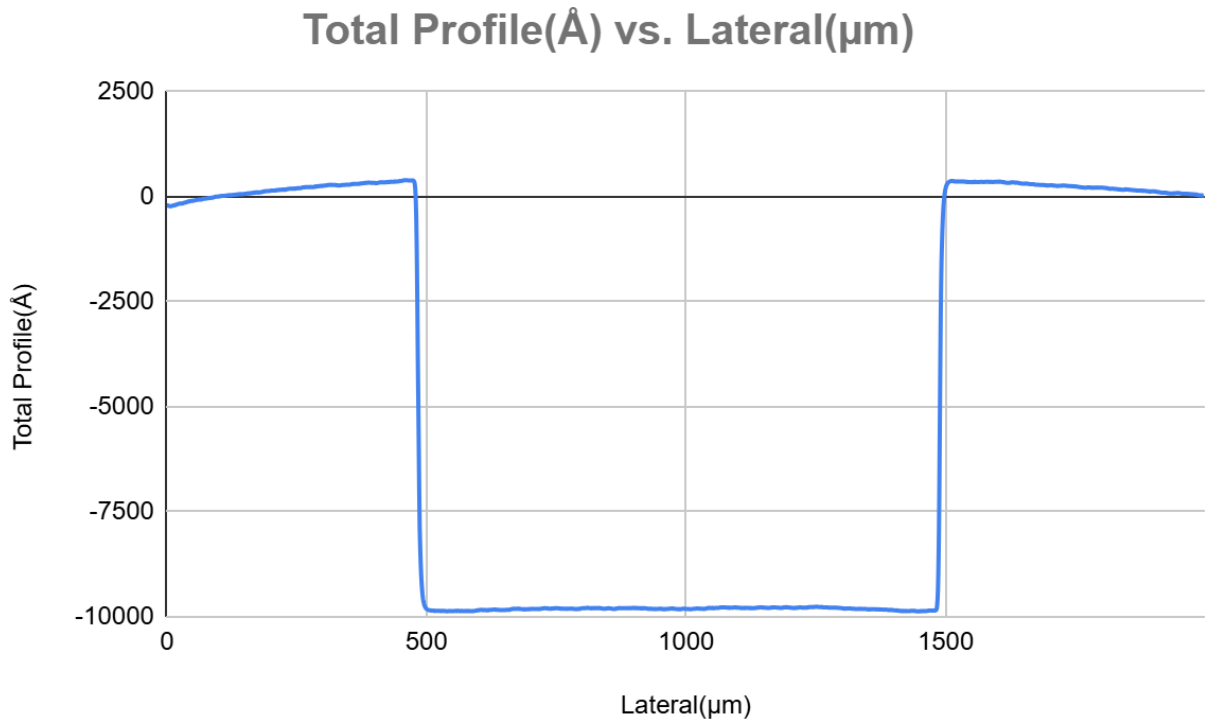

Figure 2: Dektak Measurement of successful SiO_2 etching

The following step was to use an n-type Spin on Dopant (SOD), in this case PDC5-2500, a phosphorus dopant. The spinner was set to 3000 RPM, and afterwards the wafer was baked for 120 seconds at 113° Celsius. We were careful not to contaminate the back of the wafer, as that could result in an undesired pn junction. The wafer was annealed for 100 minutes in the furnace to drive in the dopant. The wafer was loaded into a boat, placed into the elephant, and then pushed 30 inches into the tube for it to cook. After the annealing process was finalized, the boat was unloaded into the Teflon base and left to cool for 15 minutes. Finally, to remove the residual SOD on the wafer, HF was used in the same manner as before to remove what was left of the

SOD. It was harder to tell when the SOD had been removed than for the photoresist because the color change was less pronounced. Thus, we probably spent more time submerging the wafers in HF than was necessary. Nonetheless, this had no negative impact on our diodes.

Similarly to how the first photoresistor layer was added, another photoresist layer was added. Lithography was used again and in the same way, except this time we used the patterning for the metal contacts we designed. Afterwards, a metal layer was added through lift-off metallization, where a metal (in this case, Titanium and Aluminum) is evaporated and then adhered to the wafer. For this, a high-pressure vacuum is created by pumping out air and opening the main gate for the metal to be deposited. After 50 armstrong of Ti had been added, we also added 700-1000 armstrong of Al. The wafer was then removed carefully by retracting it from the main chamber after removing the vacuum. There was still some metal on top of the photoresist, so we proceeded to remove it through the same method of etching with HF, eventually removing both the photoresist and metal from the undesired parts of the wafer. Finally, we RCA cleaned and dried the wafer.

To test the diode's performance, an indium back contact was added to the other side of the wafer contact. Testing of our diodes was then done using a semiconductor parameter analyzer. This measuring process is highly accurate due to the minute dimensions of the diodes and the precision of the semiconductor parameter analyzer.

Fabrication Step Results

Overall, and perhaps unexpectedly, fabrication went flawlessly. The Dektak measurements in Figure 2 show that the etching went through exactly 1 micrometer of the SiO_2, which was exactly what we needed. The measurement also indicates that the etching was exactly 1000 micrometers, which we wanted for the 1mm square diodes. The biggest mistake when fabricating the diodes was simply dropping the wafer. However, the wafer was never dropped from a height of more than several inches, and there were never any noticeable or measured defects on the wafer.

Analysis of Electronic Measurements

To characterize the performance of our diodes, we measured I-V curves for one diode of each size from each of the four quadrants of our wafer, sweeping -5 to 1.2V. We also took extra measurements for each quadrant's smallest and largest sizes. Firstly, the turn-on voltage V_T is ~ 0.4V across all diodes. Next, we calculated the ideality factors *n* for each diode by extracting the slope of the logarithmic I-V curve in its linear region. This result comes from the diode current equation:

$$I = I_s e^{\frac{qV}{nkT}} \Rightarrow ln(I) = ln(I_s) + \frac{qV}{nkT}$$

Where we can see that the slope *m* of the linear region of the log plot will be:

$$m = \frac{q}{nkT}$$

Which rearranging for *n* gives:

$$n = \frac{q}{mkT}$$

A summary of current rectification ratios at +/- 1.2V, current values under a forward bias of 1.2V, and ideality factors is shown in Table 1 below. Note for the diode sizes, where two measures were taken, only the better of the two is shown.

Table 1: Summary of current rectification ratios at +/- 1.2V, current values under a forward bias of 1.2V, and ideality factors in each quadrant of the wafer

	Bottom-Left			**Top-Left**			**Bottom-Right**			**Top-Right**		
Size (um)	I_F / I_R	I_F *(mA)*	*n*	I_F / I_R	I_F *(mA)*	*n*	I_F / I_R	I_F *(mA)*	*n*	I_F / I_R	I_F *(mA)*	*n*
400	10^4	3.09	1.37	10^4	6.53	1.30	10^4	4.80	1.30	10^4	2.24	1.39
600	10^3	3.37	1.47	10^4	6.96	1.36	10^4	4.72	1.36	10^3	2.11	1.54
800	10^3	3.55	1.57	10^4	7.86	1.42	10^4	5.18	1.40	10^3	2.28	1.64
1000	10^3	3.62	1.67	10^4	8.28	1.48	10^6	5.22	1.40	10^3	2.38	1.76

Thankfully, *all* our diodes met specifications, that is, achieved a rectification ratio of at least 10^3 at +/- 1.2V (10/16 achieved at least 10^4!) and forward bias current of at least 1 mA at 1.2V, with our best ratio being 10^6 and current 8.28 mA, for two separate diodes highlighted in red in Table 1. Thus our yield is 100%. Overall, forward bias currents varied from around 2-7 mA for each size across the four quadrants, so the measures of the bottom right quadrant, which were at about the medians for each size, are presented in Figures 3, 4, and 5 as representative data samples. In the log plot, there is a flat curve leading up to close to V_T, after which it enters the exponential range and we see a sloped line. Then, the curve eventually starts to bend downward as series resistance starts to have a greater effect. In the linear plot, we see the near zero current leading up to the turn-on voltage, after which we see the exponential rise in current with increasing voltage. Ideality factors increased with increasing size by fairly consistent amounts over each quadrant. For example, in the bottom left we see an increase from 1.37 to 1.67 in 0.1 step increments, and a similar pattern is shown in the top left where we go from 1.3 to 1.48 in 0.06 step increments. The bottom right was the best performer in maintaining a constant ideality factor across sizes, which is nicely shown in Figure 4 through the nearly constant slope across the sizes. This is expected since size should shift curves up or down on a log scale, nothing more (ideality factors should remain the same). Then, if we zoom into the linear region at 0.4V, as shown in Figure 4, we see that current is scaling linearly with area, as it should be. Expected current ratios, along with measured ratios, are summarized in Table 2 below.

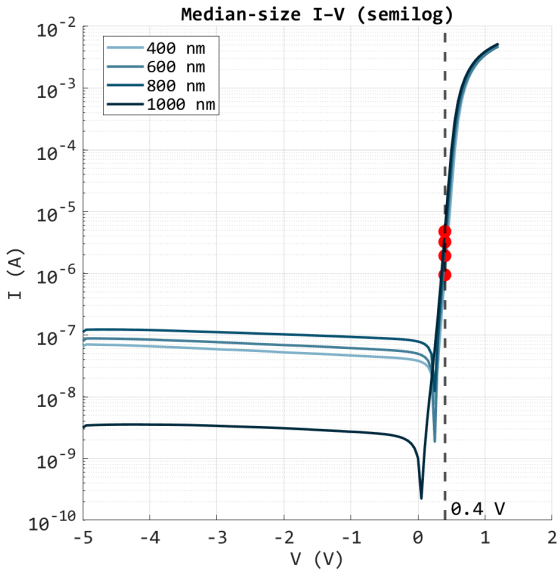

Figure 3: Log plot of I-V curves for the bottom-right quadrant, one of each size

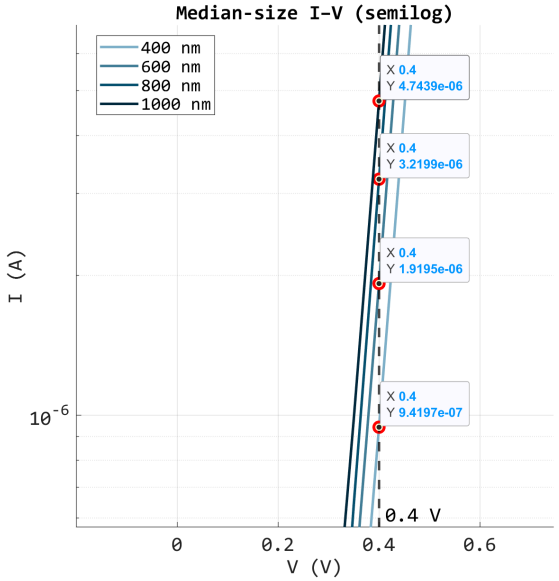

Figure 4: Zoomed-in region of log plot, showing current values at 0.4V for each size

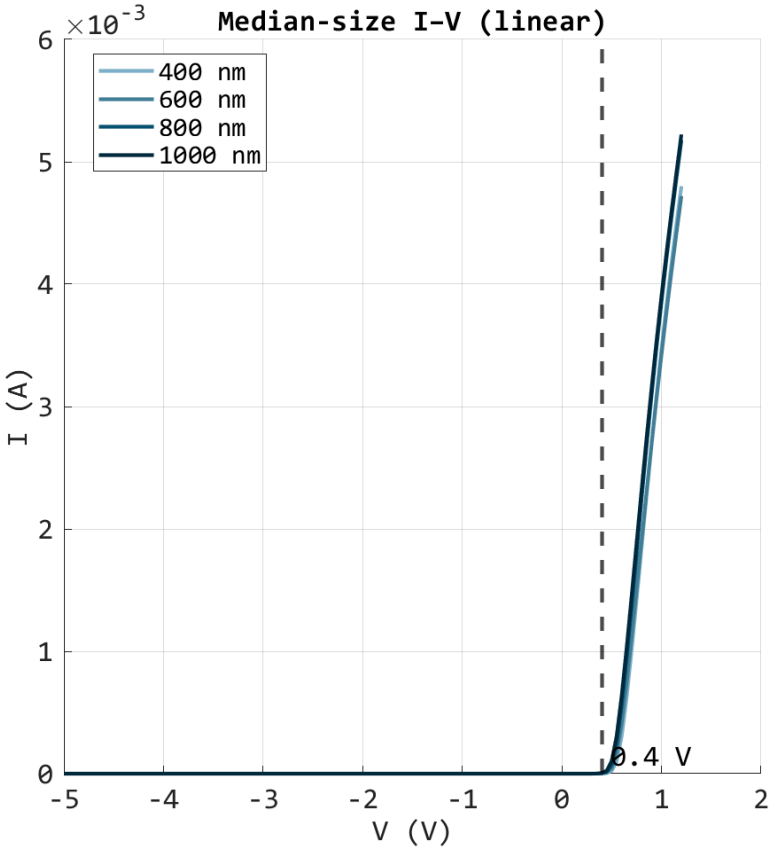

Figure 5: Linear plot of I-V curves for the bottom-right quadrant, one of each size

Table 2: Summary of current ratios

Ratio	Expected	Measured
I(600^2) / I(400^2)	2.25	2
I(800^2) / I(400^2)	4	3.4
I(1000^2) / I(400^2)	6.25	5

Lastly, we measured the breakdown of one of the large diodes (1000 um) in the bottom-right quadrant shown in Figure 6 and found it to be about -38V. With this value, we can get an estimate for our doping using the following equation:

$$\left|V_{BR}\right| = \frac{\epsilon_s * E_{crit}^2}{2qN_d} \Rightarrow N_D = \frac{\epsilon_s E_{crit}^2}{2q\left|V_{BR}\right|}$$

With $\varepsilon_S = 11.8 * \varepsilon_0$ and E_{crit} = 1-3 x 10^5 V/cm (rough estimate found online), we get:

$$N_D = 8.6 \times 10^{14} - 7.7 \times 10^{15} cm^{-3}$$

Which is relatively light doping, suggesting vast depletion regions.

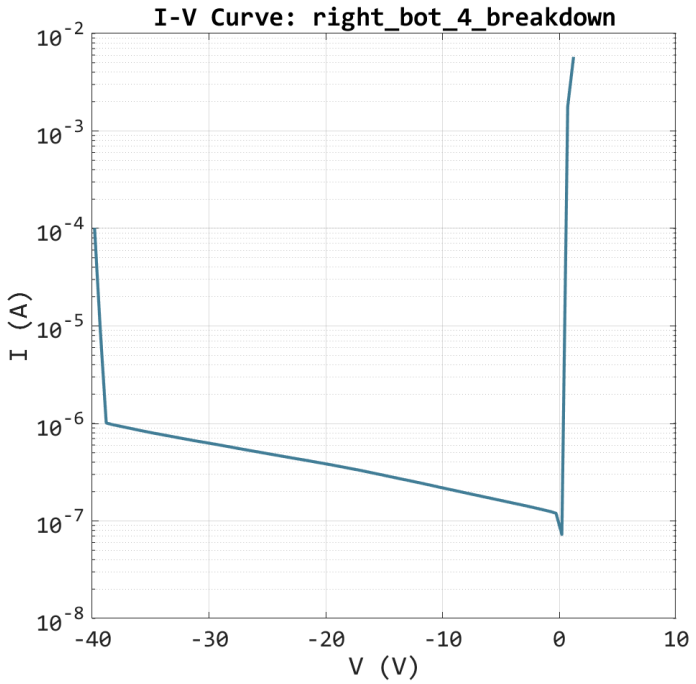

Figure 6: Plot showing breakdown of a diode of size 1000 um

Economic Analysis

The cost for each component for one wafer of diodes is shown below.

- Pre-coated Si wafer - 30$
- Cleaning wafers - $15
- Lithography - $50
- HF cleaning - $15
- Spin on Dopant - $15
- Anneal wafers - $15

The total cost is then $140. The total number of diodes Van Wickle Wafers manufactured was 324. Therefore, the cost per diode is $0.43. We set the vendor price to ~ $0.55 to $0.60 per diode. This is because the $0.43 does not account for factors such as labor and time. Additionally, yields may differ from wafer to wafer. This additional $0.12 ~0.17 gives us a buffer for potential defects and allows us to profit.

Typically, a 4148 diode on DigiKey is $0.10 per unit. Unfortunately, our cost of $0.43/ diode is not competitive. However, considering our small-scale manufacturing process, this price range is justifiable. To improve, we could repeat this process and increase the number of diodes per wafer since we still had space on our wafer that was not filled up. For example, we can make a wafer with only the smallest-sized diodes, 400 μm by 400 μm, with a 200 μm spacing in between.

The wafer area is:

$$A_{wafer} = \pi r^2 = \pi\,(25.4mm)^2 = 2027\,mm^2$$

The area of each 400 um square (including spacing):

$$A_{square} = (400um + 200\,um + 200\,um)^2 = 0.64\,mm^2$$

If the wafer were perfectly rectangular, we could fit:

$$\text{N} = \frac{A_{wafer}}{A_{square}} = 3167 \text{ squares}$$

A circle covers roughly 75 % of a square with the same diameter, and our yield is 100%, an incredibly impressive yield:

$$\text{N} = 3167\,(0.75)(1) = 2375 \text{ squares}$$

This results in a cost per diode of $0.06. If we estimate the cost to package per diode is ~ $0.10, then our total cost is $0.16, which is competitive in the market.

Discussion and Conclusion

The fabrication and electrical testing of our p-n junction diodes demonstrated successful device behavior across all measured parameters, making our devices "market-ready," as reflected by our economic analysis. Each device tested met or exceeded our rectification requirement of 10^3, with the majority reaching 10^4 and one reaching an exceptional 10^6! Our forward bias currents at 1.2V ranged from 2 to 8.3mA, comfortably surpassing the required 1mA.

A key observation of our testing was that the ideality factors increased with diode size, possibly due to enhanced series resistance or edge effects in larger structures. The bottom right quadrant of our silicon wafer consistently produced diodes with the most uniform and ideal behavior. This suggests that our wafer had spatial uniformity in doping, even though slight thermal or lithographic variations may still exist.

The measured current appeared to scale with the square root of the area of the diode, which likely reflects the influence of series resistance from the probe contact, non-uniform doping, or some contact resistance at the metal-oxide interface. This deviation from expected behavior highlights the practical limitations of small-scale fabrication environments like the clean room used in our fabrication process. Further, our measured breakdown voltage of around 38V allowed us to estimate a doping concentration of about 10^{15} cm^{-3}, consistent with expected light doping from the Phosphorus spin-on-dopant and validating the junction formation.

Overall, the project was successful in terms of the fabrication process and the measured behavior of our diodes, meeting both of the required specifications.

Dektak Measurements Spreadsheet