

# **Semiconductor Manufacturing Technology**

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## **Chapter 15**

# **Photolithography: Resist Development and Advanced Lithography**

# Objectives

After studying the material in this chapter, you will be able to:

1. Explain why and how a **post exposure bake** is done for conventional and Chemically amplified DUV resist.
2. Describe the negative and positive resist **development** process for conventional and chemically amplified DUV resist.
3. List and discuss the two **most common** resist development methods and the critical development parameters.
4. State why a **hard** bake is done after resist development.
5. Explain the benefits of a post-develop inspection.
6. List and describe the **four** different alternatives for advanced lithography, including the challenges for introducing each alternative into production.
7. Describe and give the benefit for the advanced resist process of **top surface imaging**.

# Eight Basic Steps of Photolithography

Step	Chapter Covered
1. Vapor prime	13
2. Spin coat	13
3. Soft bake	13
4. Alignment and exposure	14
<b>5. Post-exposure bake</b>	<b>15</b>
<b>6. Develop</b>	<b>15</b>
<b>7. Hard bake</b>	<b>15</b>
<b>8. Develop inspect</b>	<b>15</b>

Table 15.1

# Post Exposure Bake

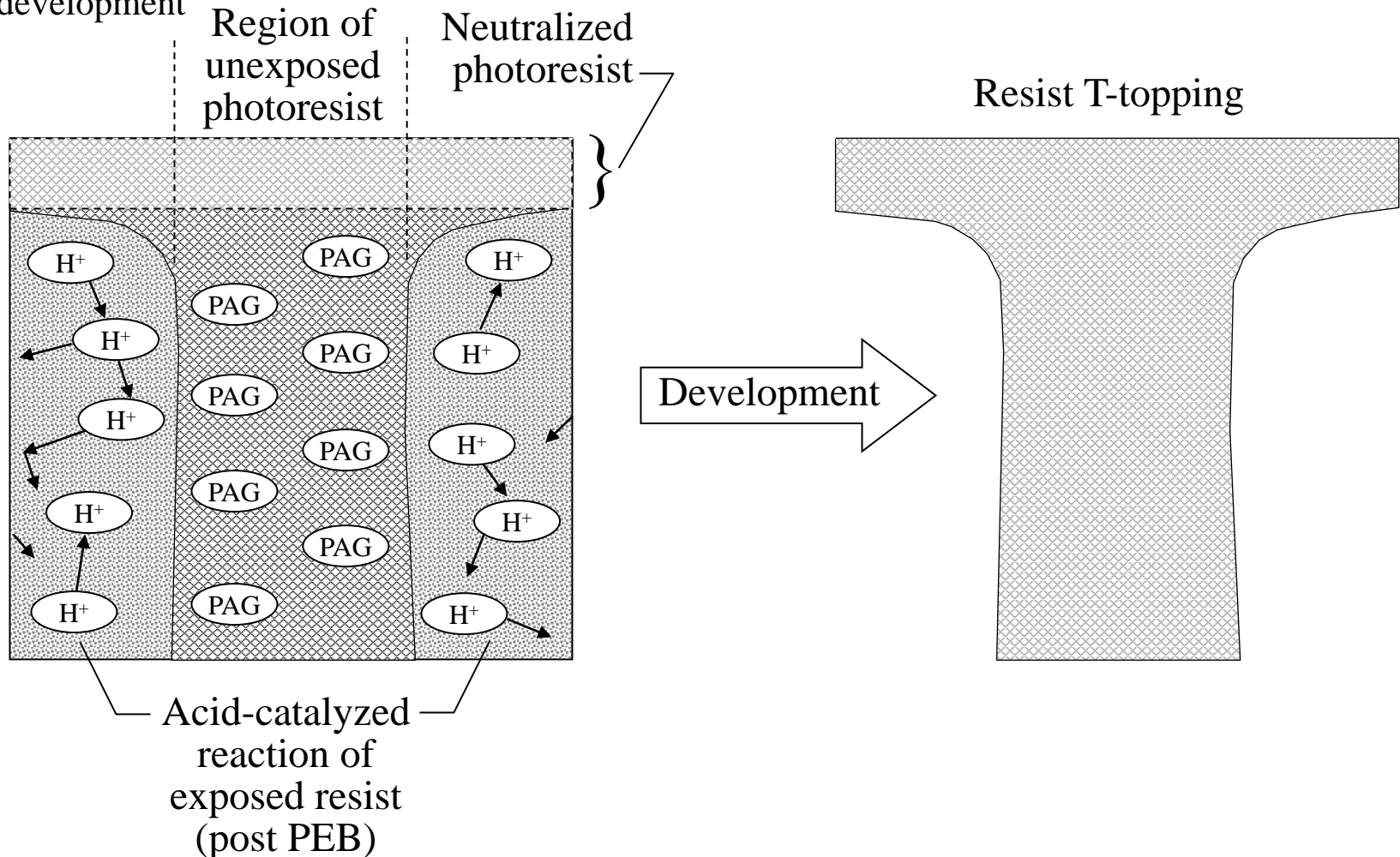
- Deep UV Exposure Bake
  - Necessary for CA DUV resists to **catalyze** chemical reactions
  - Temperature Uniformity
  - PEB Delay
- Conventional I-Line PEB
  - Improve adhesion and reducing **standing waves**

# Temperature Uniformity

- Temperature variations affect the acid catalytic reaction
- Typical PEB: 90-130°C for 1-2 min, 10-15°C hotter than soft bake
- For DUV, CD variation ~ 5 nm/°C
- To reduce CD variation, temperature controlled within 0.1°C

# Amine Contamination of DUV Resist leading to “T-top” Formation

- It is desirable to develop the resist as soon as possible after exposure to **minimize** any potential chemical reaction that can inhibit the development process (~ 30-min)
- Amine contamination from the ambient neutralize the surface to form a “**T-top**” after development



# Reduction of Standing Wave Effect due to PEB

- The increased temperature caused the PAC sensitizer to **diffuse** through the novolak polymer matrix, essentially producing an **average** effect across the standing wave boundary

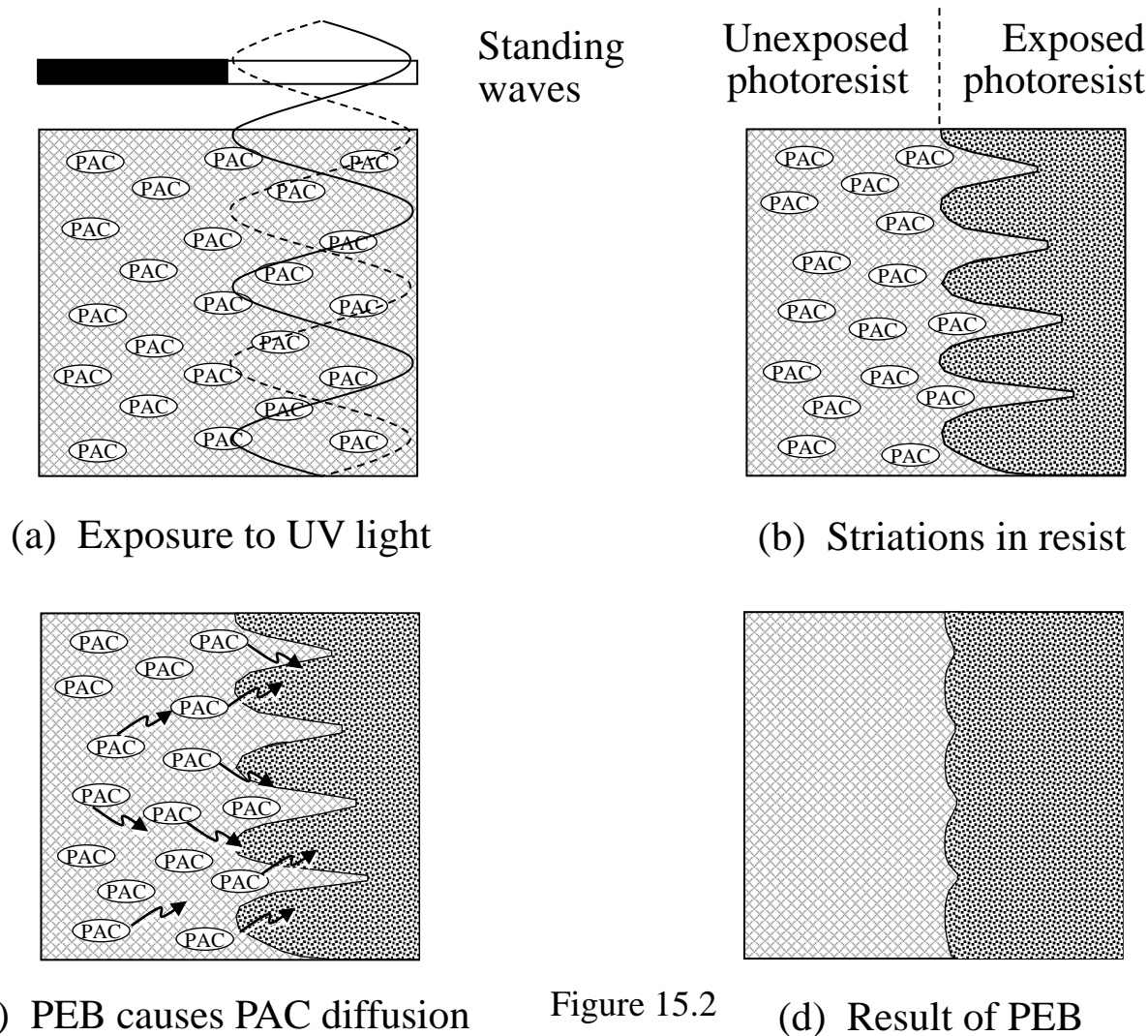


Figure 15.2

# Develop

- Negative Resist
- Positive Resist
- Development Methods
- Resist Development Parameters



# Photoresist Development Problems

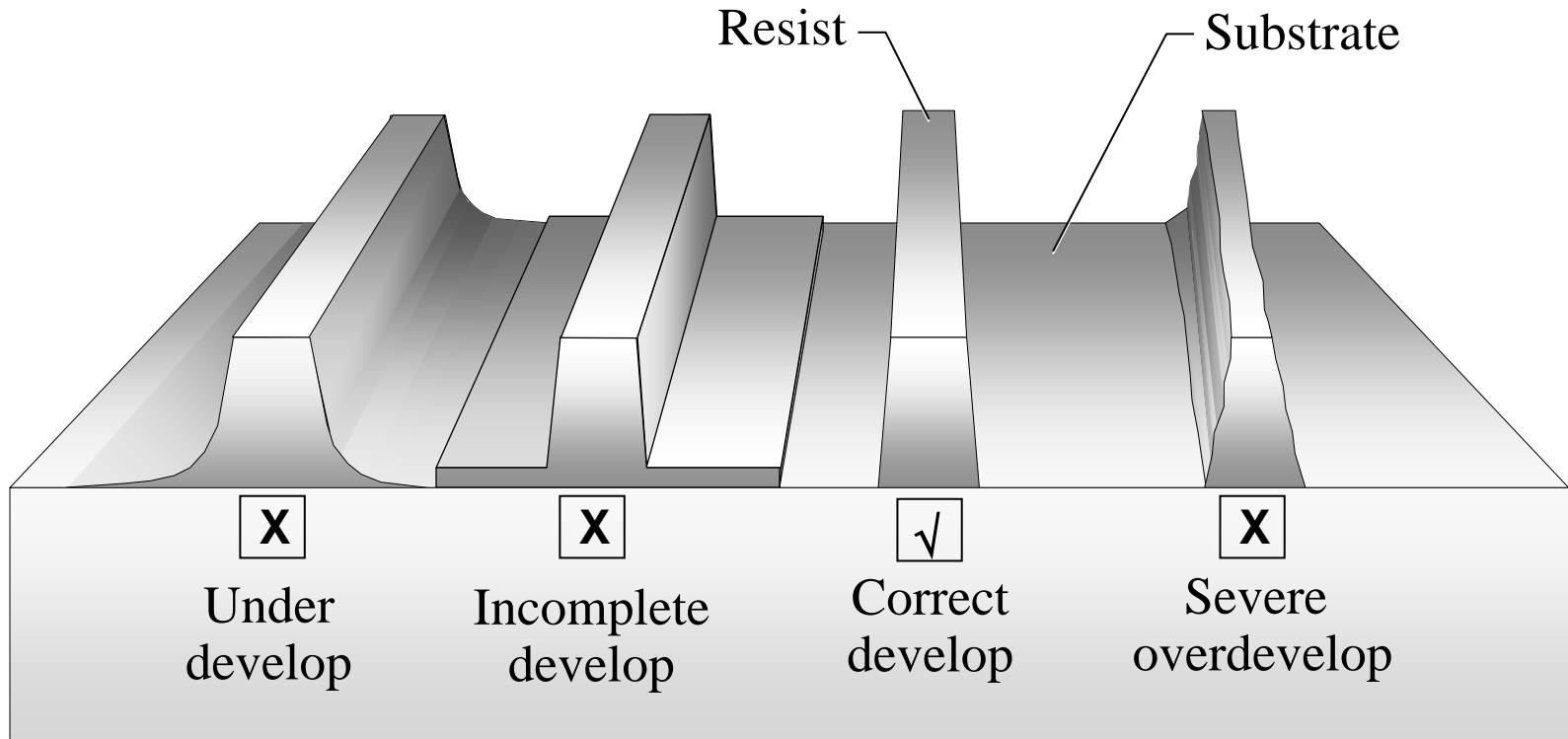
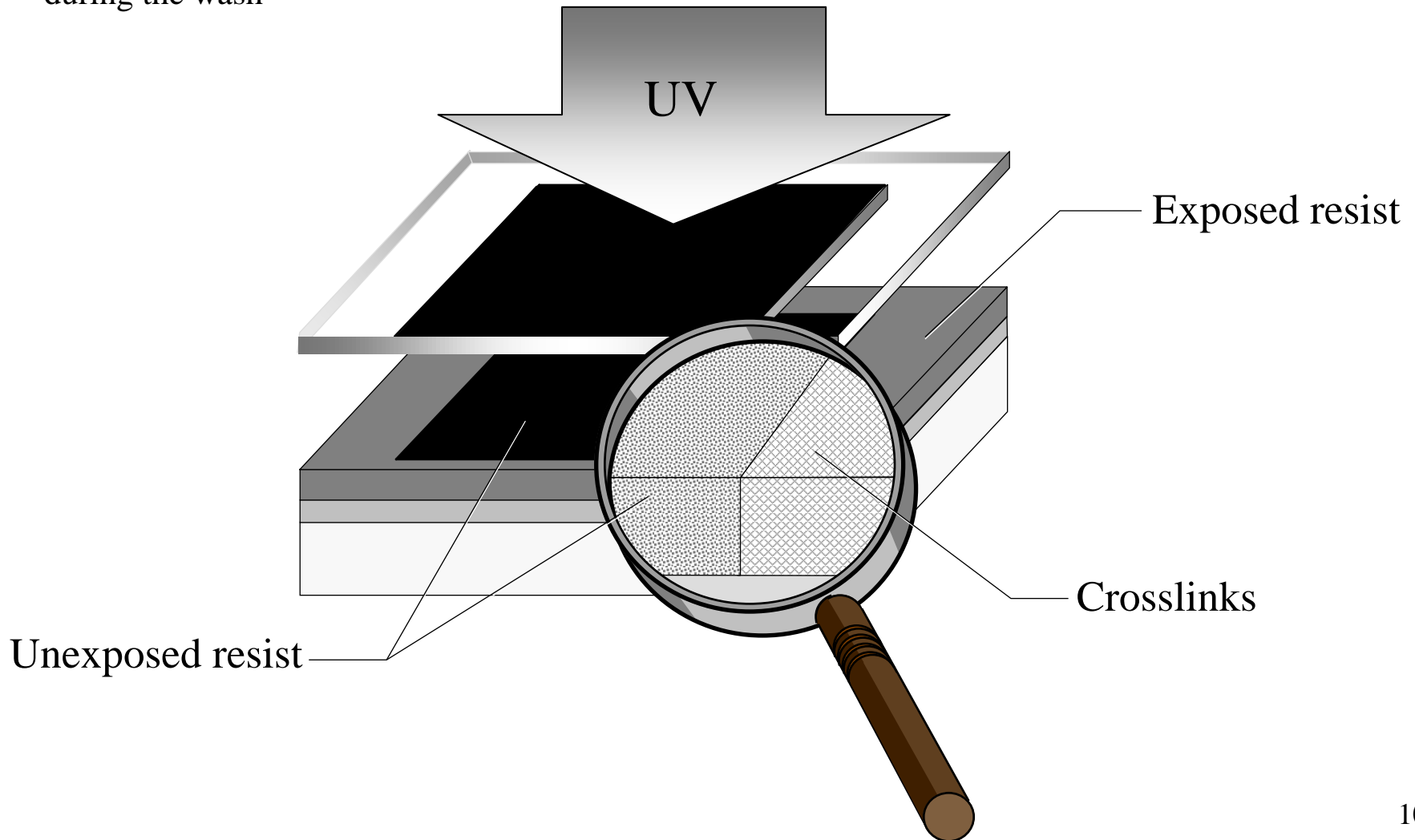


Figure 15.3

# Negative Resist Crosslinking

- Using **organic** solvent (xylene) to develop
- **An organic solvent** rinse cycle is used clean
- Problem: **swelling and distortion** of crosslinked resist due to absorption of the developer solution during the wash



# Development of Positive Resist

- DNQ for i-line, and CA for DUV
- Both are phenolic-based resin, is soluble in a **base** solution
- **TMAH** is used to develop with low metal ions
- The unexposed resist **does not** absorb developer
- Using DI water to **rinse**

Resist exposed to light  
dissolves in the  
develop chemical

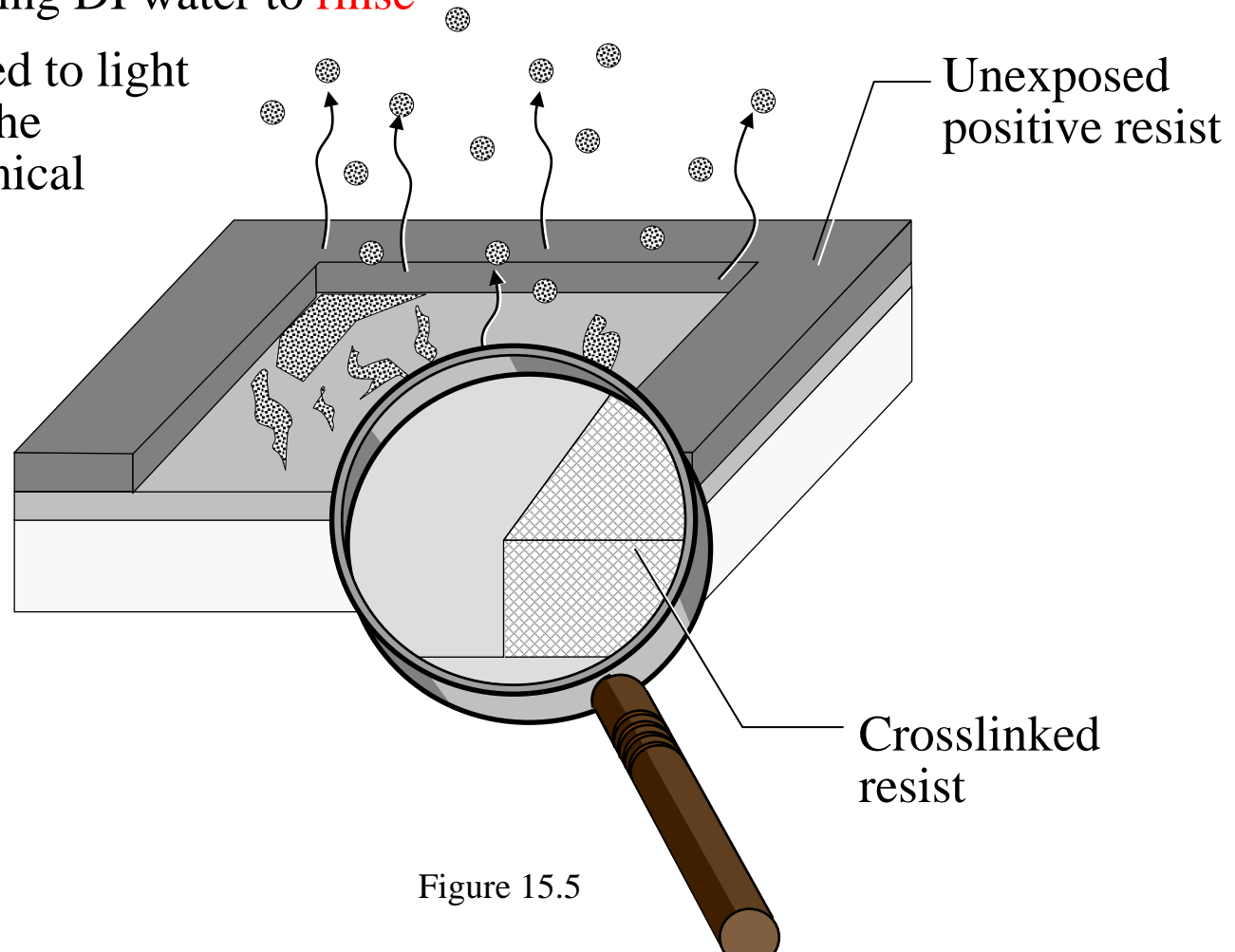
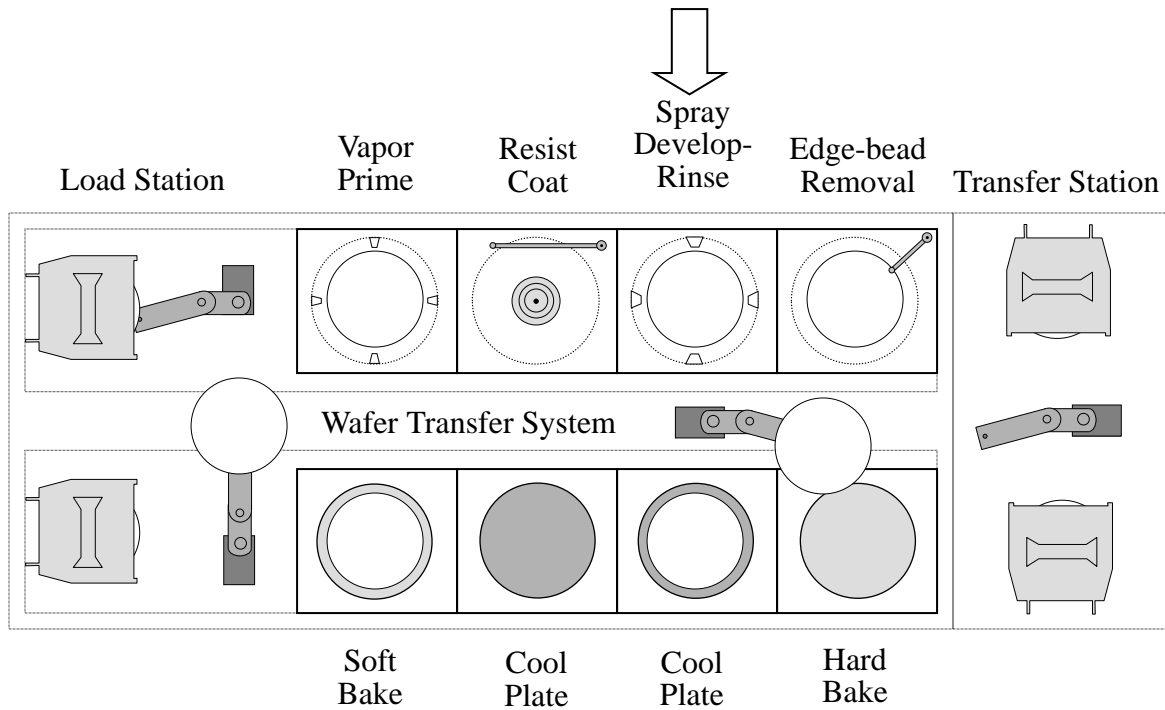


Figure 15.5

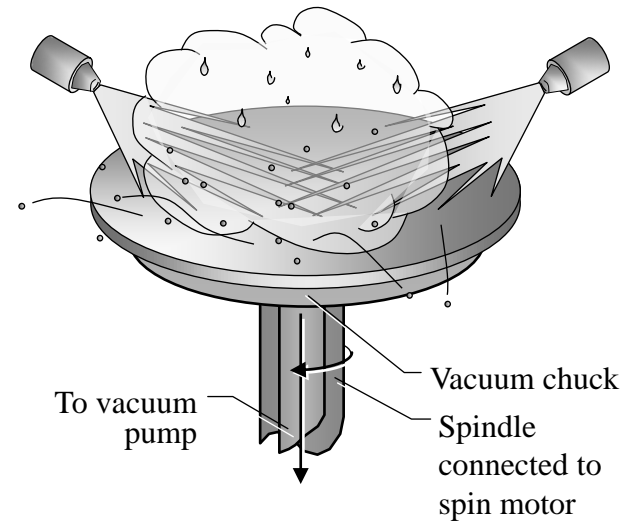
# Development Methods

- Continuous Spray Development
- Puddle Development [dominant]

# Resist Development with Continuous Spray



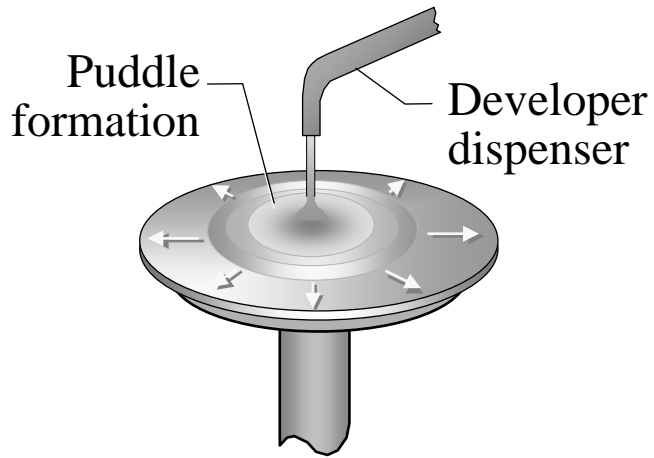
(a) Wafer track system



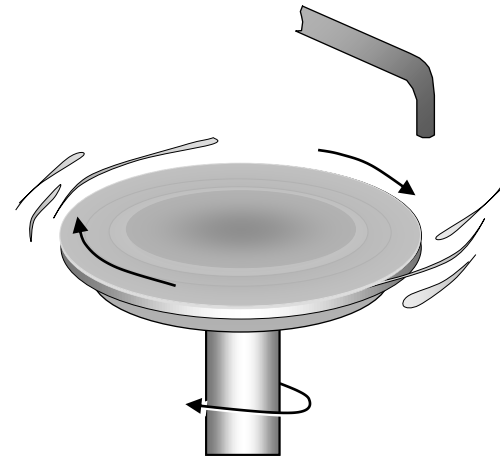
(b) Developer spray dispenser

# Puddle Resist Development

- Puddle development introduces fresh chemicals, improve **wafer-to-wafer uniformity**
- It minimizes temperature gradients and permits control of the variables affecting uniformity



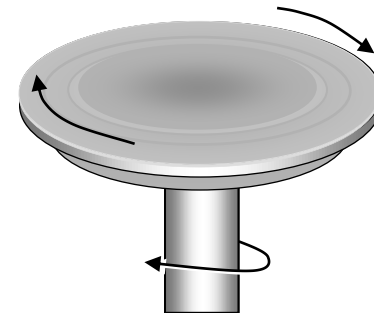
(a) Puddle dispense



(b) Spin-off excess developer



(c) DI H<sub>2</sub>O rinse



(d) Spin dry

Figure 15.7

# Resist Development Parameters

- Developer Temperature
  - 15-25°C, within 1°C
- Developer Time
  - In-situ dissolution rate monitor to endpoint detection, light reflection and phase difference
- Developer Volume
  - Inadequate developer volume results in scumming
- Normality
- Rinse
- Exhaust Flow
- Wafer Chuck

# Hard Bake

- Characteristics of Hard Bake:
  - Post-Development Exposure
  - Evaporates Residual Solvent in Photoresist
  - Hardens the Resist, 130-150°C
  - Improves Resist-to-Wafer Adhesion
  - Prepares Resist for Subsequent Processing
  - Higher Temperature than Soft Bake, but not to Point Where Resist Softens and Flows
- Resist Hardening with Deep UV



# Softened Resist Flow at High Temperature

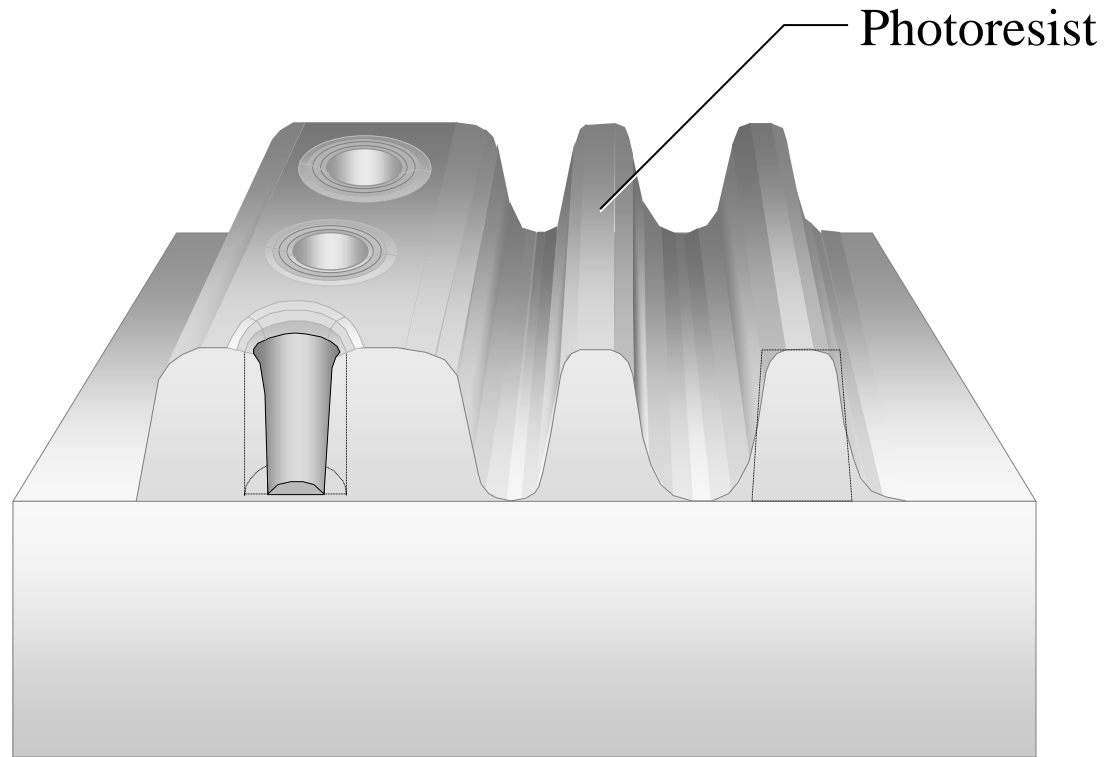


Figure 15.8

# Develop Inspect

- Post-Develop Inspection to Find Defects
- Find Defects before Etching or Implanting
- Prevents Scrap [報廢]
- Characterizes the Photo Process by Providing Feedback Regarding Quality of the Lithography Process
- Develop Inspect Rework Flow

# Automated Inspection Tool for Develop Inspect



Photograph courtesy of Advanced Micro Devices, Leica Auto Inspection station

# Develop Inspect Rework Flow

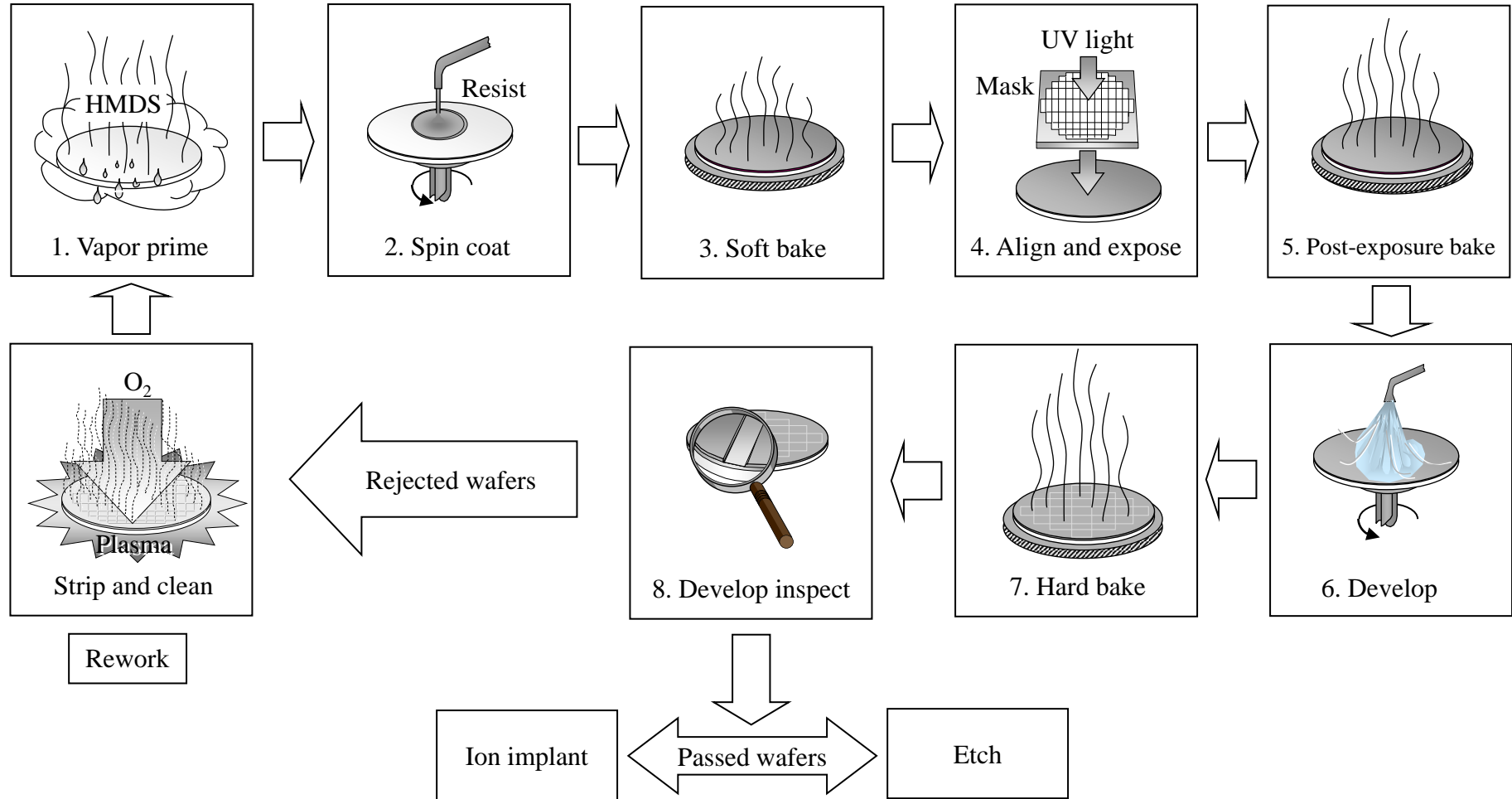


Figure 15.9

# Advanced Lithography

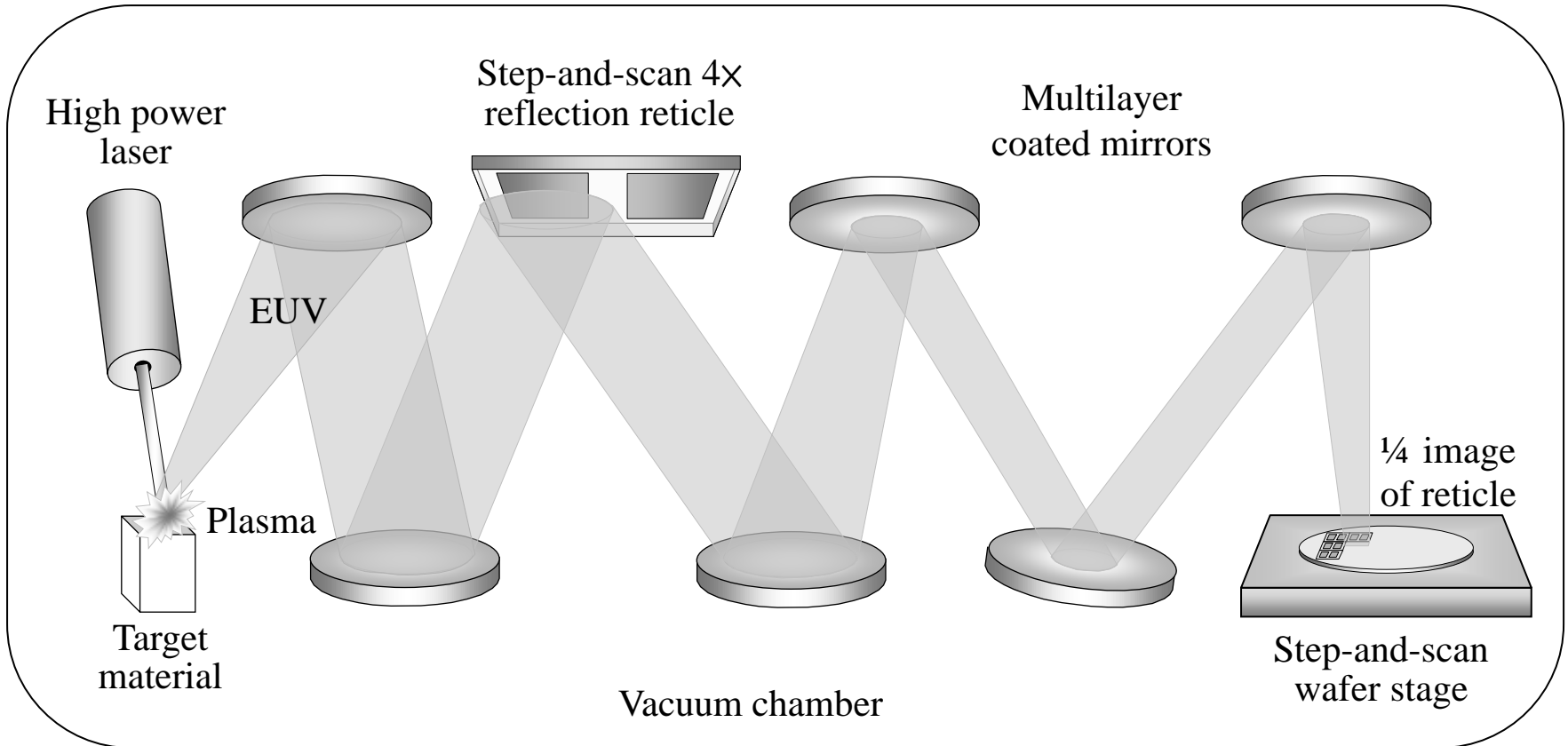
- Next Generation Lithography
  - Extreme UV (EUV)
  - SCALPEL
  - Ion Projection Lithography (IPL)
  - X-Ray
- Advanced Resist Processing
  - Development Trends of Photoresist and Lithography
  - DESIRE Process

# Photolithography Improvements

1. Reduction in wavelength of the UV light source.
2. Increase in numerical aperture.
3. Chemically amplified DUV resists
4. Resolution enhancement techniques (e.g., phase-shift masks and optical proximity correction).
5. Wafer planarization (chemical mechanical planarization, or CMP) to reduce surface topography.
6. Advances in photolithography equipment (e.g., stepper and step-and-scan).

# Concept for Extreme Ultraviolet Lithography

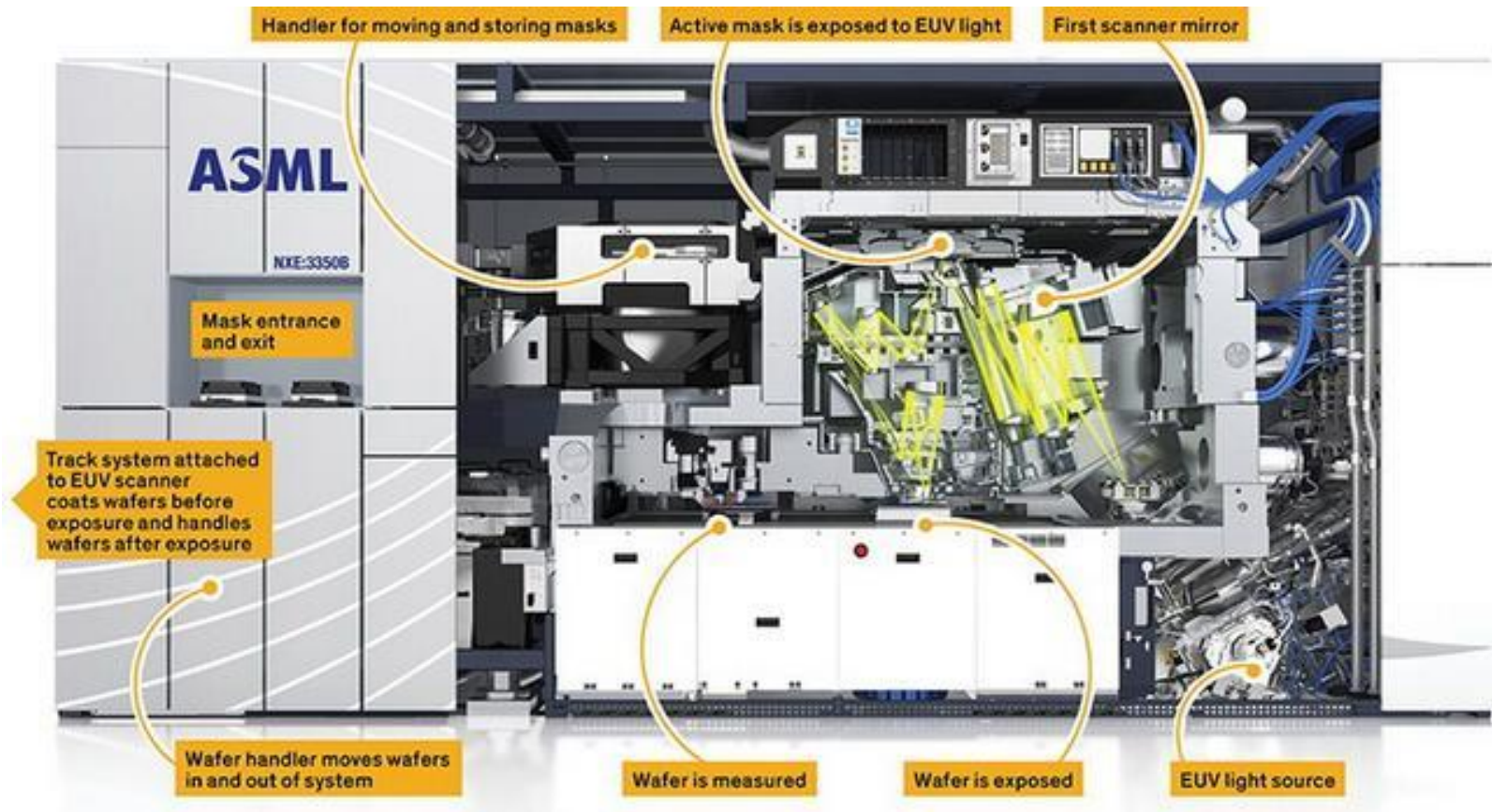
- Wavelength  $\sim 13$  nm, an all reflective 4X projection optics will image the UV beam onto a resist-coated wafer



Redrawn from International SEMATECH's Next Generation Lithography Workshop Brochure

Figure 15.10

# ASML EUV

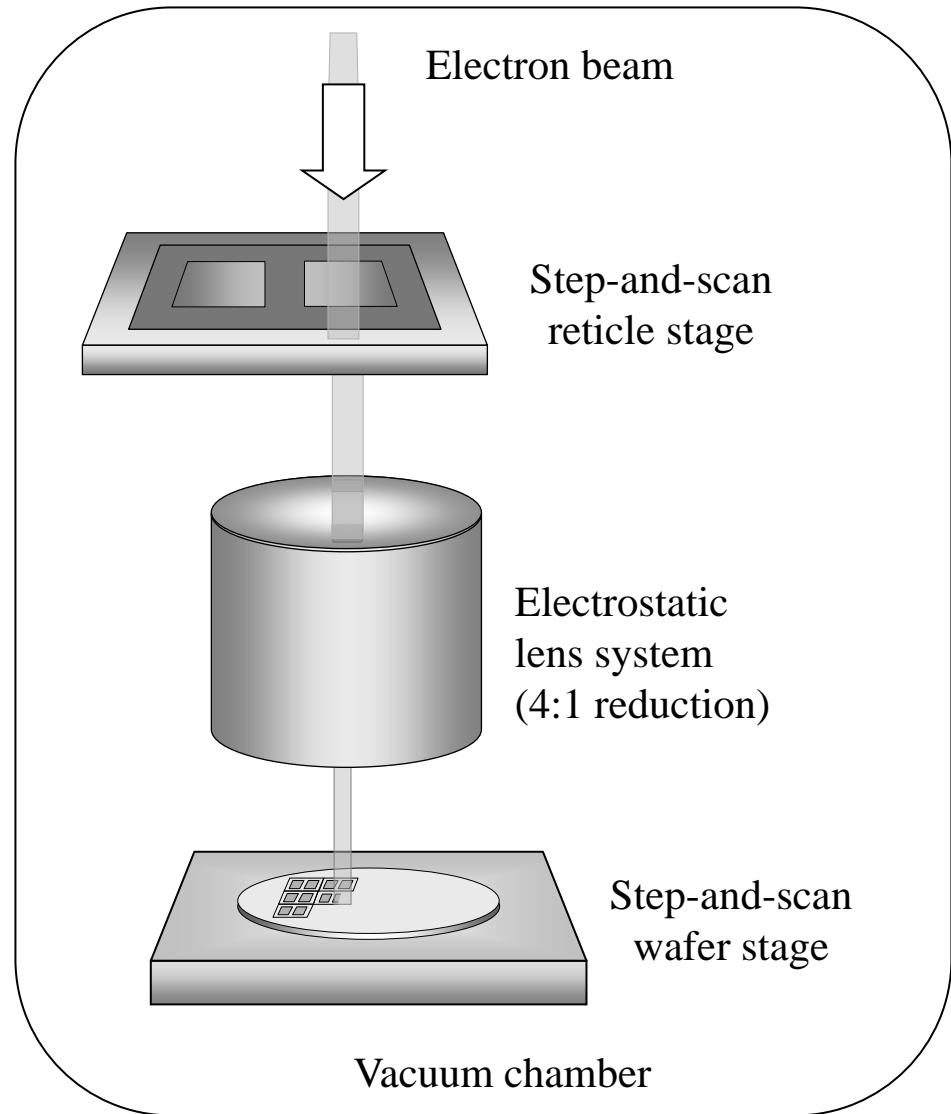


ASML 進一步表示，當前半導體先進製程中不可或缺要角的 EUV 設備，每一部都有超過 10 萬個零件，加上 3 千條的電線、4 萬個螺栓、以及 2 公里長的軟管等零組件。其最大重量達到 18 萬公斤，每次的運輸必須要動用 40 個貨櫃，20 輛卡車、並且利用 3 架次的貨機才能夠運輸完畢，而且每部的造價超過 1 億美元。所以，在這樣龐大的數字下，就可以想見，ASML 為什麼一年只有 30 部 EUV 的最大產量了。2019 年 06 月



# Concept of SCALPEL

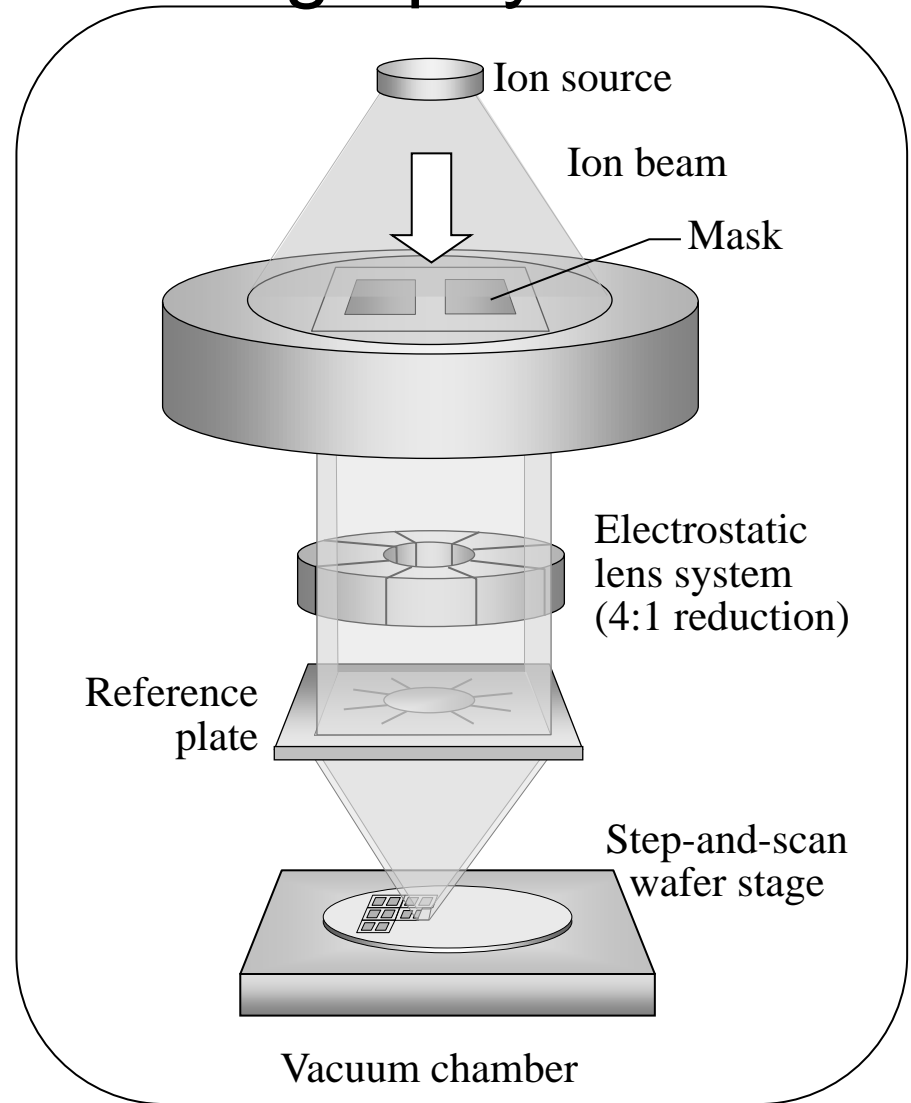
- Scattering with Angular Limitation Projection Electron Beam Lithography
- Electron beam source
- A multi-layer membrane mask is used that absorbs few electrons
- A high atomic number layer in the mask that **scatters** the electrons for a high-contrast image.
- Using a **step-and-scan** writing strategy that produces **strips** of exposed resist.



Redrawn from International SEMATECH's Next Generation Lithography Workshop Brochure  
Figure 15.11

# Ion Projection Lithography

- Use hydrogen or helium ions.
- Ions transfer their energy more efficiently than electron beam due to larger mass.
- No electron **backscatter**, creating proximity effects.



Redrawn from International SEMATECH's Next Generation Lithography Workshop Brochure

Figure 15.12

# X-ray Spectrum

- The most common X-ray source for lithography is known as a synchrotron (an electron storage ring)
- High-energy electrons are forced into closed curved paths by magnetic fields and made intense and reasonably collimated

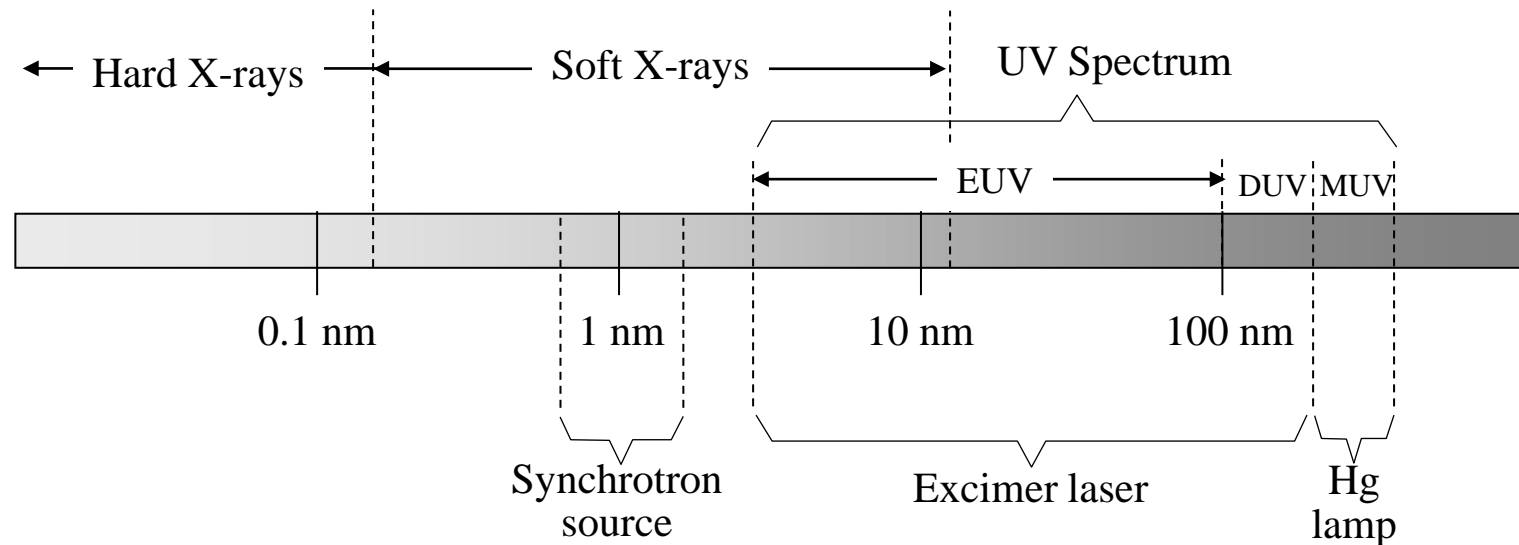
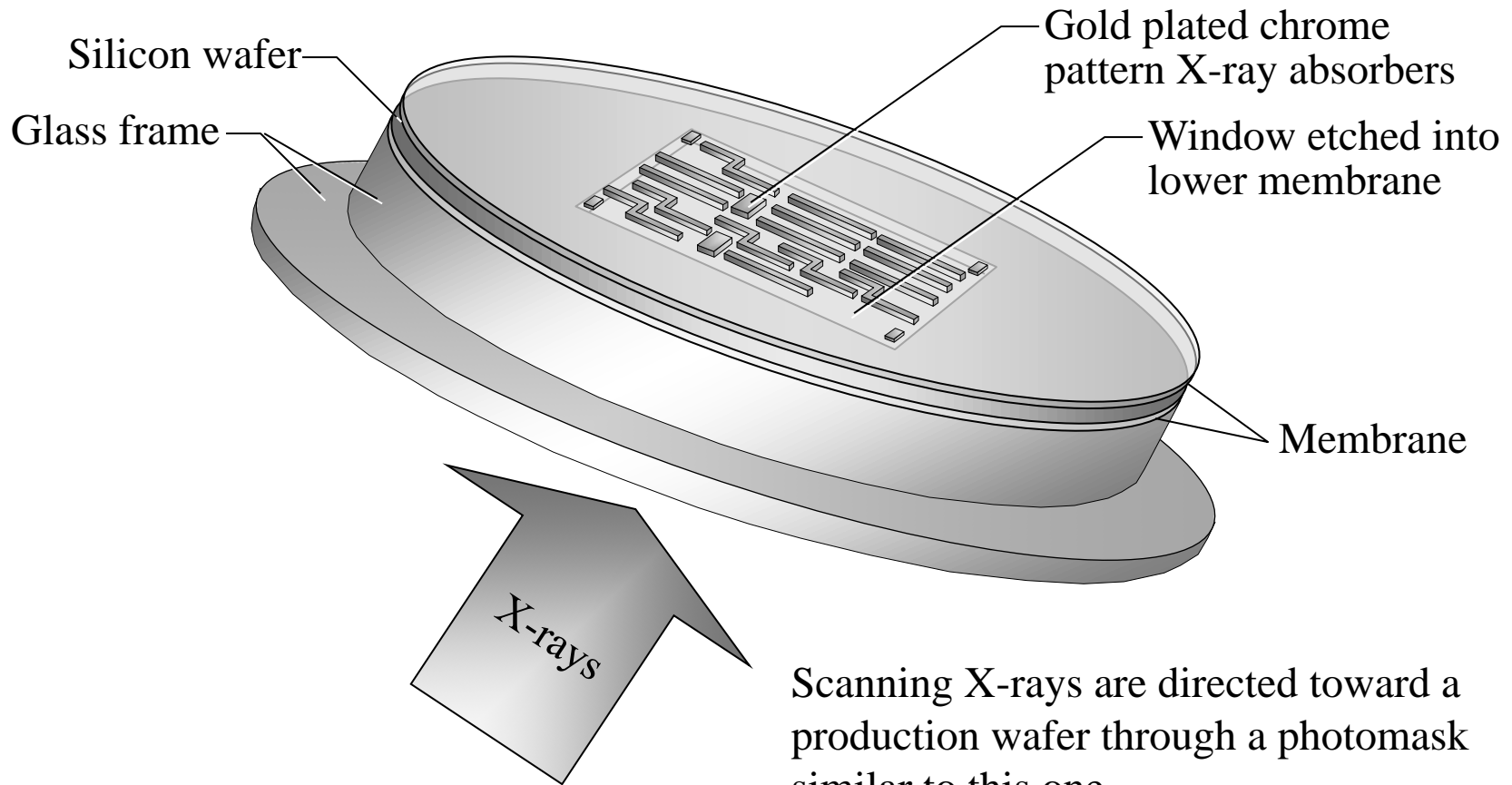


Figure 15.13

# Concept of X-ray Photomask :1X



Scanning X-rays are directed toward a production wafer through a photomask similar to this one.

Redrawn from C. Y. Chang and S. M. Sze, *ULSI Technology*, edited by C. Y. Chang and S. M. Sze (New York: McGraw-Hill 1996) p.314

Figure 15.14

# Development Trends of Photoresist and Lithography

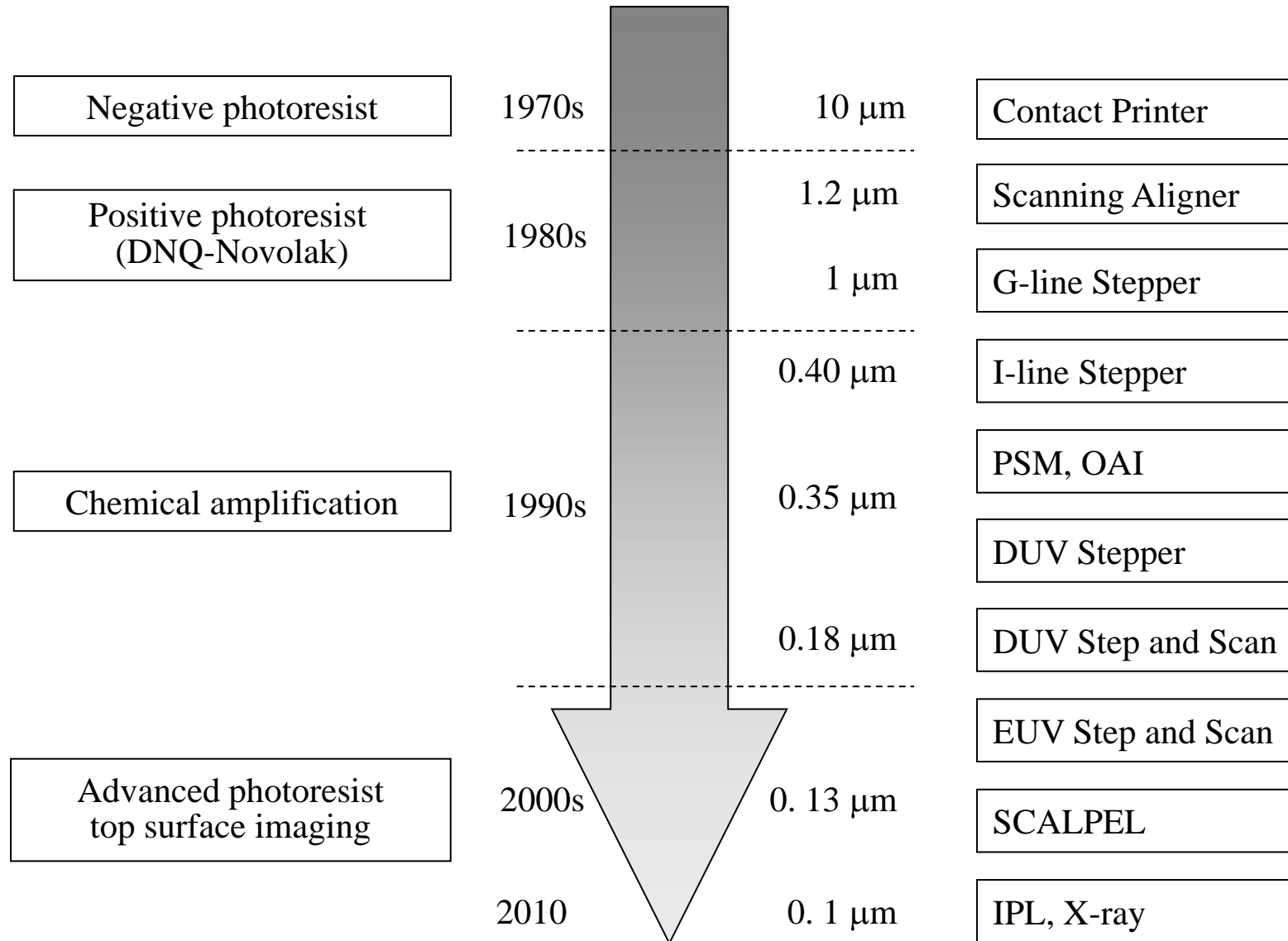
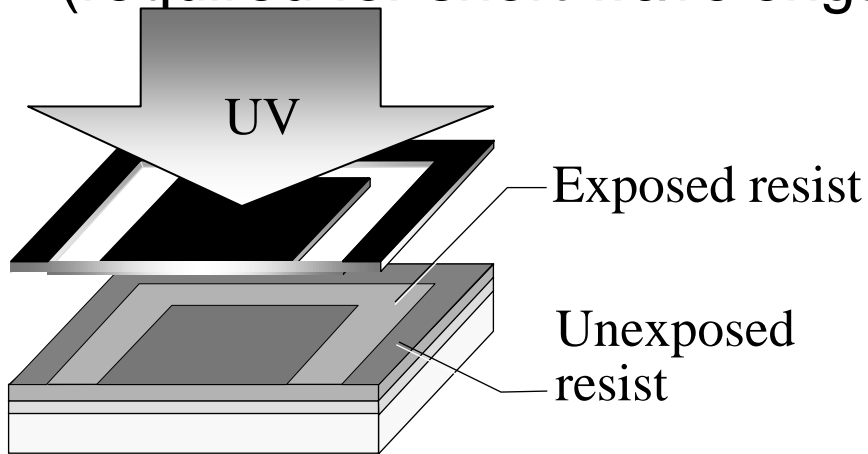


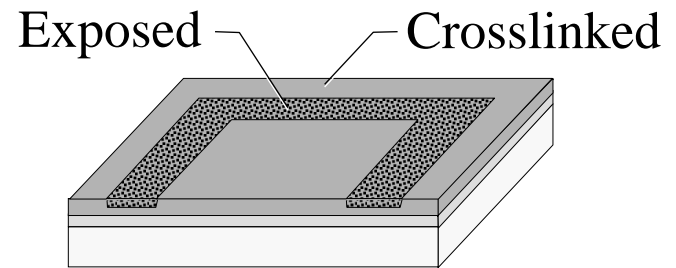
Figure 15.15

# Top Surface Imaging

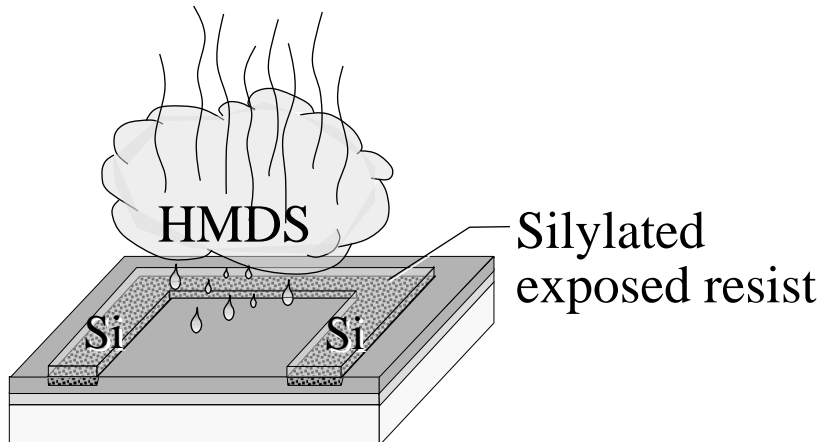
(required for short wavelength and penetration depth)



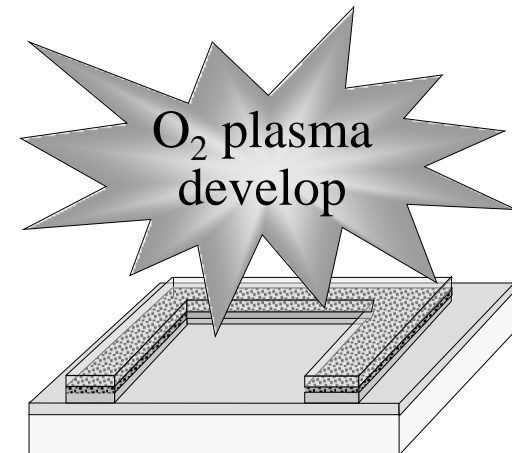
(a) Normal exposure process



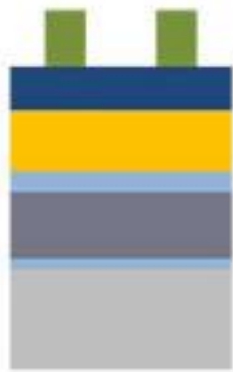
(b) Post exposure bake



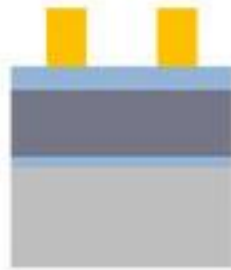
(c) Vapor phase silylation



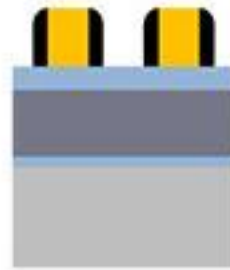
(d) Final developed pattern



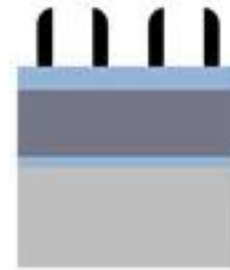
Print litho



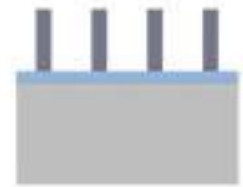
Etch  
mandrel



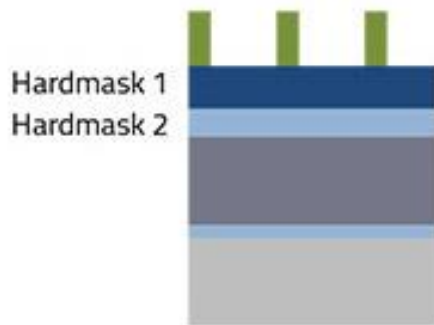
Deposit  
and etch  
spacer



Remove  
mandrel



Etch final  
pattern



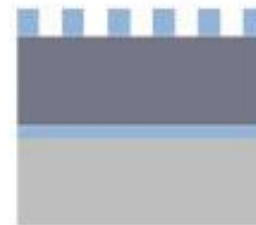
Print  
first litho



Etch  
hardmask 1



Print  
second litho

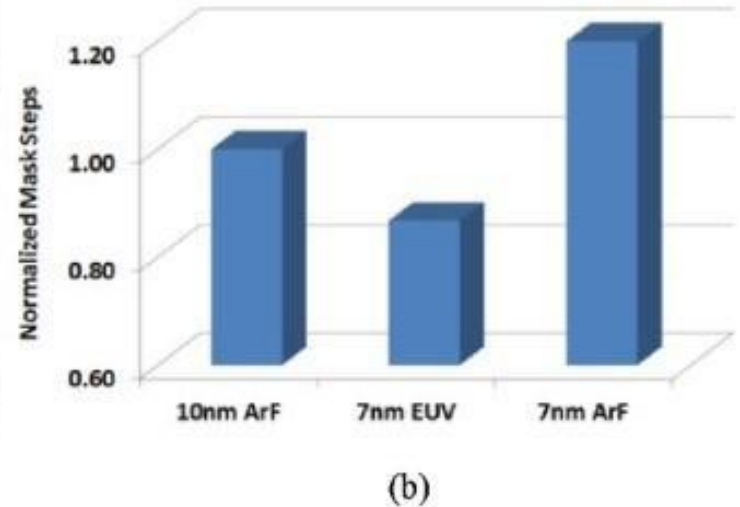
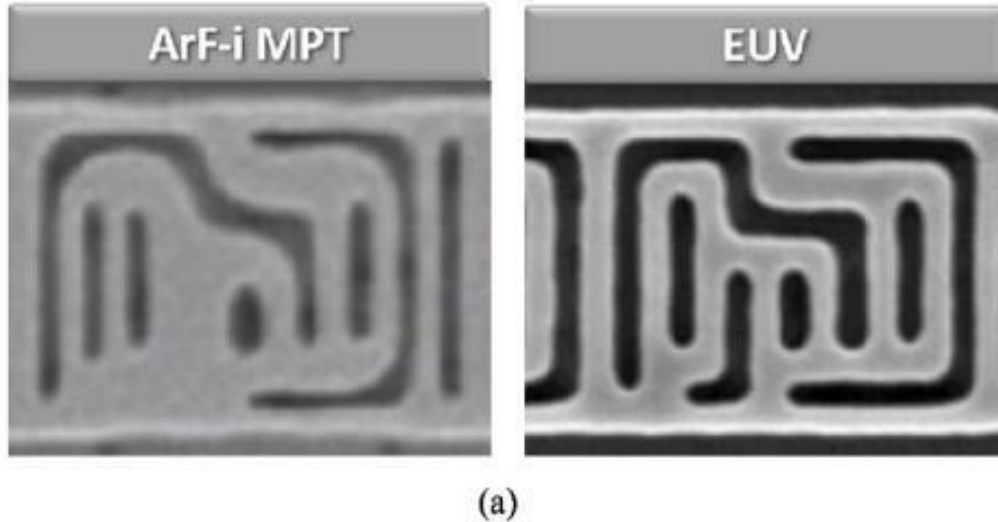


Etch  
hardmask 2



Etch final  
pattern

# EUV vs. ArF-I MPT



Progress in EUV lithography toward manufacturing", Proc. SPIE 10143, Extreme Ultraviolet (EUV) Lithography VIII, 1014306 (24 March 2017))

EUV帶來的價值還包括(1)圖案解析度會明顯更高。傳統多重曝光技術的一大問題就是圖案解析度並不好，就像上面這個圖案一樣，最終獲得的圖案與預期存在出入。三星表示，EUV 2D解析度較ArF多重曝光要優秀70%；(2)設計彈性更大，如雙向金屬配線，路徑、配線變得更簡單；(3)更緊密的關鍵尺寸分佈(CD distribution)；(4)在SRAM快取儲存部份，單次曝光2D EUV的佈局圖案變小至多50%