Semiconductor Manufacturing Technology

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Chapter 17

Doping Processes

Objectives

After studying the material in this chapter, you will be able to:

1. Explain the purpose and applications for doping in wafer fabrication.
2. Discuss the principles and process of dopant diffusion.
3. Provide an overview of ion implantation, including its advantages and disadvantages.
4. Discuss the importance of dose and range in ion implant.
5. List and describe the five major subsystems for an ion implanter.
6. Explain annealing and channeling in ion implantation.
7. Describe different applications of ion implantation.

Common Dopants Used in Semiconductor Manufacturing

- Doping is the introduction of a dopant into the crystal structure of a semiconductor material to modify its electronic properties
- Dopants are referred to as impurities
- Two techniques: thermal diffusion and ion implantation (dominant)

Acceptor Dopant Group IIIA (P-Type)		**Semiconductor Group IVA**		**Donor Dopant Group VA (N-Type)**	
Element	**Atomic Number**	**Element**	**Atomic Number**	**Element**	**Atomic Number**
Boron (B)	**5**	Carbon	6	Nitrogen	7
Aluminum	13	Silicon (Si)	14	**Phosphorus (P)**	**15**
Gallium	31	Germanium	32	**Arsenic (As)**	**33**
Indium	49	Tin	50	**Antimony**	**51**

CMOS Structure with Doped Regions

- Transistor performance is increasing dependent on precise doping profiles in the silicon that are achievable **only** with ion implant

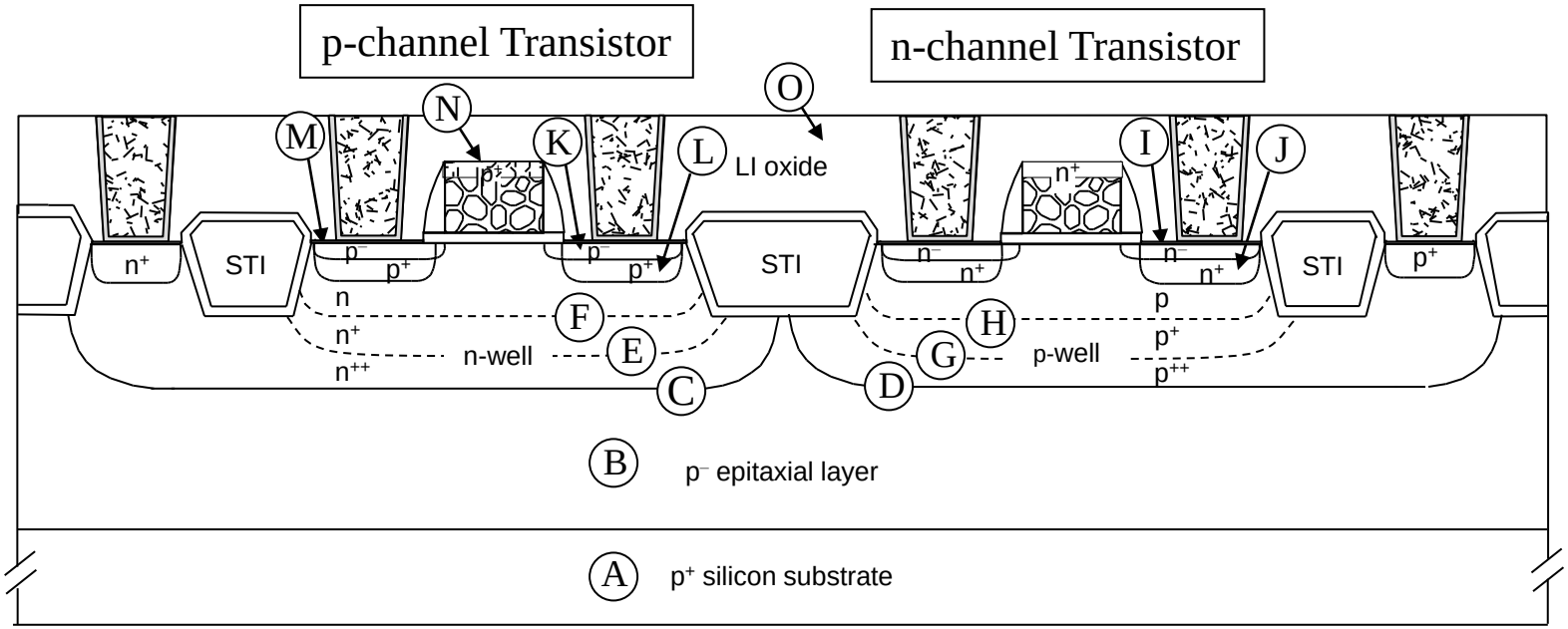


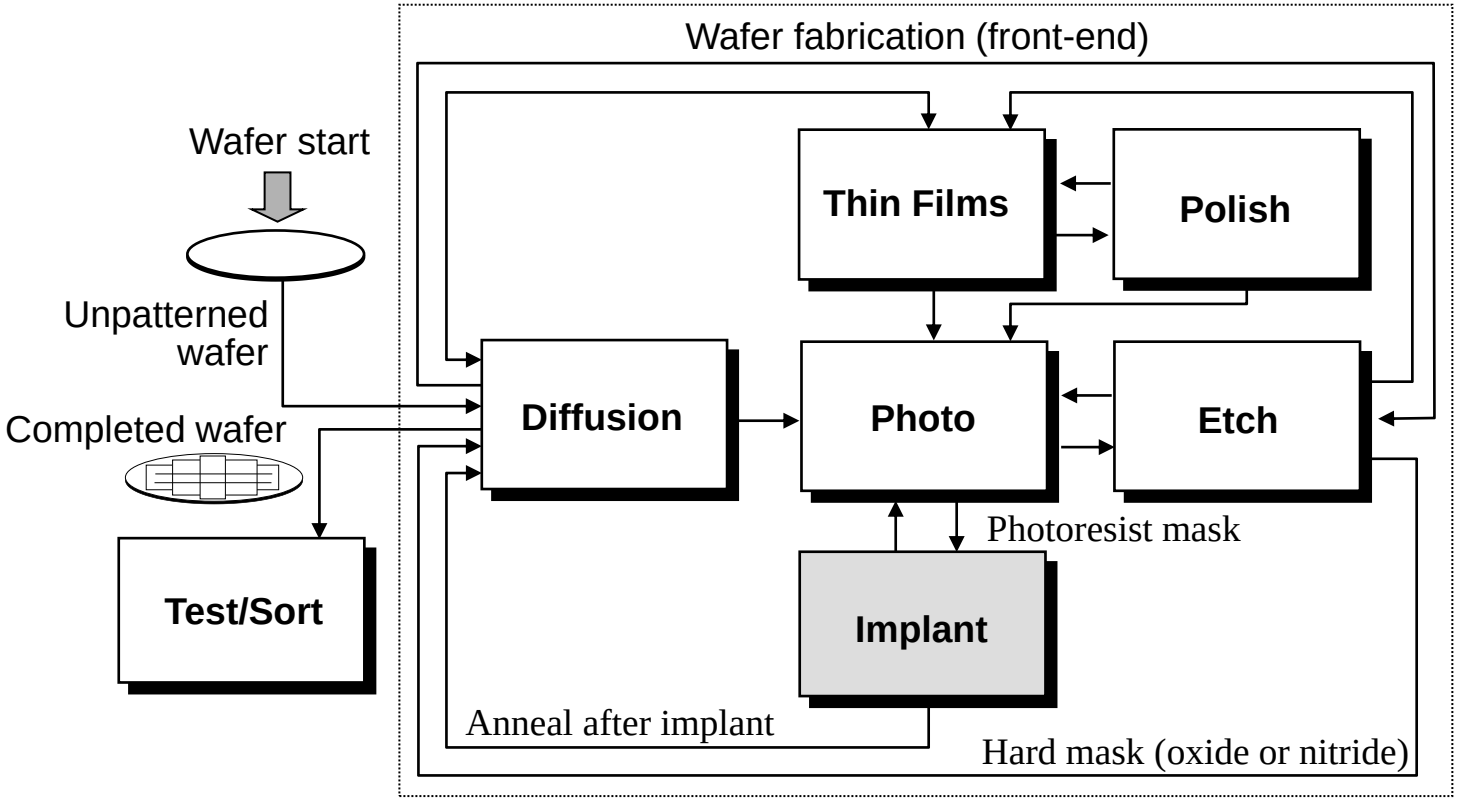
Figure 17.1

Common Dopant Processes in CMOS Fabrication

Process Step	Dopant	Method
A. p+ Silicon Substrate	B	Diffusion
B. p^- Epitaxial Layer	B	Diffusion
C. Retrograde n-Well	P	Ion Implant
D. Retrograde p-well	B	Ion Implant
E. p-Channel Punchthrough	P	Ion Implant
F. p-Channel Threshold Voltage (V_T) Adjust	P	Ion Implant
G. p-Channel Punchthrough	B	Ion Implant
H. p-Channel V_T Adjust	B	Ion Implant
I. n-Channel Lightly Doped Drain (LDD)	As	Ion Implant
J. n-Channel Source/Drain (S/D)	As	Ion Implant
K. p-Channel LDD	BF_2	Ion Implant
L. p-Channel S/D	BF_2	Ion Implant
M. Silicon	Si	Ion Implant
N. Doped Polysilicon	P or B	Ion Implant or Diffusion
O. Doped SiO_2	P or B	Ion Implant or Diffusion

Table 17.2

Ion Implant in Process Flow

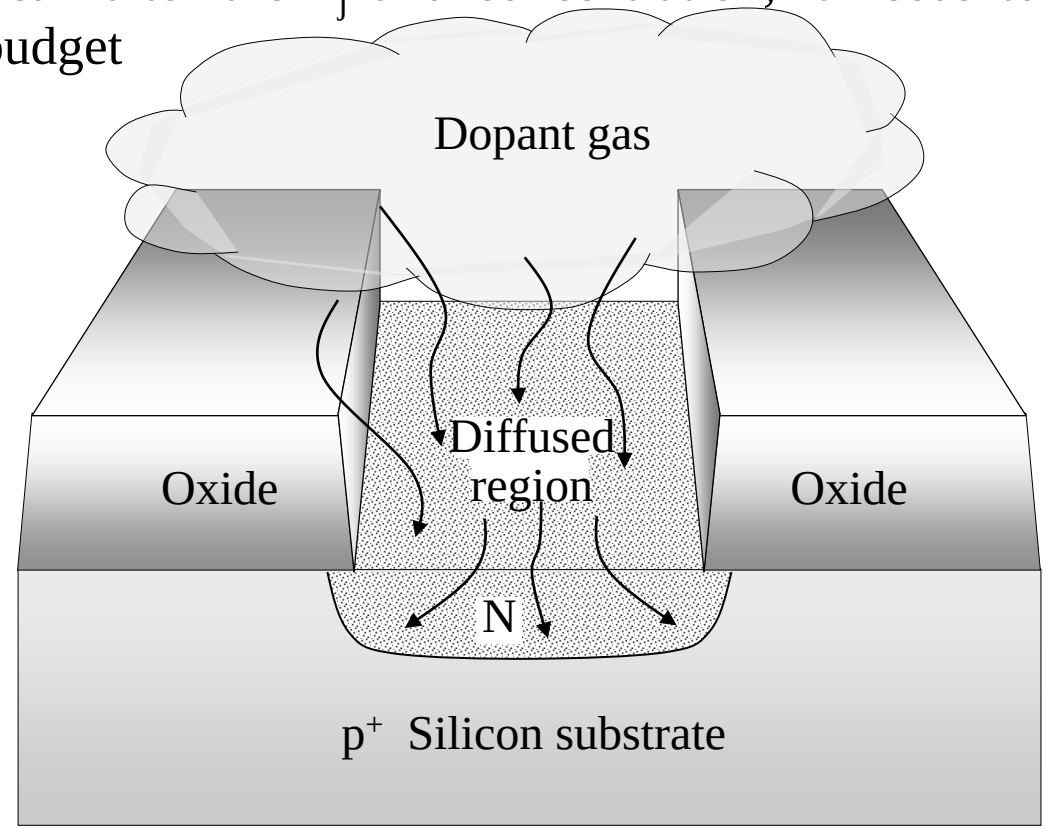


Used with permission from Lance Kinney, AMD

Figure 17.2

Doped Region in a Silicon Wafer

- The selective introduction of dopants into masked openings on the wafer forms a doped region
- Dopant profile: amount of dopant as a function of depth
- Mask: low temperature: PR, high temperature: oxide or nitride
- The exact depth in the wafer where the p-type dopant meets the n-type dopant is the junction depth, x_j
- Thermal can alter the x_j and concentration, it needs to minimize the thermal budget



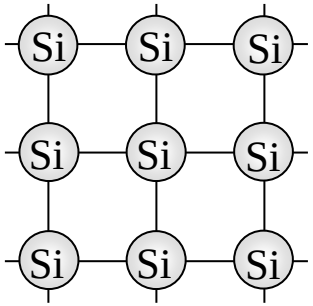
Diffusion

- Diffusion occurs from a region of relatively higher concentration into a region of lower concentration, resulting from the motion of atoms

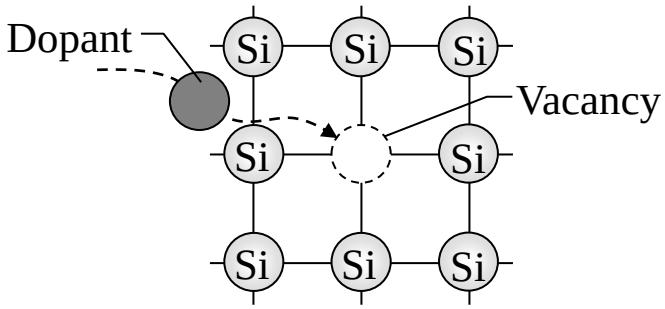
  - Diffusion Principles
    - Three Steps
      - Pre-deposition:
        - at high temperature, dopant introduces from source cabinet to the furnace
        - a cap oxide is grown to prevent dopant out diffusion
      - Drive-in:
        - to desired depth, redistribution at SiO_2/Si interface, B tends to oxide, and P push away
      - Activation
        - Enable the dopant to bond with silicon atom

Dopant Movement in Silicon

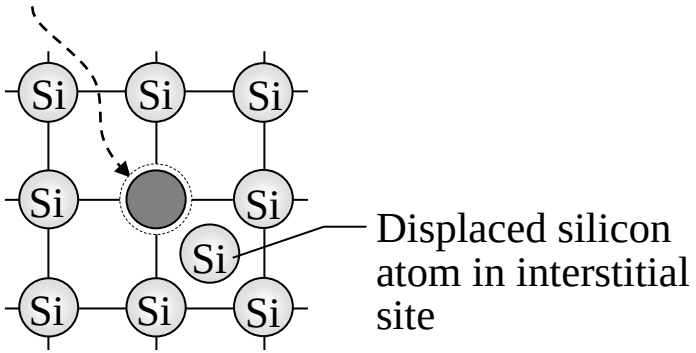
- The higher the diffusivity, the faster the dopant moves
- Diffusivity increases with temperature, in a term as diffusion coefficient, D
- High D: Au, Cu, Ni, using primarily interstitial movement
- Slow D: P and As, using primarily substitutional movement



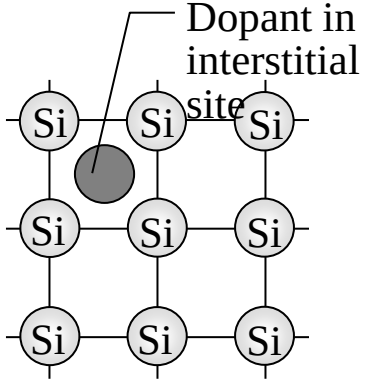
a) Silicon lattice structure



b) Substitutional diffusion



c) Mechanical interstitial displacement



d) Interstitial diffusion

Solid Solubility Limits in Silicon at 1100°C

- At a given temperature, there is a limit to how much dopant can be absorbed by the silicon, referred to as the solid solubility limit
- Diffusion in all direction, down to the silicon, laterally, and back out of the wafer
- Lateral diffusion: along the surface of the wafer is 75 to 85% of the vertical depth. It is undesirable in advanced MOS device, because it can reduce channel length, affect device density and performance

Dopant	**Solubility Limit (atoms/cm^3)**
Arsenic (As)	1.7×10^{21}
Phosphorus (P)	1.1×10^{21}
Boron (B)	2.2×10^{20}
Antimony (Sb)	5.0×10^{19}
Aluminum (Al)	1.8×10^{19}

Table 17.3

Diffusion Process

Eight Steps for Successful Diffusion:

1. Run qualification test to ensure the tool meets production quality criteria.
2. Verify wafer properties with a lot control system.
3. Download the process recipe with the desired diffusion parameters.
4. Set up the furnace, including a temperature profile.
5. Clean the wafers and dip in HF to remove native oxide.
6. Perform predeposition: load wafers into the deposition furnace and diffuse the dopant.
7. Perform drive-in: increase furnace temperature to drive-in and activate the dopant bonds, then unload the wafers.
8. Measure, evaluate and record junction depth and sheet resistivity.

Typical Dopant Sources for Diffusion

- Dopants are typically supplied as a gaseous or liquid source in the form of a compound
- B and P are solids at room temperature with low vapor pressure
- A liquid source (bubbler) has a carrier gas bubbled through it and is delivered to the furnace tube as a vapor
- The dopant is diluted for safety, AsH_3 and B_2H_6 are the most toxic

Dopant	Formula of Source	Chemical Name
Arsenic (As)	AsH_3	Arsine (gas)
Phosphorus (P)	PH_3	Phosphine (gas)
Phosphorus (P)	$POCl_3$	Phosphorus oxychloride (liquid)
Boron (B)	B_2H_6	Diborane (gas)
Boron (B)	BF_3	Boron tri-fluoride (gas)
Boron (B)	BBr_3	Boron tri-bromide (liquid)
Antimony (Sb)	$SbCl_5$	Antimony pentachloride (solid)

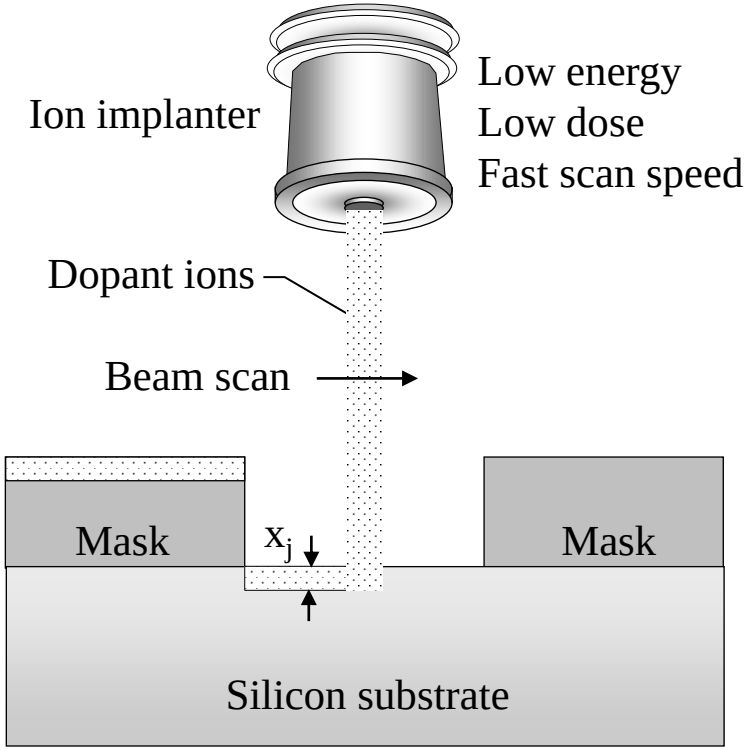
Table 17.4

Ion Implantation

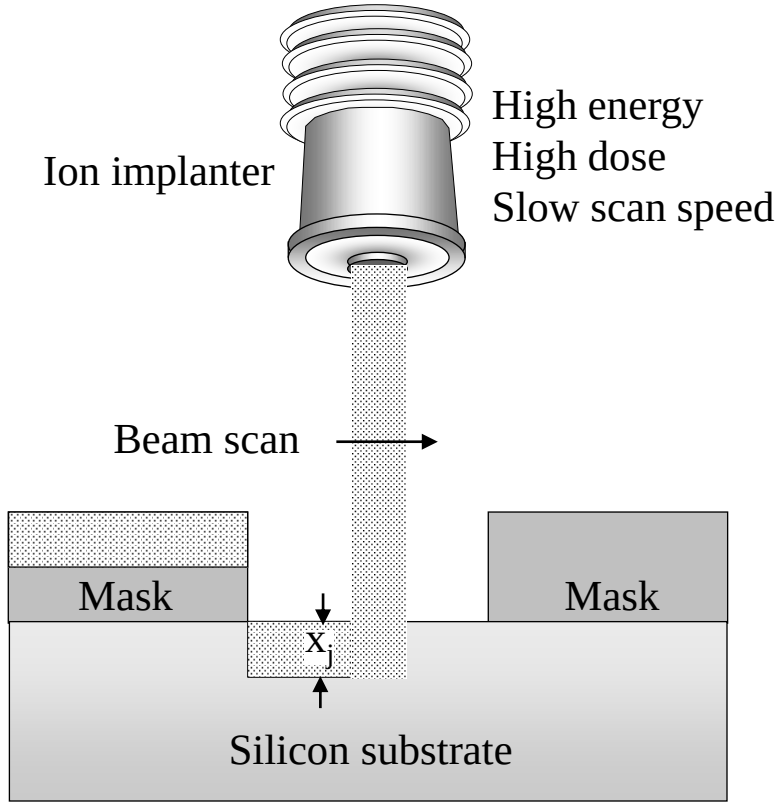
- Ion implantation is a method for introducing controlled amounts of dopants into the silicon substrate to change its electronic properties
- It is a physical process

  - Overview
    - Controlling Dopant Concentration
    - Advantages of Ion Implant
    - Disadvantages of Ion Implant
  - Ion Implant Parameters
    - Dose
    - Range

Controlling Dopant Concentration and Depth



a) Low dopant concentration (n^-, p^-) and shallow junction (x_j)

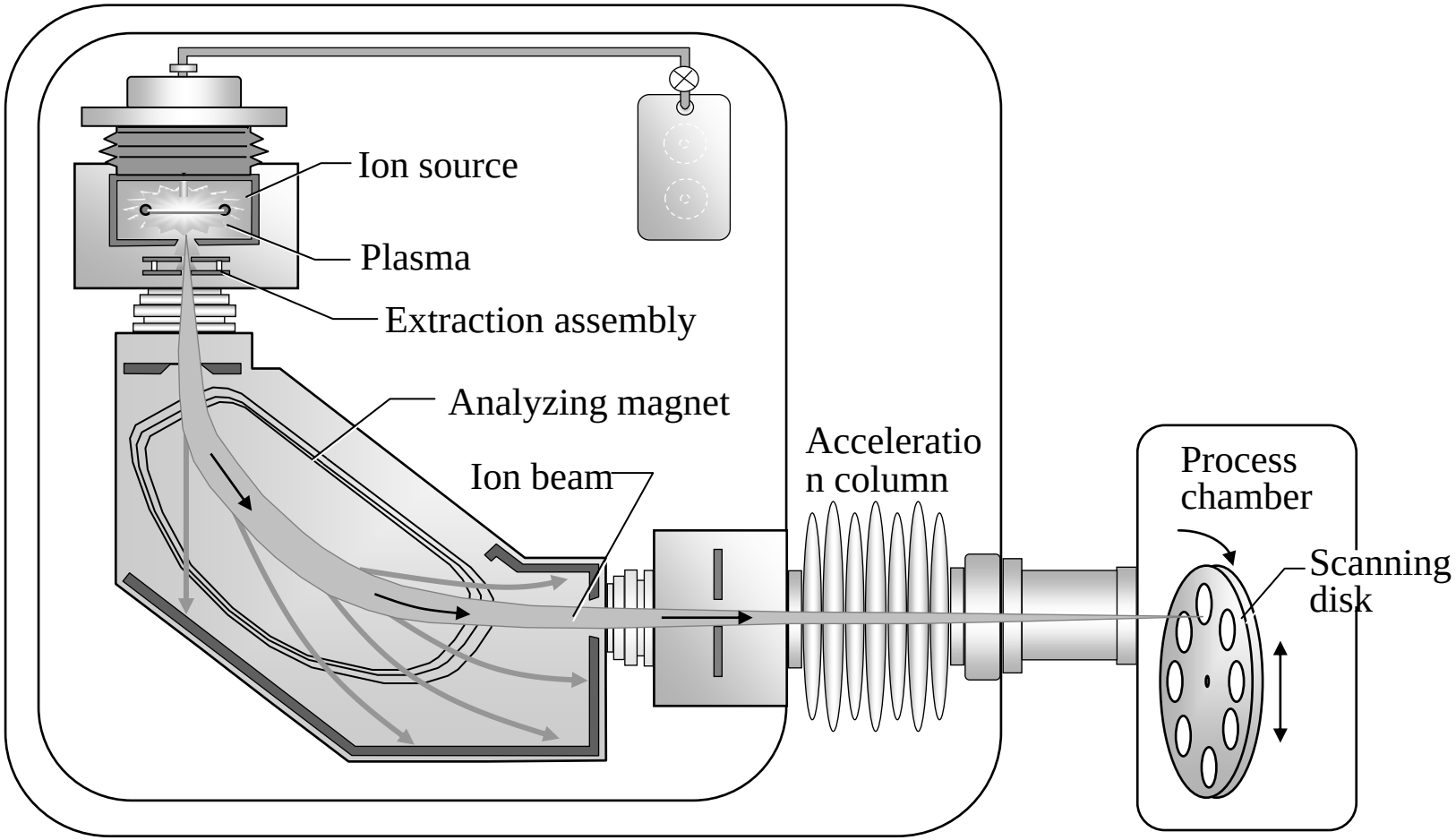


b) High dopant concentration (n^+, p^+) and deep junction (x_j)

Figure 17.5

General Schematic of an Ion Implanter

- Ion source: positive charge
- Extraction assembly: extract ions
- Mass Analyzer: form a beam of the desired dopant ions
- Acceleration column: to attain a high velocity



Ion Implanter

Two major goals:

1.To introduce a uniform, controlled amount of a specific dopant into the wafer

2.To place the dopants at a desired depth

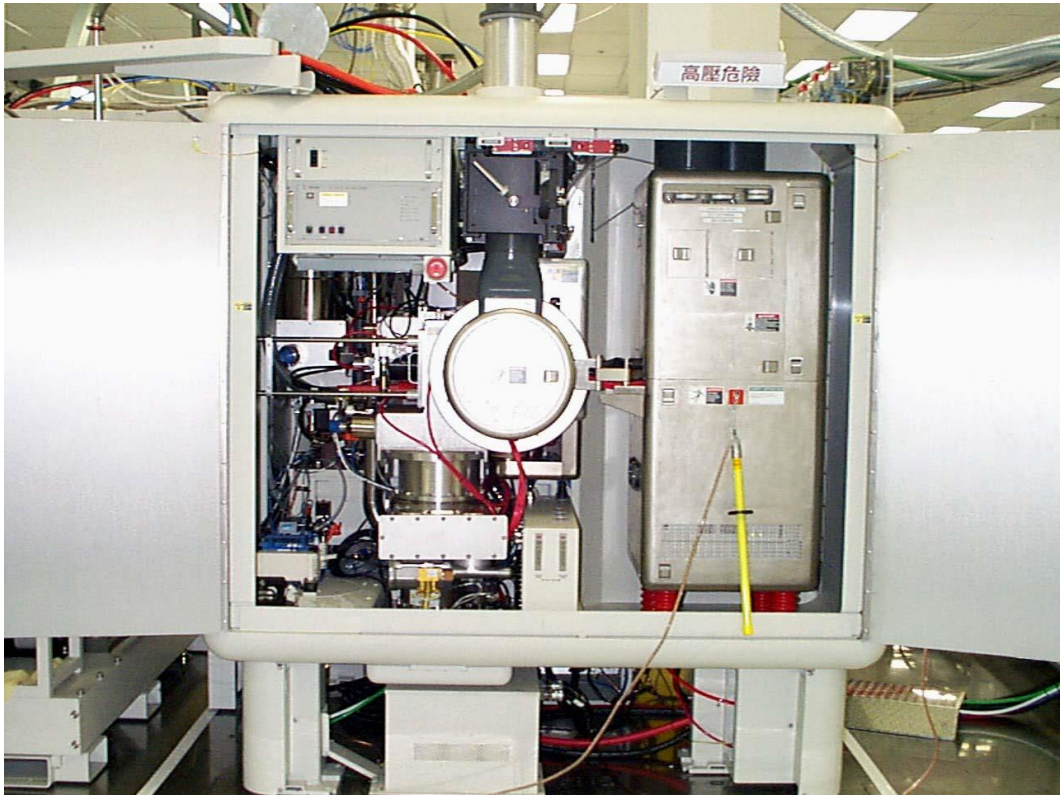


Photo 17.1

Photograph courtesy of Varian Semiconductor, VIISion 80 Source/Terminal side

Advantages of Ion Implantation (from Table 17.5)

1. Precise Control of Dopant Concentration
2. Good Dopant Uniformity
3. Good Control of Dopant Penetration Depth
4. Produces a Pure Beam of Ions
5. Low Temperature Processing
6. Ability to Implant Dopants Through Films
7. No Solid Solubility Limit

- Disadvantages: damage to the crystal structure
- Needs a high-temperature anneal

Table 17.5

Ion Implant Parameters

- Dose:
  - ions/cm^2= It/enA (n: charge per ion)
  - A high beam current is often desirable to increase wafer throughput, but create uniformity problem
  - Low-to-medium beam current: 0.1-1 mA, while a high beam: 10-25 A
- Range:
  - KE=nV (kinetic energy in electron volts, eV)
  - High energy: 200 keV- 2~3MeV, used for retrograde well
  - Retrograde well has higher doping concentration deeper in the well than at the surface
  - Ultralow energy down to 200 eV to form a very shallow depths source/drain

Classes of Implanters

Class of Implanter System	Description and Applications
Medium Current	• Highly pure beam currents <10 mA. • Beam energy is usually < 180 keV. • Most often the ion beam is stationary and the wafer is scanned. • Specialized applications of punchthrough stops.
High Current	• Generate beam currents > 10 mA and up to 25 mA for high dose implants. • Beam energy is usually <120 keV. • Most often the wafer is stationary and the ion beam does the scanning. • Ultralow-energy beams (<4keV down to 200 eV) for implanting ultrashallow source/drain junctions.
High Energy	• Beam energy exceeds 200 keV up to several MeV. • Place dopants beneath a trench or thick oxide layer. • Able to form retrograde wells and buried layers.
Oxygen Ion Implanters	• Class of high current systems used to implant oxygen in silicon-on-insulator (SOI) applications.

Table 17.6

Range and Projected Range of Dopant Ion

- R_P is how far the implanted ions travel into the wafer, depending on the ion mass and energy, the target mass and the beam direction
- ΔR_p (straggle) represents the spread of the implanted species around R_p
- As energy increases, R_p increases, but peak concentration decreases because the ΔR_p increases

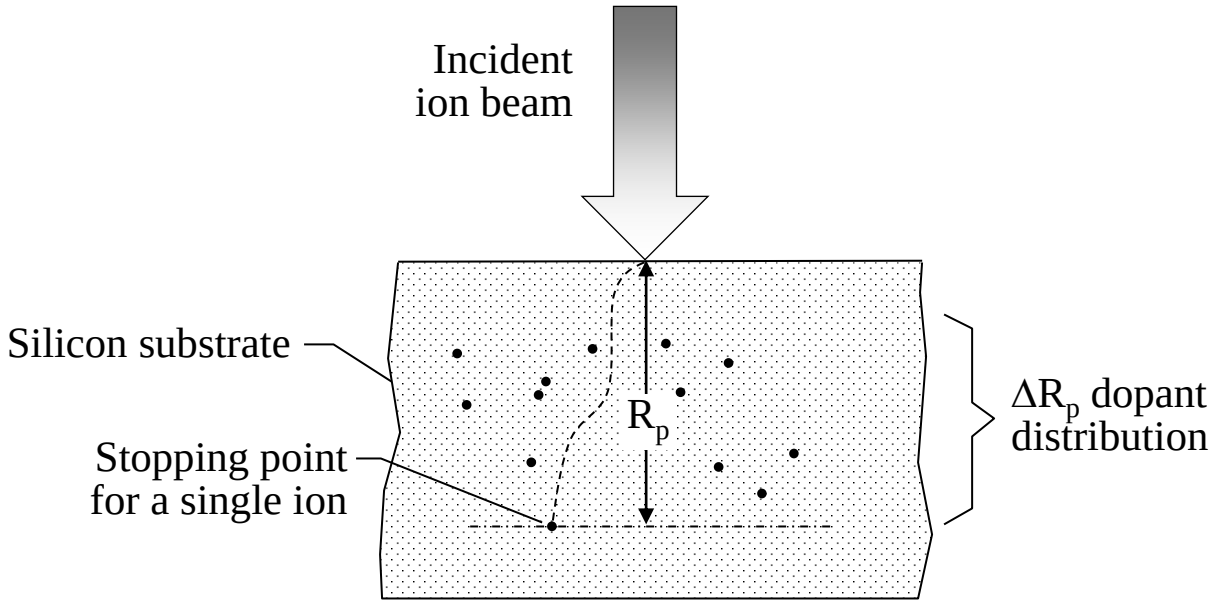
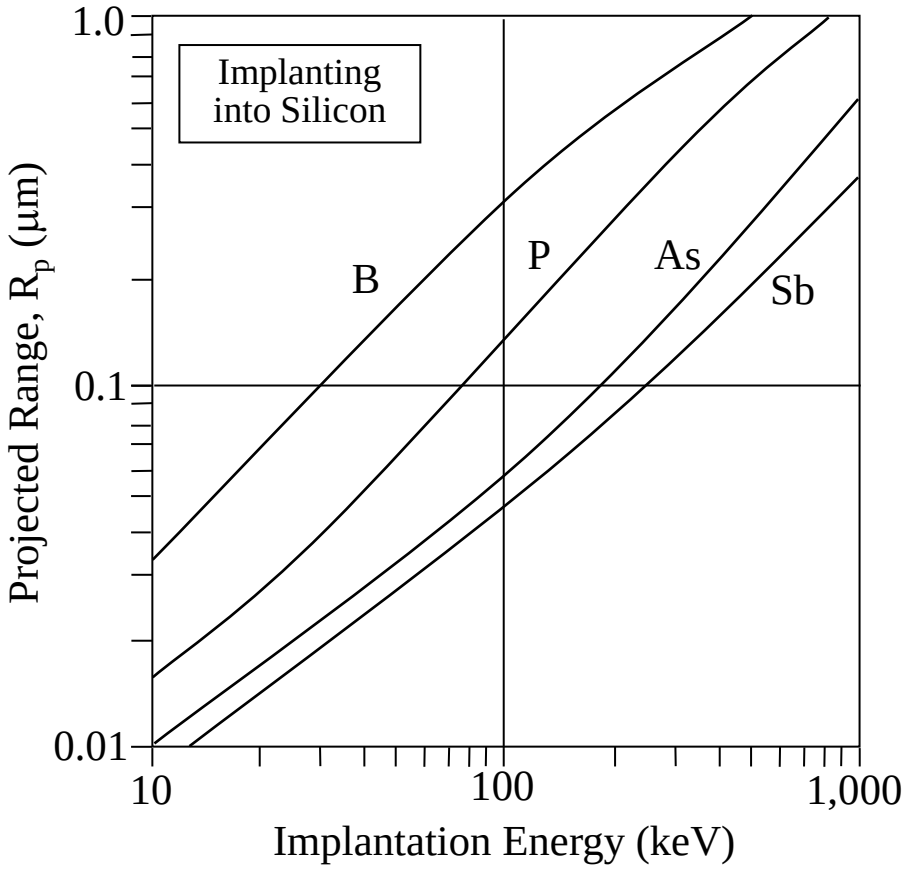


Figure 17.7

Projected Range Chart

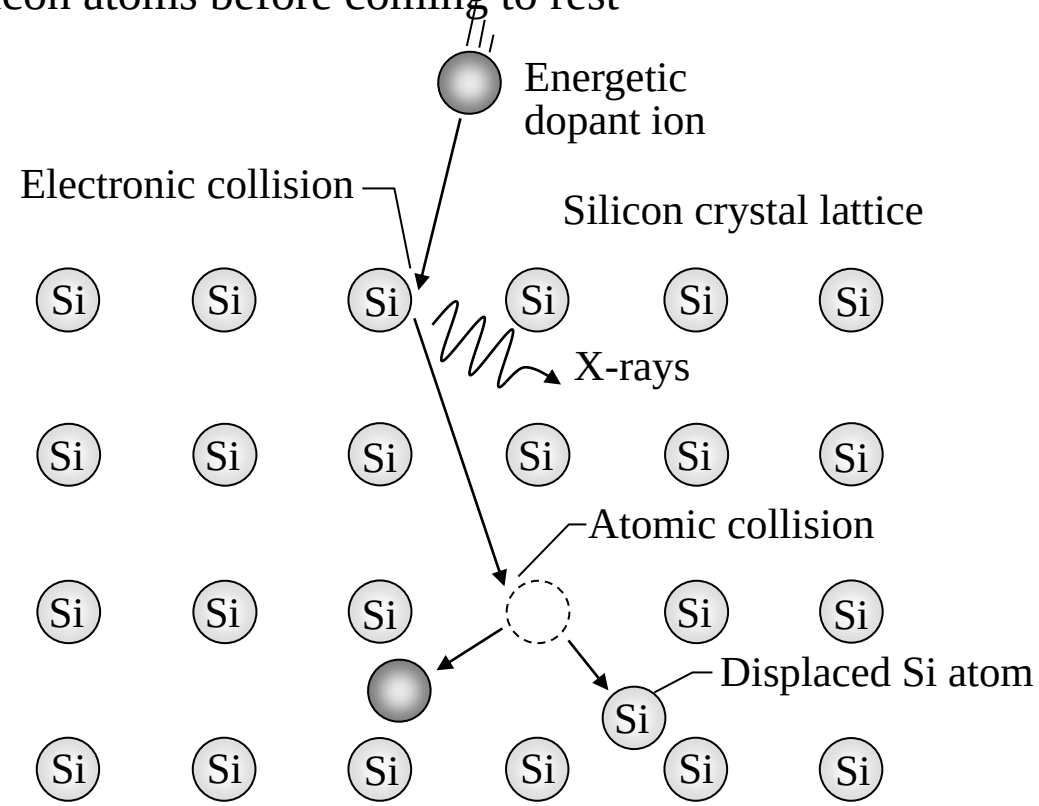


Redrawn from B.El-Kareh, *Fundamentals of Semiconductor Processing Technologies*, (Boston: Kluwer, 1995), p. 388

Figure 17.8

Energy Loss of an Implanted Dopant Atom

- The implanted ions will travel some depth into the target wafer before they are brought to rest by energy loss due to collision with silicon atoms
- There are two energy loss mechanisms: electronic stopping and nuclear stopping
- Electronic stopping: caused by interactions with the target electrons (child jump into plastic ball pool)
- Nuclear stopping: collision between atoms (billiard ball)
- Depending on the ion mass and energy, an implanted atom can displace as many as 10000 silicon atoms before coming to rest



Crystal Damage Due to Light and Heavy Ions

- A light dopant atom glances off silicon atoms with little energy transfer
- A heavy ion has a large energy transfer each time

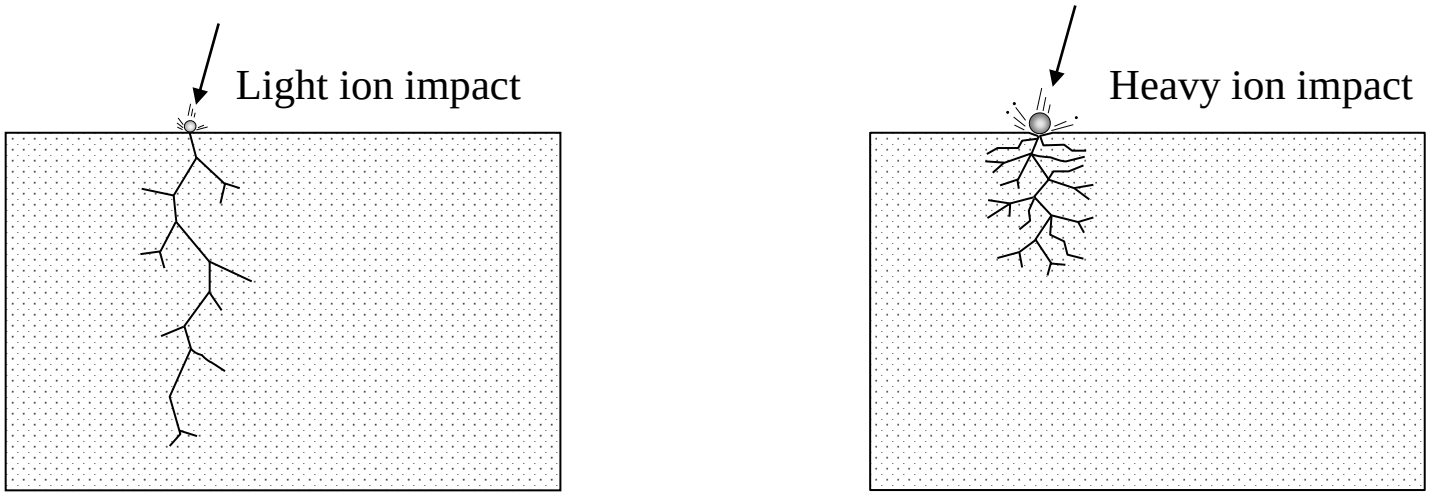


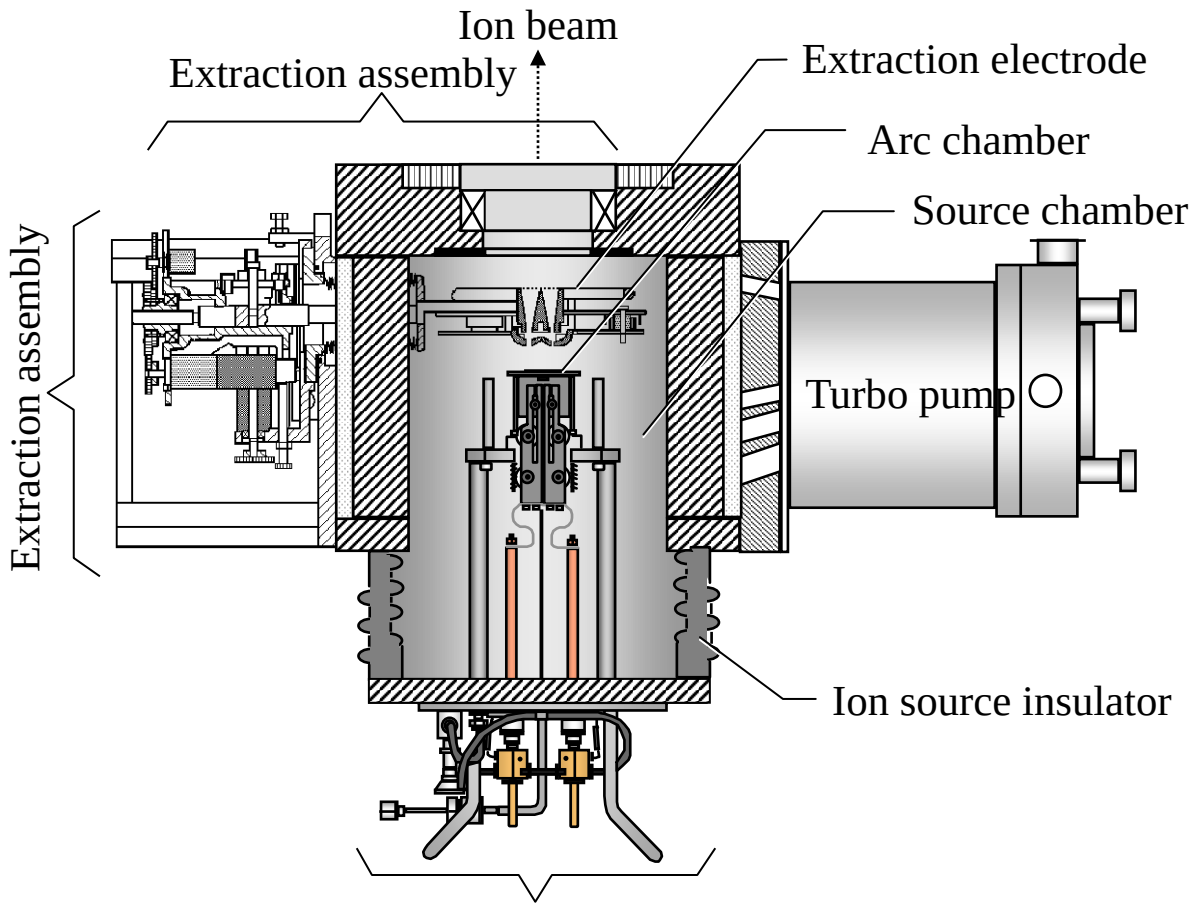
Figure 17.10

Ion Implanters

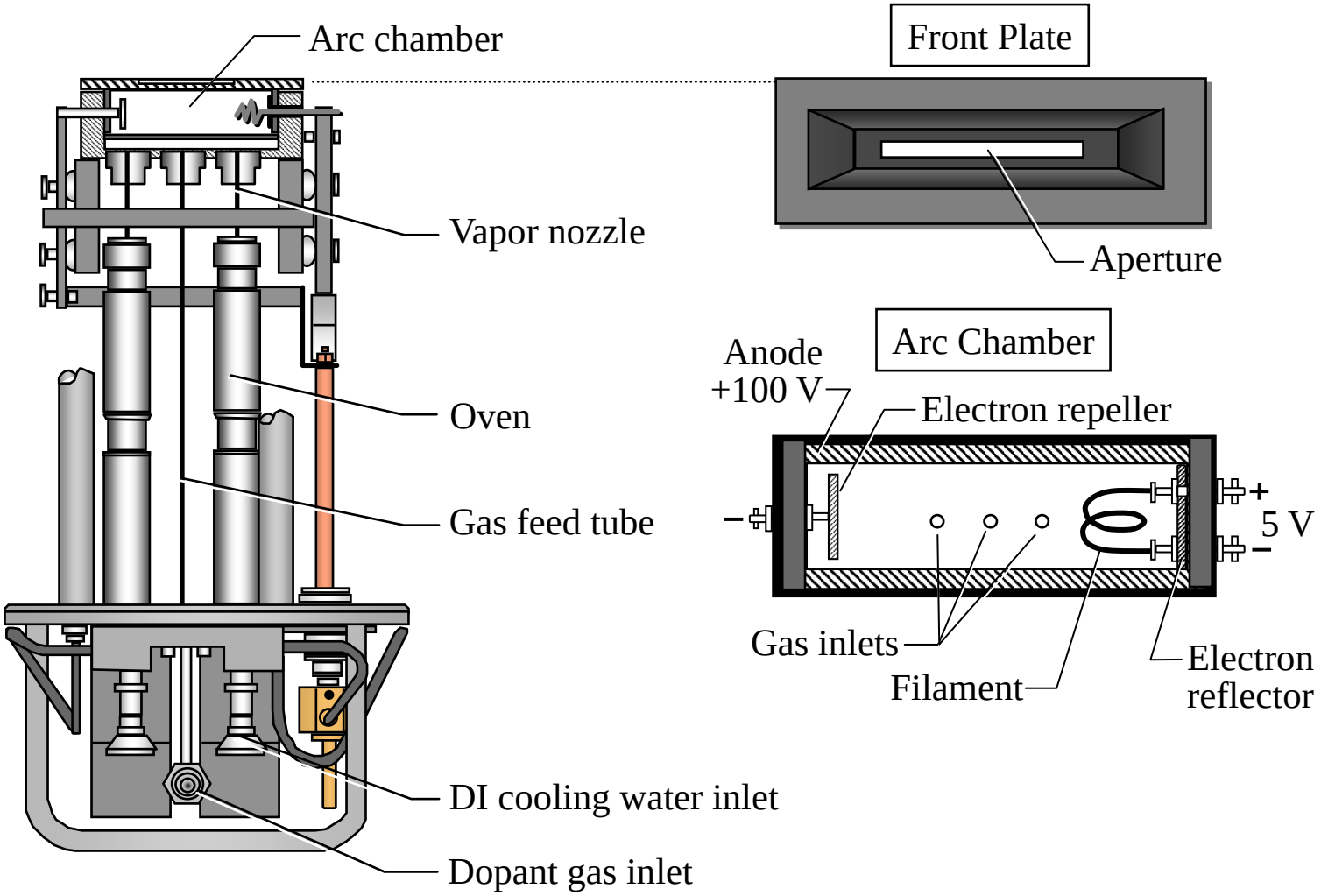
- Ion Source
- Extraction and Ion Analyzer
- Acceleration Column
- Scanning System
- Process Chamber
- Annealing
- Channeling
- Particles

Schematic of Ion Source Chamber

- The ion source and extraction assemblies are generally mounted in the same vacuum chamber
- Extraction assembly uses the electric field of a negative high voltage to draw the positive ions out of ion source



Schematic of Bernas Ion Source

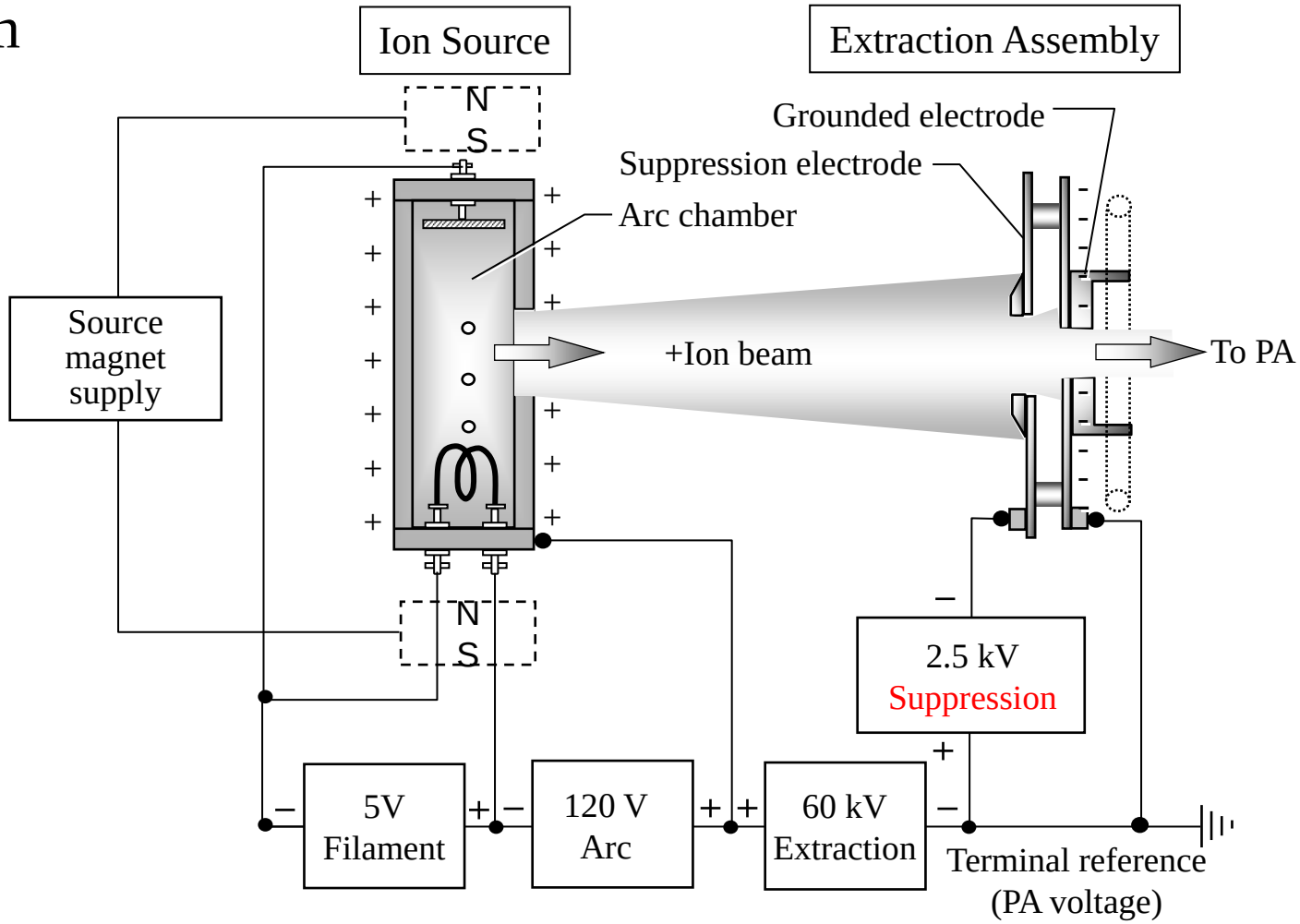


Ion Source

- Because of their electrical charge, ions can be controlled and accelerated with electric and magnetic fields
- Typically ions are produced by ionization of molecules
- The gas is packaged in a relatively small cylinder and diluted with hydrogen to reduce the risks of leakage
- Ions are generated in the ion source by bombarding the feed gas atoms with ***electrons***
- Electrons are produced by hot tungsten filament source
- An external source magnet to increase ionization and to stabilize the plasma
- Bombardment of electrons breaks up the gas, BF_3 is broken up into many different species, such as B^+, B_{10}^+, B_{11}^+, BF^+, BF_2^+, F^+, and F_2^+
- The B^+ will be selected through the analyzer magnet

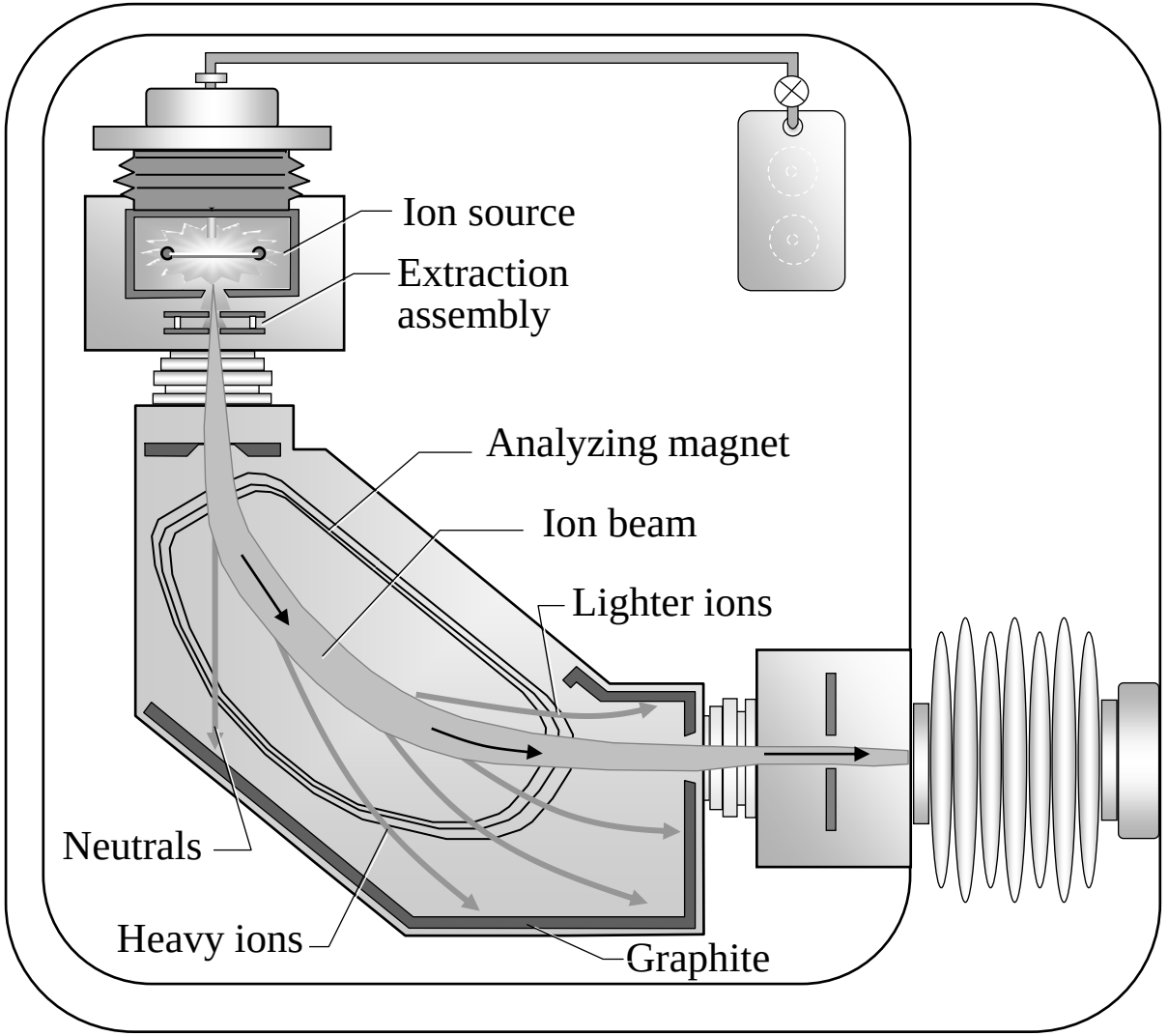
Interaction of ion Source and Extraction Assemblies

- Collects all positive ions created inside the ion source and forms them into a beam
- A negative biased suppression electrode is used to focus the in beam

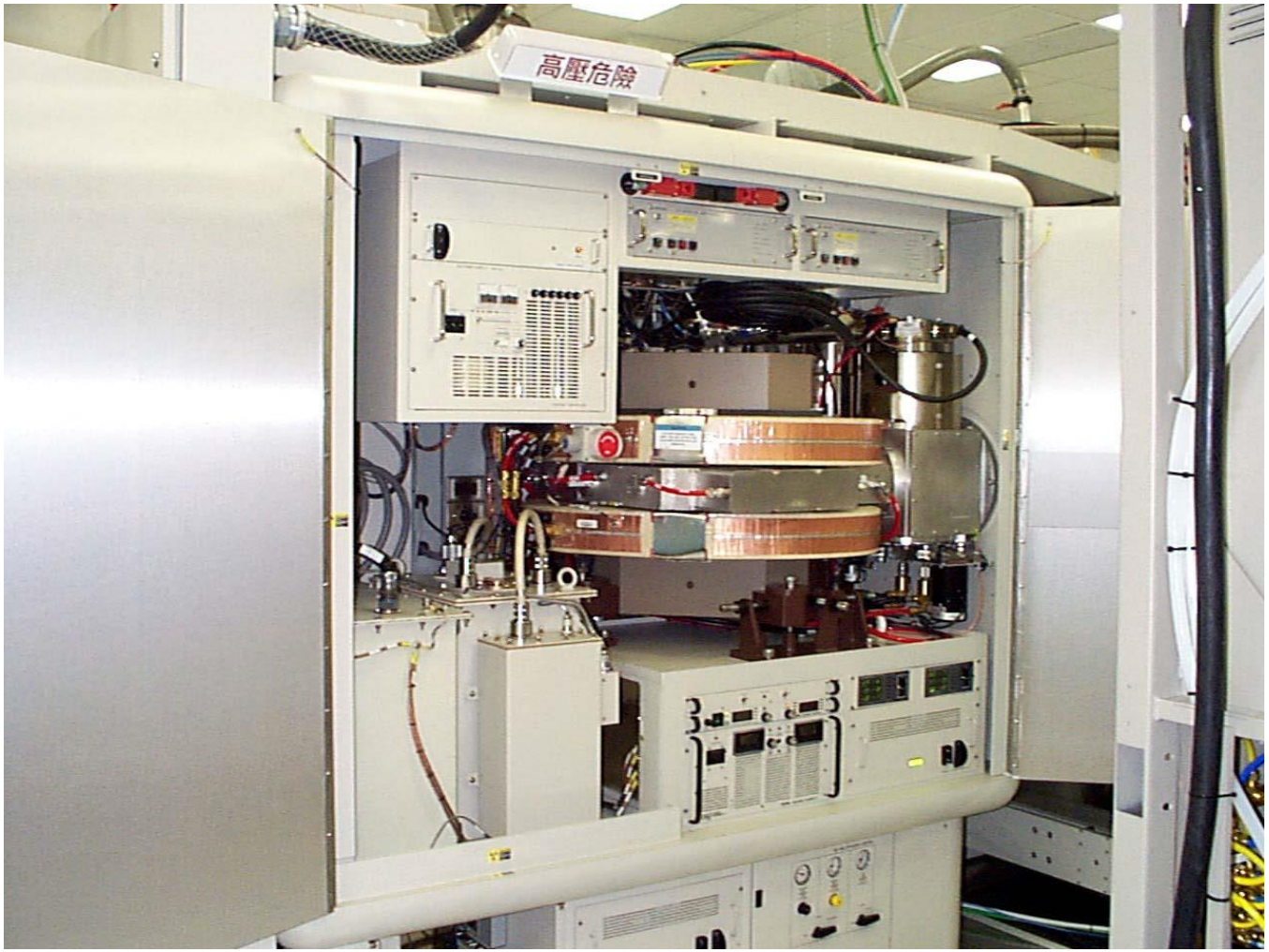


Analyzing Magnet

- The radius of the arc formed by the ion depends on the mass, speed, the magnetic field, and ion's charges, $r = \frac{mv}{qB}$



Ion Implanter Analyzing Magnet



Photograph courtesy of Varian Semiconductor, VIISion 80 analyzer side

Photo 17.2

Acceleration Column

- To achieve additional ion acceleration beyond the analyzer, positive ions are accelerated in an electric field inside an acceleration column
- High current and low energy is needed for shallow junction, a beam deceleration is used

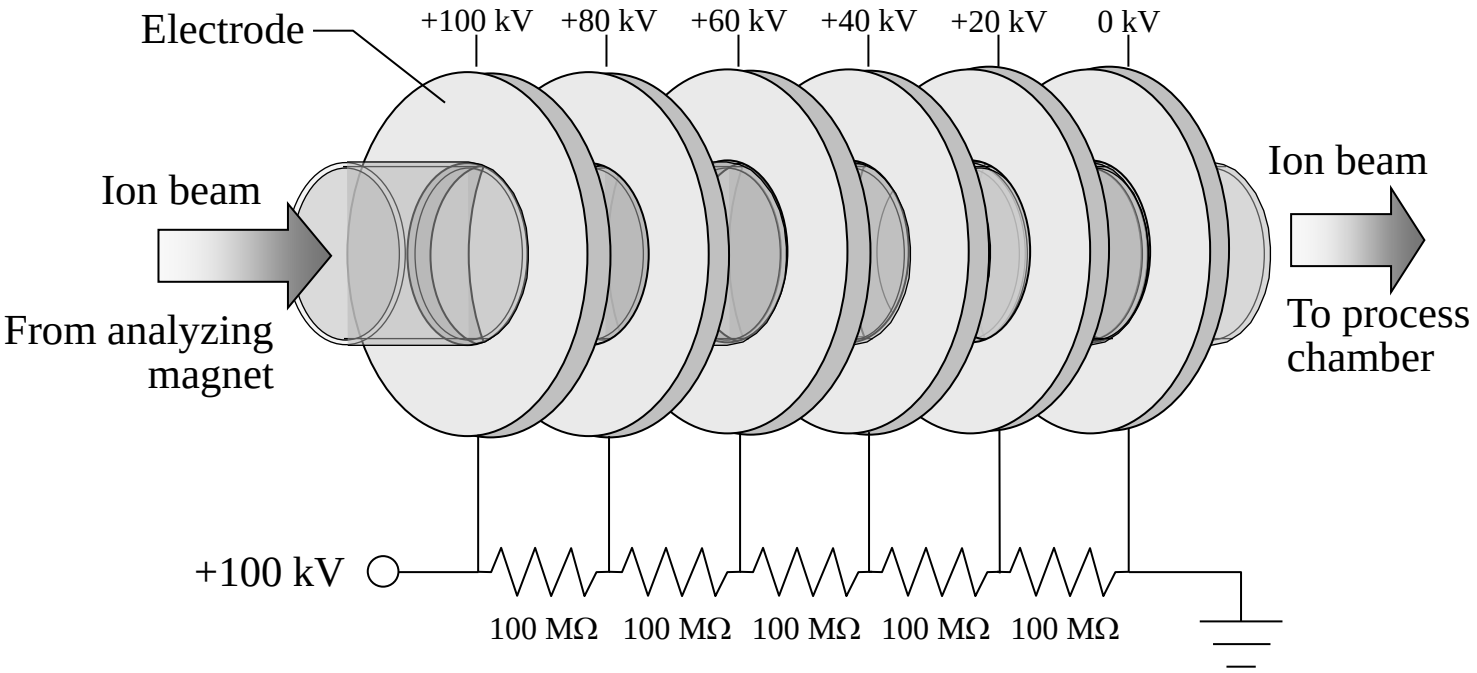
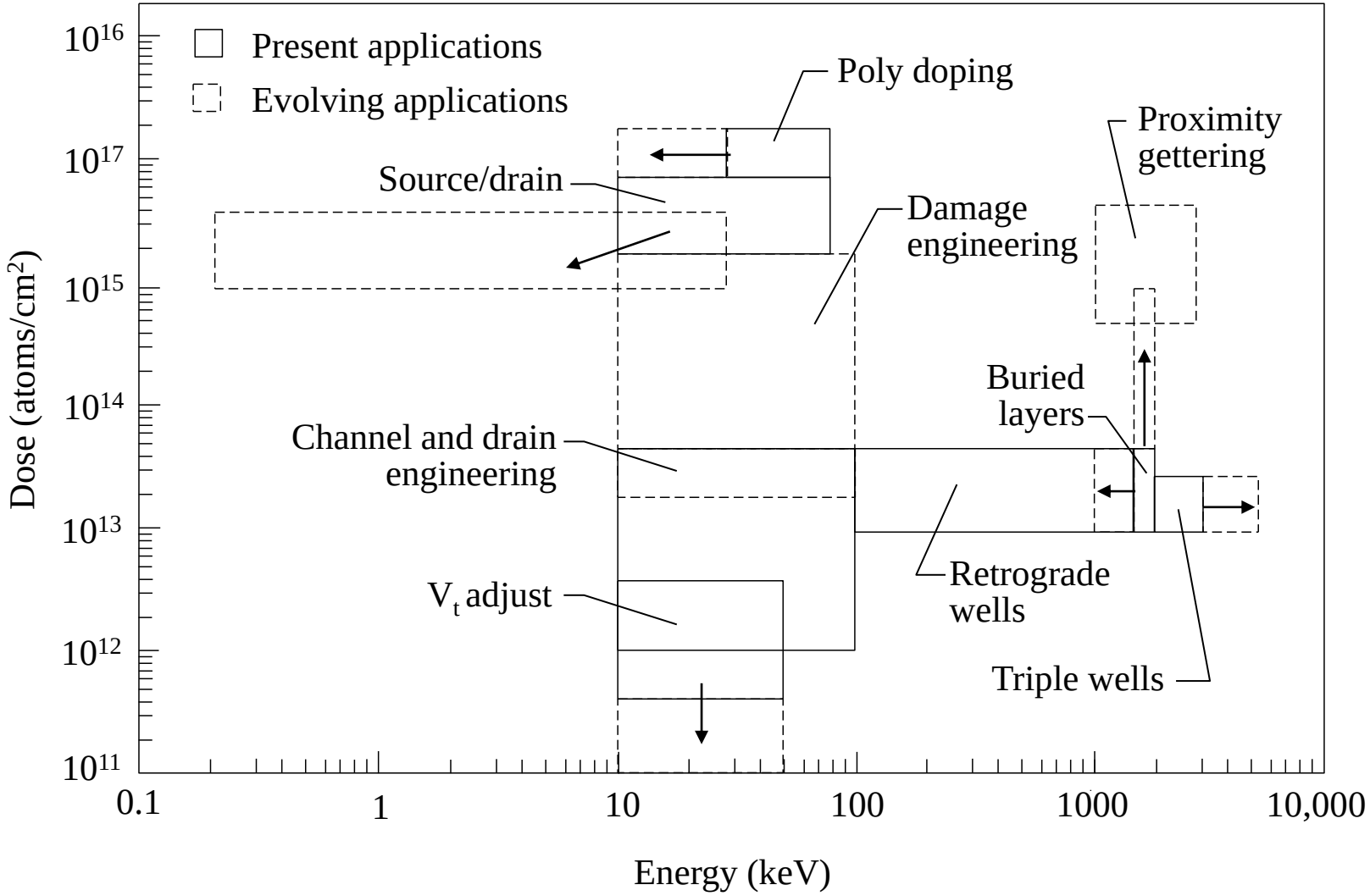


Figure 17.15

Dose Versus Energy Map



Used with permission from Varian Semiconductor Equipment

Figure 17.16

Linear Accelerator for High-Energy Implanters

- A traditional bending magnet is located at the end of the linear accelerator that serves as an energy analyzer to ensure that a pure, mono-energetic beam is formed for wafer implant

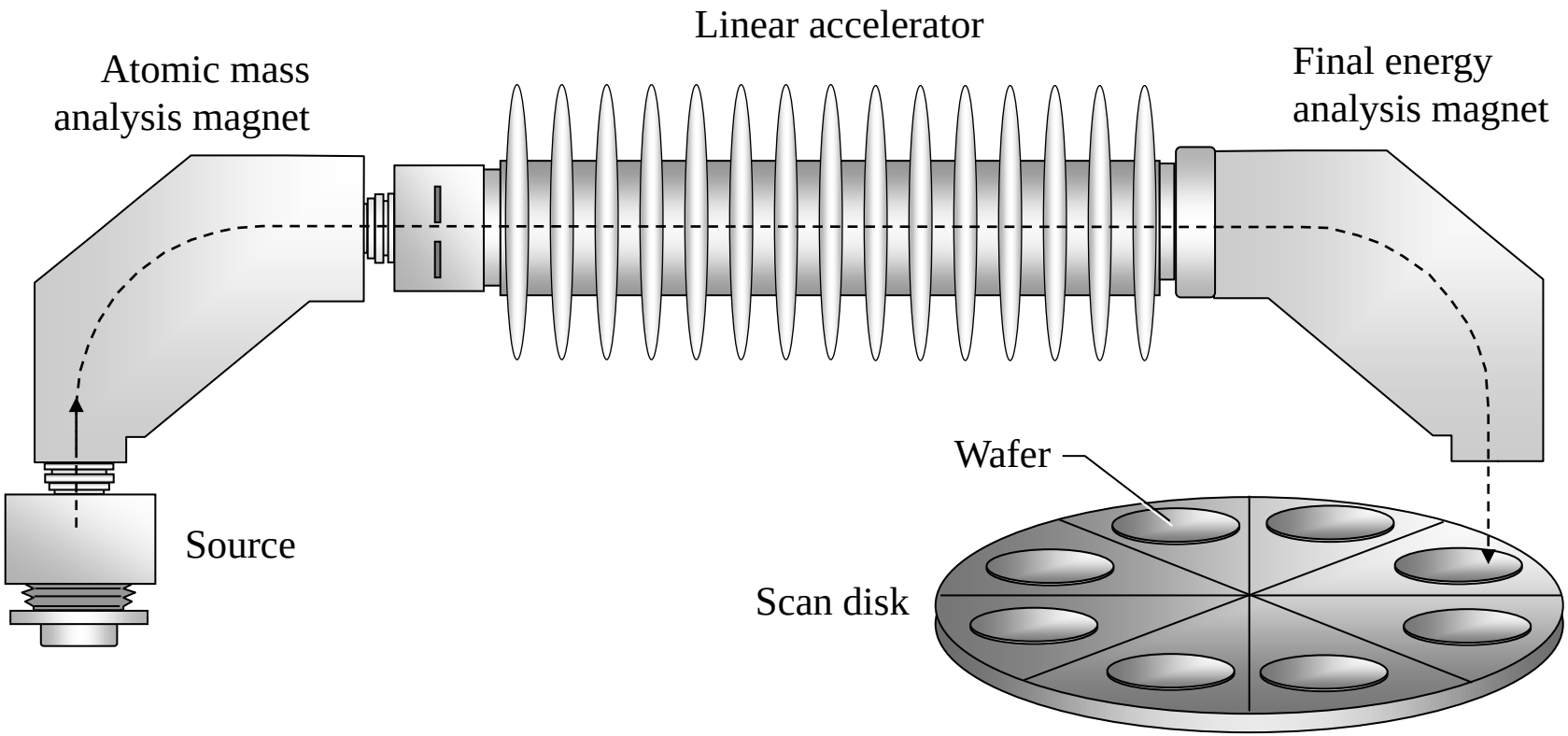
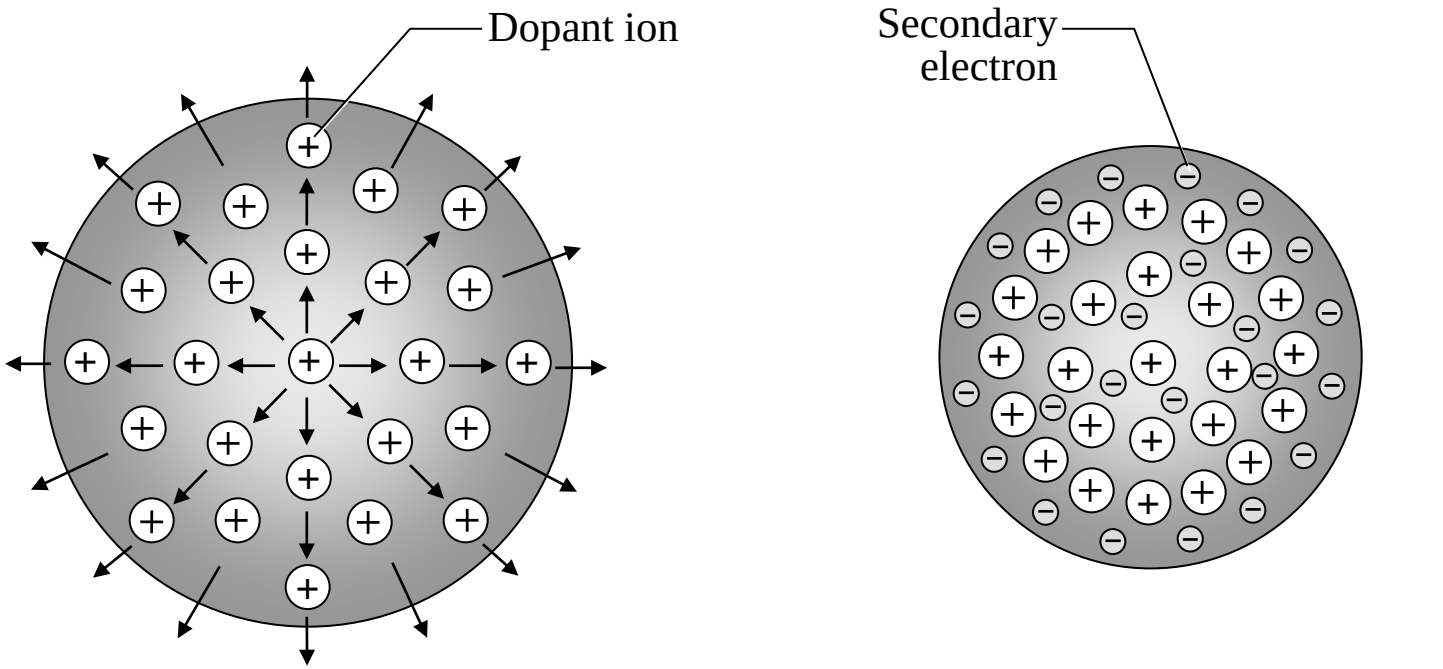


Figure 17.17

Space Charge Neutralization

- Secondary electrons are generated when high-energy dopant ion strike a surface as they pass along the beam line
- The trapped electrons serve to neutralize the beam and prevent or reduce beam blow-up



Cross section of beam blow-up

Cross section of beam with space charge neutralization

Figure 17.18

Neutral Beam Trap

- Neutral ions are formed in the beam when a dopant ion gains an electron by colliding with a residual gas molecule
- Since the neutral ions will not deflected by the electrodes at the bend, they travel straight and collide with a grounded collector plate

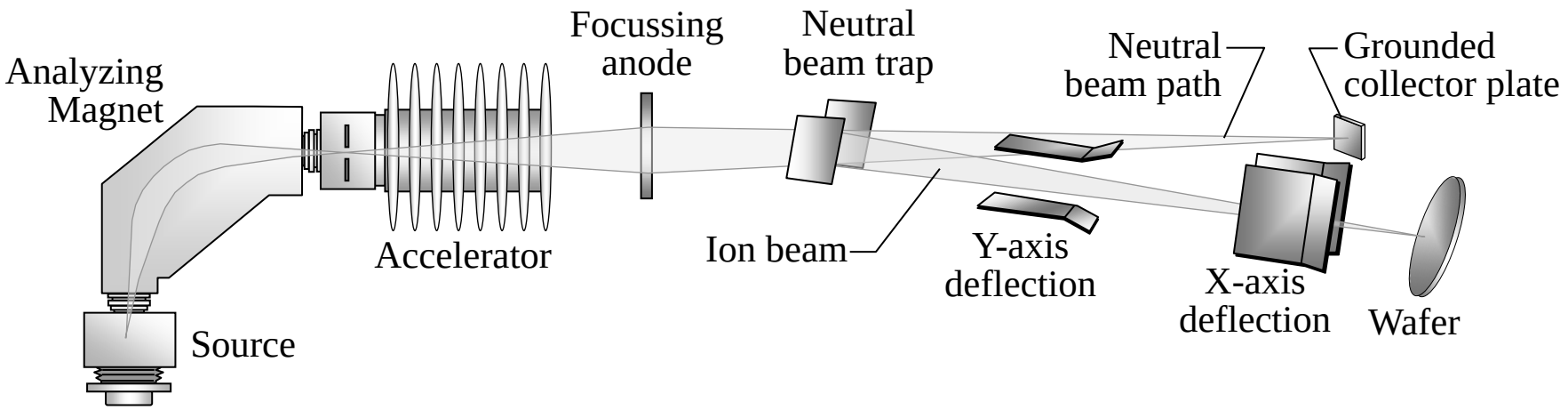


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Figure 17.19

Electrostatic Ion Beam Scanning of Wafer

- Focused beam is small, 1 cm^2 for medium implanters, and 3 cm^2 for high-current implanters
- Wafers scanning is done either by moving the beam over a stationary wafer (low- to medium-current implanter) or moving the wafers through a stationary beam (high-current implanter)

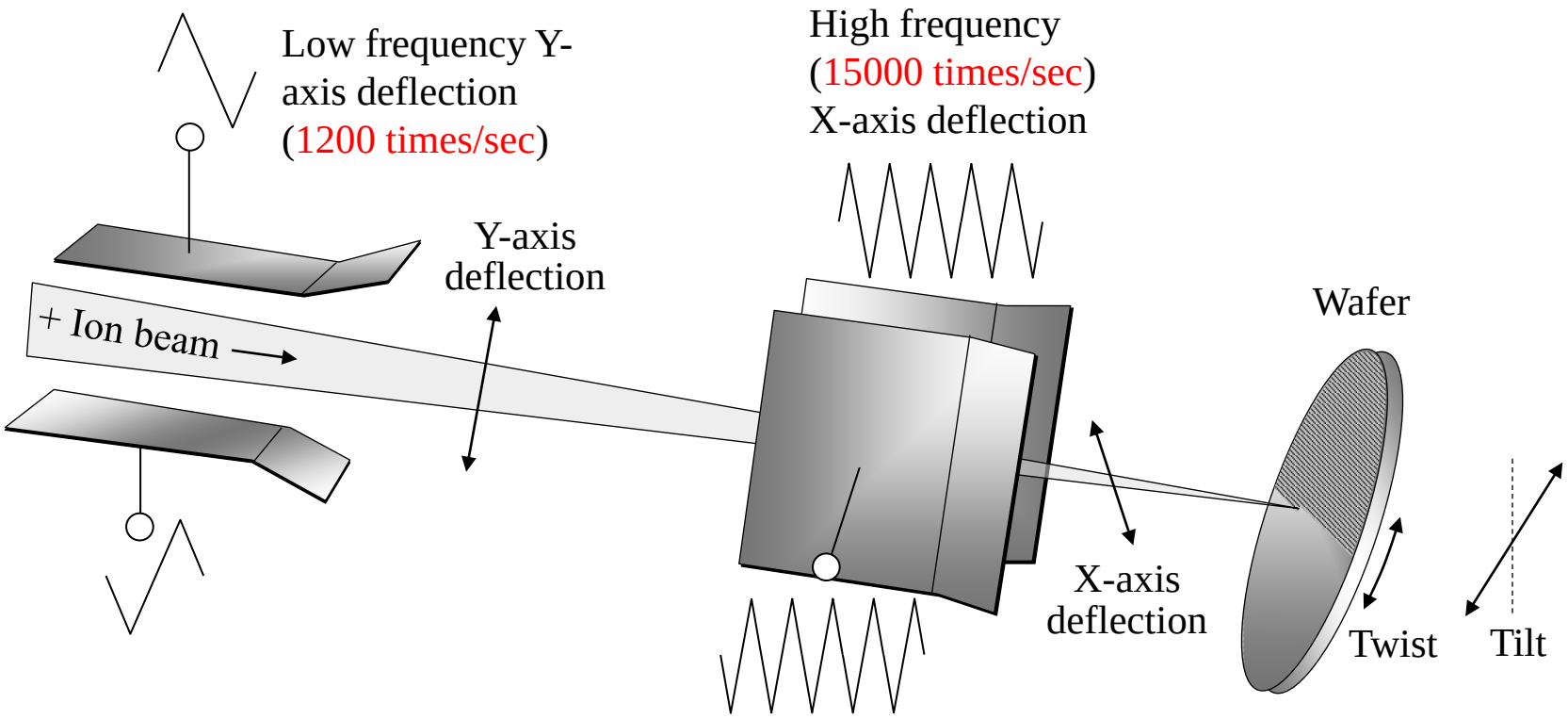
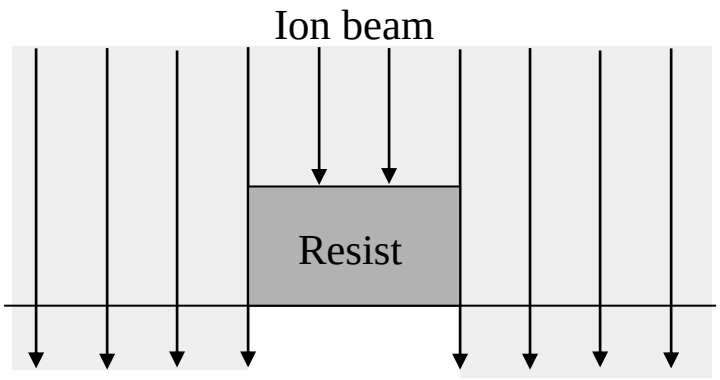


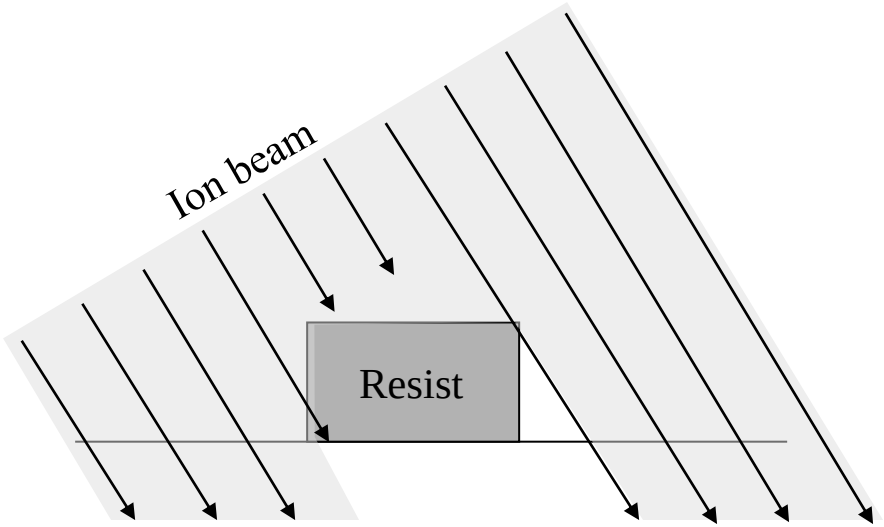
Figure 17.20

Implant Shadowing

- When tilting, an undesirable shadowing from the mask material that partially blocks implantation of the ion beam



a) Mechanical scanning with no tilt

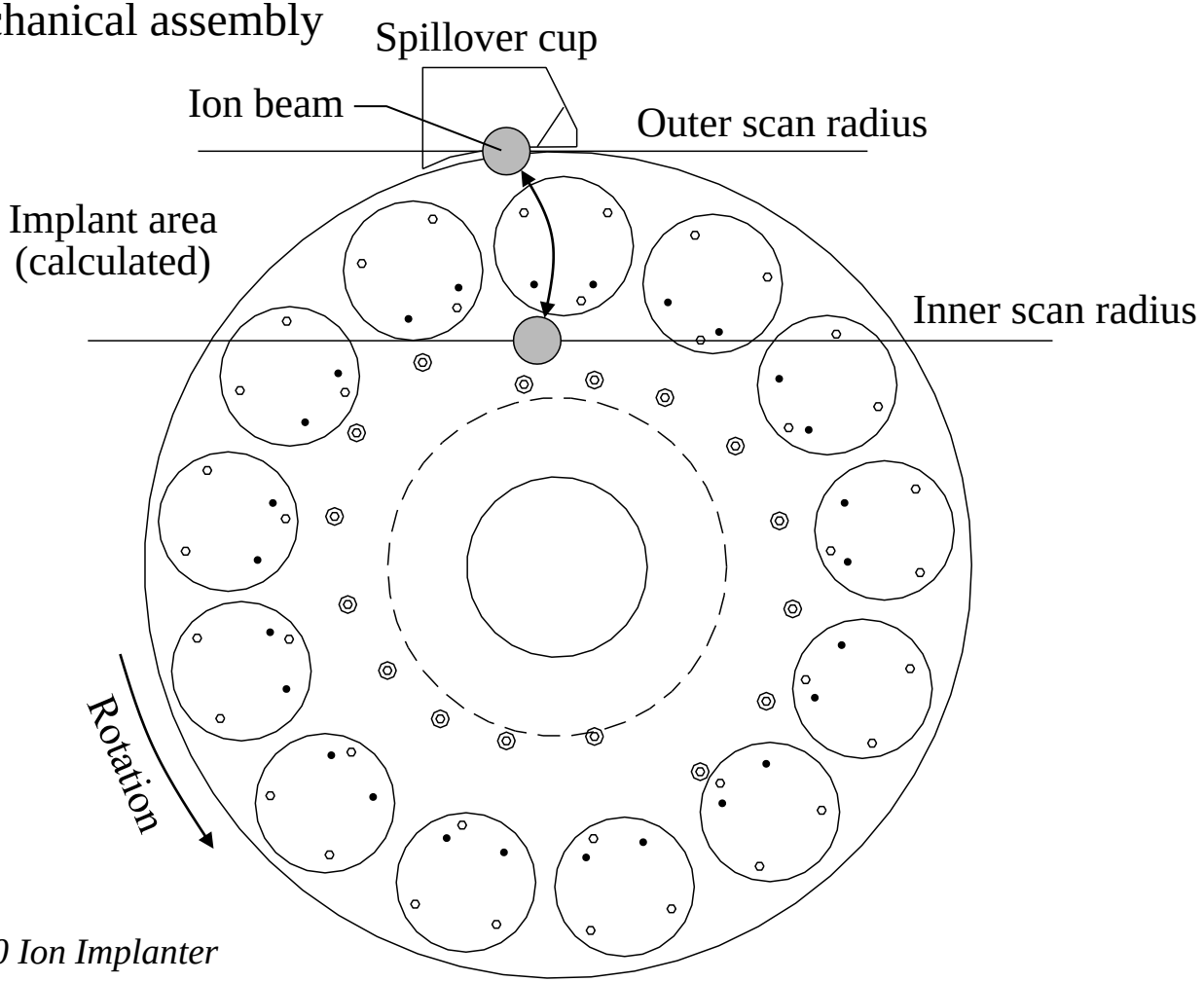


b) Electrostatic scanning with normal tilt

Figure 17.21

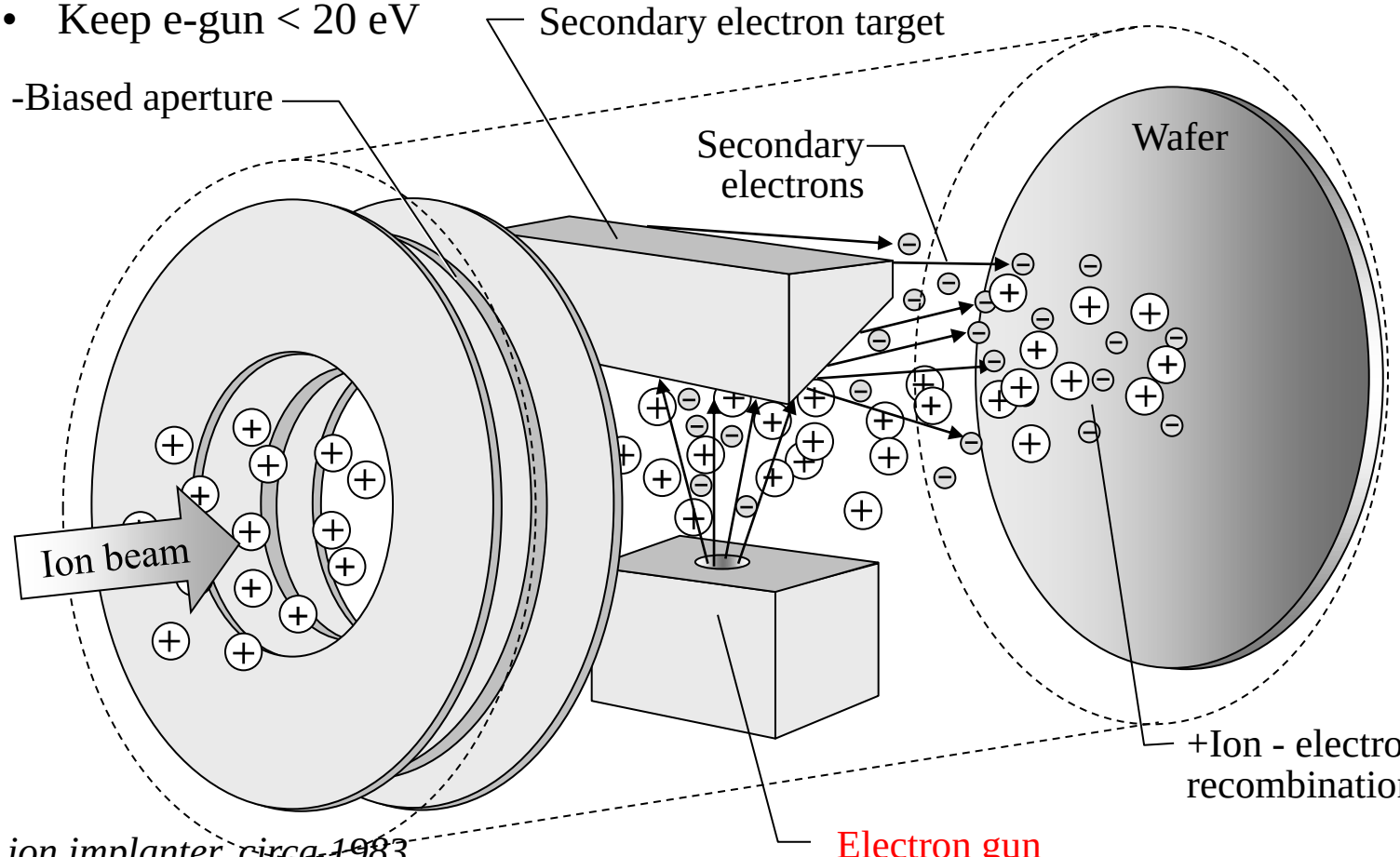
Mechanical Scanning of Implanted Wafers

- Used for high-current implanters because electrostatic beam deflection is difficult at high currents and energies
- Rotating at 1000-1500 rpm
- Reducing heat over a large area, high throughput, but more particles generated from the mechanical assembly



Electron Shower for Wafer Charging Control

- The energy of the ion beam striking the wafer is converted into heat
- Usually controlling the wafer < 50˚C, PR will blister and flake off > 100˚C and become difficult to remove
- Some positive ions accumulate in the masking layer, causing wafer charging
- Charging: causing beam blow-up, damage a surface oxide
- Keep e-gun < 20 eV



Eaton ion implanter, circa 1983

Plasma Flood to Control Wafer Charging

- The main advantage of plasma flood over the electron shower is no high-energy electrons are generated in the plasma

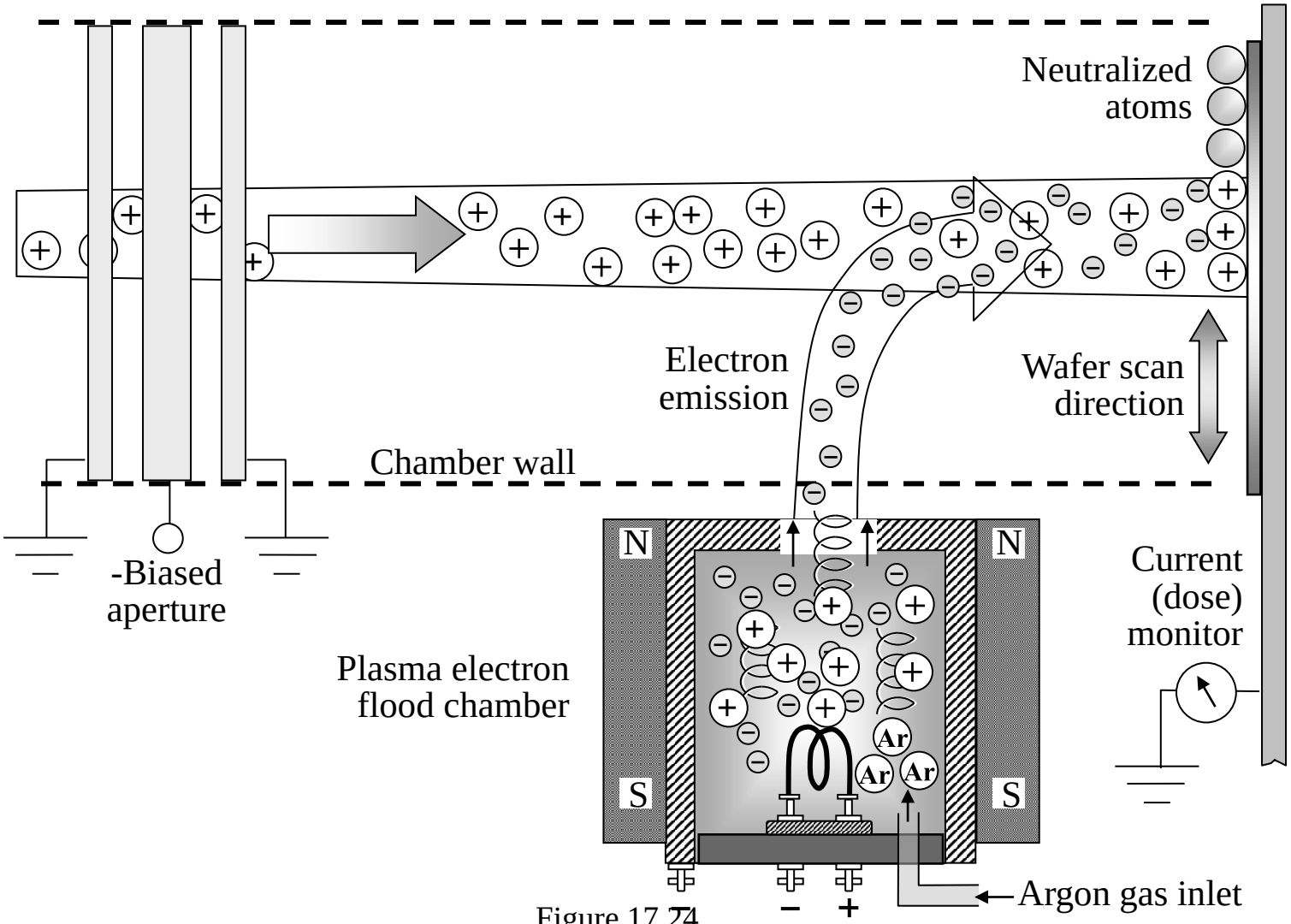


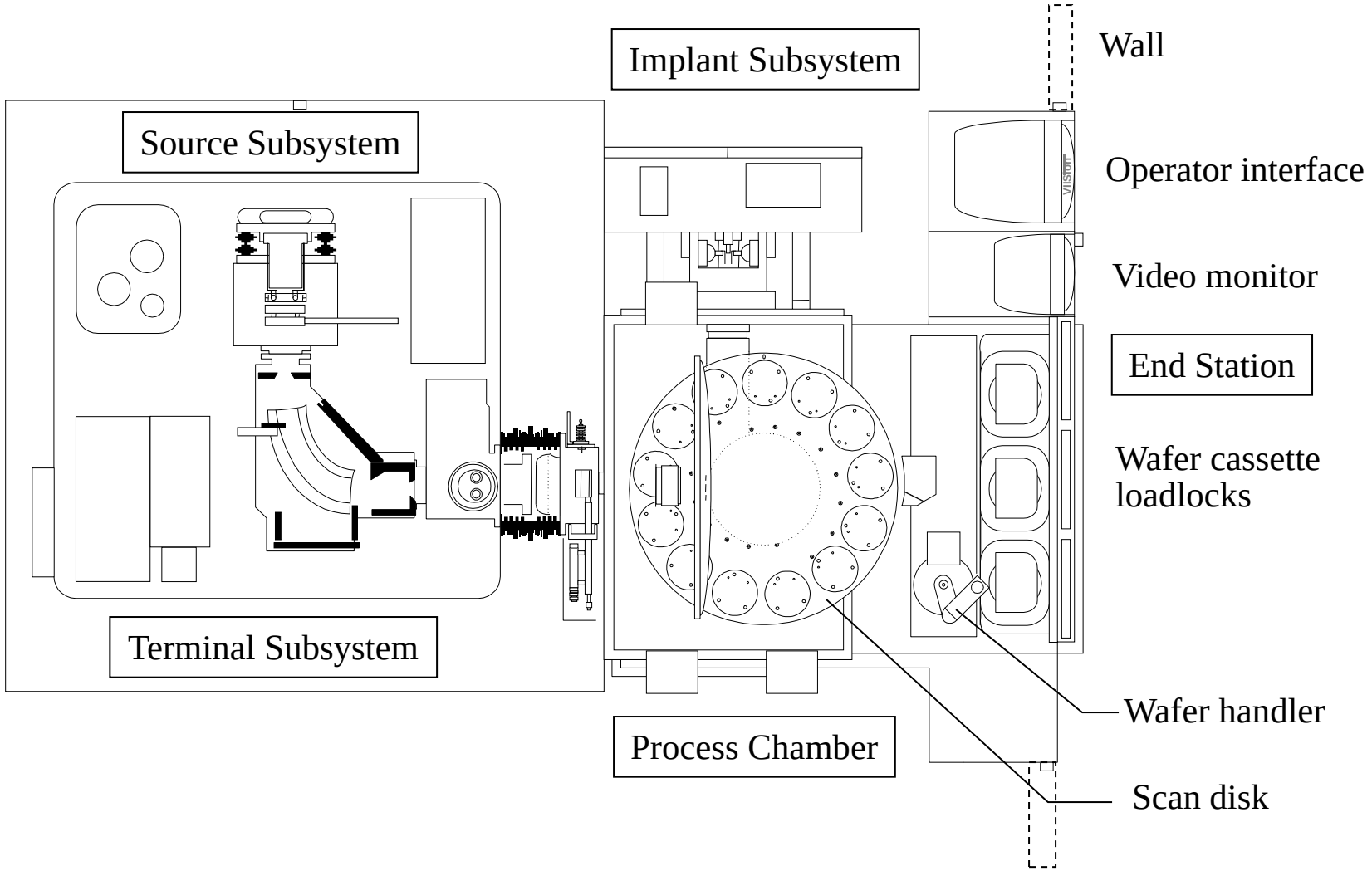
Figure 17.24

End Station for Ion Implanter

Photograph provided courtesy of International SEMATECH

Photo 17.3

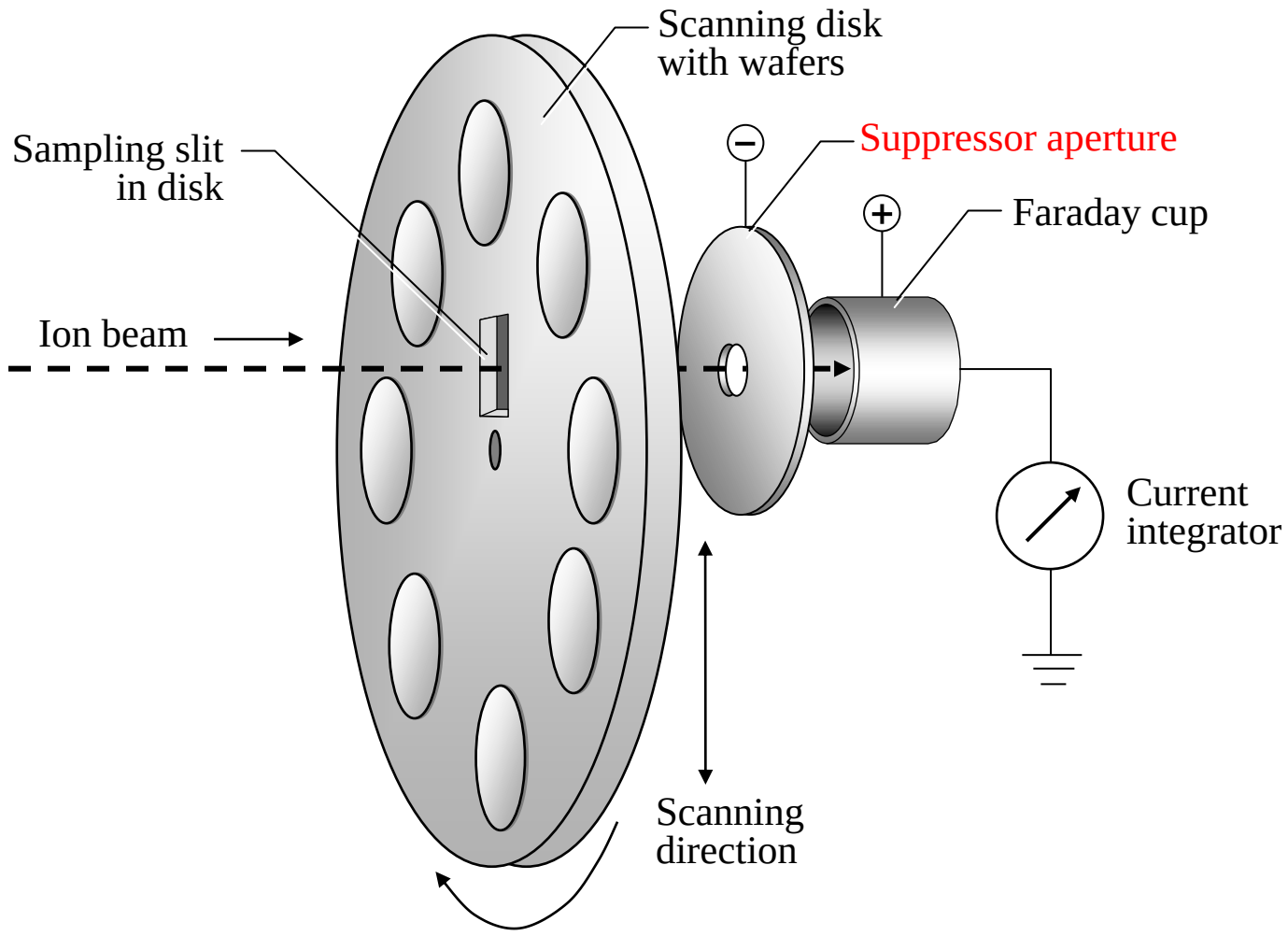
Wafer Handler for an Implant Process Chamber



Used with permission from Varian Semiconductor Equipment, VIISion 200 Ion Implanter

Figure 17.25

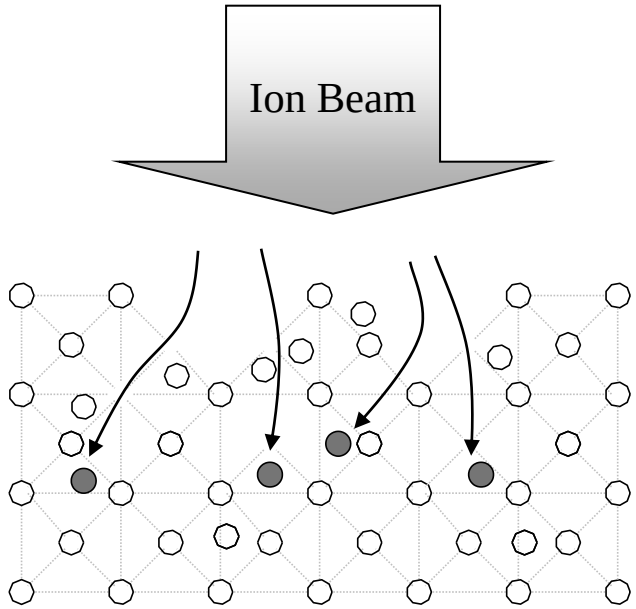
Faraday Cup Beam Current Measurement



Redraawn from S. Ghandhi, VLSI Fabricaton Principles: Silicon and Gallium Arsenide, 2d ed., (New York: Wiley, 1994), p. 417

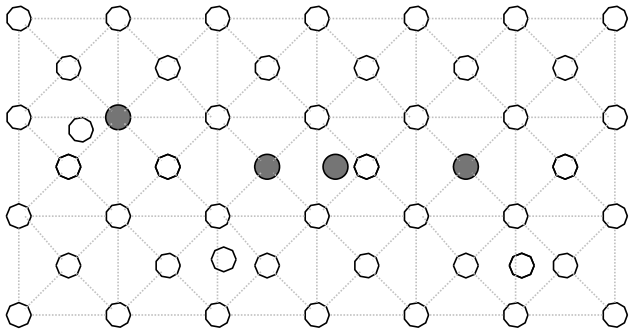
Figure 17.26

Annealing of Silicon Crystal



a) Damaged Si lattice during implant

Repaired Si lattice structure and activated dopant-silicon bonds

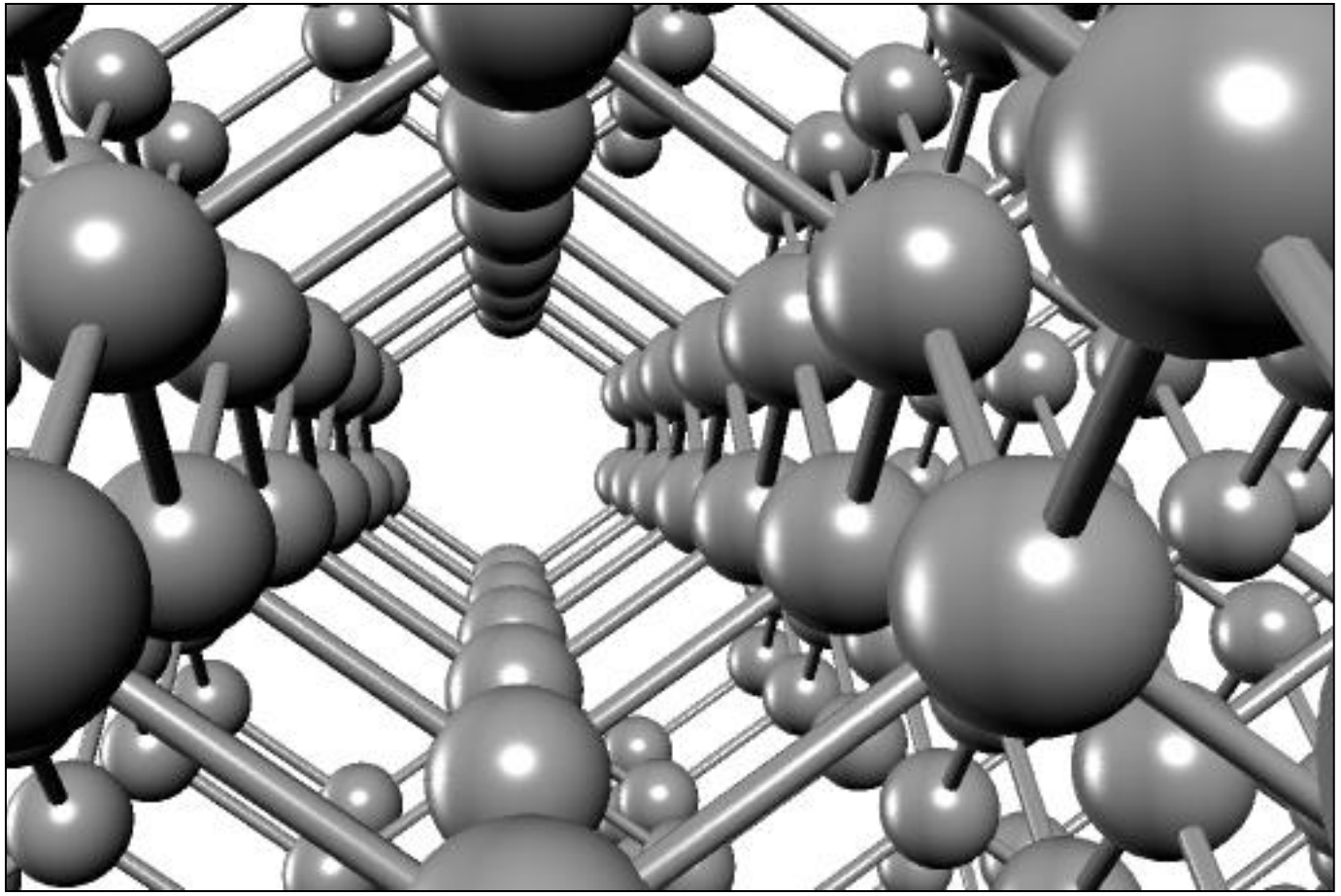


b) Si lattice after annealing

- Using Furnace or RTA, hot-wall furnace using high temperature causes extensive dopant diffusion and is undesirable
- RTA minimizes a phenomenon known as transient enhanced diffusion, to achieve acceptable junction depth control in shallow implants (~150°C/sec)

Figure 17.27

Silicon Lattice Viewed Along <110> Axis

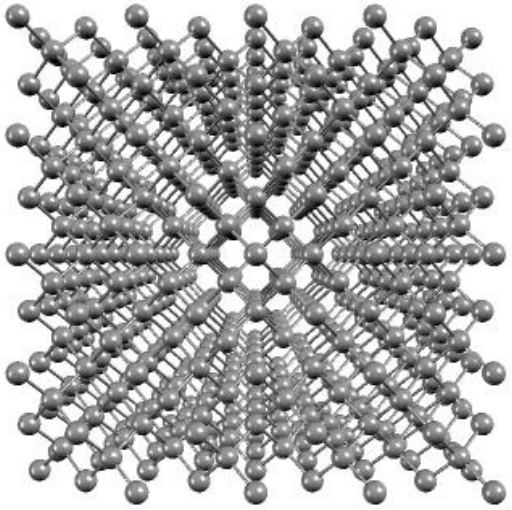


Used with permission from Edgard Torres Designs

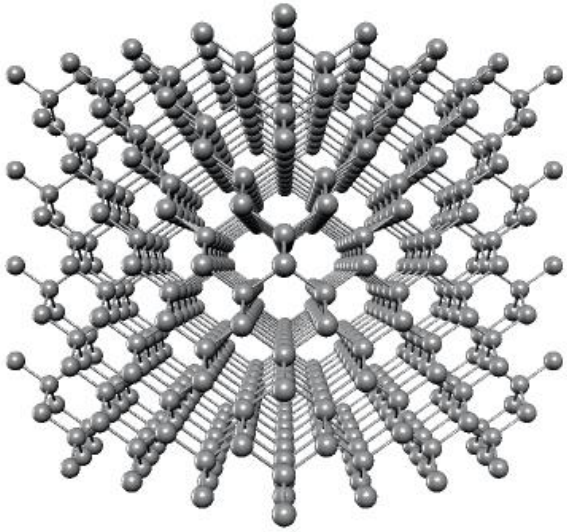
Figure 17.28

Ion Entrance Angle and Channeling

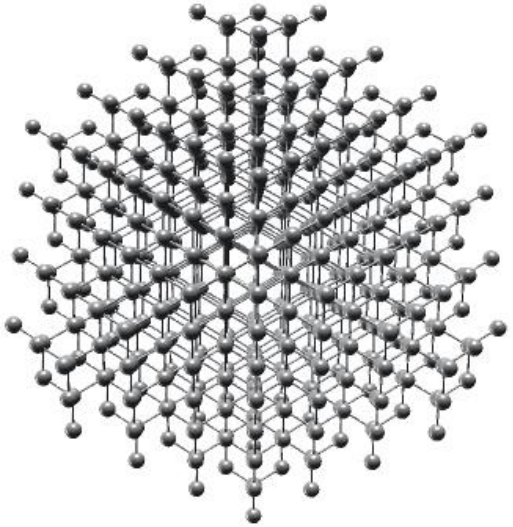
- Channeling occurs when the implanted ions are not slowed by collisions with silicon atoms and instead pass through the interstitial areas of the crystal
- There are four ways (a) wafer tilt, (b) screen oxide layer, (3) pre amorphization of the silicon , and (4) using dopant with greater amu's and lower diffusivity
- (a) Wafer tilt: the most widely used is 7° for (100)
- (b) Screen oxide (sacrificial oxide) randomization the directions of the ions as they enter the silicon lattice to reduce the channel effect
- (c) Pre-amorphization: using Ge or Si to destroy the single structure in a thin layer of the silicon
- (d) Using BF_2, not B



<100>



<110>



<111>

Implantation Damage from Particulate Contamination

- A particle located on the wafer surface can block the incident beam and cause improper implantation

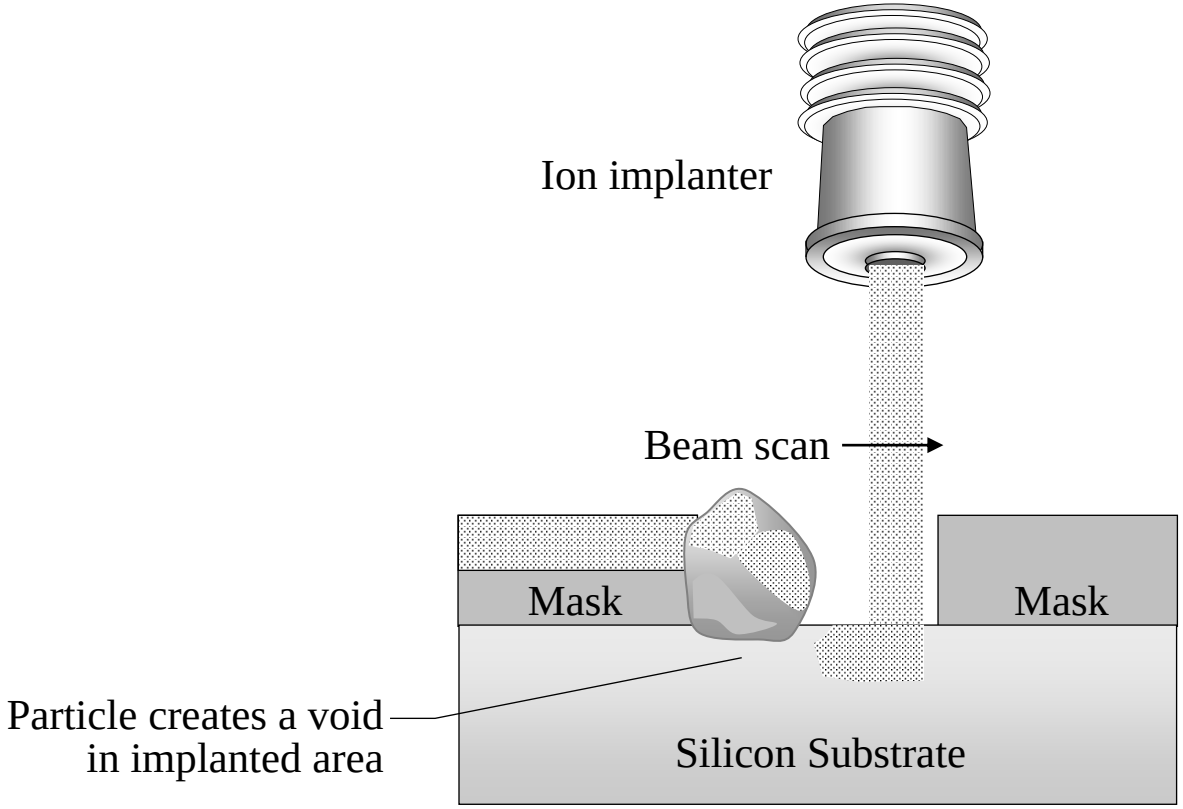


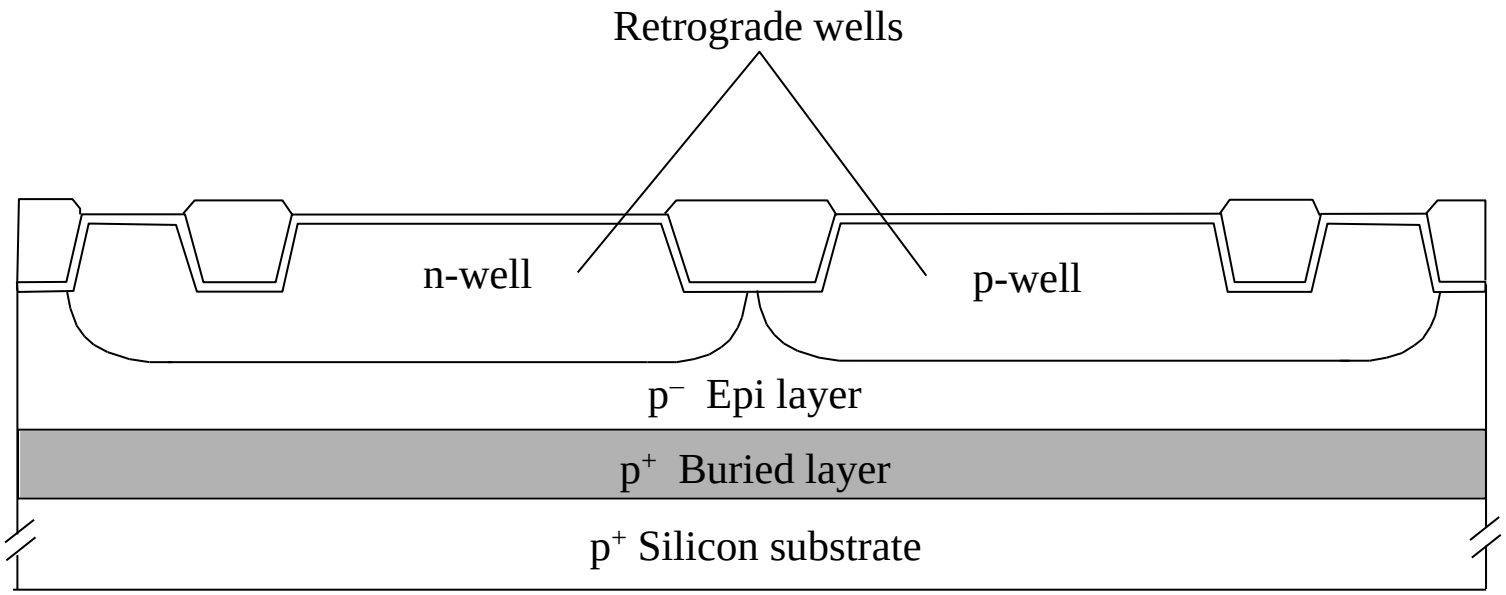
Figure 17.30

Ion Implant Trends in Process Integration

Examples of Different Implant Processes

- Deep buried layers
- Retrograde wells
- Punchthrough stoppers
- Threshold voltage adjustment
- Lightly doped drain (LDD)
- Source/drain implants
- Polysilicon gate
- Trench capacitor
- Ultra-shallow junctions
- Silicon on Insulator (SOI)

Buried Implanted Layer



- A triple well has a buried implanted well layer beneath the standard n- and p-retrograde wells for improved device performance and packing density

Figure 17.31

Retrograde Well

- Diffusion the dopant profile always has the maximum concentration at the silicon surface
- Retrograde well has the peak implanted dopant profile buried at a certain depth
- To solve the latch-up problem in CMOS

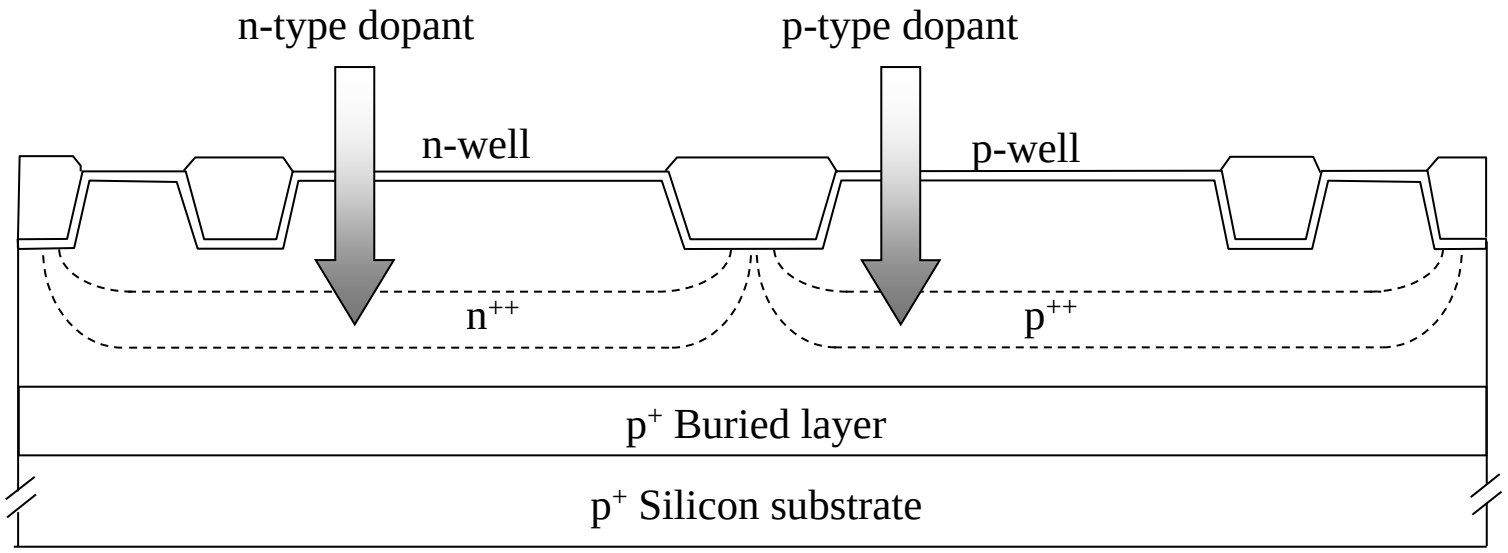


Figure 17.32

Punchthrough Stop

- It occurs when the channel length is reduced for scaling and high electric fields occur at the drain end of the channel
- Using boron implant for n-channel and phosphorus for p-channel

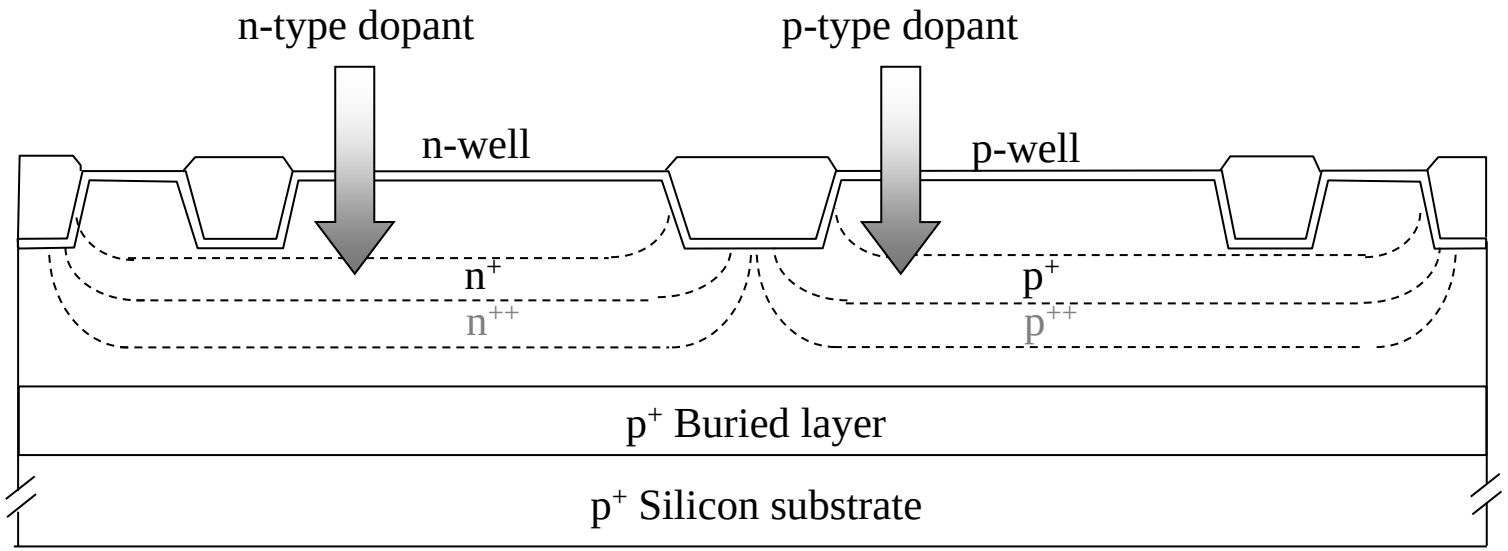


Figure 17.33

Implant for Threshold Voltage Adjustment

- The threshold voltage, V_{TH}, is the amount of voltage required to form the conductive channel between the source and drain that causes enhancement mode transistors to turn on
- For optimum device performance, a dopant is implanted beneath the silicon layer to adjust the channel region to the required dopant concentration: called the MOS gate threshold voltage implant adjustment

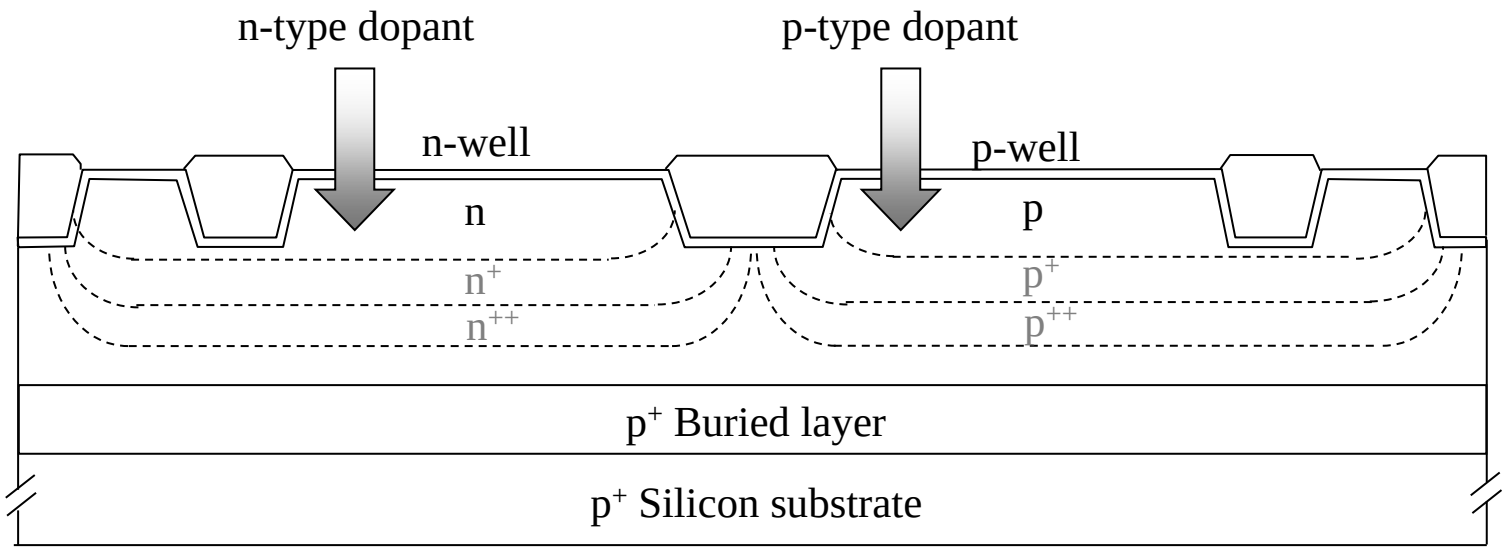
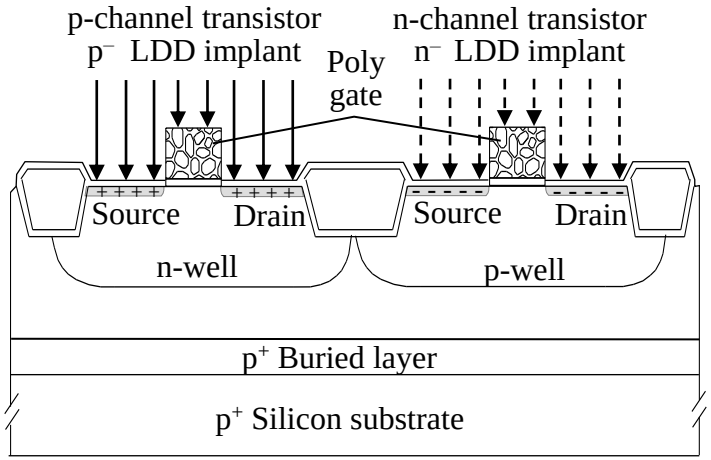


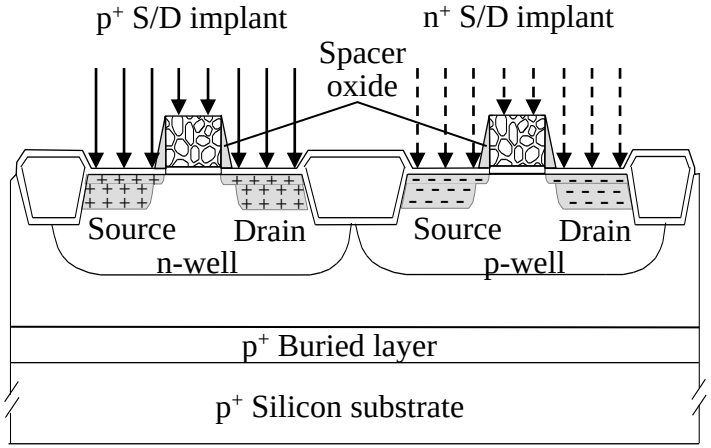
Figure 17.34

Source-Drain Formations

- Lightly doped drain (LDD, 10^{16}-10^{17} atoms/cm^3) is used to reduce electric field between the junction and channel region
- Electrons are accelerated in electric field, called hot electron, trapped in oxide, causing reliability problem
- S/D implant: 10^{20}-10^{21} atoms/cm^3
- Poly-Si gate is doped when S/D are implanted



a) p⁻ and n⁻ lightly-doped drain implants (performed in two separate operations)



b) p⁺ and n⁺ Source/drain implants (performed in two separate operations)

Figure 17.35

Dopant Implant on Vertical Sidewalls of Trench Capacitor

- The trench capacitor has replaced the planar storage capacitor because of the shrinking DRAM memory cell size
- To obtain sufficient capacitance, a dopant level of about 10^{19} atoms/cm^3 is placed in a very shallow layer into the vertical sidewall

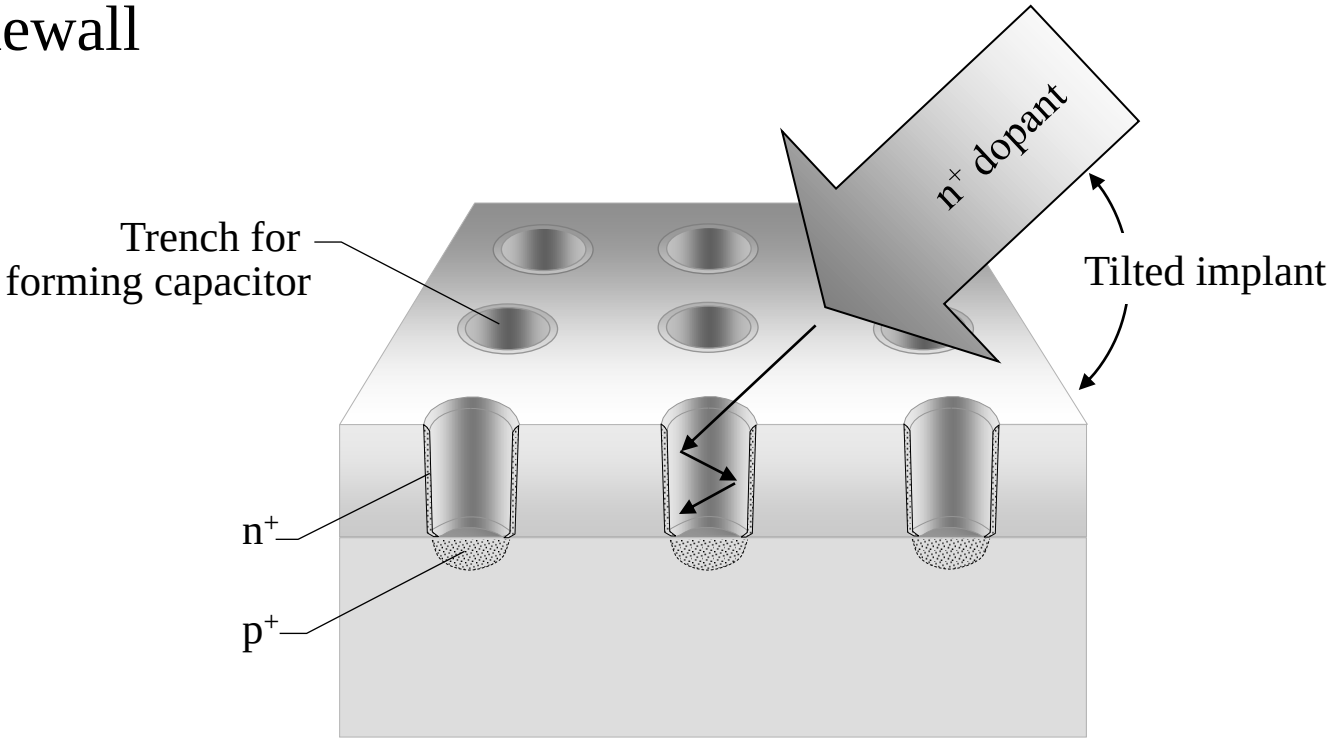


Figure 17.36

Ultra-Shallow Junctions

- To reduce short channel effect, the depth of S/D should be shallow
- Ultra shallow junctions are implanted using a high beam current, low-energy implanter
- The large mass forms an amorphous layer to assist in depth control by minimizing channeling
- Using BF_2, not B

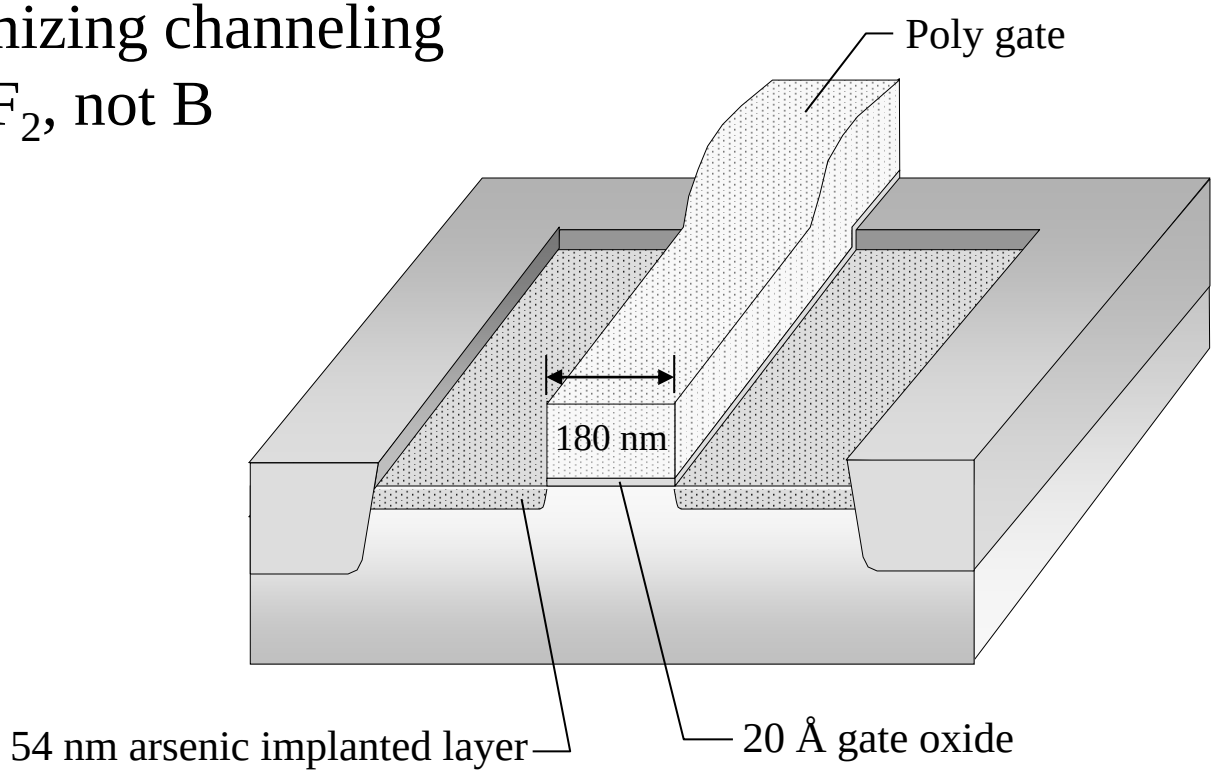
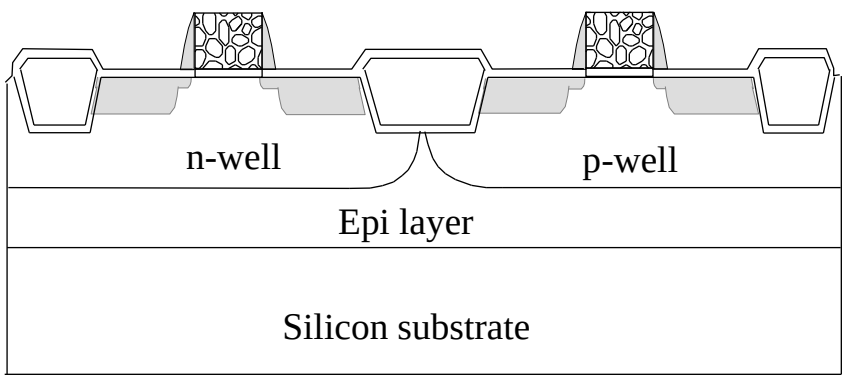


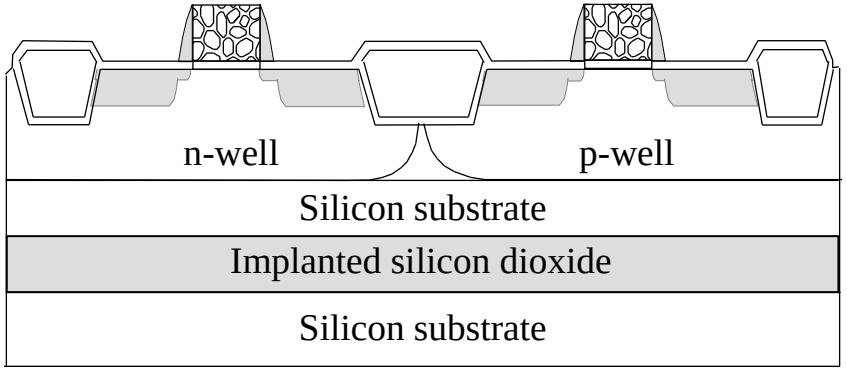
Figure 17.37

CMOS Transistors with and without SIMOX Buried Oxide Layer

- SOI technology is based on an insulator layer buried within the silicon that effectively isolates the devices on the silicon surface
- Advantages: complete elimination of latch up, reduced electric field, and reduced parasitic capacitance
- SIMOX: separation by Implanted Oxygen (200 keV, at 1300°C)



a) Common CMOS wafer construction



b) CMOS wafer with SIMOX buried layer

Figure 17.38