Semiconductor Manufacturing Technology

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Chapter 4

Silicon and Wafer Preparation

Objectives

After studying the material in this chapter, you will be able to:

1. Describe how raw silicon is refined into semiconductor grade silicon.
2. Explain the crystal structure and growth method for producing monocrystal silicon.
3. Discuss the major defects in silicon crystal.
4. Outline and describe the basic process steps for wafer preparation, starting from a silicon ingot and finishing with a wafer.
5. State and discuss seven quality measures for wafer suppliers.
6. Explain what is epitaxy and why it is important for wafers.

Semiconductor-Grade Silicon

Steps to Obtaining Semiconductor Grade Silicon (SGS)		
Step	**Description of Process**	**Reaction**
1	Produce metallurgical grade silicon (MGS) by heating silica with carbon	$SiC\ (s) + SiO_2\ (s) \rightarrow Si\ (l) + SiO(g) + CO\ (g)$ (98%)
2	Purify MG silicon through a chemical reaction to produce a silicon-bearing gas of trichlorosilane ($SiHCl_3$)	$Si\ (s) + 3HCl\ (g) \rightarrow SiHCl_3\ (g) + H_2\ (g) + heat$ (99.9999999%)
3	$SiHCl_3$ and hydrogen react in a process called Siemens to obtain pure semiconductor-grade silicon (SGS)	$2SiHCl_3\ (g) + 2H_2\ (g) \rightarrow 2Si\ (s) + 6HCl\ (g)$

Table 4.1

Crystal Structure

- Amorphous Materials
- Unit Cells
- Polycrystal and Monocrystal Structures
- Crystal Orientation

Siemens Reactor for SG Silicon

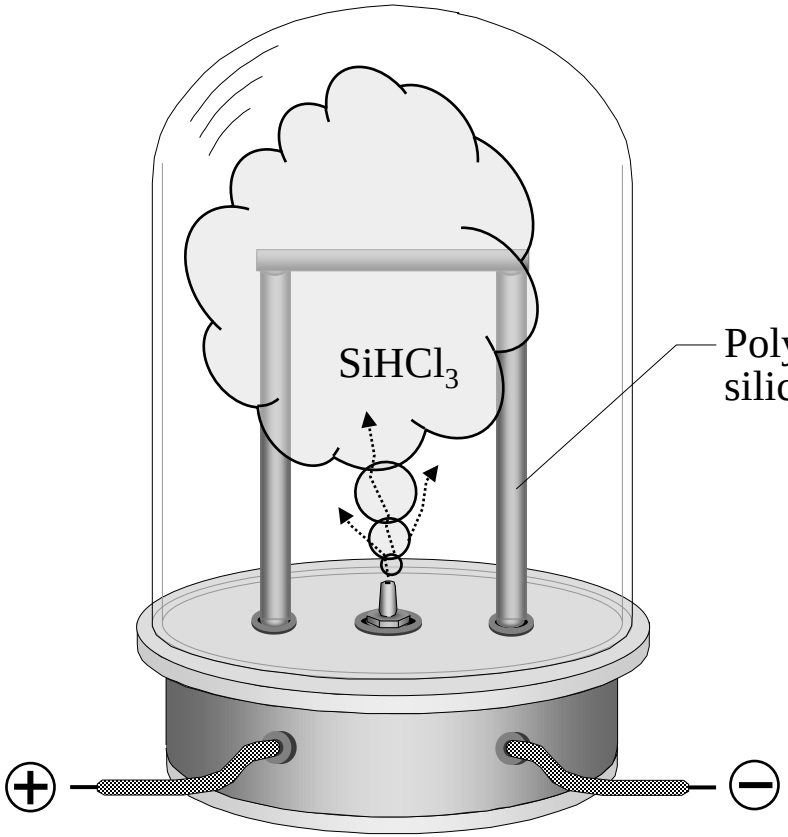


Figure 4.1

Atomic Order of a Crystal Structure

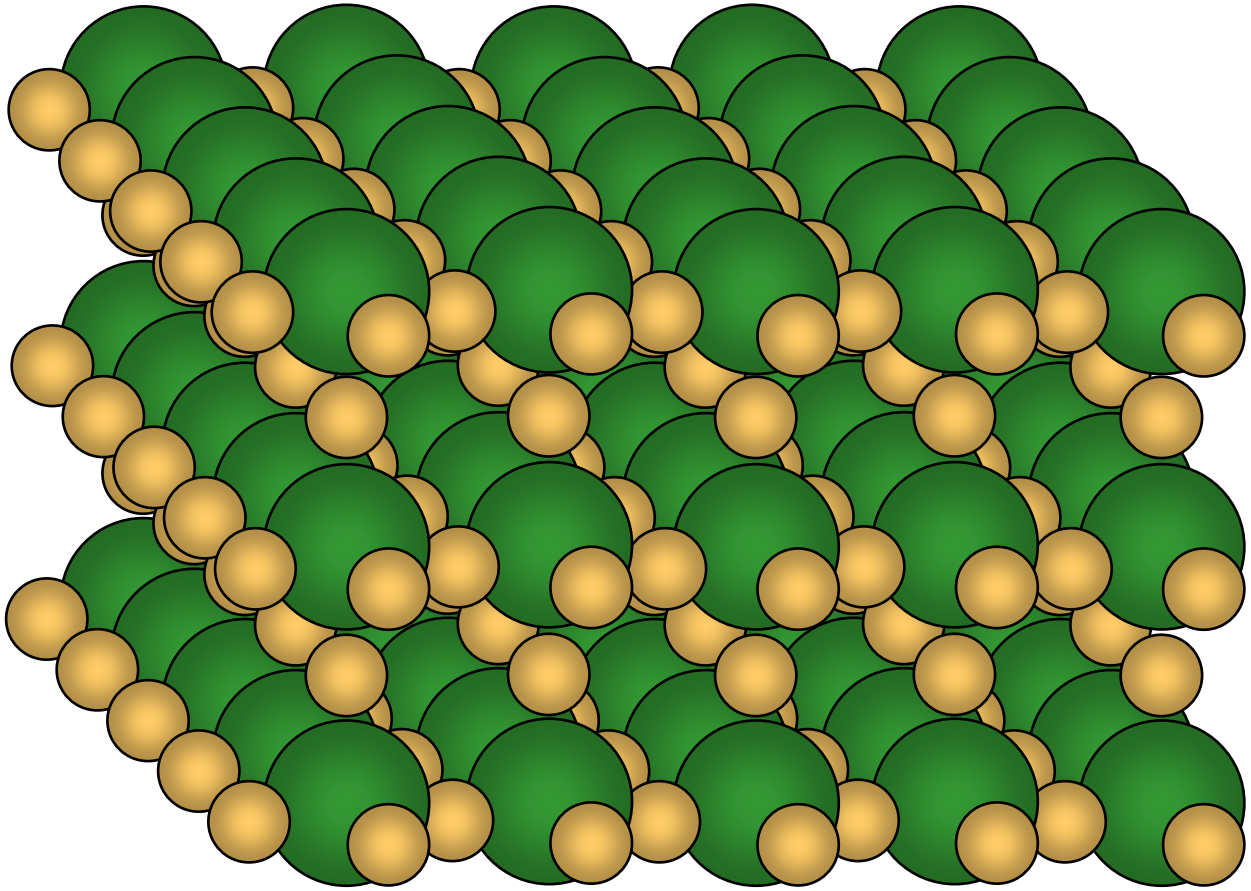


Figure 4.2

Amorphous Atomic Structure

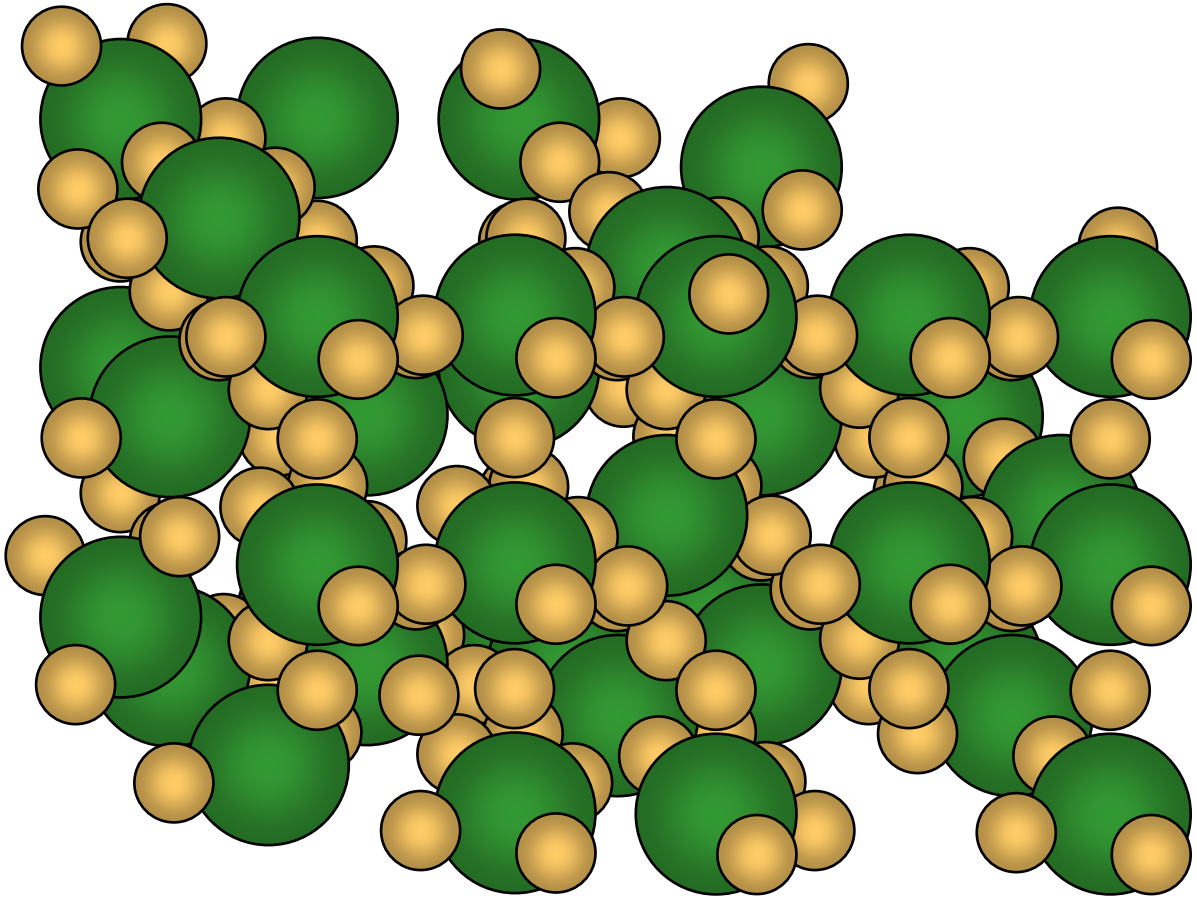
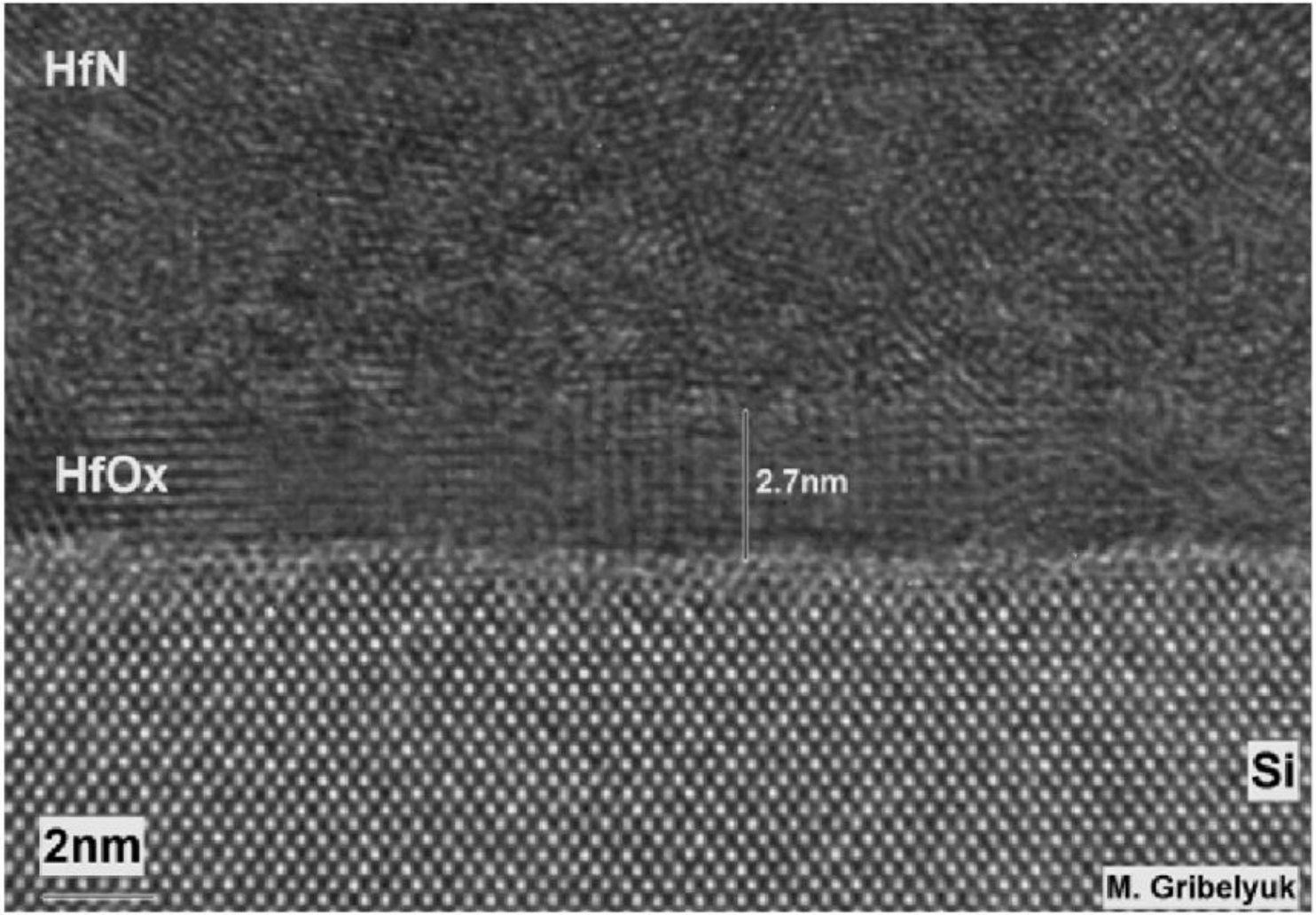


Figure 4.3

HRTEM of Metal/HK/Silicon Interface



Unit Cell in 3-D Structure

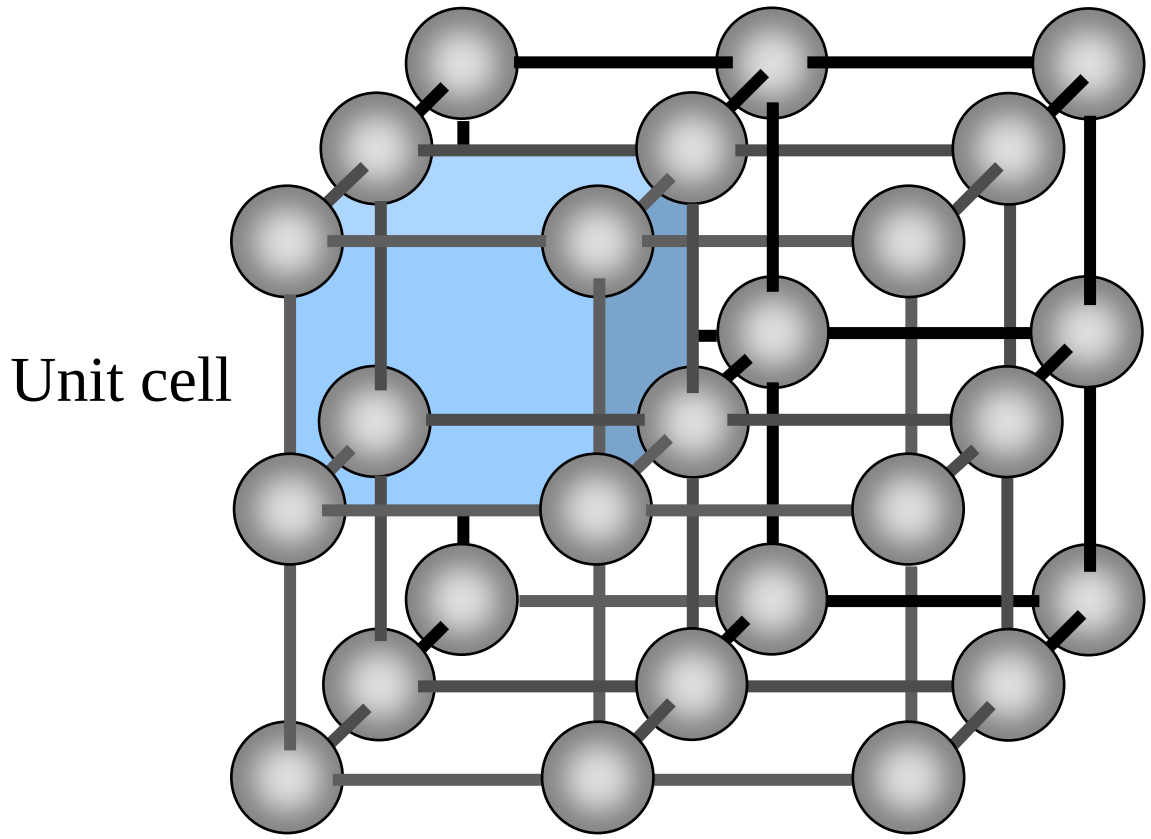


Figure 4.4

Faced-centered Cubic (FCC) Unit Cell

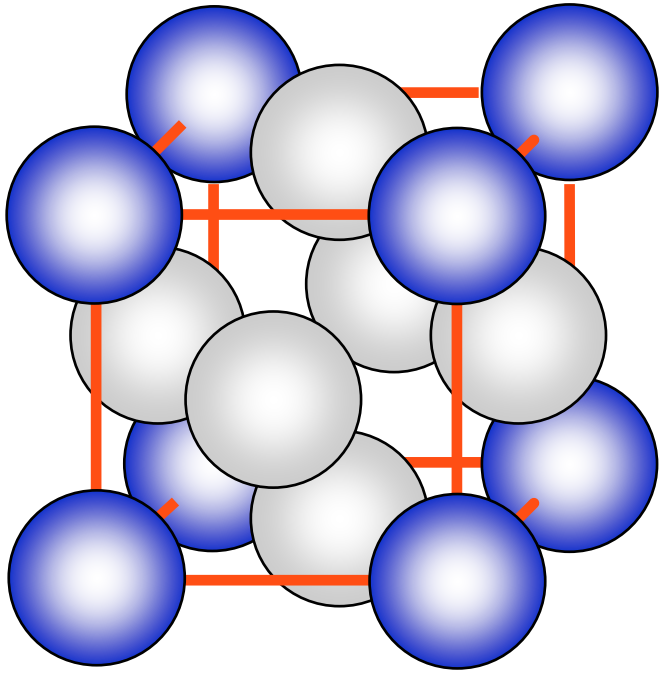
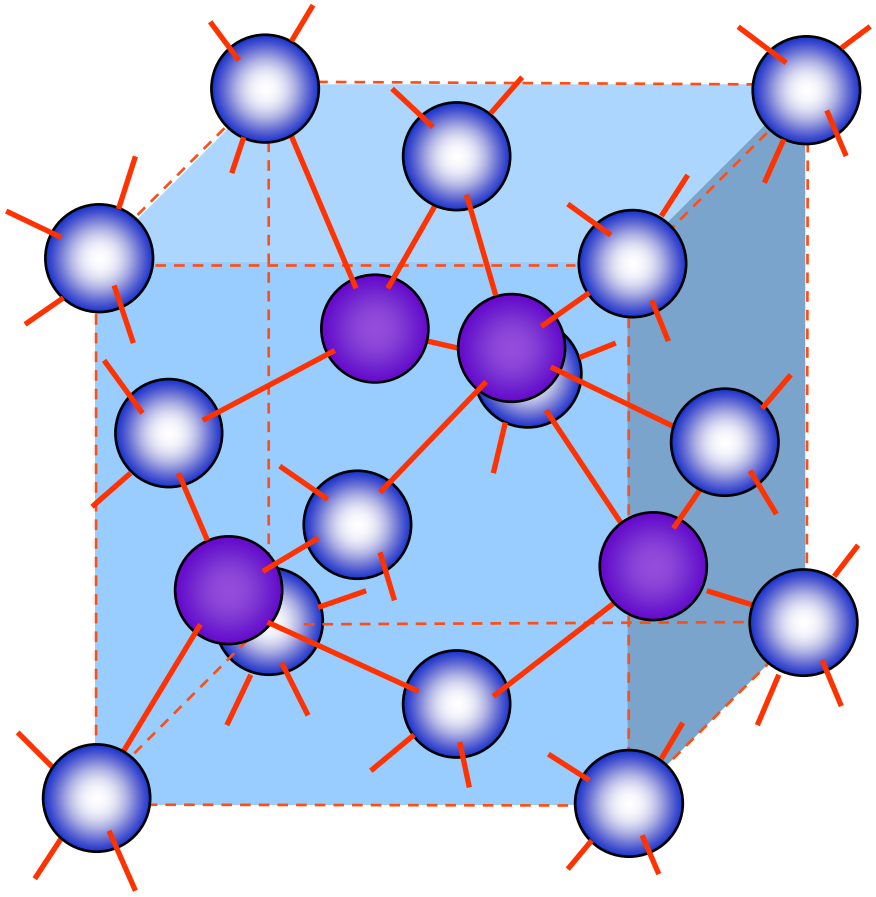


Figure 4.5

Silicon Unit Cell: FCC Diamond Structure

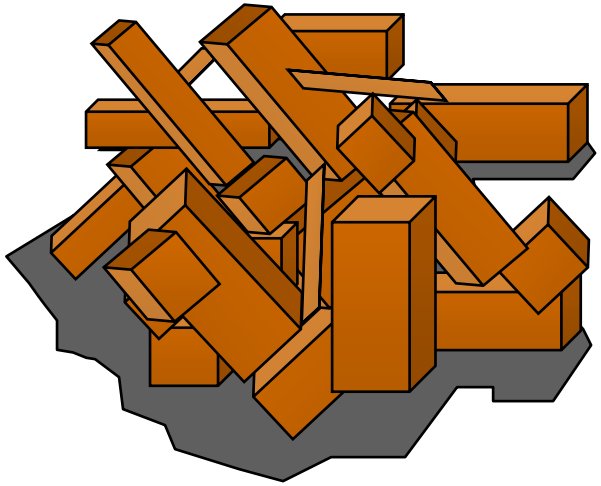


There are four complete atoms with four shared and four unshared. (Total: 8-atom)

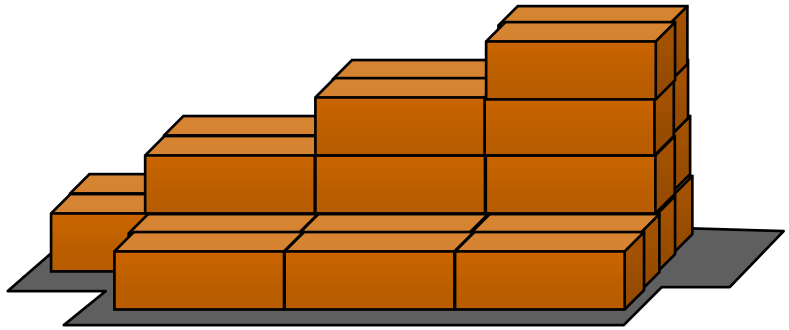
Figure 4.6

Polycrystalline and Monocrystalline Structures

Monocrystalline provides the desirable electrical and mechanical properties necessary for silicon wafer processing and performance



Polycrystalline structure



Monocrystalline structure

Poly-Si

Figure 4.7

Axes of Orientation for Unit Cells

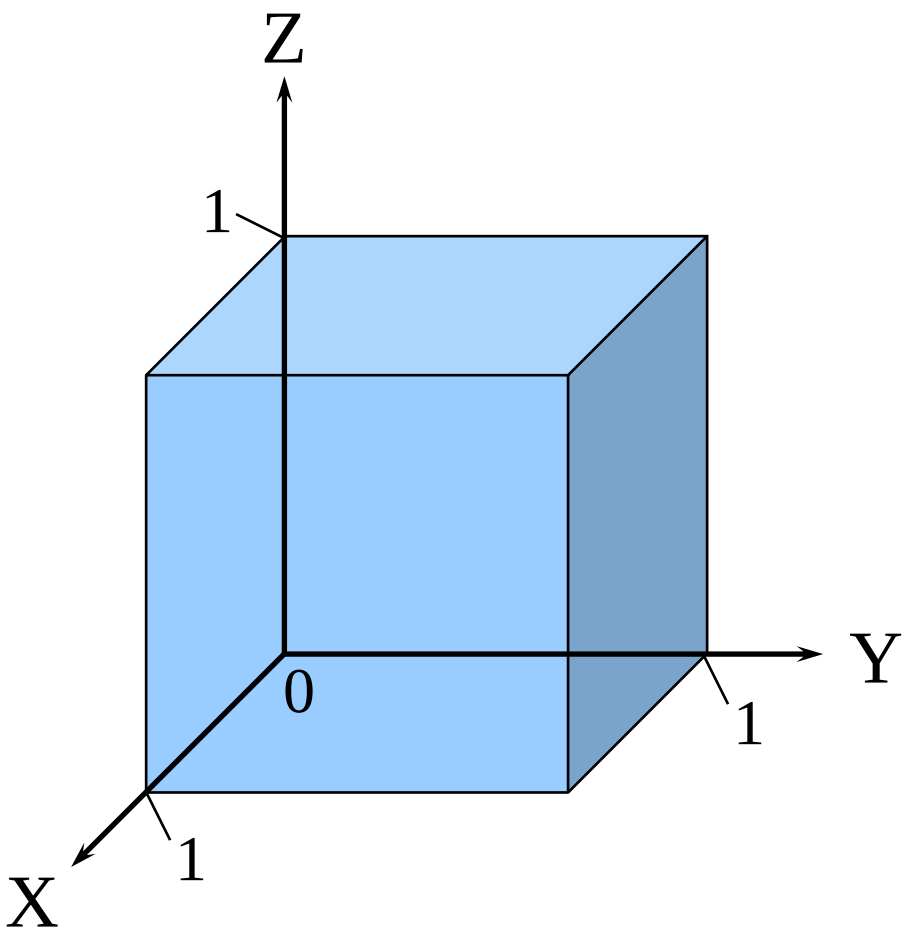
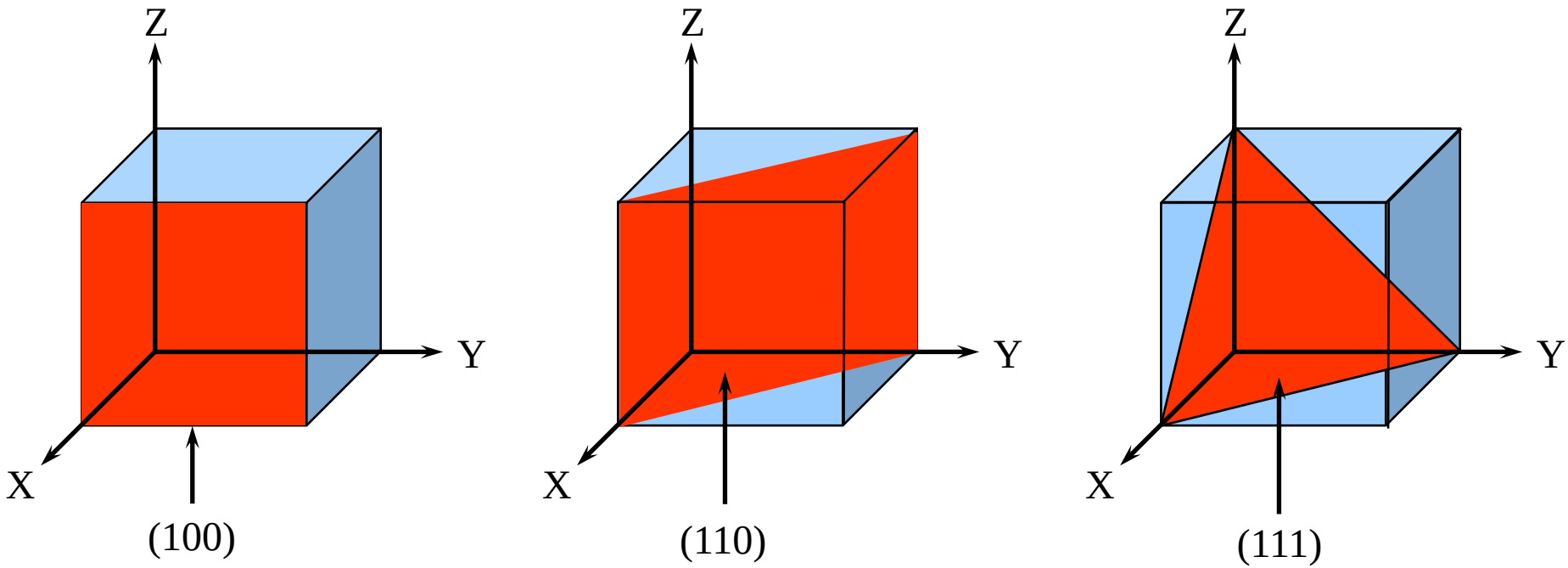


Figure 4.8

Miller Indices of Crystal Planes

In the Miller system of notation, ( ) are used to denote a specific plane,
Whereas < > denote groups of equivalent direction.



- The surface state condition for (100) silicon is more conductive toward controlling the threshold voltage for MOSFETs.
- The (111) has a tighter packing density, making it easier to grow.

Figure 4.9

Monocrystal Silicon Growth (from SGS to crystal)

- CZ Method (Czochralski)
  - CZ Crystal Puller
  - Doping
  - Impurity Control
- Float-Zone Method
- Reasons for Larger Ingot Diameters

CZ Crystal Puller

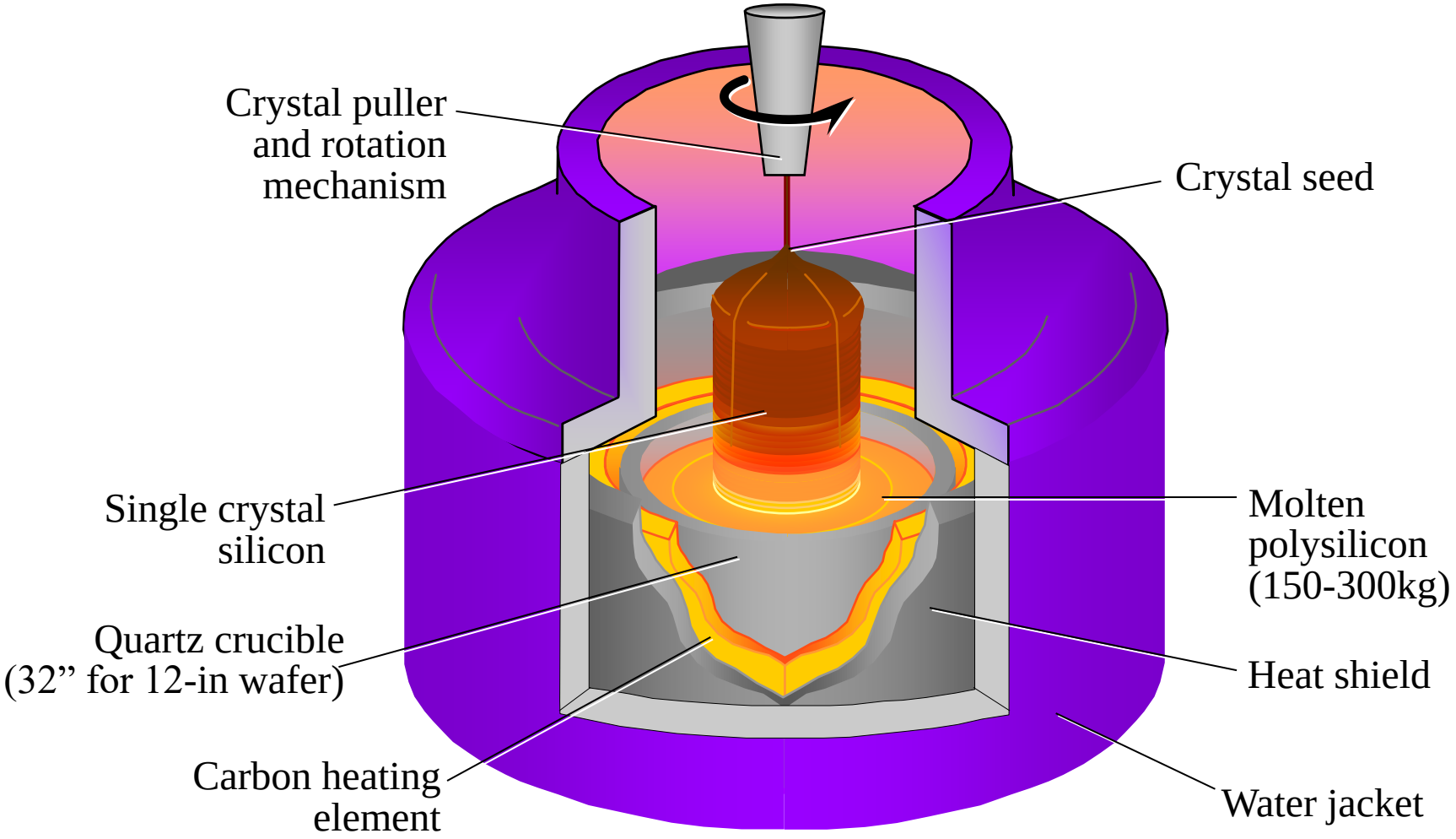
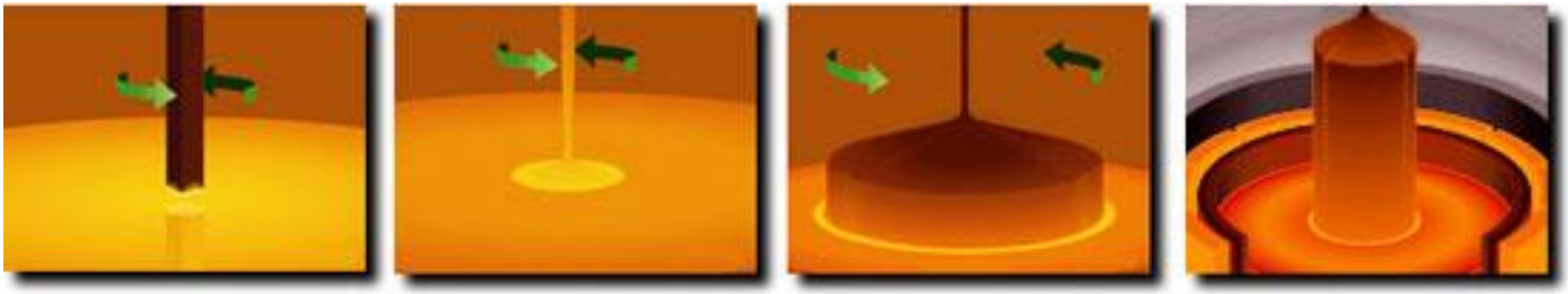
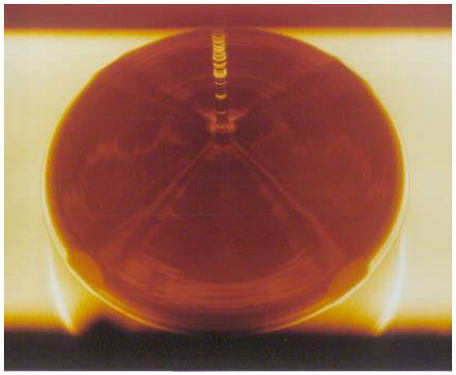


Figure 4.10

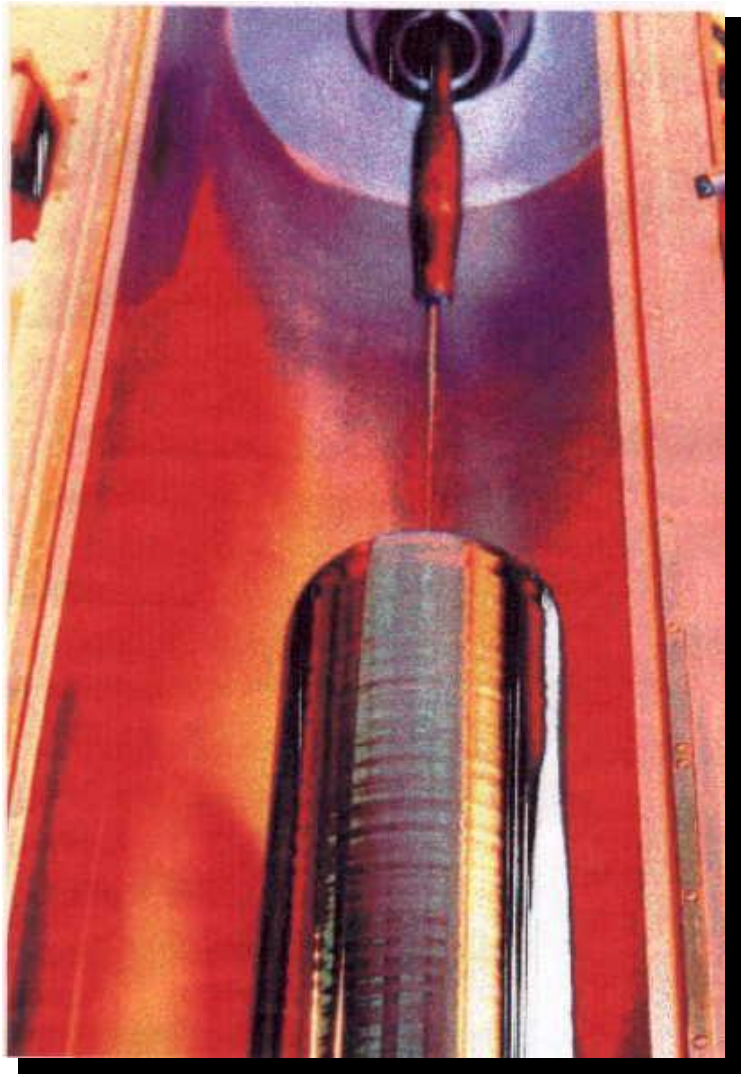
CZ Crystal Pulling





Source: http://www.fullman.com/semiconductors/_crystalgrowing.html

Silicon Ingot Grown by CZ Method



Photograph courtesy of Kayex Corp., 300 mm Si ingot

Photo 4.1

Next Wafer Size?

200 mm/1990 300 mm/2001 450 mm/2012?

Every 10-11 years wafer size increases. Will history repeat itself?

CZ Crystal Puller

Photograph courtesy of Kayex Corp., 300 mm Si crystal puller

Photo 4.2

Dopant Concentration Nomenclature

		Concentration (Atoms/cm^3)			
Dopant	**Material Type**	$< 10^{14}$ (Very Lightly Doped)	10^{14} to 10^{16} (Lightly Doped)	10^{16} to 10^{19} (Doped)	$>10^{19}$ (Heavily Doped)
Pentavalent	n	n^{--}	n^{-}	n	n^{+}
Trivalent	p	p^{--}	p^{-}	p	p^{+}

Oxygen from crucible (20-30 ppm) can be useful as the **getter site** for impurities in the center region of wafer

Table 4.2

Float Zone (FZ) Crystal Growth

- Smaller diameter (4-6 in).
- By not using a crucible, FZ results in a high-purity silicon with low oxygen and carbon.
- Heating of the polysilicon bar is the most important aspect of the FZ process, as each section of the bar is molten only for about 30-min.

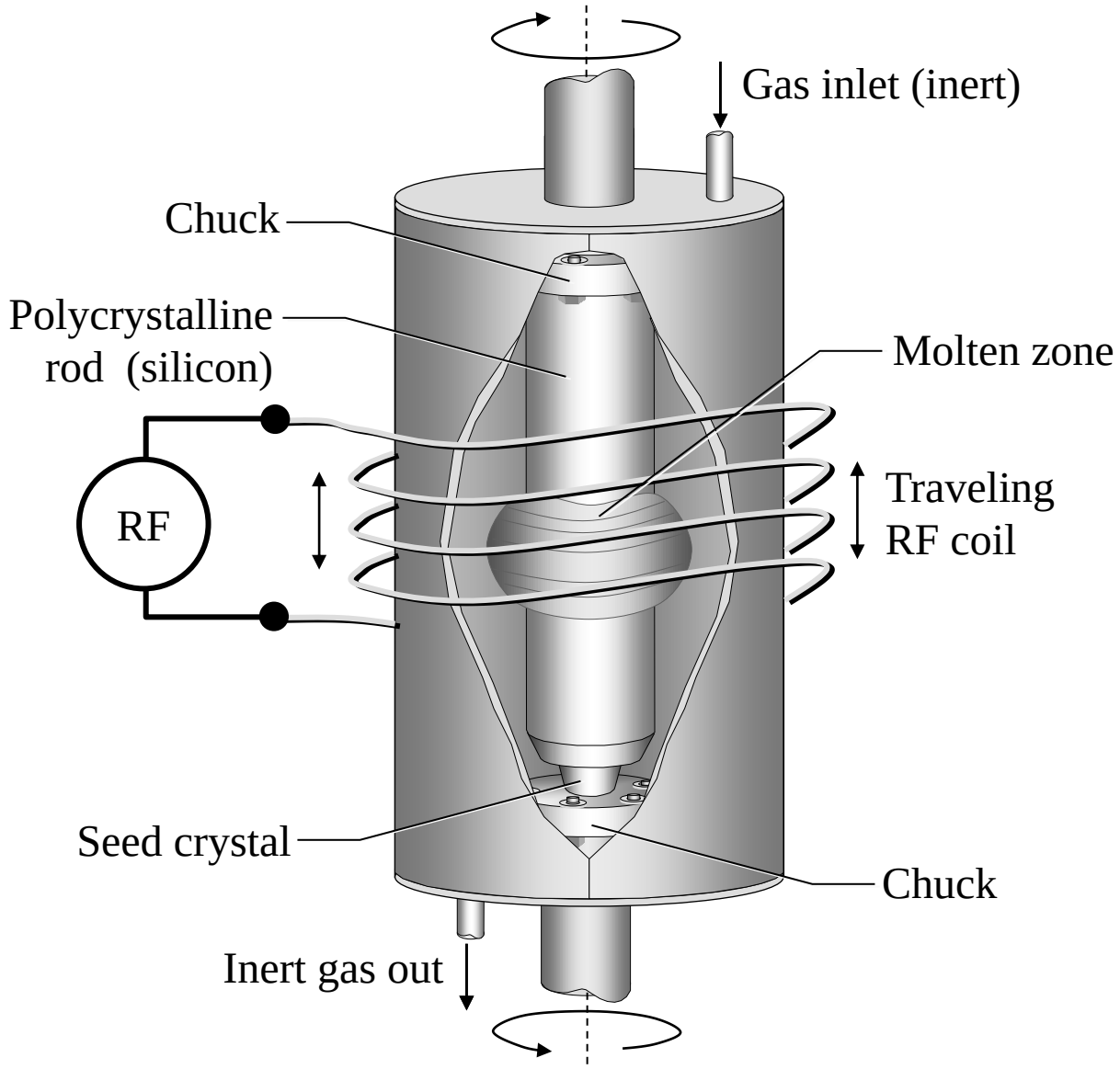


Figure 4.11

Wafer Diameter Trends

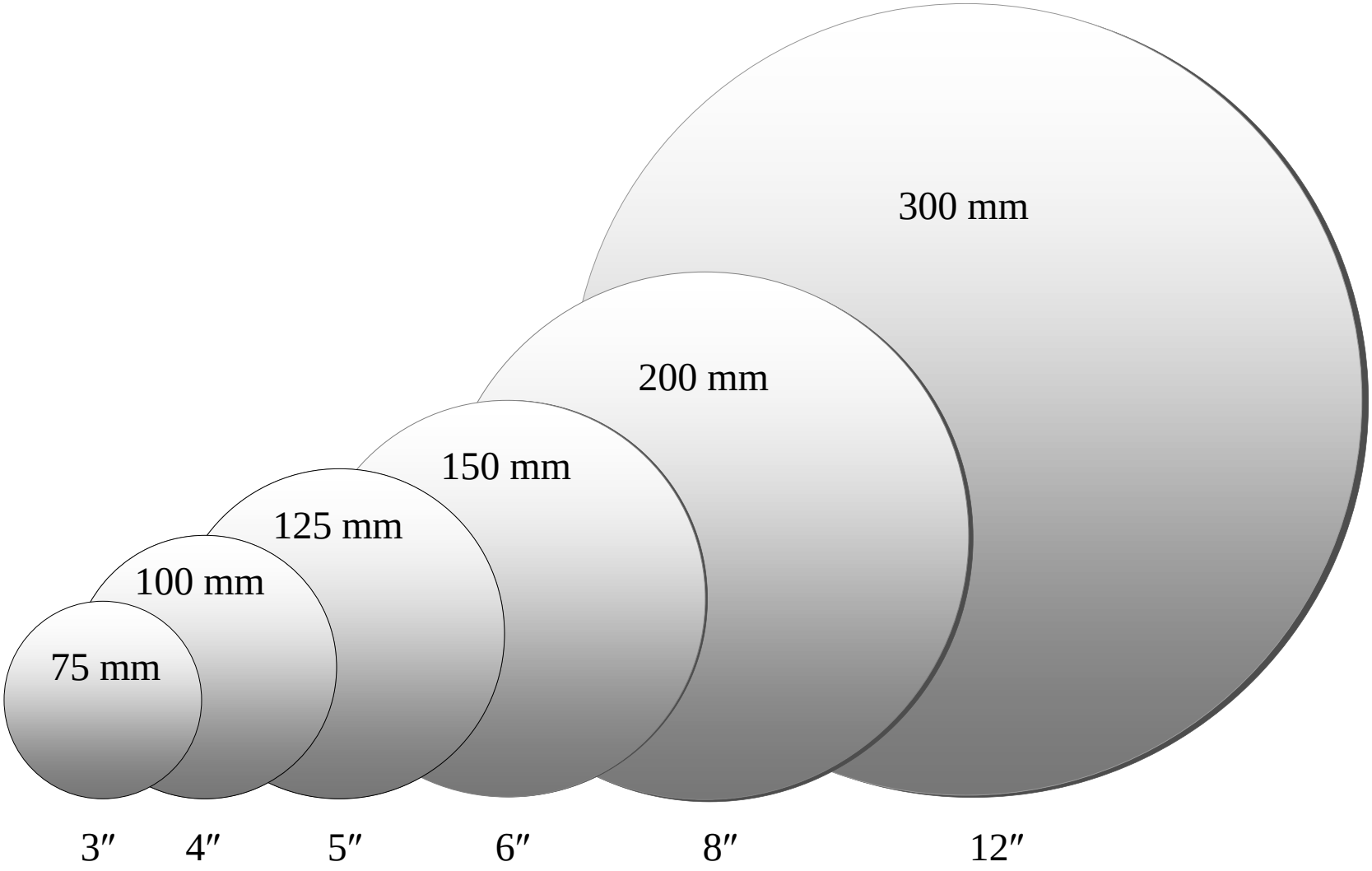


Figure 4.12

Wafer Dimensions & Attributes

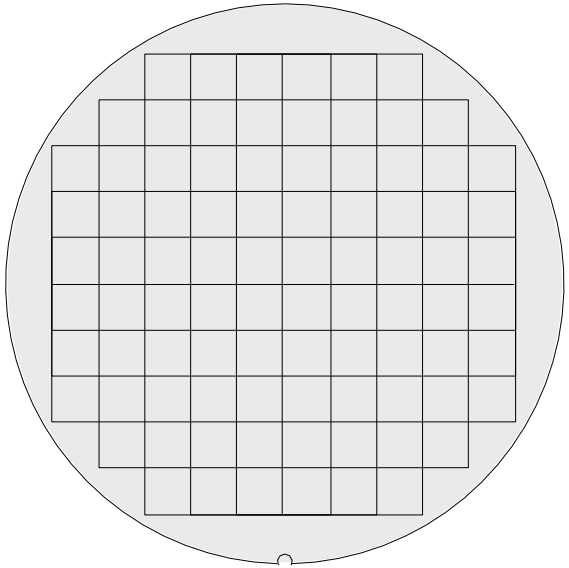
Cost !

Diameter (mm)	Thickness (μm)	Area (cm^2)	Weight (grams/lbs)	Weight/25 Wafers (lbs)
150 (6”)	675 ± 20	176.71	28 / 0.06	1.5
200 (8”)	725 ± 20	314.16	53.08 / 0.12	3
300 (12”)	775 ± 20	706.86	127.64 / 0.28	7
450 (18”)	825 ± 20	1256.64	241.56 / 0.53	13

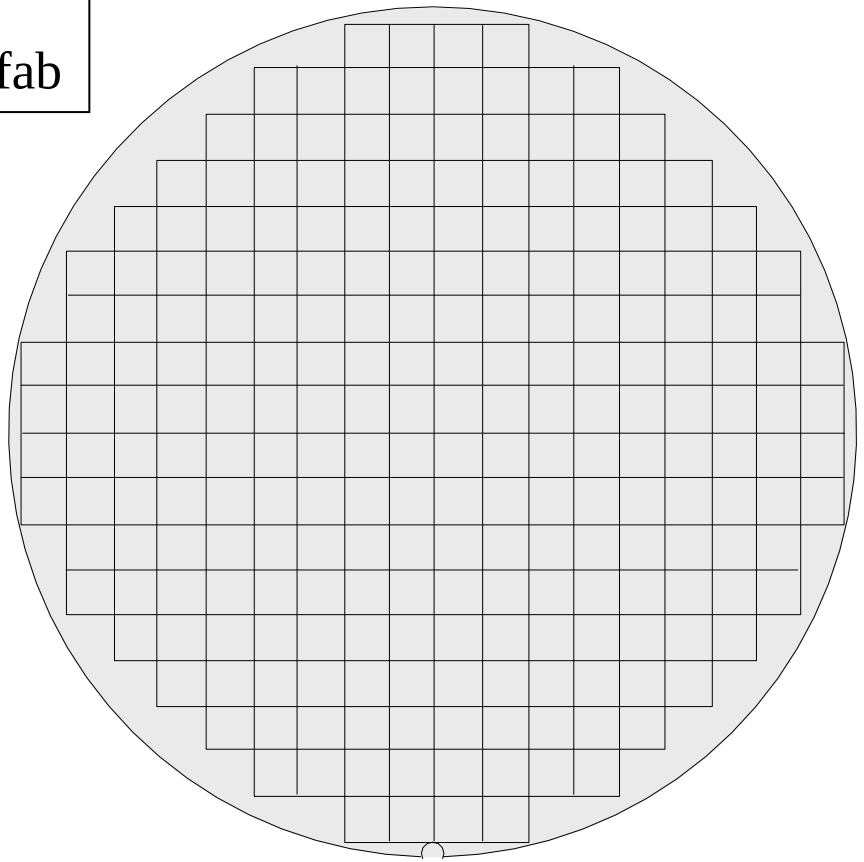
Table 4.3

Increase in Number of Chips on Larger Wafer Diameter

- Total cost reduced ~ 30%
- $13-15 billion to build a 12-in fab



88 die
200-mm wafer



232 die
300-mm wafer **(<u>2.25 times</u>)**

Figure 4.13

Developmental Specifications for 300-mm Wafer Dimensions and Orientation

Parameter	Units	Nominal	Some Typical Tolerances
Diameter	mm	300.00	± 0.20
Thickness (center point)	μm	775	± 25
Warp (max)	μm	100	
Nine-Point Thickness Variation (max)	μm	10	
Notch Depth	mm	1.00	+ 0.25, -0.00
Notch Angle	Degree	90	+5, -1
Back Surface Finish		Bright Etched/Polished	
Edge Profile Surface Finish		Polished	
FQA (Fixed Quality Area – radius permitted on the wafer surface)	mm	147	

From H. Huff, R. Foodall, R. Nilson, and S. Griffiths, "Thermal Processing Issues for 300-mm Silicon Wafers: Challenges and Opportunities," ULSI Science and Technology (New Jersey: The Electrochemical Society, 1997), p. 139.

Table 4.4

Crystal Defects in Silicon

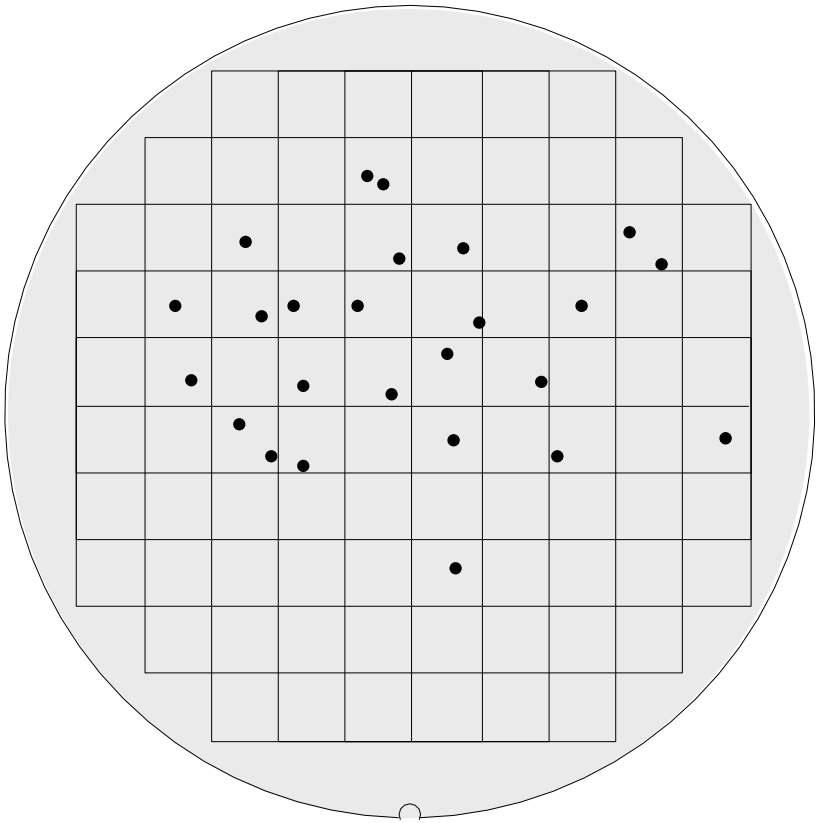
A crystal defect (*microdefect*) is any interruption in the repetitive nature of the unit cell crystal structure.

Three general types of crystal defects in silicon:

1. Point defects - Localized crystal defect at the atomic level
2. Dislocations - Displaced unit cells
3. Gross defects - Defects in crystal structure

Yield of a Wafer

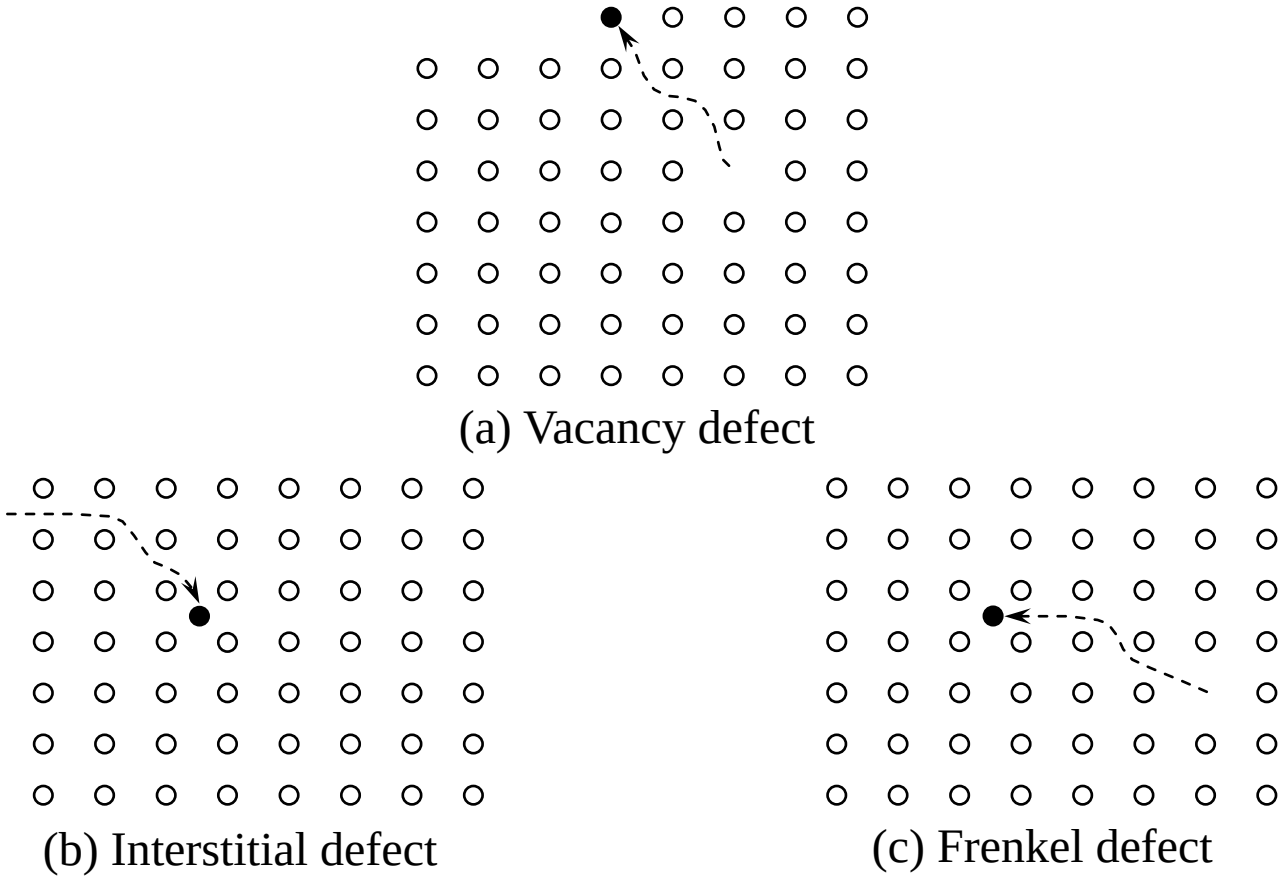
$$\text{Yield} = \frac{66 \text{ good die}}{88 \text{ total die}} = 75\%$$



Reduction in defect density is a critical aspect for increasing wafer yield.

Figure 4.14

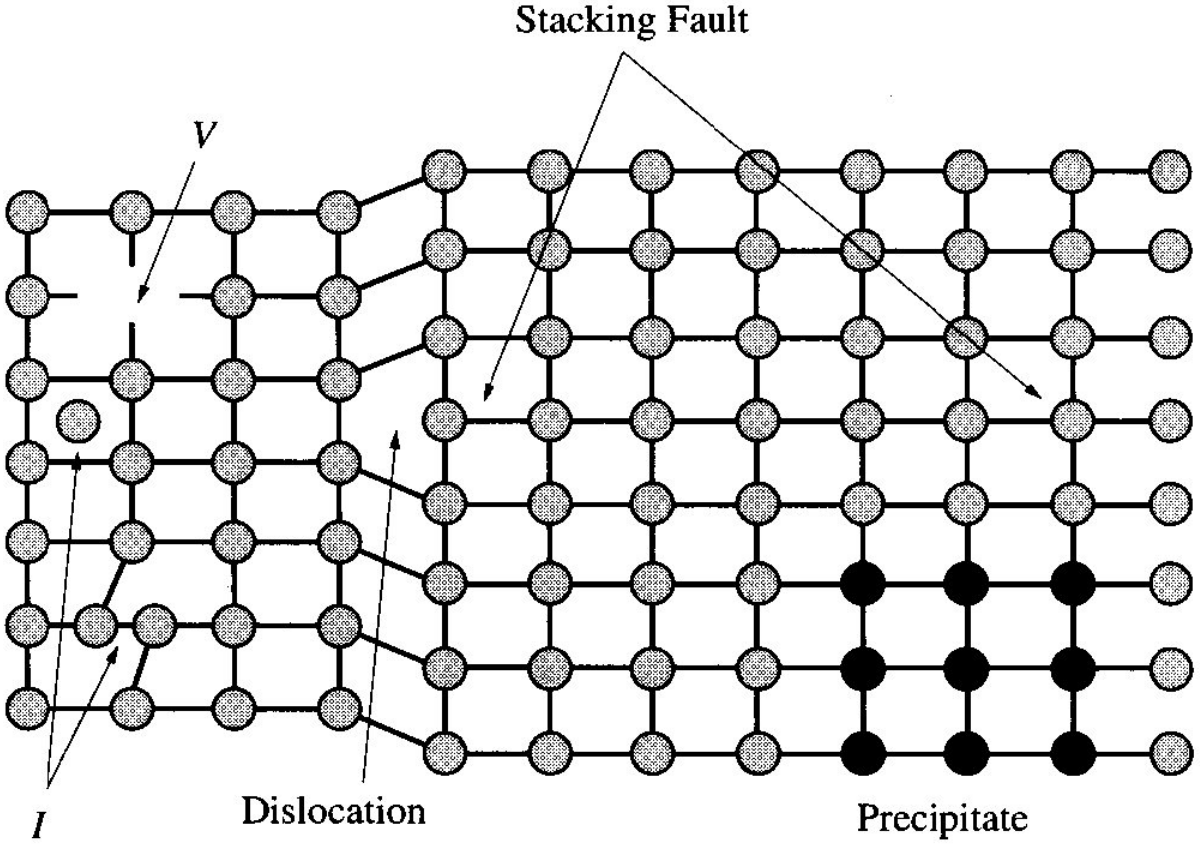
Point Defects



Redrawn from Sorab K. Ghandi, *VLSI Fabrication Principles: Silicon and Gallium Arsenide,* 2nd edition, New York, Wiley, 1994, page 23

Figure 4.15

Dislocations in Unit Cells

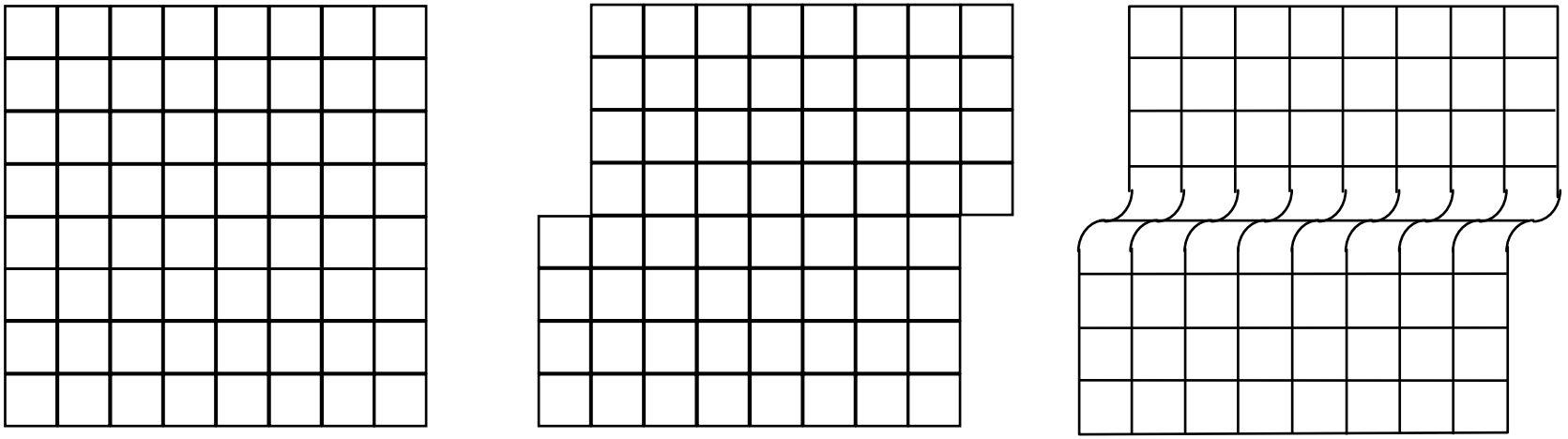


- A neat stack of bricks that has a group of bricks displaced along a row.
- A form of dislocation is stacking faults which is due to layer stacking errors.
- Caused by process: uneven heating & cooling or excessive force applied to the wafer
- Necking down in the beginning of the pull at high speed so that high vacancy densities remove the edge dislocation

Figure 4.16

図 1.2　FZ 結晶の種しぼり部の X 線トポグラフ
（試料の厚さ約 1 mm）

Crystal Slip
(Gross Defects)

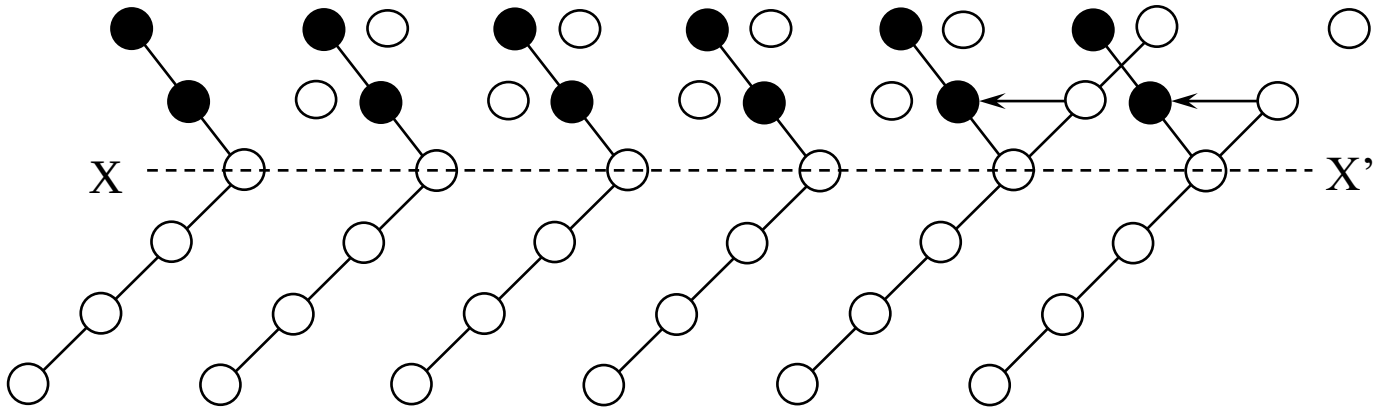


Redrawn from Sorab K. Ghandi, *VLSI Fabrication Principles: Silicon and Gallium Arsenide,* 2nd edition, New York, Wiley, 1994, page 49

Figure 4.17

Crystal Twin Planes (Gross Defects)

Reason: thermal or mechanical shock during the growth process



Redrawn from Sorab K. Ghandi, *VLSI Fabrication Principles: Silicon and Gallium Arsenide,* 2nd edition, New York, Wiley, 1994, page 55

Figure 4.18

Basic Process Steps for Wafer Preparation

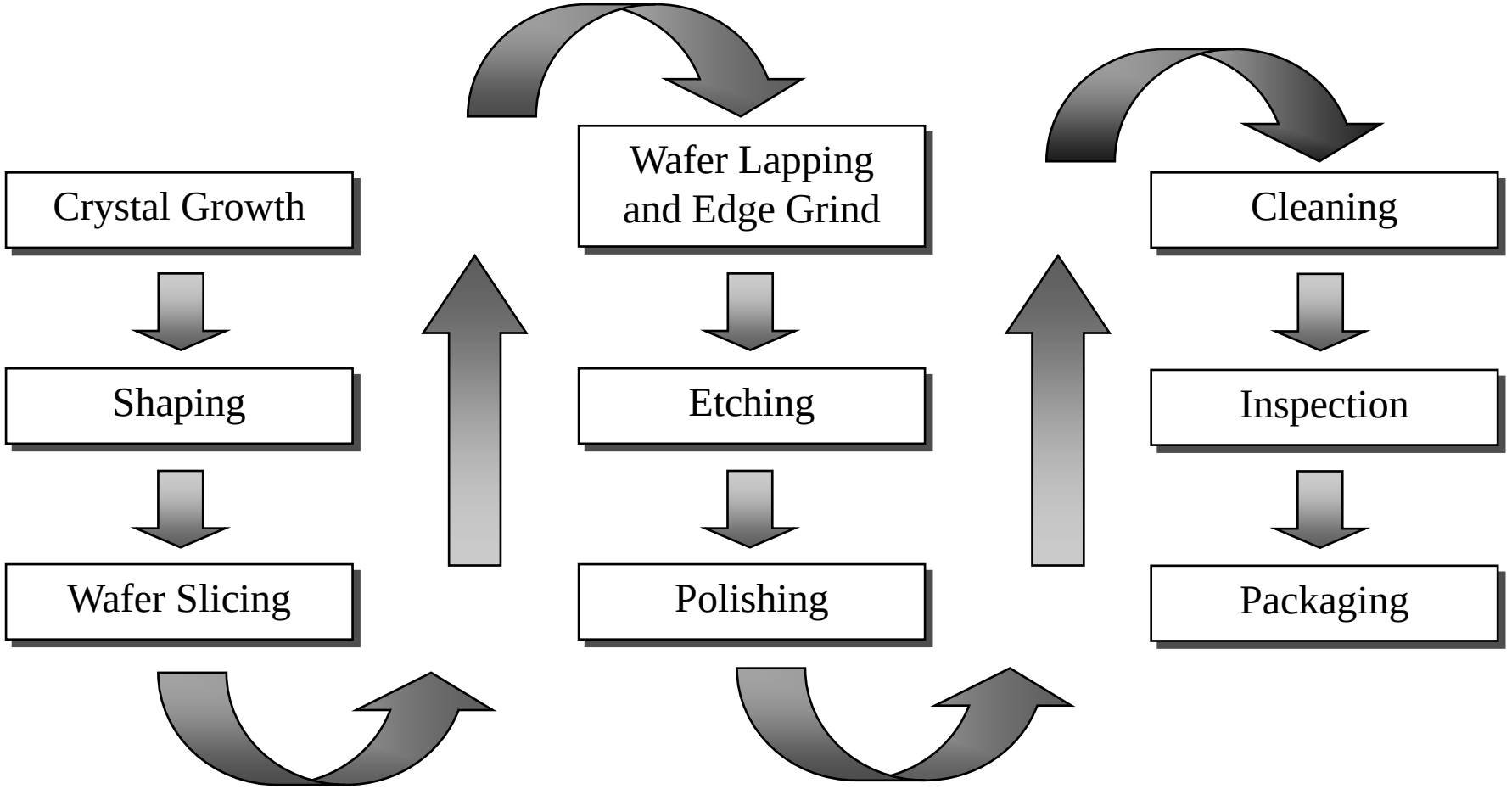


Figure 4.19

Ingot Diameter Grind

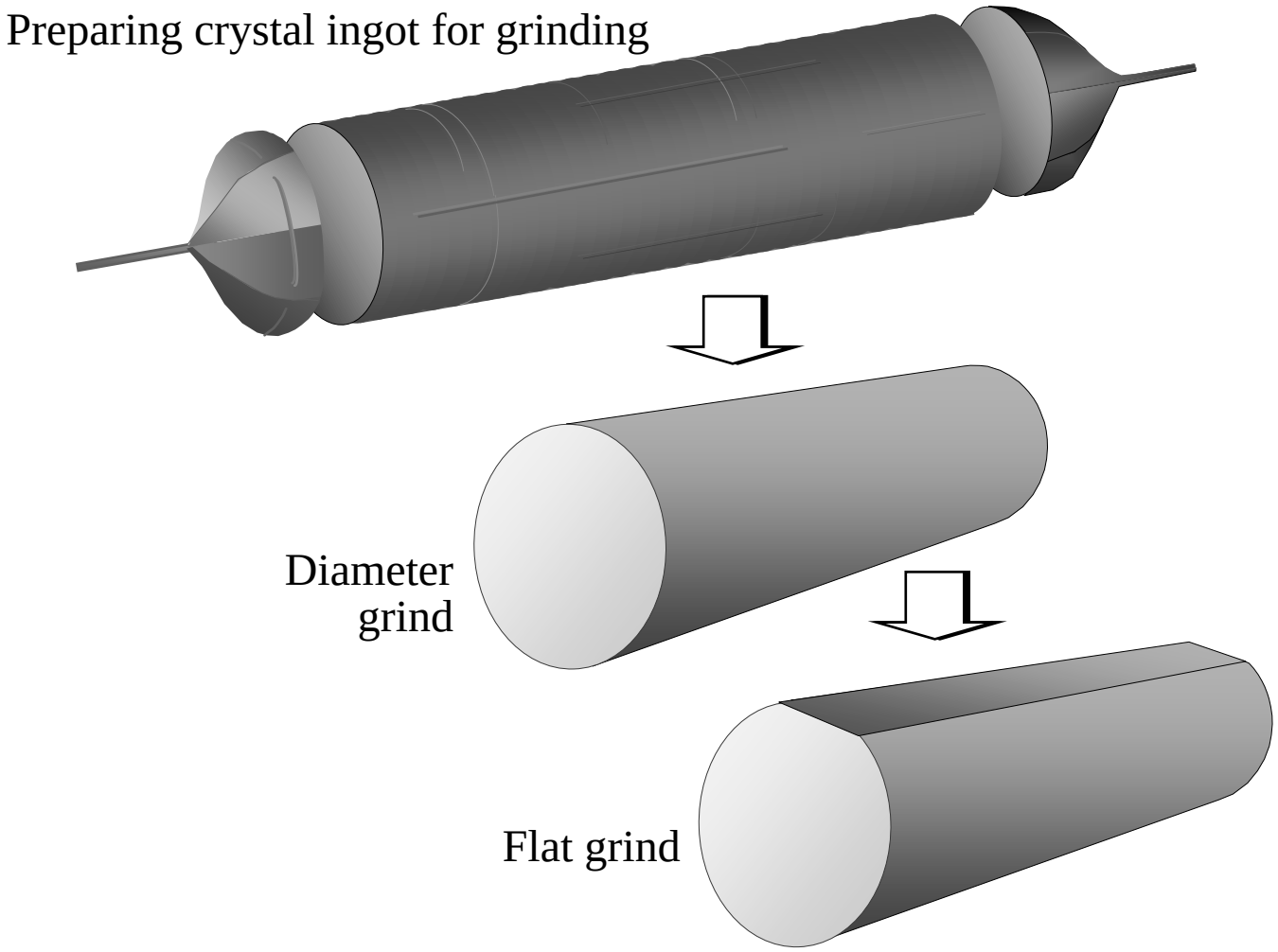
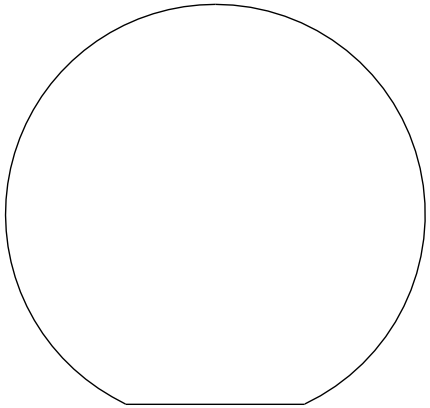
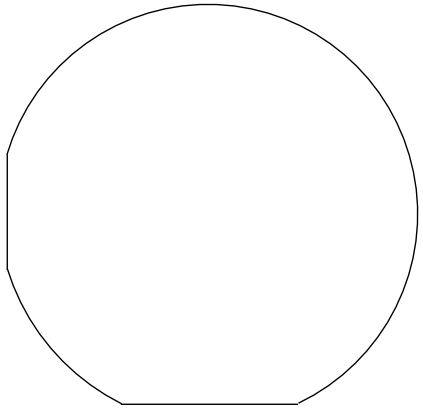


Figure 4.20

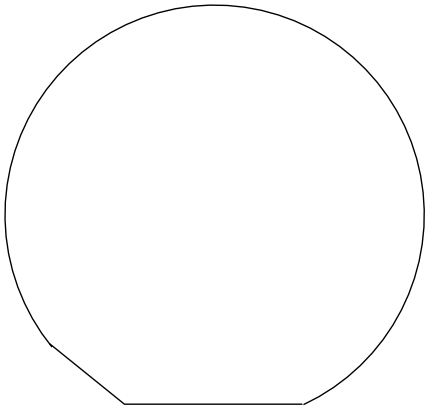
Wafer Identifying Flats



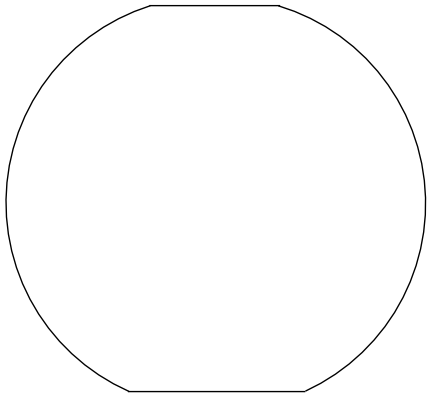
P-type (111)



P-type (100)



N-type (111)



N-type (100)

Figure 4.21

Wafer Notch and Laser Scribe

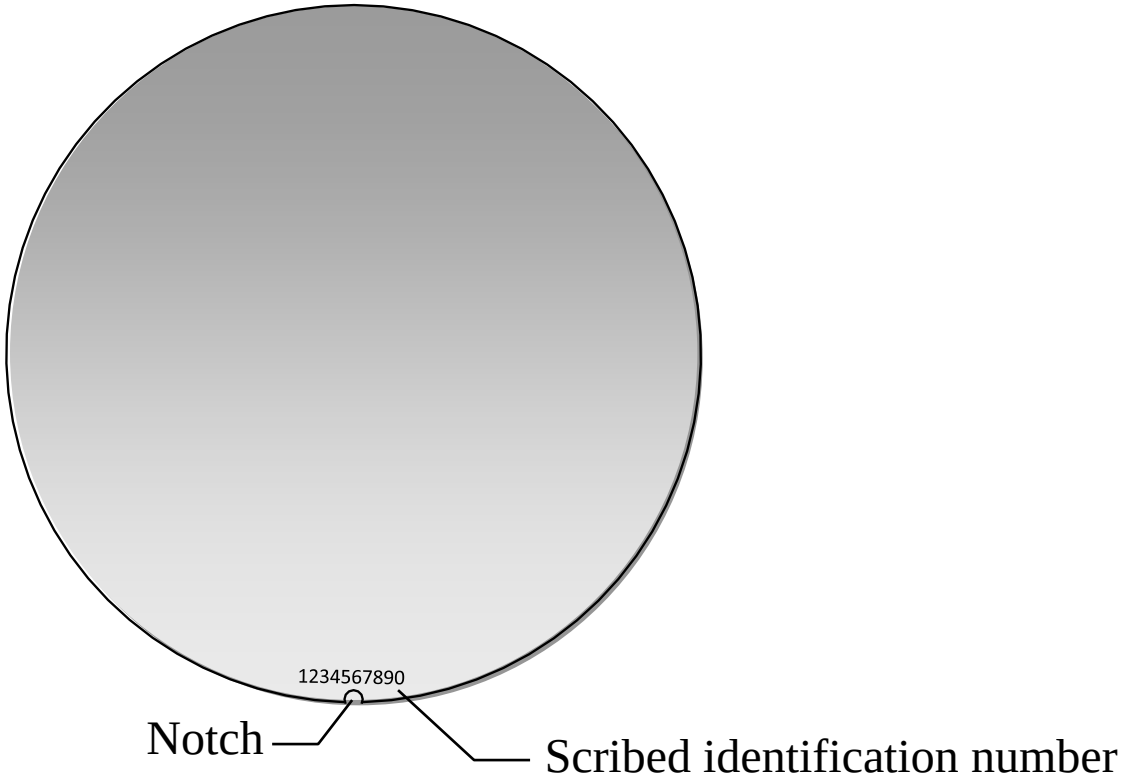
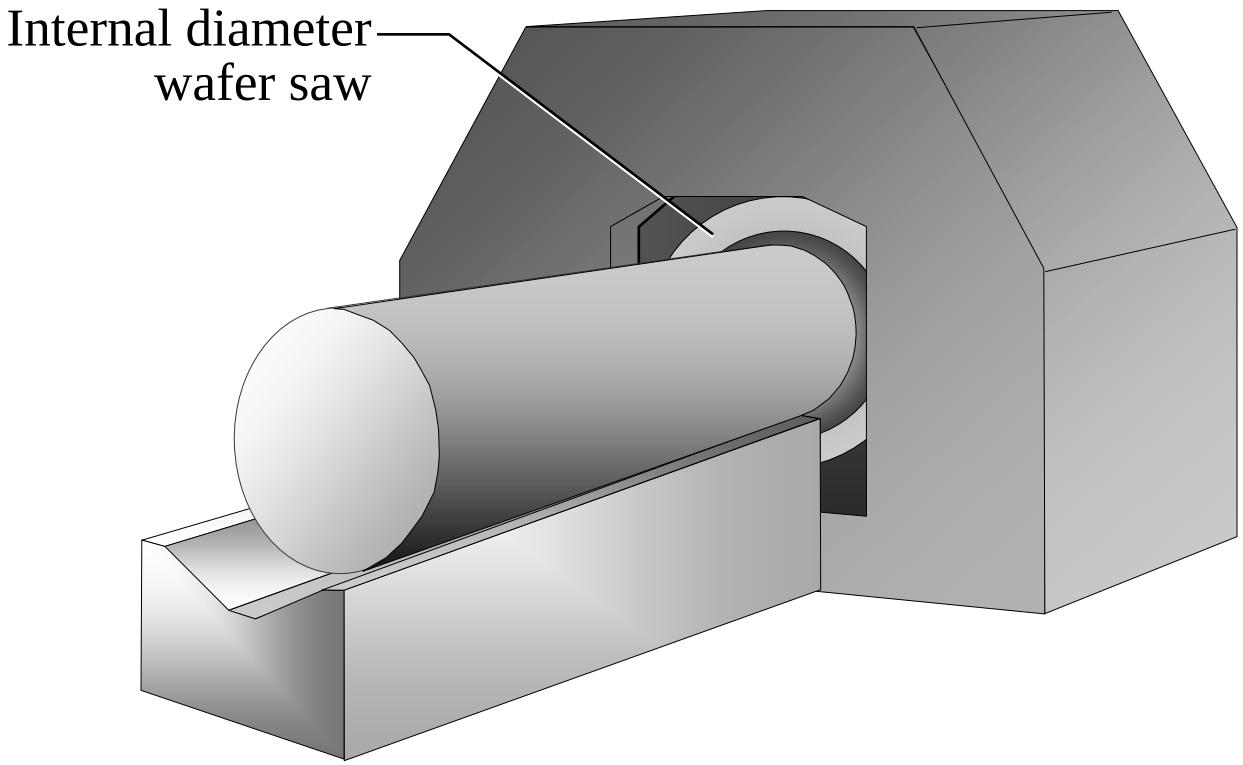


Figure 4.22

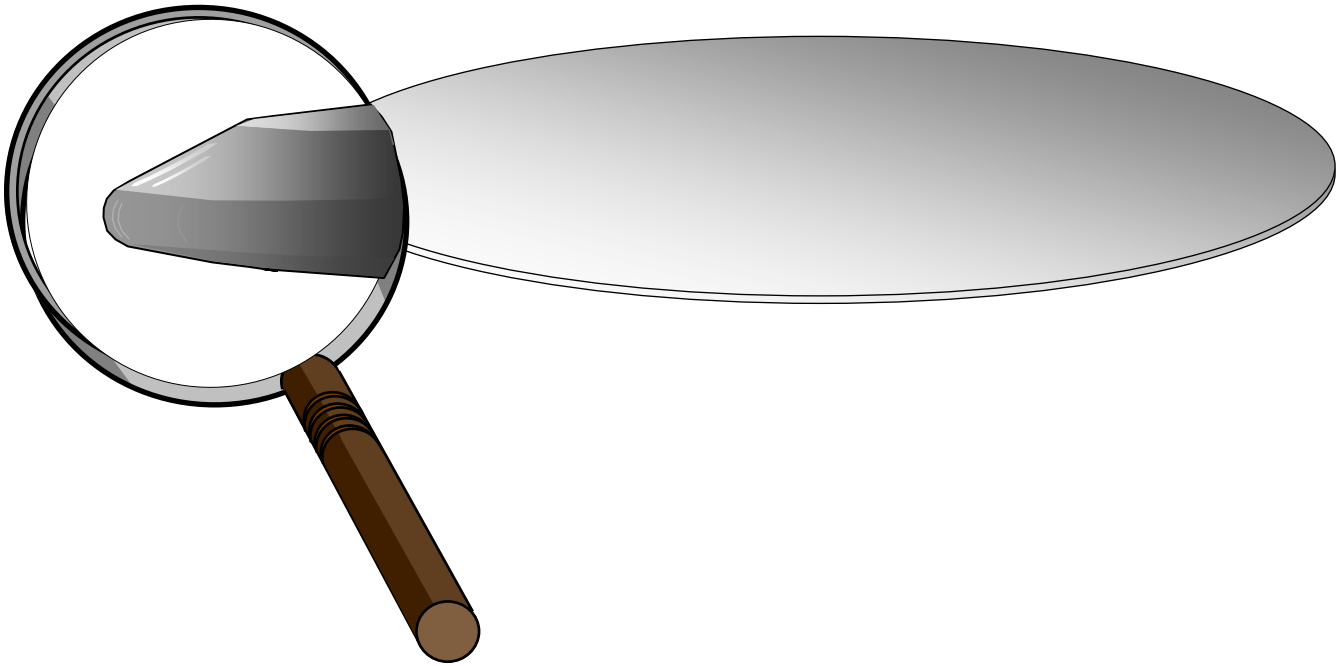
Internal Diameter Saw



- Wafer slicing for 300-mm ingots is currently bring done with wire saws, yield more wafer slices per inch

Figure 4.23

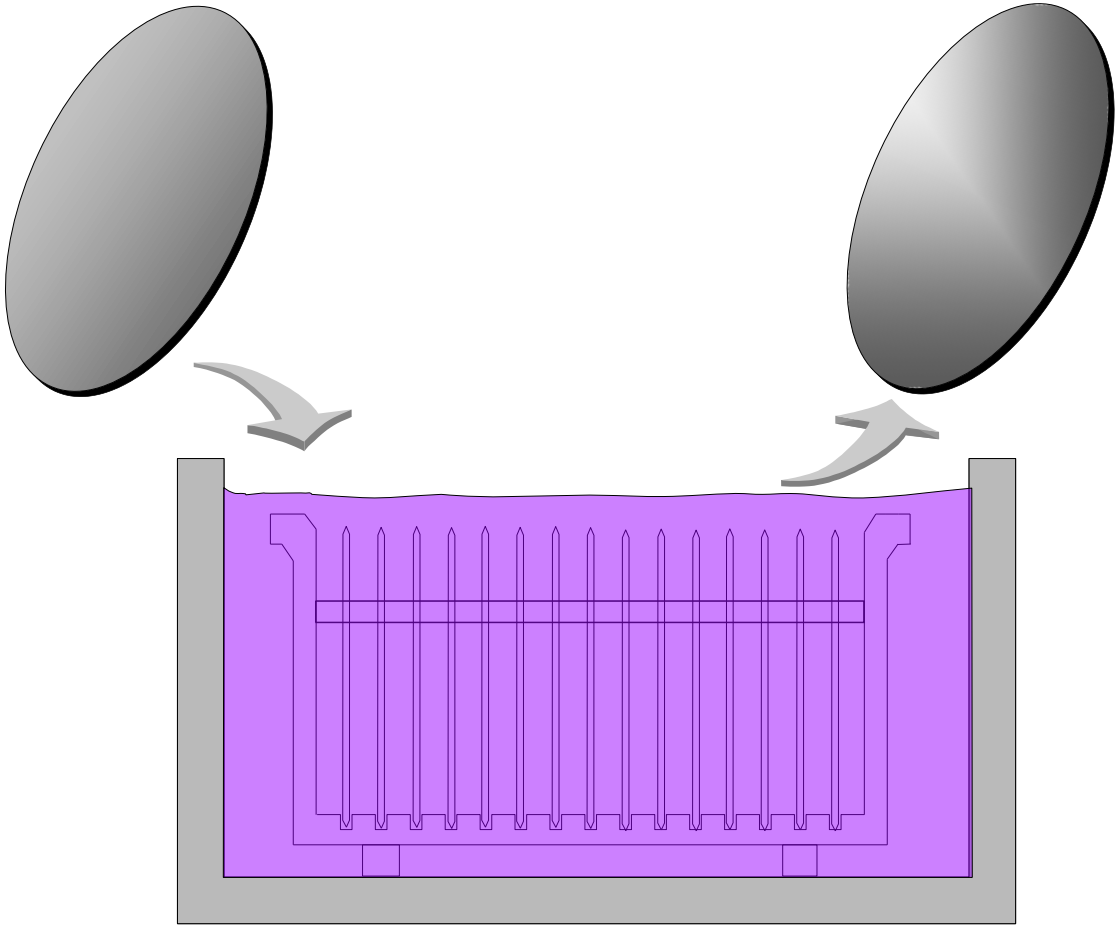
Polished Wafer Edge



- Cracks and small crevices at the edge of the wafer create mechanical stress in wafer that activates crystal dislocations, especially during thermal process
- Chipped edges are a source of edge dislocation growth during thermal cycles.

Figure 4.24

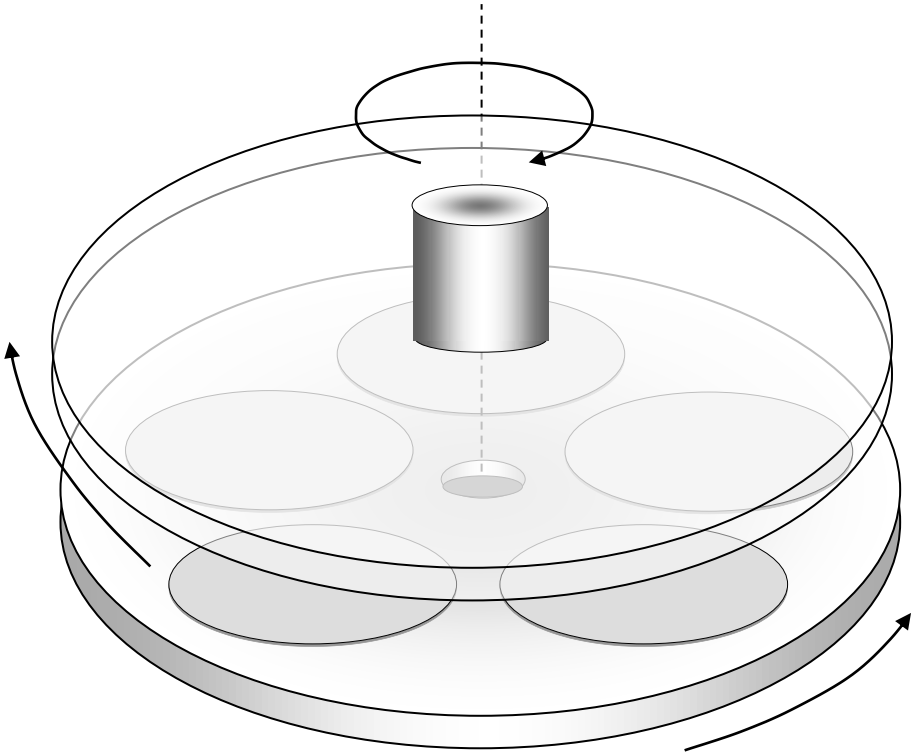
Chemical Etch of Wafer Surface to Remove Damage

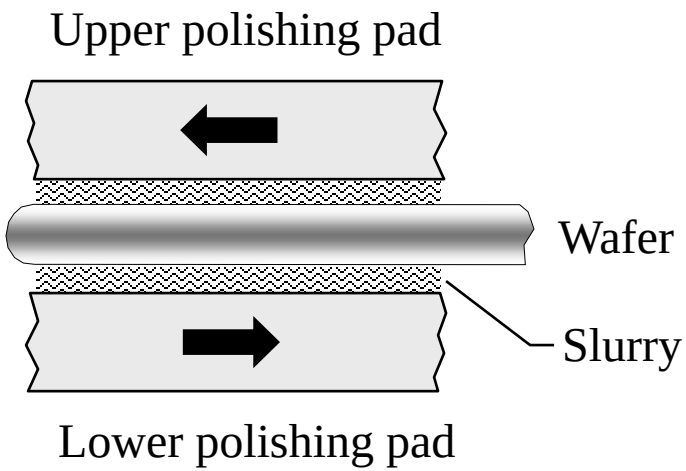


- Shaping the wafer leaves the surface and edges damaged and contaminated
- 20 μm is removed

Figure 4.25

Double-Sided Wafer Polish





- packaging: Cassette is made by conducting Teflon not to generate an electrostatic discharge
- Cassette is filled with nitrogen to prevent oxidation and contamination

Figure 4.26

Quality Measures

- Physical dimensions
- Flatness
- Microroughness
- Oxygen content
- Crystal defects
- Particles
- Bulk resistivity

Improving Silicon Wafer Requirements

	Year (Critical Dimension)			
	1995 (0.35 μm)	**1998 (0.25 μm)**	**2000 (0.18 μm)**	**2004 (0.13 μm)**
Wafer diameter (mm)	200	200	300	300
Site flatness[A] (μm) Site size (mm x mm)	0.23 (22 x 22)	0.17 (26 x 32)	0.12 26 x 32	0.08 26 x 36
Microroughness[B] of front surface (RMS)[C] (nm)	0.2	0.15	0.1	0.1
Oxygen content (ppm)[D]	≤ 24 ± 2	≤ 23 ± 2	≤ 23 ± 1.5	≤ 22 ± 1.5
Bulk microdefects[E] (defects/cm^2)	≤ 5000	≤ 1000	≤ 500	≤ 100
Particles per unit area (#/cm^2)	0.17	0.13	0.075	0.055
Epilayer[F] thickness (± % uniformity) (μm)	3.0 (± 5%)	2.0 (± 3%)	1.4 (± 2%)	1.0 (± 2%)

Adapted from K. M. Kim, "Bigger and Better CZ Silicon Crystals," *Solid State Technology* (November 1996), p. 71.

Improving Silicon Wafer Requirements

Notes:

A. Flatness is the linear thickness variation across the wafer or a site on a wafer (see below).

B. See below for a description of microroughness.

C. RMS is a method for determining the best estimate of group of measurements – in this case, the surface finish measurements (see below). It is calculated by taking the root-mean-square (square root of the average of all measurements squared). Surface finish measurements are obtained by measuring the highest point relative to the lowest point on a surface.

D. ppm is part per million.

E. Bulk microdefects represents all defects within a square centimeter.

F. See below to define epilayer.

Wafer Deformation

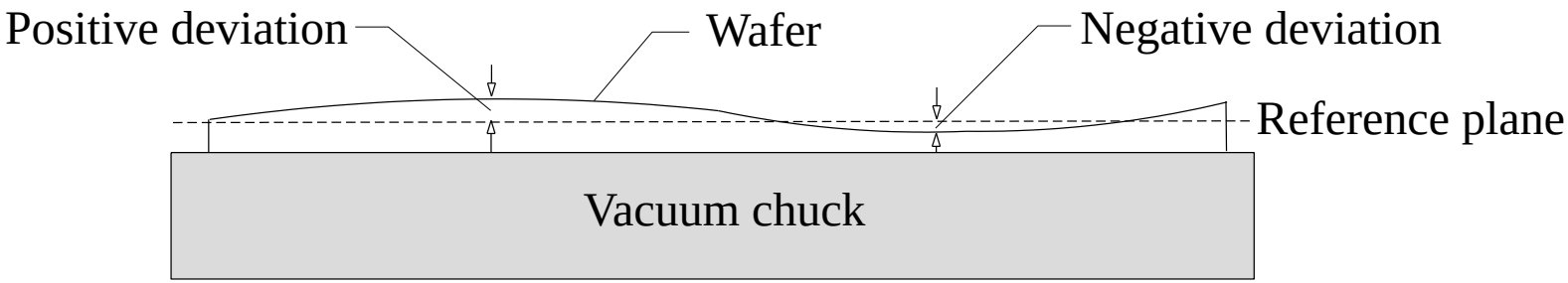


Figure 4.27

Flatness of Wafer Front Surface

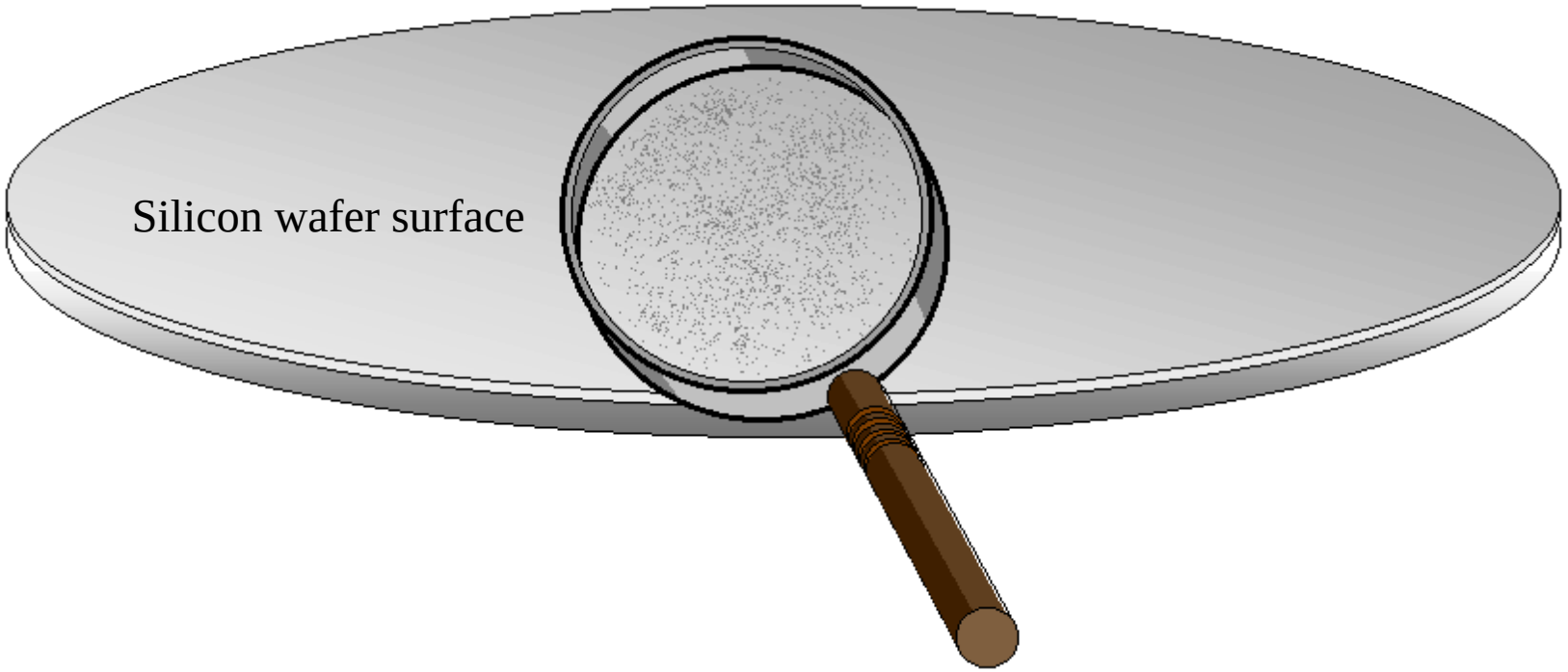
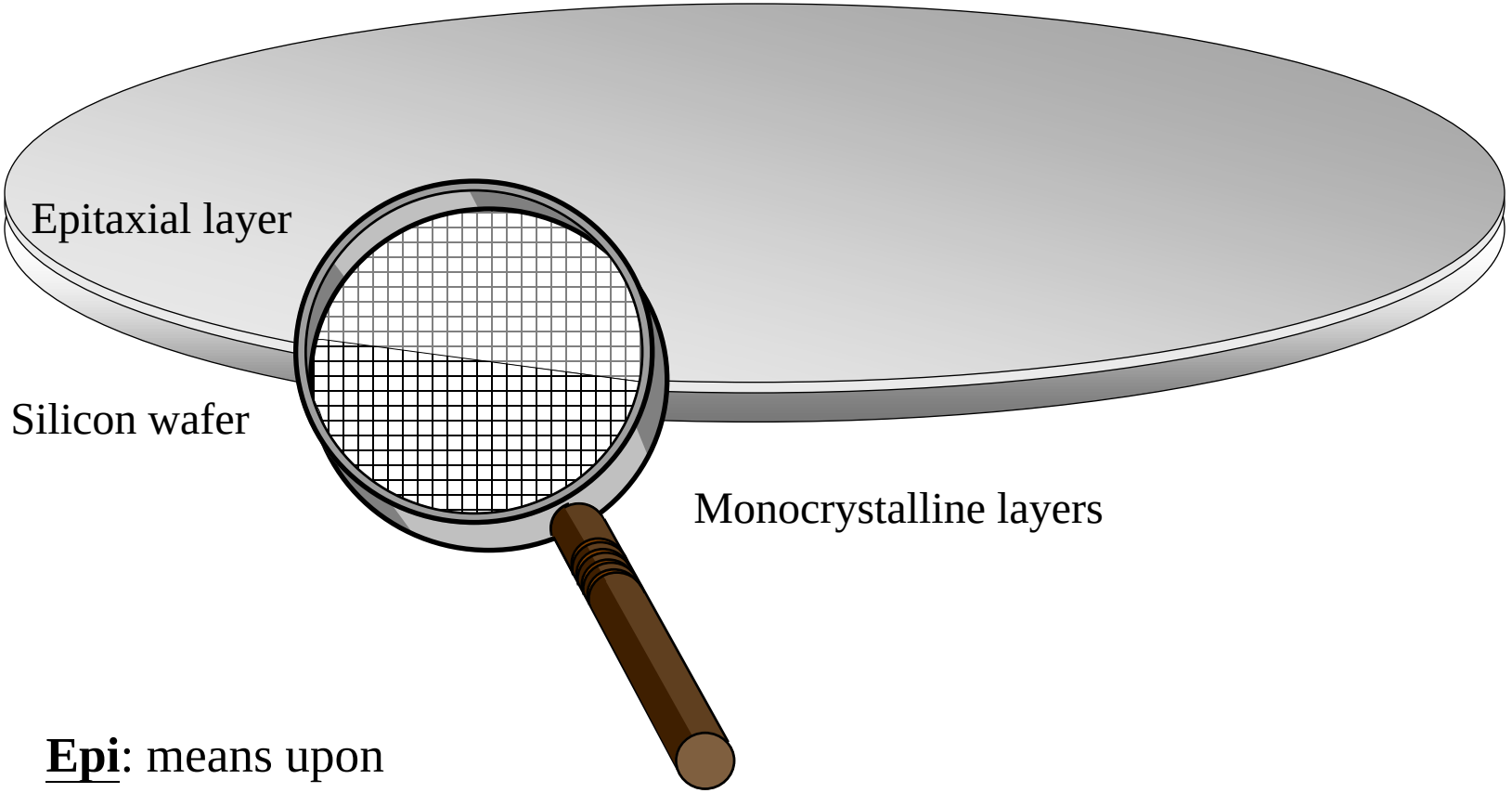


Figure 4.28

Formation of Epitaxial Silicon Layers



- **Epi**: means upon
- **Taxis**: means ordered
- In epitaxial silicon, the base wafer is used as a seed crystal to grow a thin layer of silicon on wafer
- The epi-layer can be n- or p-type and is **independent** of the initial wafer type

Figure 4.29