

Semiconductor Manufacturing Technology

**Michael Quirk & Julian Serda
© October 2001 by Prentice Hall**

Chapter 16

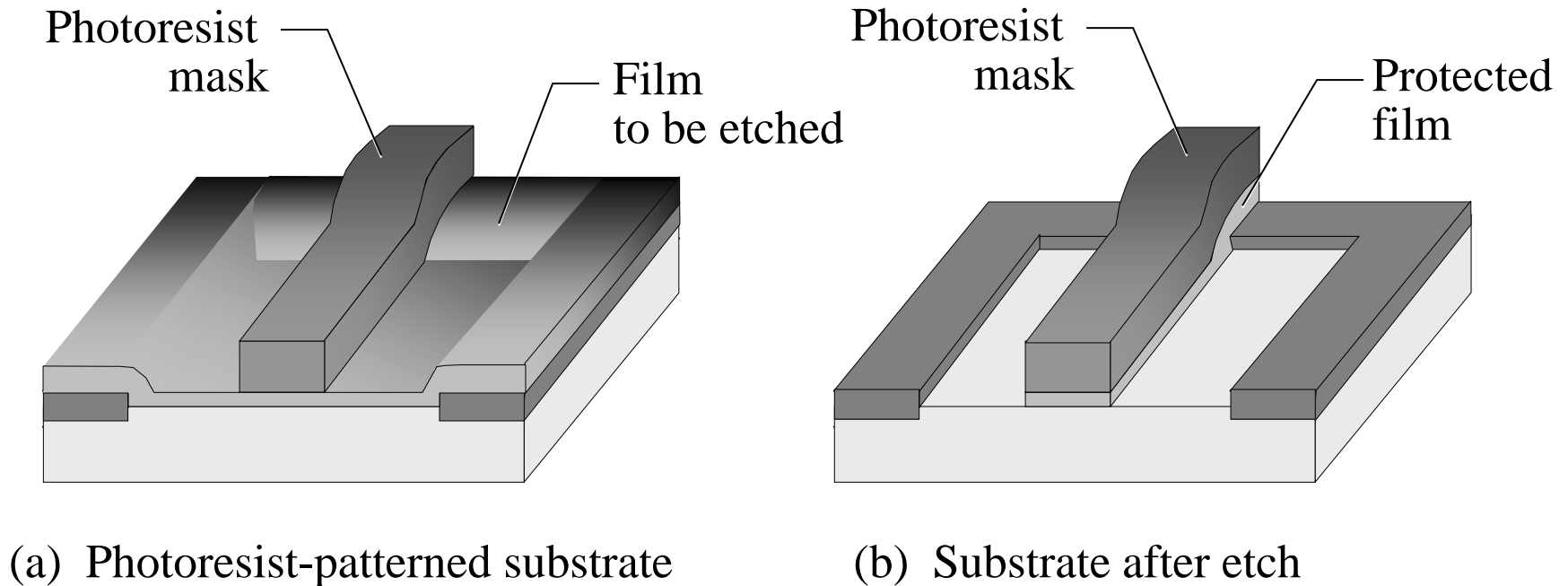
Etch

Objectives

After studying the material in this chapter, you will be able to:

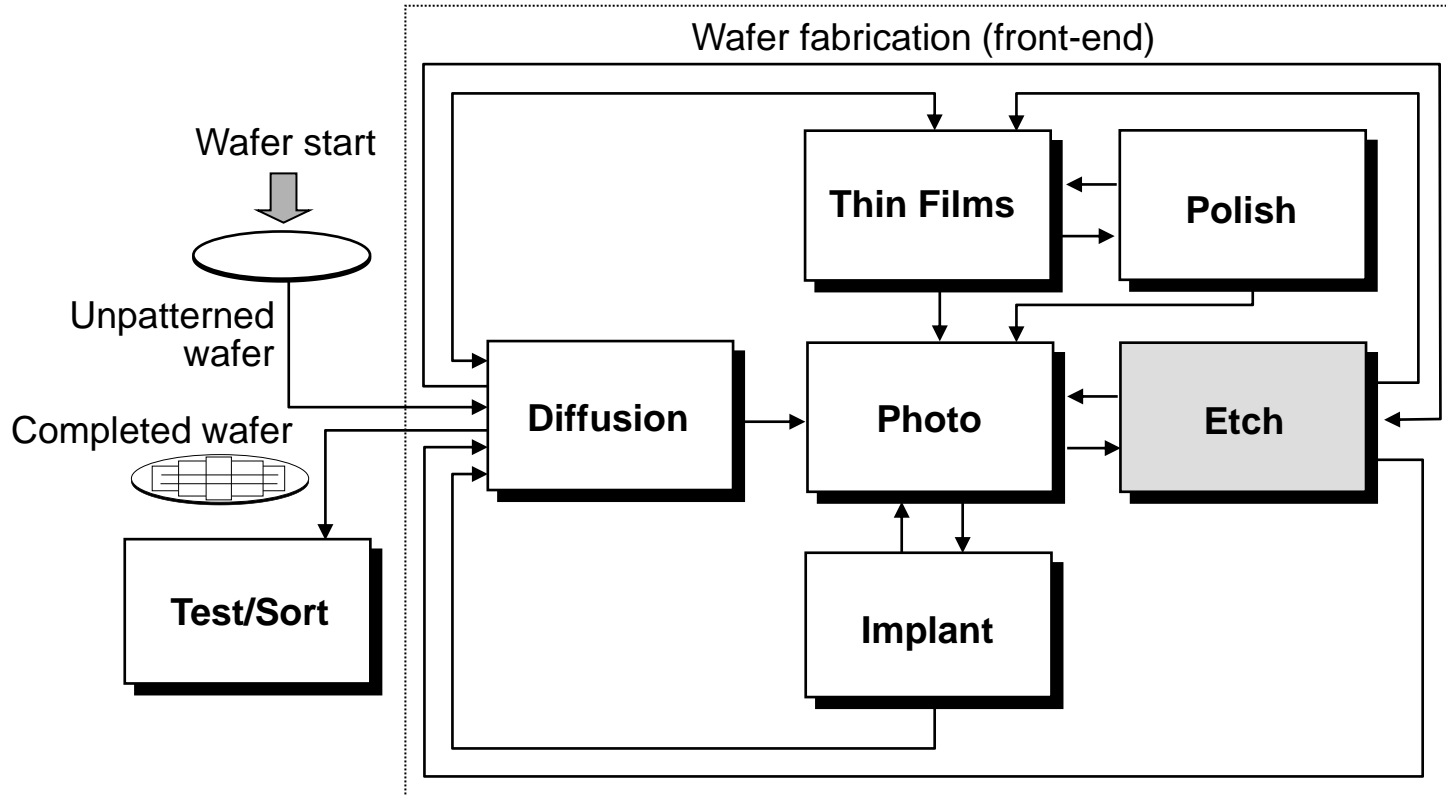
1. List and discuss **eight** important etch parameters.
2. Explain dry etch, including its advantages and how **etching** action takes place.
3. List and describe the **equipment** systems for seven dry plasma etch reactors.
4. Explain the benefits of **high-density plasma (HDP)** etch and the discuss the four types of HDP reactors.
5. Give an application example for dielectric, silicon and metal dry etch.
6. Discuss **wet** etch and its applications.
7. Explain how **photoresist** is removed.
8. Discuss etch inspection and important quality measures.

Applications for Wafer Etch in CMOS Technology



- Etch is the process of **selectively removing unneeded** material from the wafer surface by using either chemical or physical means
- The patterned resist layer is not attacked significantly by etchant

Process Flow in a Wafer Fab



Used with permission from Advanced Micro Devices

Figure 16.2

What Is Plasma

- A plasma is a **ionized gas** with equal numbers of positive and negative charges.
- A more precise definition: *a plasma is a **quasi-neutral** gas of charged and neutral particles which exhibits **collective** behavior.*
- Examples: Sun, flame, neon light, etc.

Generation of a Plasma

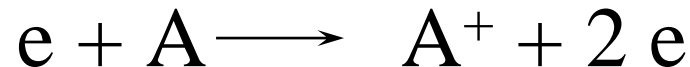
- **External power** is needed
- Radio frequency (RF) power is the most commonly used power source
- **Vacuum** system is required to generate a stable RF plasma

Plasma Basics

- A plasma is an ionized gas with equal numbers of positive and negative charges.
- Three important collisions:
 - *Ionization* generates and sustains the plasma
 - *Excitation-relaxation* causes plasma glow colors
 - *Dissociation* creates reactive free radicals

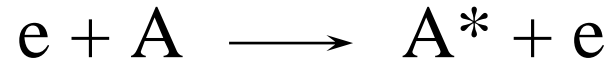
(1) Ionization

- Electron collides with neutral atom or molecule
- **Knock** out one of orbital electron



- Ionization collisions generate electrons and ions
- It **sustains** the stable plasma

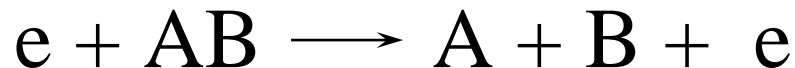
(2) Excitation-Relaxation



- Different atoms or molecules have different frequencies, that is why different gases have different **glow colors**.
- O₂: grayish-blue, N₂: pink, F: orange-red
- The change of the **glow colors** is used for etch and chamber clean process **endpoint**.

(3) Dissociation

- Electron collides with a molecule, it can break the chemical bond and generate free radicals:



- **Free radicals** have at least one unpaired electron and are chemically very **reactive**.
- Increasing chemical reaction rate
- **Very important for both etch and CVD.**

Etch Process

Categories of Etch Processes

- Wet Etch
 - Liquid, such as acids, bases, and solvent $> 3\mu\text{m}$
- Dry Etch
 - Using plasma created in the gaseous state
 - Primary method
- Three Major Materials to be Etched
 - Silicon: poly-Si
 - Dielectric: challenge is high-aspect ratio
 - Metal: Aluminum, no acceptable method for etching copper
- Patterned Etch Versus Unpatterned Etch

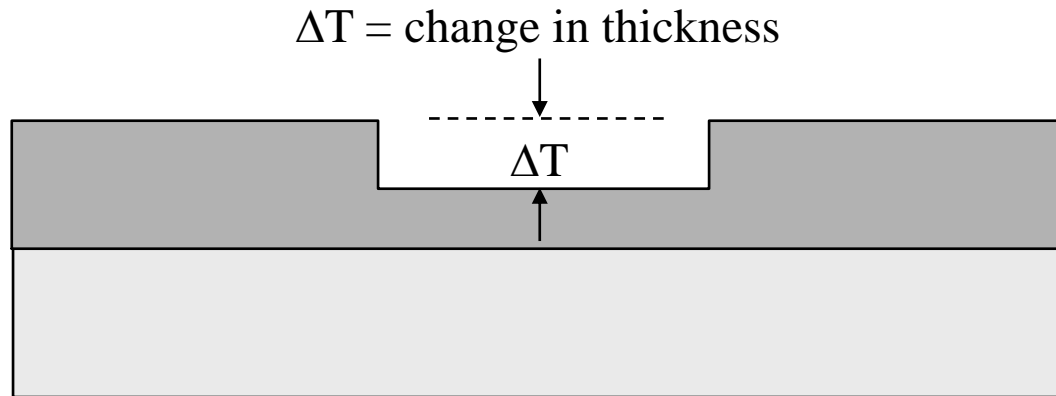
Etch on patterned and unpatterned wafer

- Patterned etch: poly-Si, metal, via, and contact hole, using a PR
- Unpatterned etch: etchback and strip
 - Etchback: reduce the overall thickness, e.g. W-etchback, **without PR**
 - Strip: usually strip masking layer e.g. STI nitride strip, Ti metal strip after salicide, PR striping
- Both etch processes can be performed using either dry-etch or wet-etch techniques

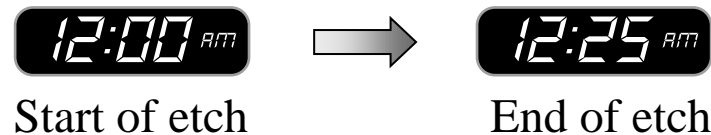
Etch Parameters

- Etch rate
- Etch profile
- Etch bias
- Selectivity
- Uniformity
- Residues
- Polymer formation
- Plasma-induced damage
- Particle contamination and defects

Etch Rate



t = elapsed time during etch



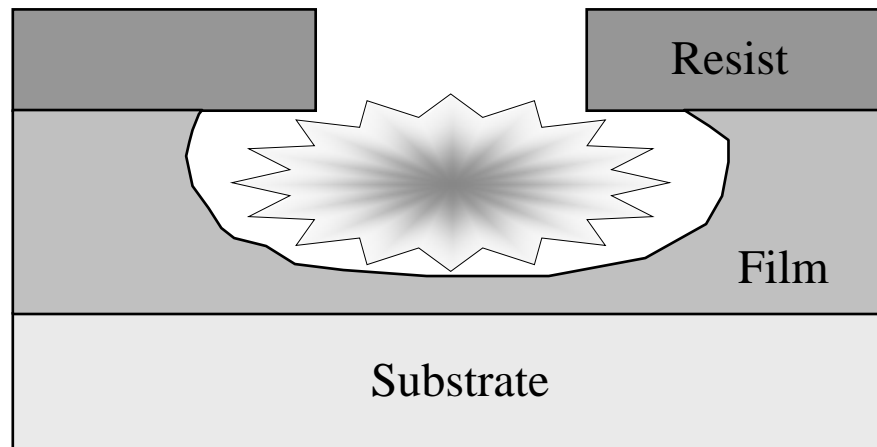
- Etch rate: $\text{\AA}/\text{min}$
- The depth of the etched opening is step high
- It is desirable to have a high etch rate to keep wafer throughput high
- **Loading effect:** wafers with small surface area for etching will etch faster
- Because etch rate is generally proportional to the concentration of the etchant

Figure 16.3

Wet Chemical Isotropic Etch

- Etch profile refers to the shape of the sidewall of the etched feature
- **Isotropic** etch profile leads to a undercutting, results in an undesirable **loss** of the linewidth

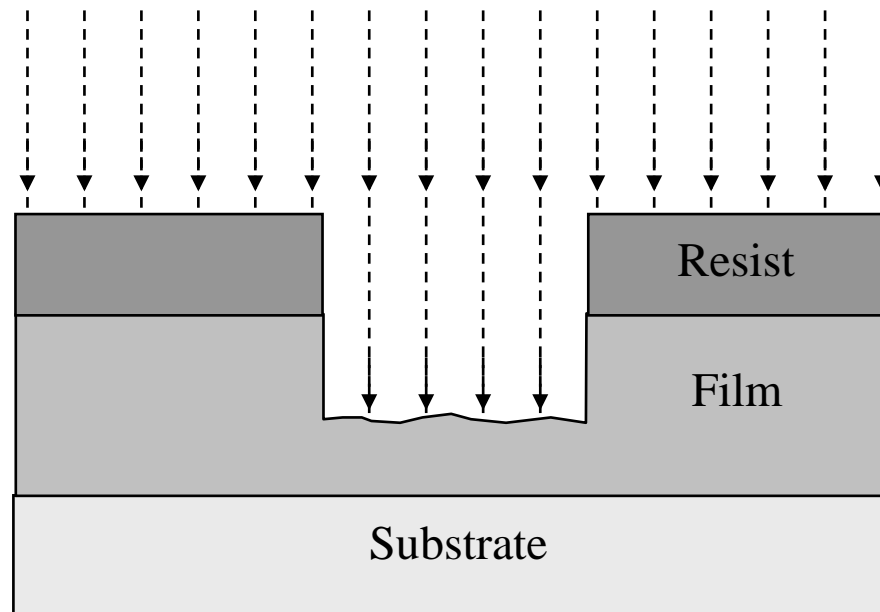
Isotropic etch - etches in all directions at the same rate



Anisotropic Etch with Vertical Etch Profile

- The rate of etching is on only **one direction** perpendicular to the wafer surface
- There is very little lateral etching activity
- This **leaves** vertical sidewalls, permitting a higher packing density of etched features on the chip
- With smaller geometries, the etch profiles have **higher aspect ratios**
- It is difficult to get etchant chemicals **in** and reaction by-products **out** of the high-aspect ratio openings

Anisotropic etch - etches
in only one direction



Sidewall Profiles for Wet Etch Versus Dry Etch

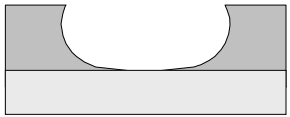
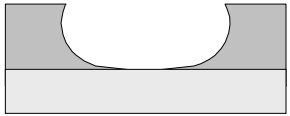
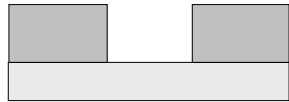
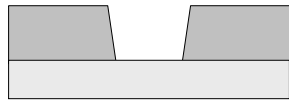
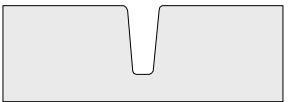
Type of Etch	Sidewall Profile	Diagram
Wet Etch	Isotropic	
Dry Etch	Isotropic (depending on equipment & parameters)	
	Anisotropic (depending on equipment & parameters)	
	Anisotropic – Taper	
	Silicon Trench	

Table 16.1

Etch Bias

- Etch bias is a measure of the change in linewidth or space of a critical dimension (CD) after performing an etch process
- Etch bias = $W_b - W_a$

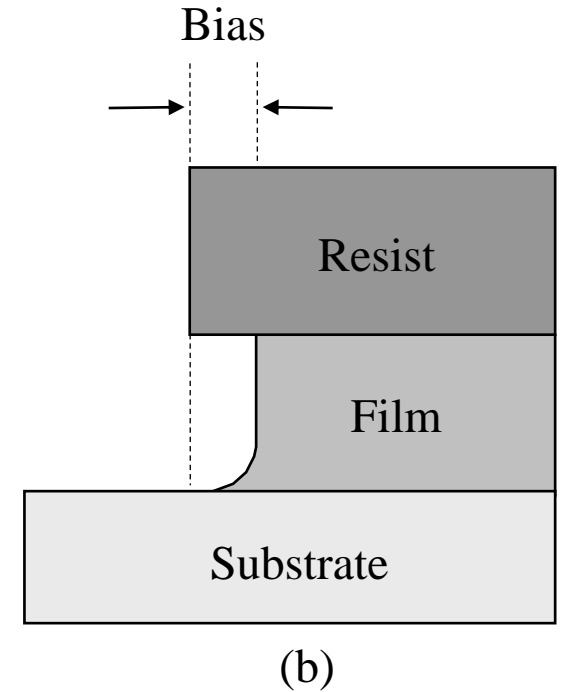
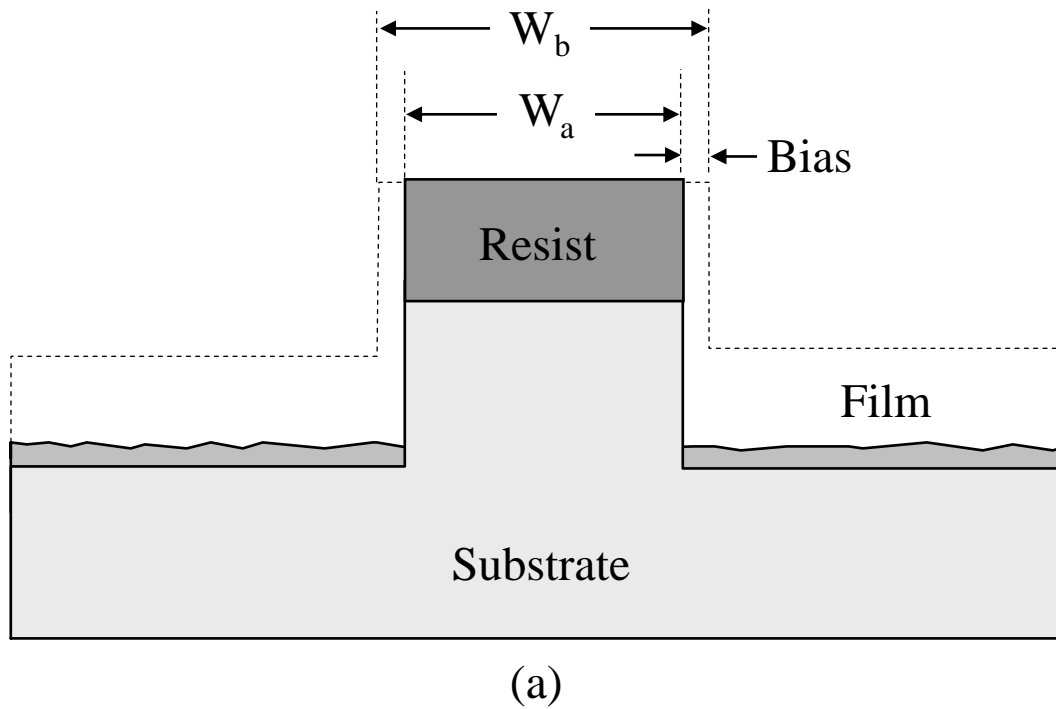


Figure 16.6

Etching Undercut and Slope

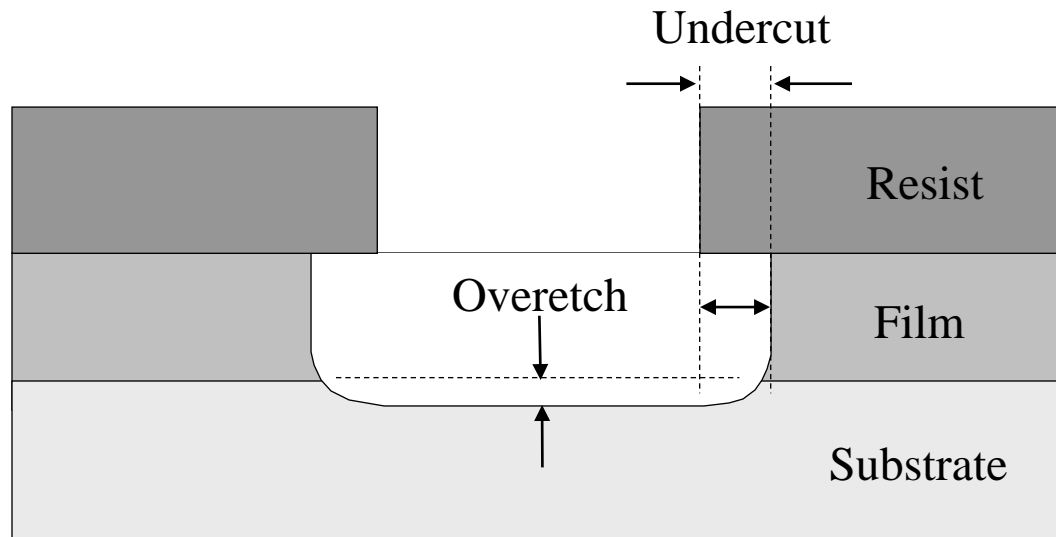


Figure 16.7

Etch Selectivity

- **Selectivity** represents how much faster one film etches than another film under the same etch conditions
- It is defined as the etch rate of the material being etching relative to the etch rate of another material
- A high selectivity etch process **does not** etch the underlying film (etching stops at the right depth) and the protective photoresist is not etched
- **High selectivity** is necessary, the smaller the CD then the higher the selectivity must be
- A good selectivity ~ **100**
- With poor selectivity, needs an **endpoint detection** system

$$S = \frac{E_f}{E_r}$$

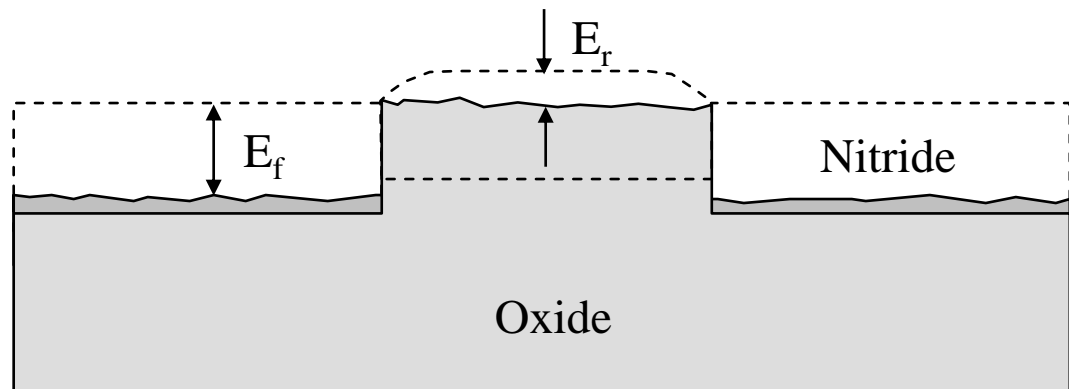
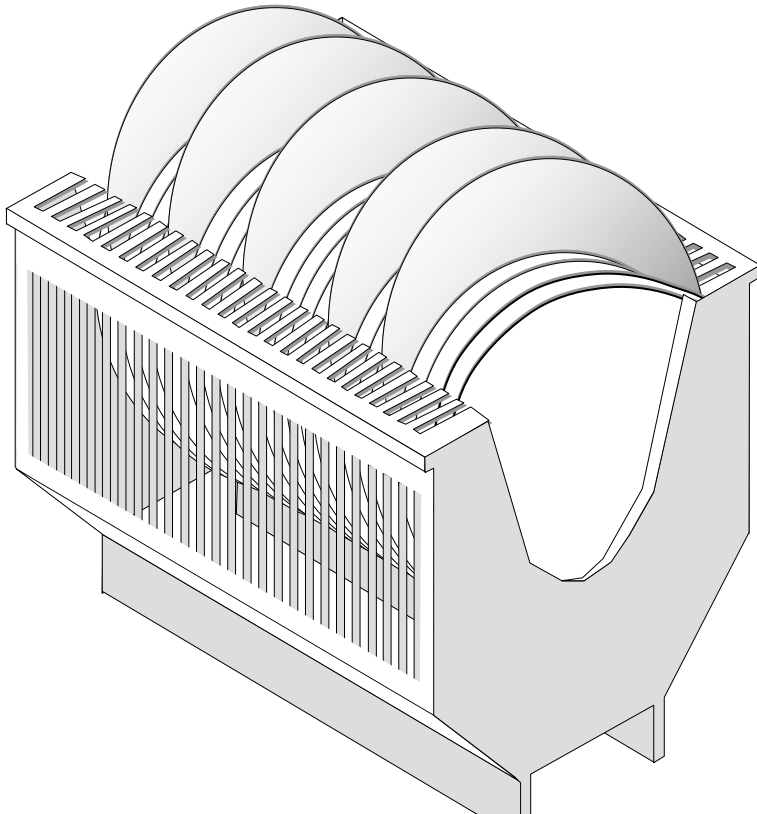


Figure 16.8

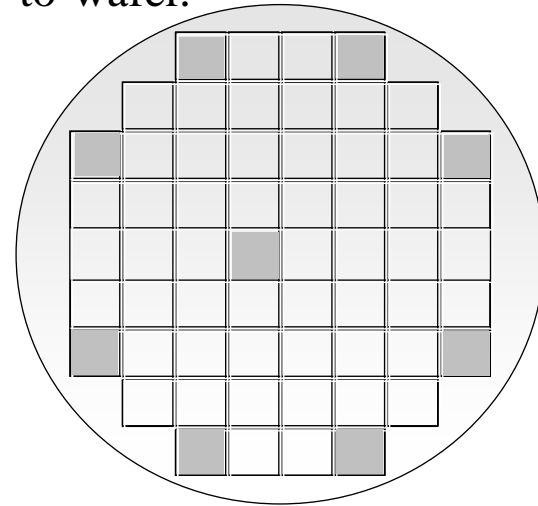
Etch Uniformity

- Etch uniformity is a measure of the capability of the process to etch **evenly** across the entire surface area of the wafer, wafer-to-wafer, and lot-to-lot
- **Non-uniformity results in additional over etch**

Randomly select 3 to 5 wafers in a lot

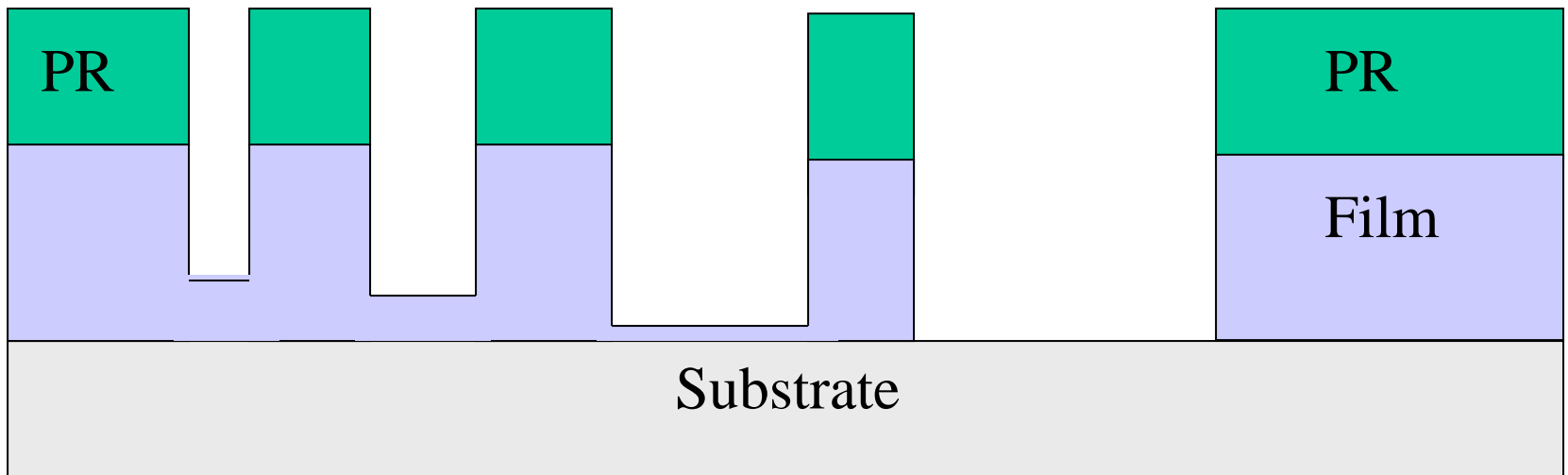


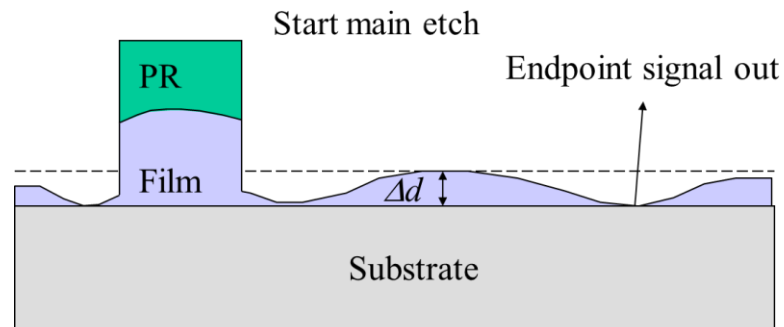
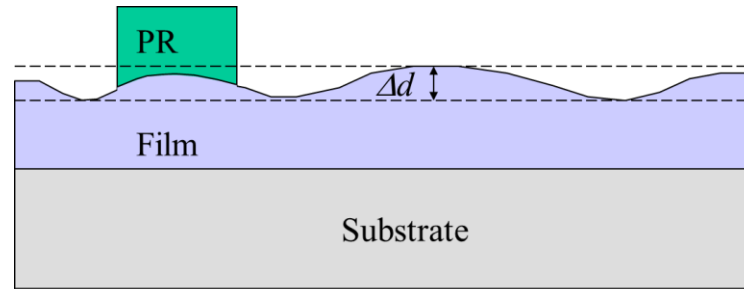
Measure etch rate at 5 to 9 locations on each wafer, then calculate etch uniformity for each wafer and compare wafer-to-wafer.



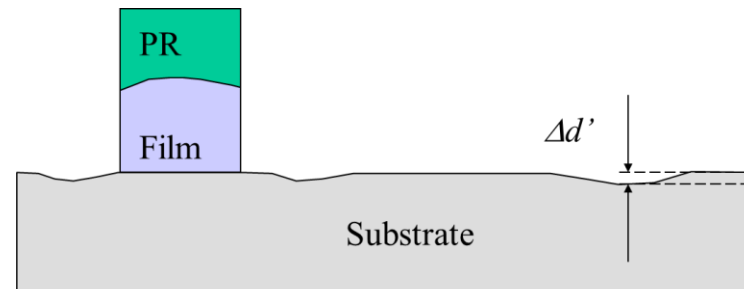
Micro Loading

- Aspect ratio dependent etching (**ARDE**), referred to as **micro-loading**: high-aspect ratio opening etch slower than trenches with a small aspect ratio opening
- An **overetch** is sometimes done at the end of etch process to remove residues





Before over etch



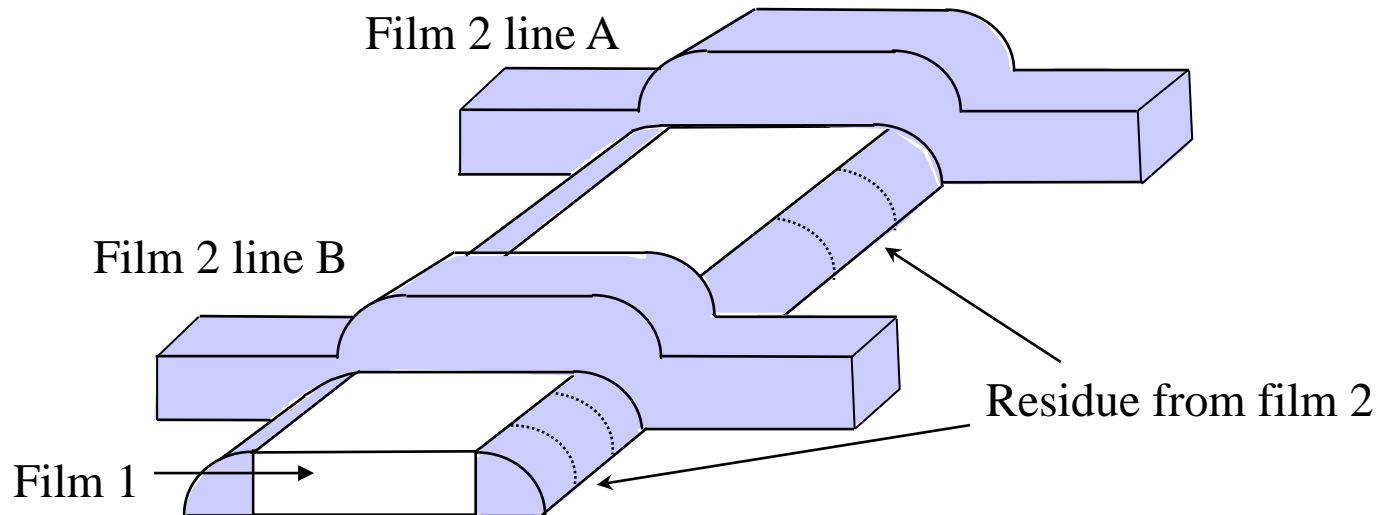
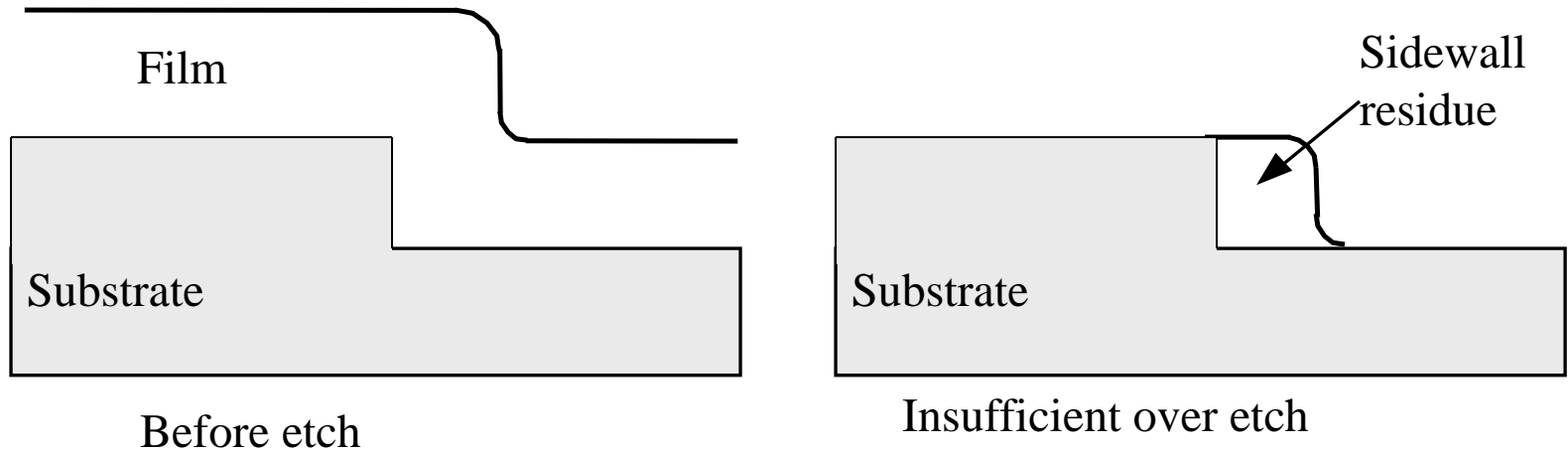
After over etch

- The minimum requirement of the film for substrate selectivity during the over etch process step is: $S > \Delta d / \Delta d'$

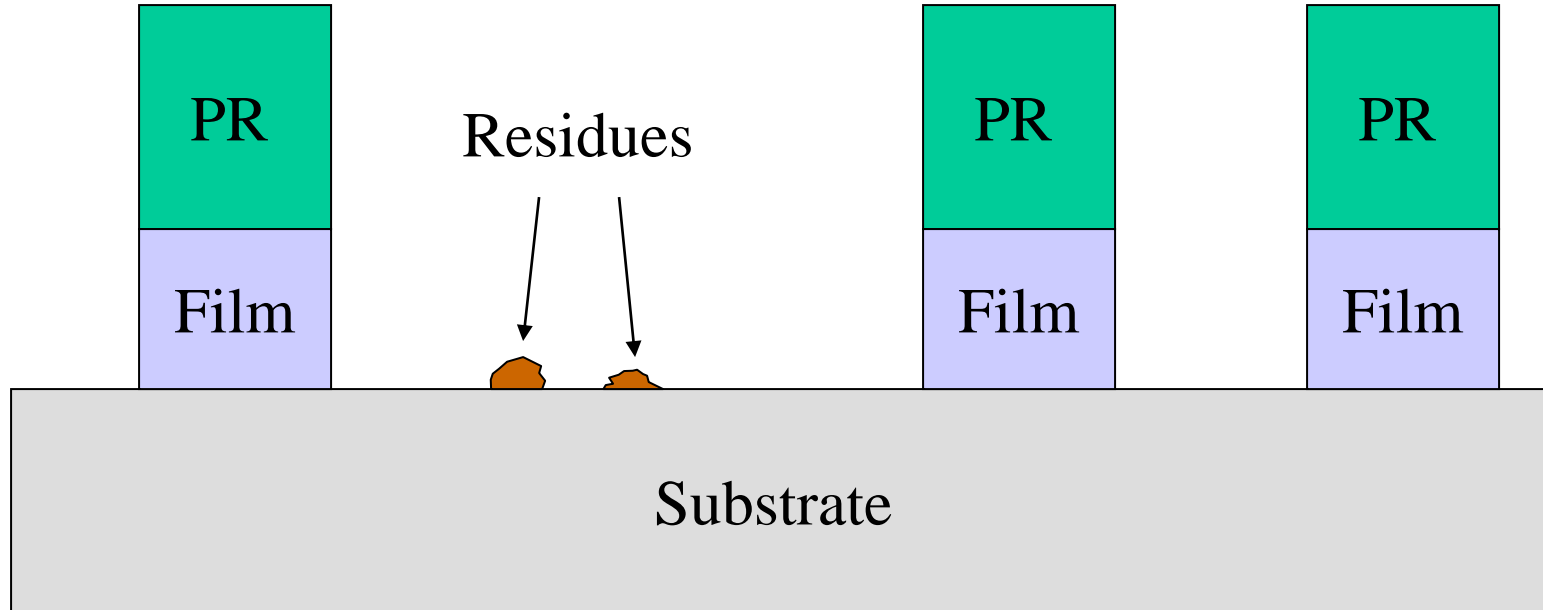
Residues

- Unwanted leftovers
- Causes
 - insufficient over etch
 - non-volatile etch byproducts
- Adequate over etch
- Removal of **non-volatile** residues
 - Sufficient ion bombardment to dislodge
 - Right amount of **chemical etch** to scoop
- Oxygen plasma ashing: **Organic** residues
- Wet chemical clean: **inorganic** residues

Insufficient Over Etch

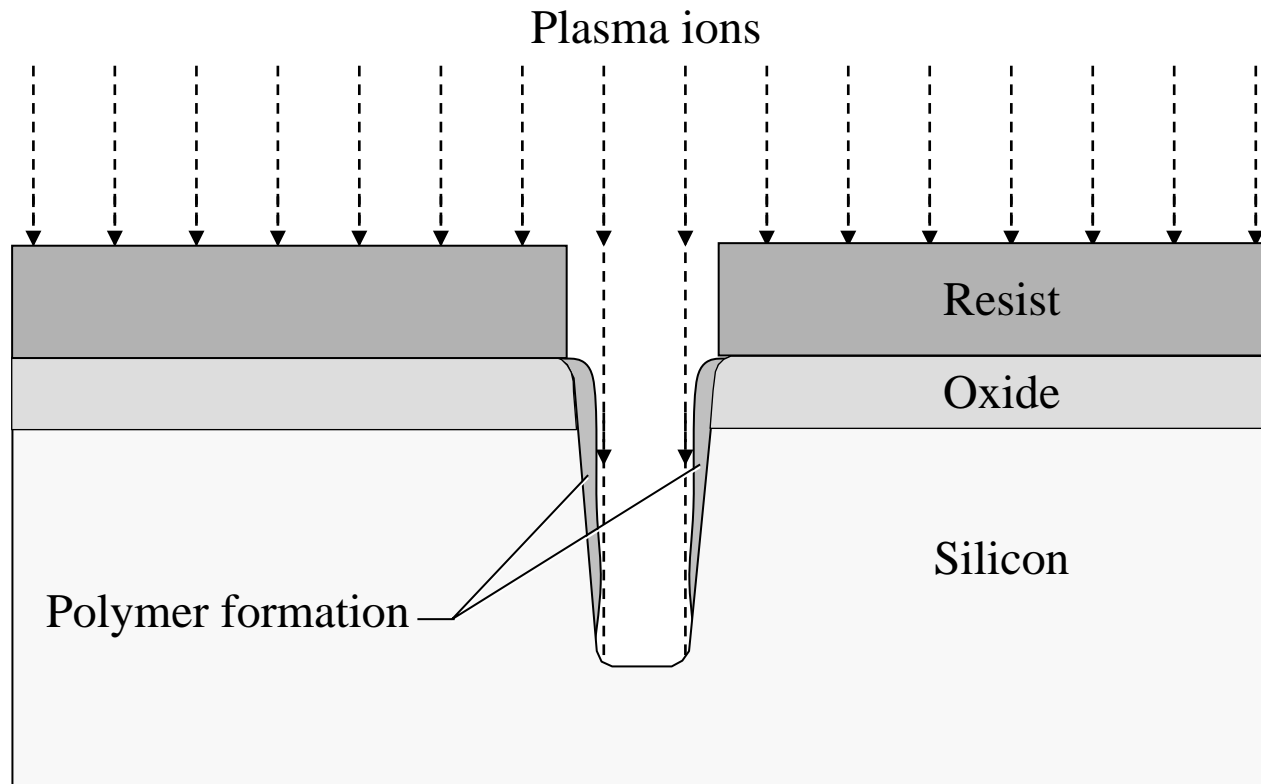


Non-volatile Residue on Surface

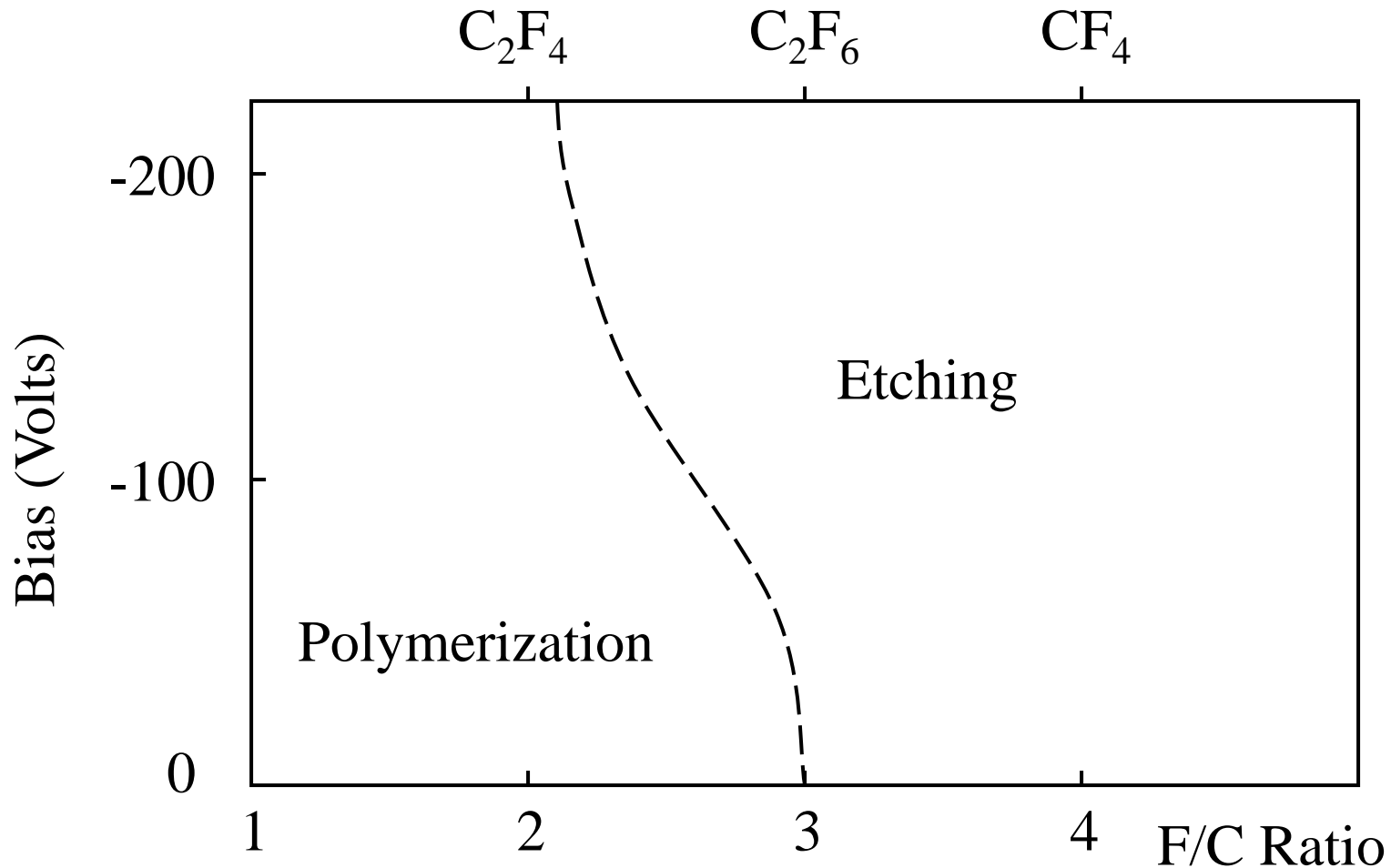


Polymer Sidewall Passivation for Increased Anisotropy

- A polymer formation is sometimes intentionally deposited on the sidewalls of the etch feature to form an etch-resistant film that prevents lateral etching
- It produces highly **anisotropic** feature
- The polymers comes from **PR carbon** converted into **polymers** during etching and combines with etching gases (i.e., **C₂F₄**) and etch by-products to form
- The polymer chains have strong **carbon-fluorine** bonds that are difficult to oxidize and remove
- It must be removed after etch process, requires special gas chemistry or strong **solvents**



F/C Ratio, DC Bias and Polymerization



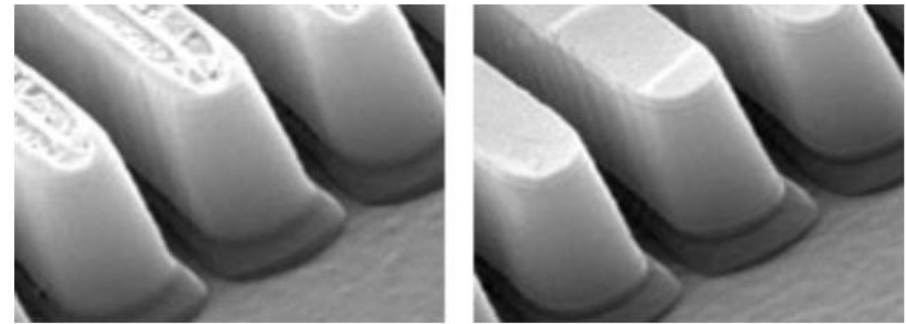
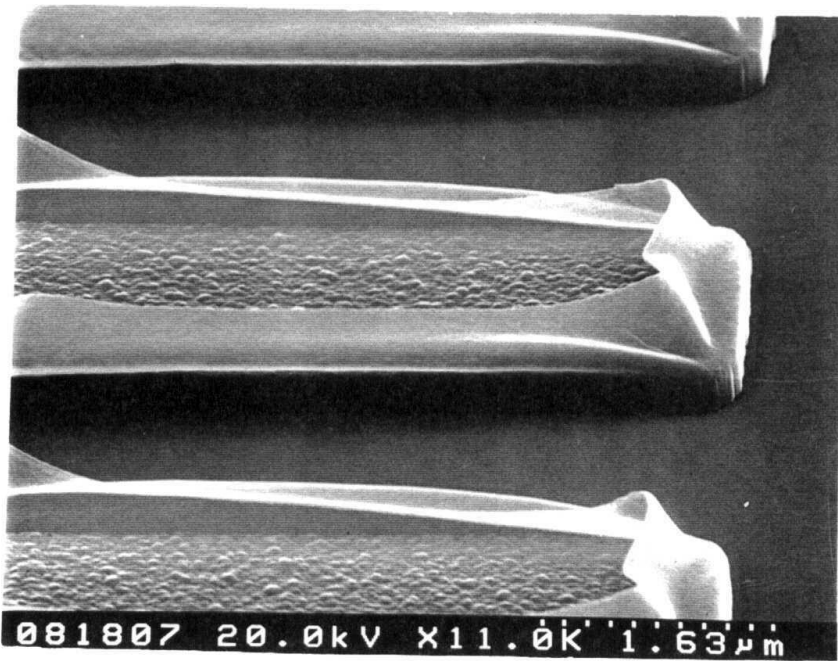


Figure 1. ACT 935 Stripper. Process: Strip (75°C, 20min.)

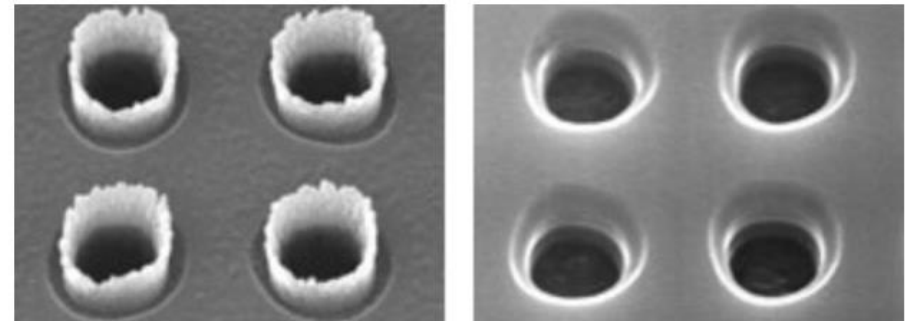


Figure 2. ACT 935 Stripper. Process: Strip (75°C, 30min.)

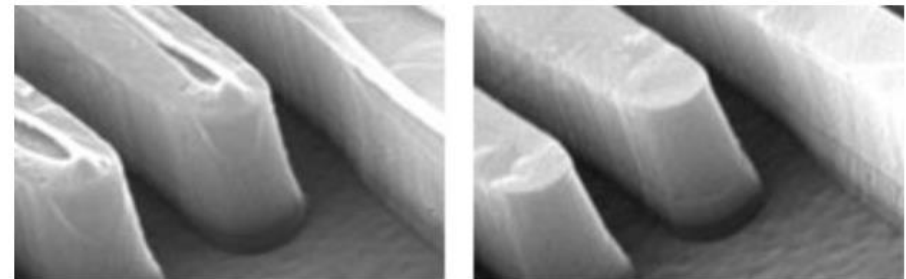
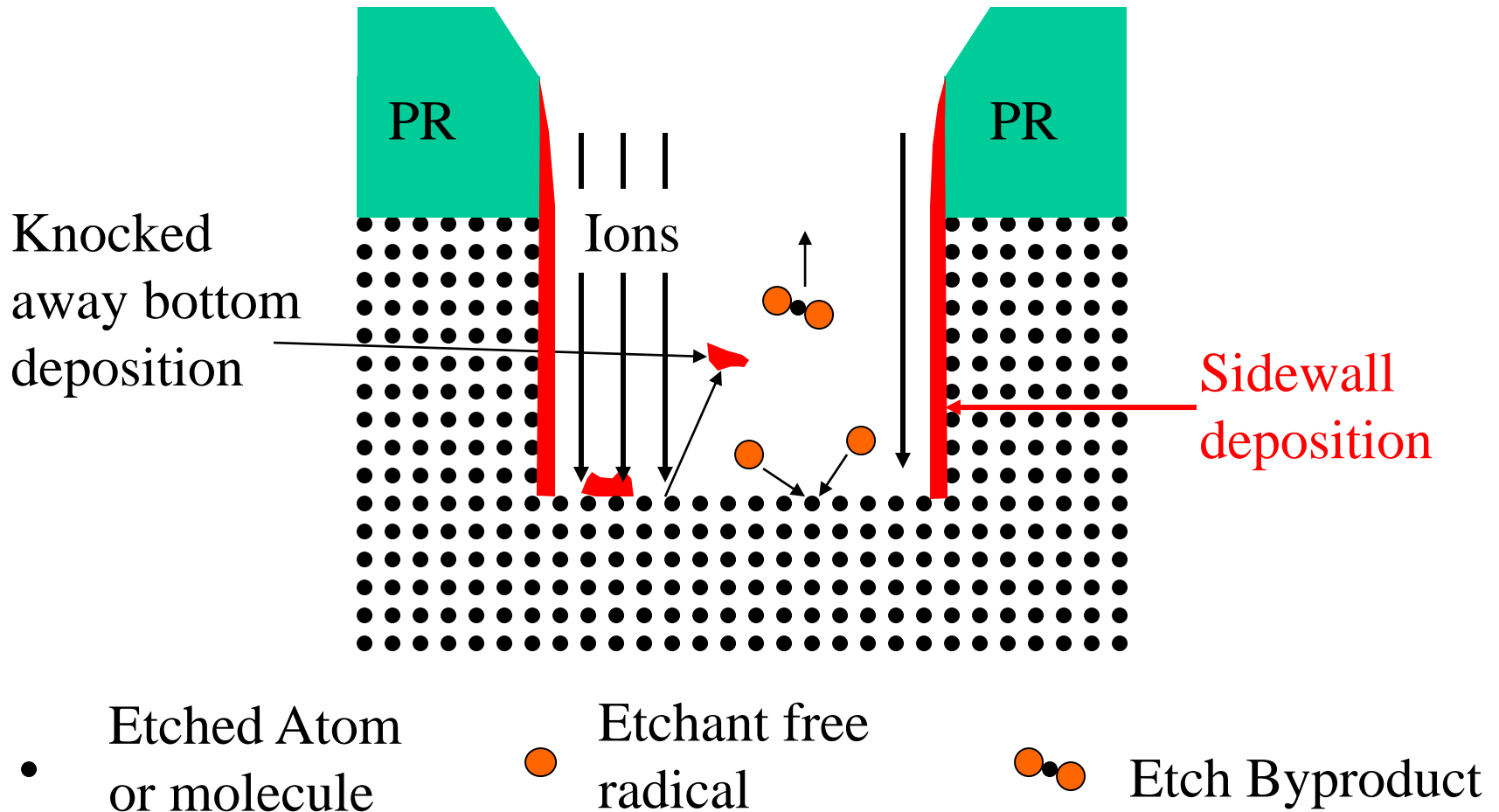


Figure 3. Process: Strip (70°C, 20 min.) DI Rinse (23°C, 3 min.)

- After oxide etching, the polymer should be removed, especially in contact holes. The polymer can be removed by an O_2 and CF_4 plasma treatment CF_4 is better at removing all the polymer and even some damaged substrate.

Blocking Mechanism



Dry Etch

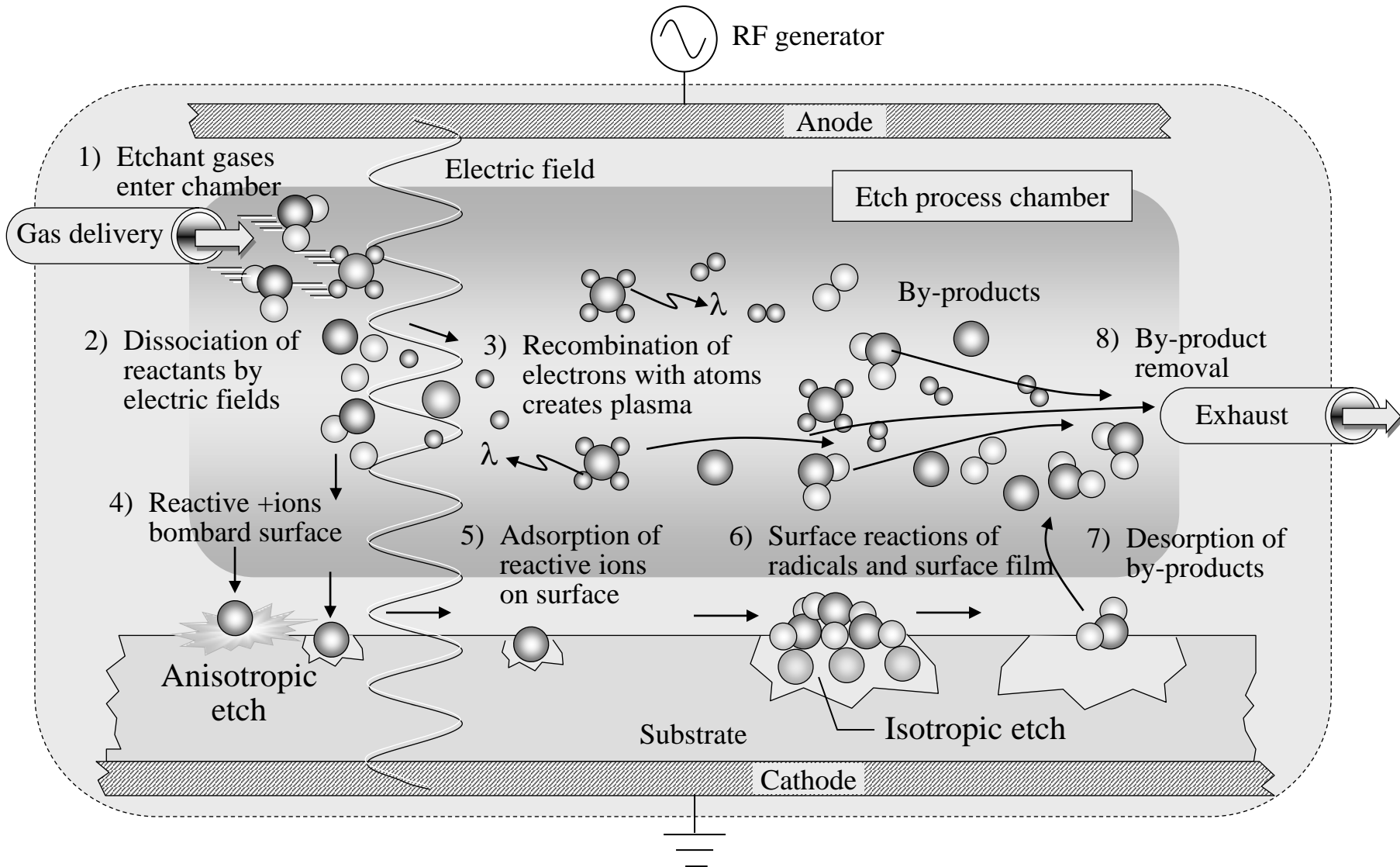
- Advantages of Dry Etch over Wet Etch
- Etching Action
- Potential Distribution

Advantages of Dry Etch over Wet Etch

1. Etch profile is anisotropic with excellent control of sidewall profiles.
2. Good CD control.
3. Minimal resist lifting or adhesion problems.
4. Good etch uniformity within wafer, wafer-to-wafer and lot-to-lot.
5. Lower chemical costs for usage and disposal.

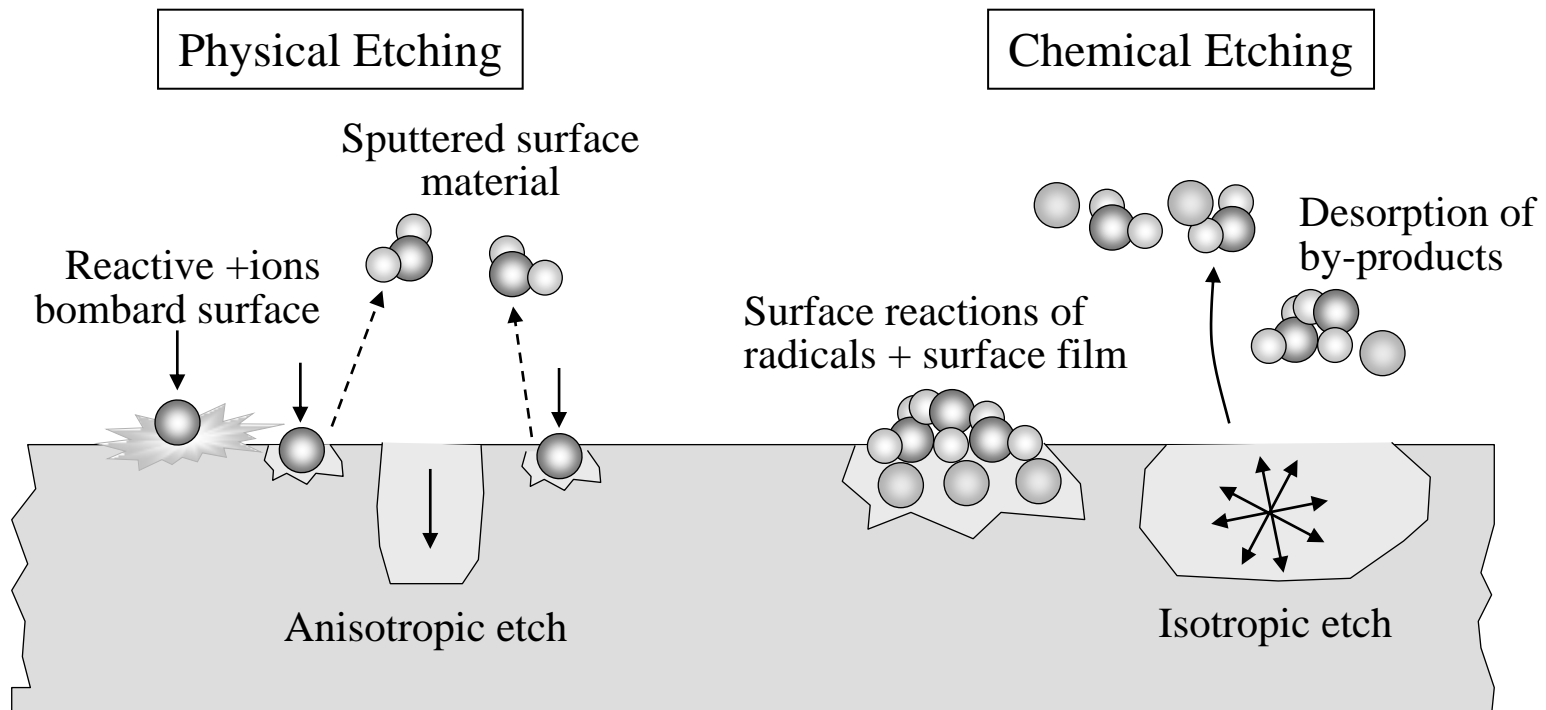
- Primary disadvantages are **poor selectivity** to the underlying layer, risk for device **damage from plasma**, and **expensive** equipment

Plasma Etch Process of a Silicon Wafer



Chemical and Physical Dry Etch Mechanisms

- Etching action in dry etch is achieved by either a **chemical** or a **physical** technique or a **combination** chemical/physical technique
- Chemical etching produces poor CD control because of its isotropic profile
- Volatile by-products of the reaction are removed by the low-pressure pumping system
- A non-reacting **Ar** is used as a bombarding positive ions, **sputter-etch** action
- Sputter etching produces a high etch rate, but it does have **poor selectivity**
- Another problem of sputtering is its **not volatile** and may **re-deposit** back on the wafer, causing particulate and chemical contamination



Chemical Versus Physical Dry Plasma Etching

- Combined physical and chemical etch produces **good CD** control with fair selectivity and is often preferred for most of the etch processes
- Combined process needs the RF electric field is **perpendicular** to the wafer surface

Etch Parameter	Physical Etch (RF field perpendicular to wafer surface)	Chemical Etch (RF field parallel to wafer surface)	Chemical Etch	Combined Physical and Chemical
Etch Mechanism	Physical ion sputtering	Radicals in plasma reacting with wafer surface*	Radicals in liquid reacting with wafer surface	In dry etch, etching includes ion sputtering and radicals reacting with wafer surface
Sidewall Profile	Anisotropic	Isotropic	Isotropic	Isotropic to Anisotropic
Selectivity	Poor/difficult to increase (1:1)	Fair/good (5:1 to 100:1)	Good/excellent (up to 500:1)	Fair/good (5:1 to 100:1)
Etch Rate	High	Moderate	Low	Moderate
CD Control	Fair/good	Poor	Poor to non-existent	Good/excellent

* Used primarily for stripping and etchback operations.

Schematic View of Reactor Glow Discharge with Potential Distribution

- The power electrode in an etch reactor develops **a negative self-bias voltage** relative to **ground** because fast **moving electrons** leave the plasma to strike the electrode
- After a certain amount of negative charge, electrons are repelled from the electrode, thus creating the **dark space (ion sheath)** region with positive ionic charge
- The plasma must assume a positive potential to produce a potential of equivalent magnitude at the grounded electrode

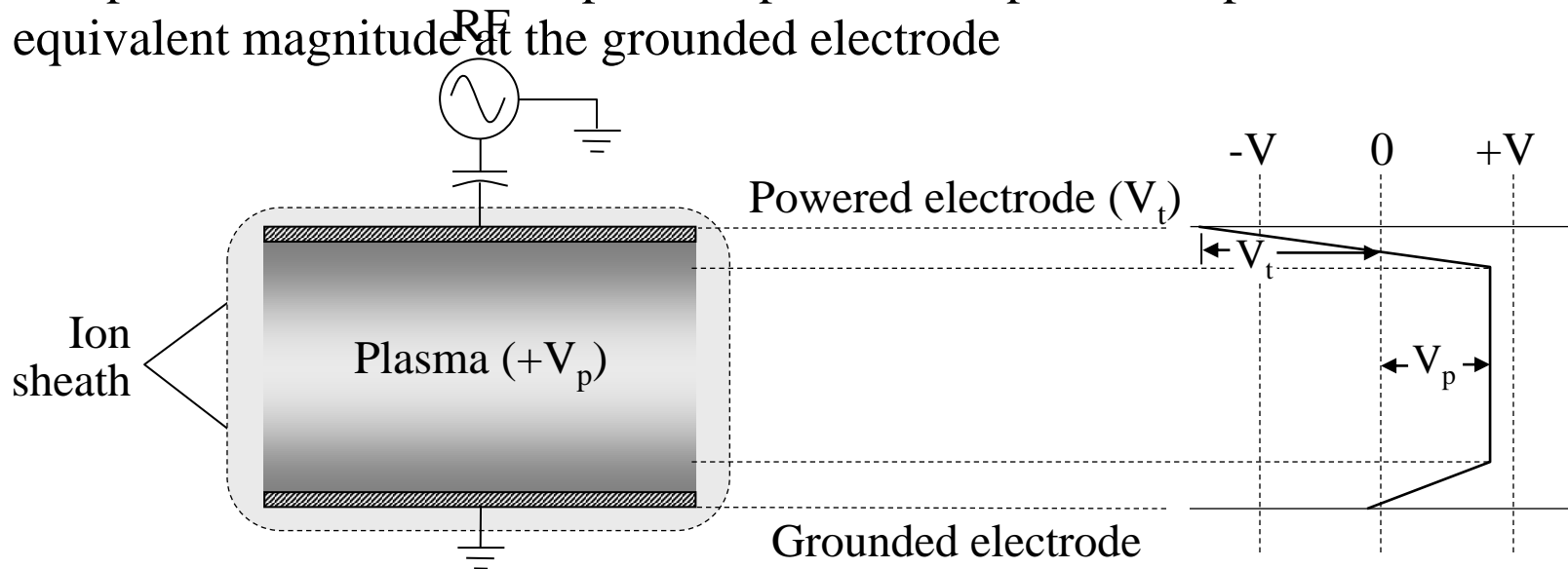
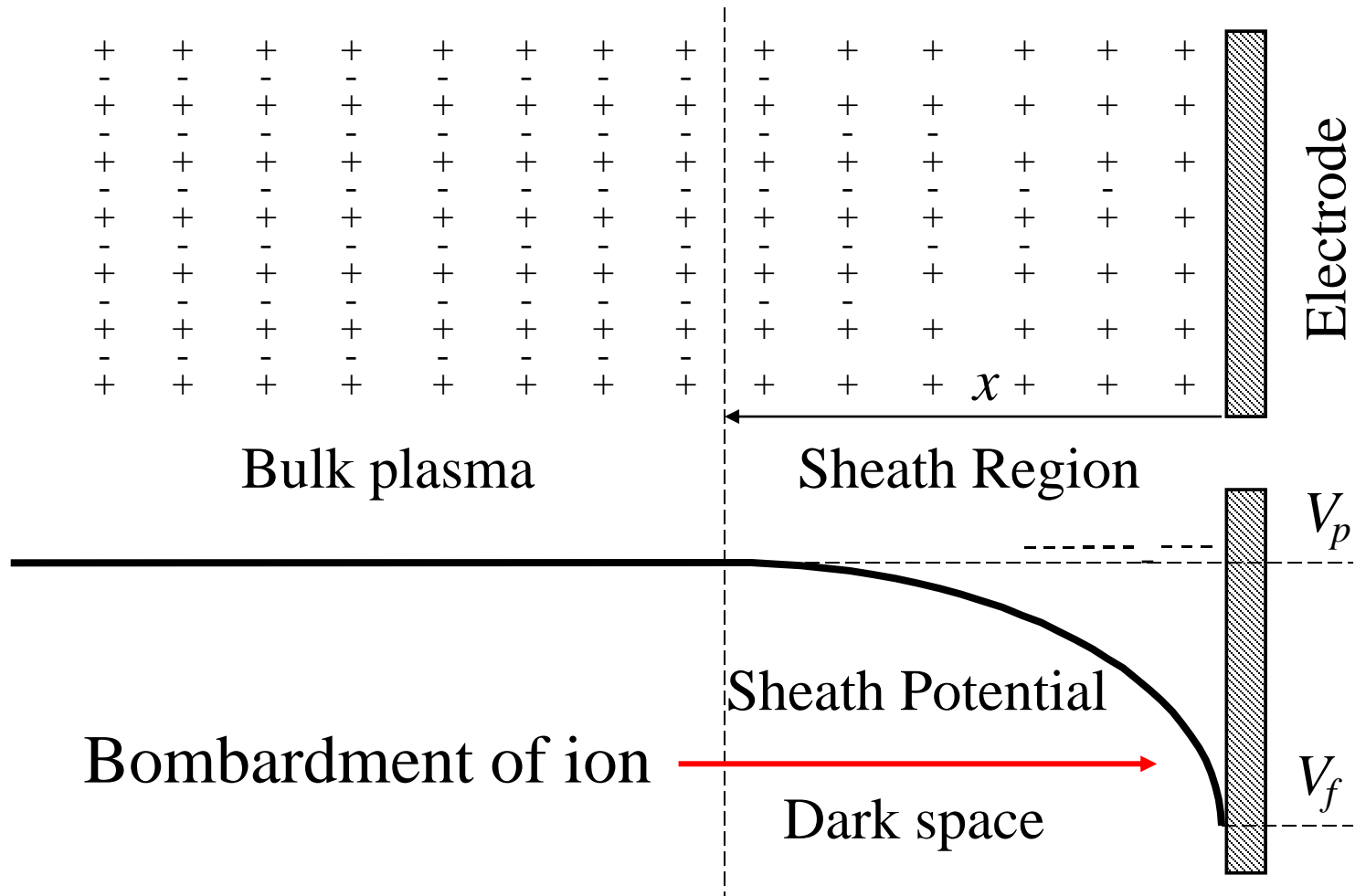


Figure 16.13

Sheath Potential



Effects of Changing Plasma Etch Parameters

Increase (↑) or Decrease (↓) in Etch Control Parameters		Ion Energy	DC Bias	Etch Rate	Selectivity	Physical Etch
RF Frequency	↑	↓	↓	↓	↑	↓
	↓	↑	↑	↑	↓	↑
RF Power	↑	↑	↑	↑	↓	↑
	↓	↓	↓	↓	↑	↓
DC Bias	↑	↑	↑	↑	↓	↑
	↓	↓	↓	↓	↑	↓
Electrode Size	↑	↓	↓	↓	↑	↓
	↓	↑	↑	↑	↓	↑

- If the frequency is reduced, **then ions efficiently** cross the plasma dark space in a small fraction of an RF cycle. This increases the ion energy and etch rate.
- For asymmetrical electrode size, smaller size has **larger voltage drop, high ion bombardment**

Plasma Etch Reactors

- Barrel plasma etcher – PR strip
- Parallel plate (planar) reactor
- Downstream etch systems – PR strip
- Triode planar reactor – 單晶矽
- Ion beam milling – Au/Pt/Cu 純轟擊有加磁
- Reactive ion etch (RIE) – 高偏壓無磁
- High-density plasma etchers – 低偏壓有磁
- Etch System Review
- Endpoint Detection
- Vacuum for Etch Chambers

Typical Barrel Reactor Configuration

- In general, **fluorine etches SiO_2** ; **chlorine etch aluminum**; **chlorine, fluorine, and bromine etch silicon**; and **oxygen removes PR**
- Prior to the 1980s, barrel reactor is popular for **batch** process, and no longer common
- It is an almost **pure chemical isotropic etching**
- The wafers are placed parallel to the electric field to minimize physical etching
- It primary used for **stripping photoresist**

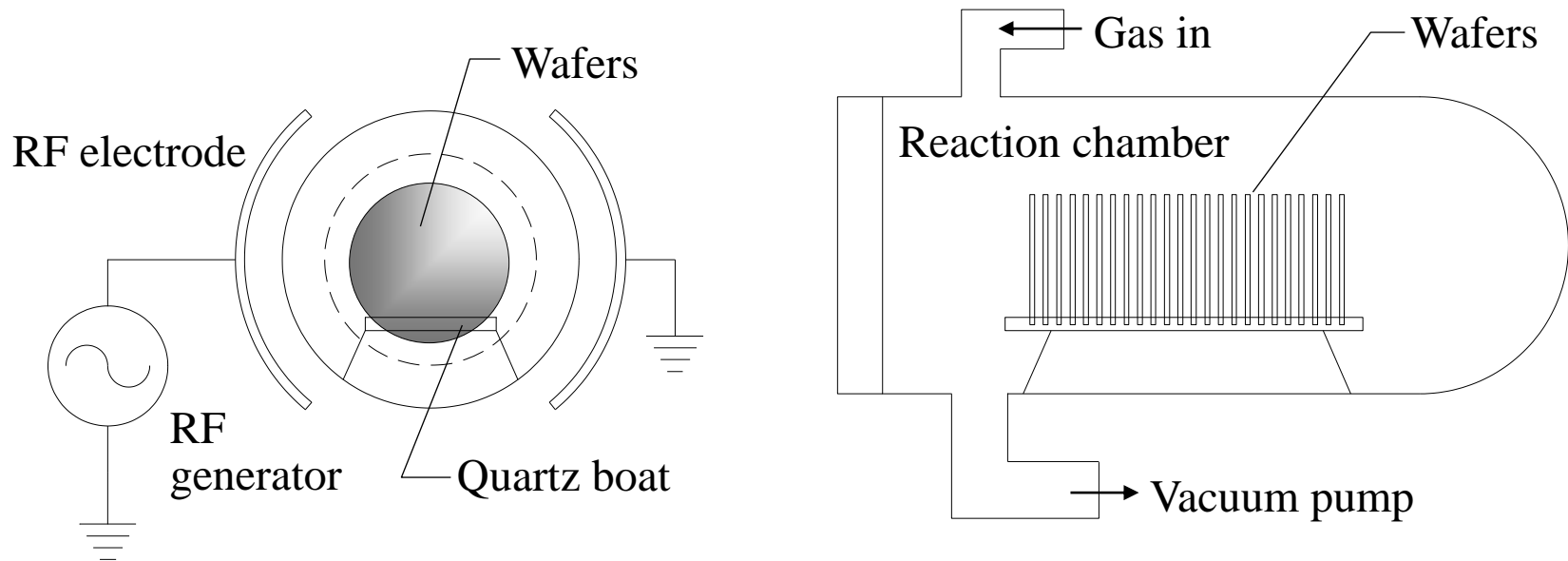
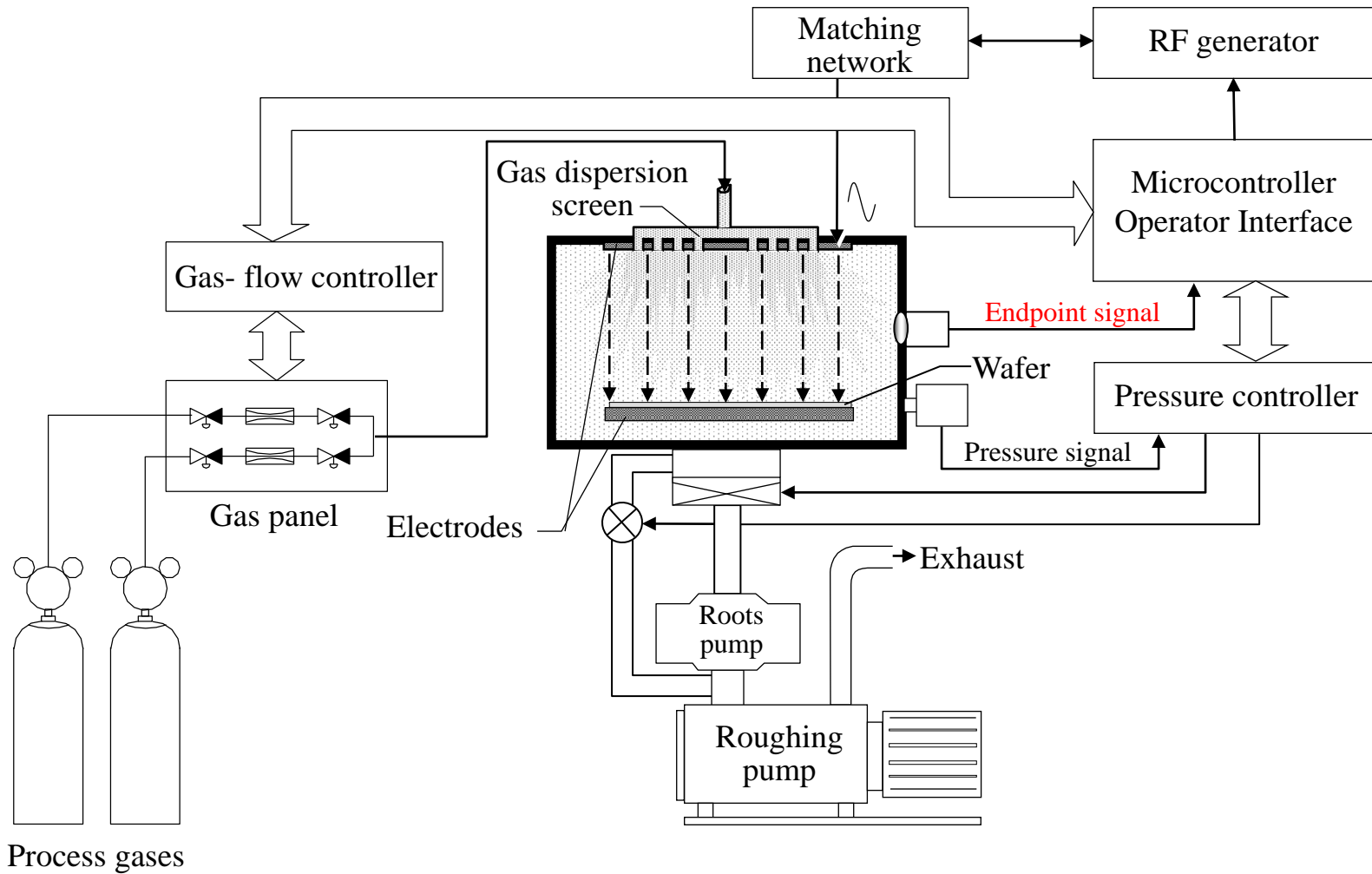


Figure 16.14

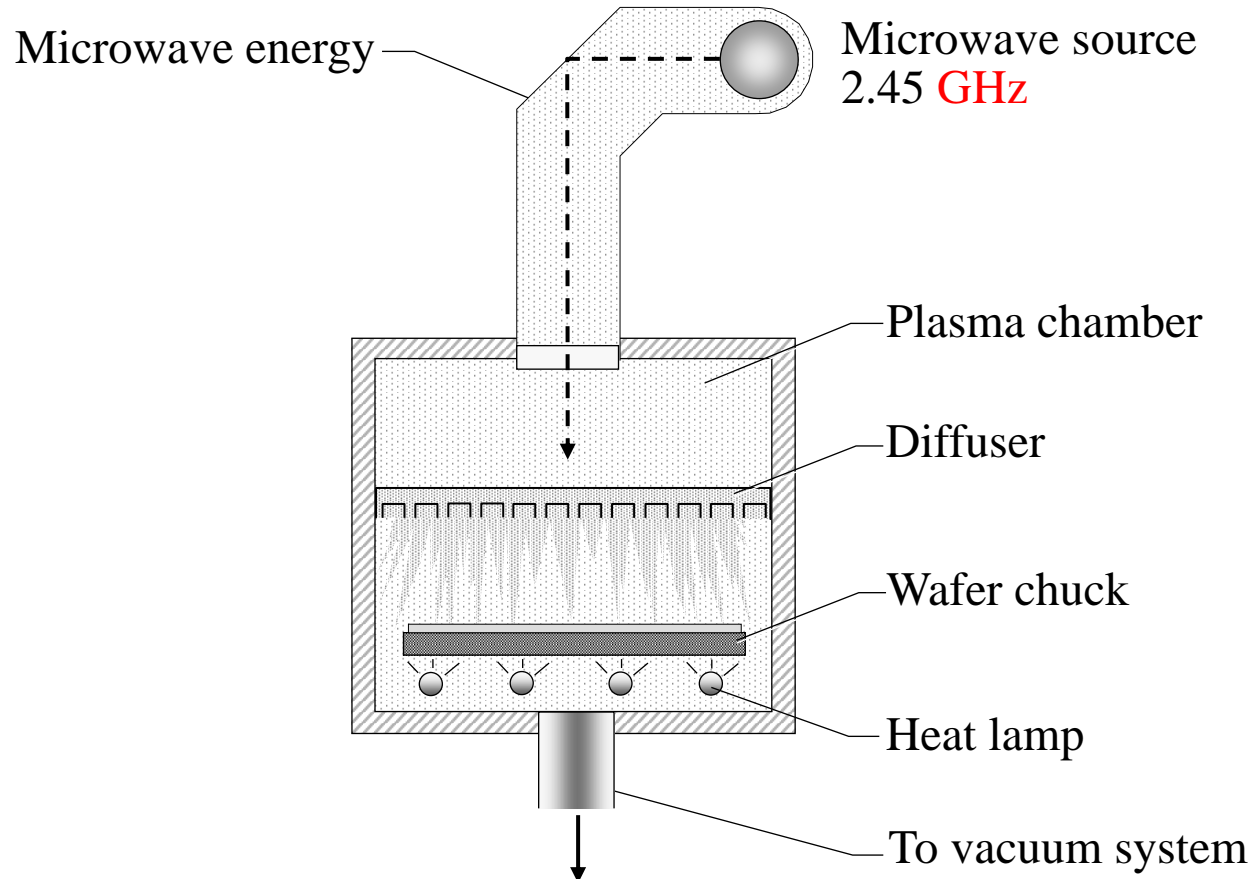
Parallel Plate Plasma Etching



- Wafer on the grounded electrode is the plasma etch mode
- Wafer on RF power electrode, resulting in high-energy ion bombardment and said to be in the reactive ion etch mode, its energy is ~ 10 times higher than etch mode

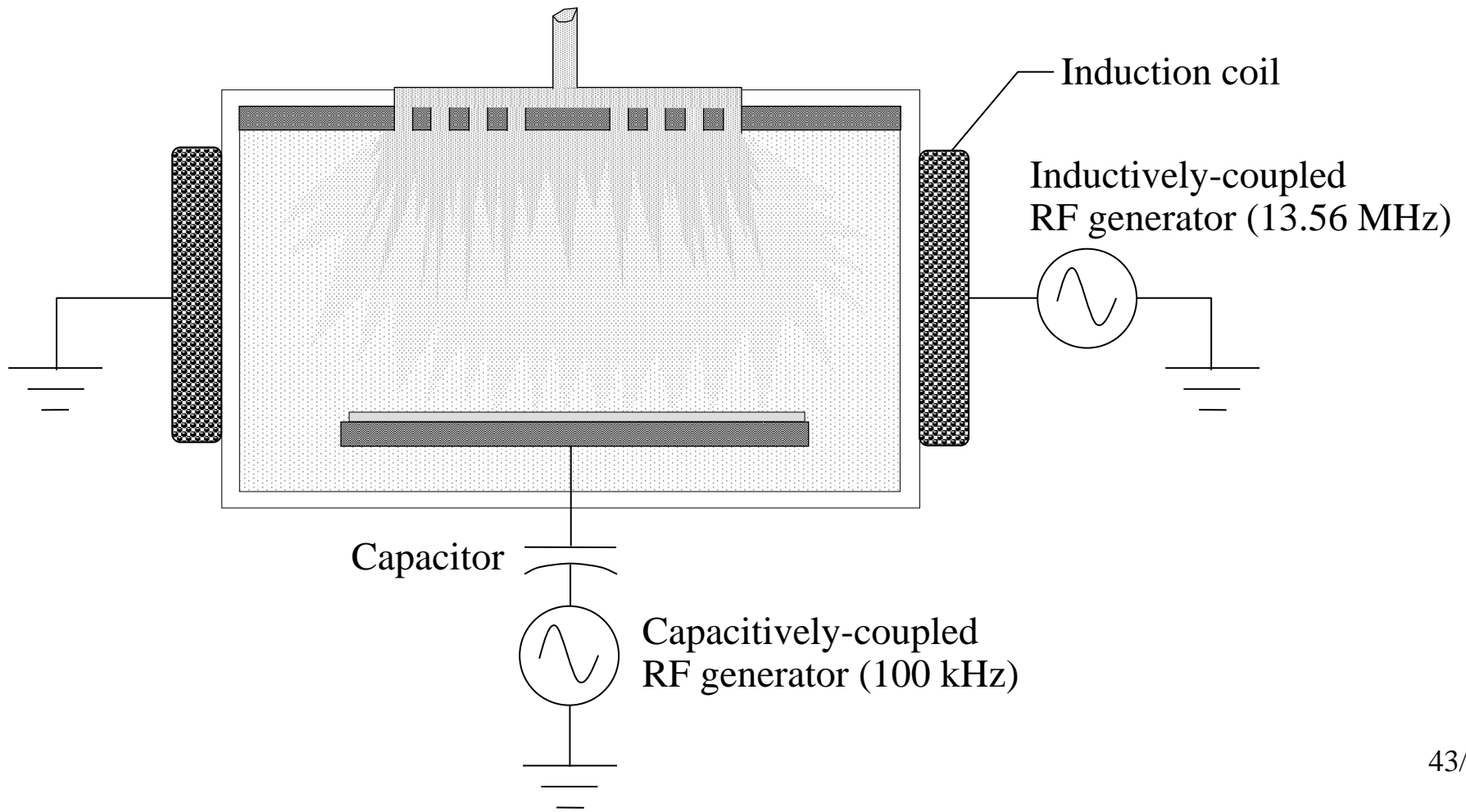
Schematic of a Downstream Reactor

- Exposure to ion bombardment increases the probability of device damage and heat
- Solution: **downstream** reactor, in which the plasma is formed in a separate source ~ 0.1 -1 torr, transferred to the process chamber, and uniformly distributed over the heated wafer surface
- Since it is **no ions** to create directional etching, it is **chemical** etching, **isotropic**, and are often used to **remove resists** or other noncritical layers

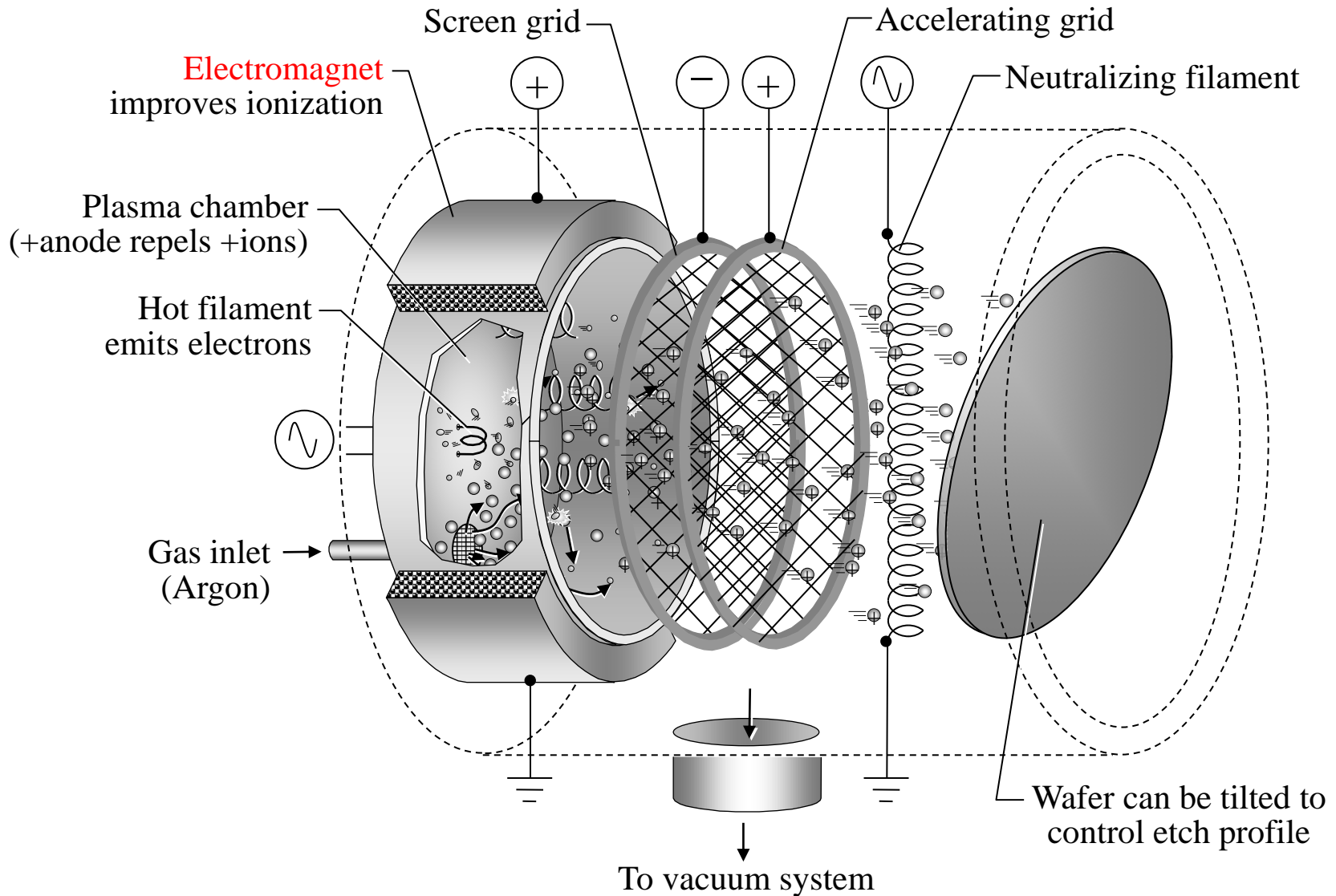


Triode Planar Reactor

- The **inductively-coupled** RF generates the plasma to create the ion and reactive species at a pressure ~ 0.001 torr
- The low-frequency generator controls the **ion bombardment**
- A typical use is in **single-crystal silicon trench etching**



General Schematic of Ion Beam Etcher

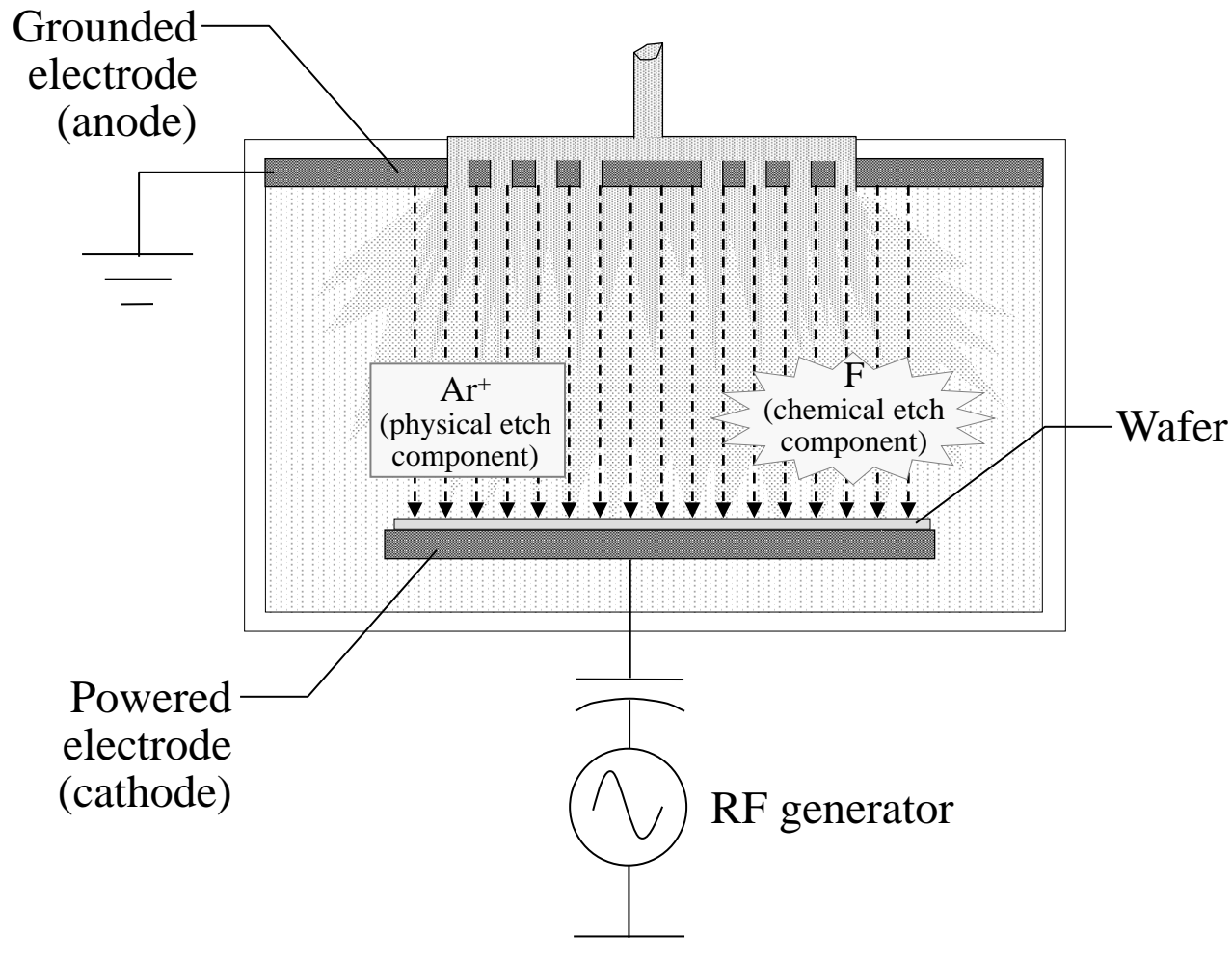


General Schematic of Ion Beam Etcher

- It has a physical etch mechanism with a strongly directional plasma (**Ar** is used)
- **Magnetic** field causes electrons to travel in circular paths, producing a high number of Ar ions
- Collimated electrodes formed into a **high-density beam**
- A **neutralizing** filament emits electrons to recombine with argon atoms to **prevent charging** of the wafer with the positive ions
- Operates in the low-pressure range of 10^{-4} torr, low plasma density
- Used to etch difficult materials, such as Au, Pt, and Cu
- Wafers can be tilted, but **low selectivity** and low etch rates, and low throughput

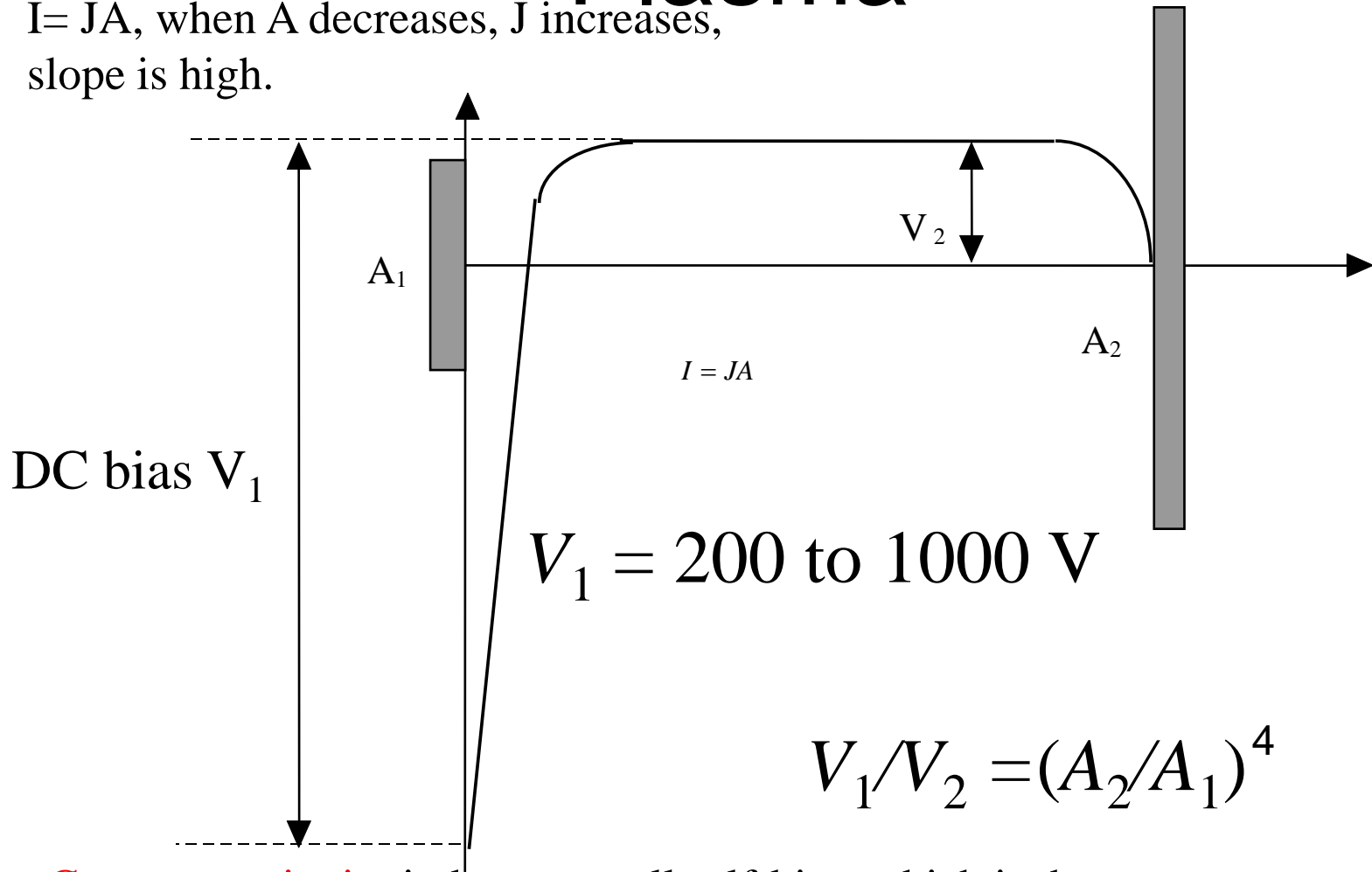
Parallel Plate **RIE** Reactor

- With both reactive chemical process and a physical process using ion bombardment
- Wafers are placed on the RF powered electrode and **electrode size** is greatly reduced relative to the grounded electrode size
- A **large DC self-bias** develops on the cathode and wafer acquire a large voltage difference with plasma, high directionality and improved **anisotropic**



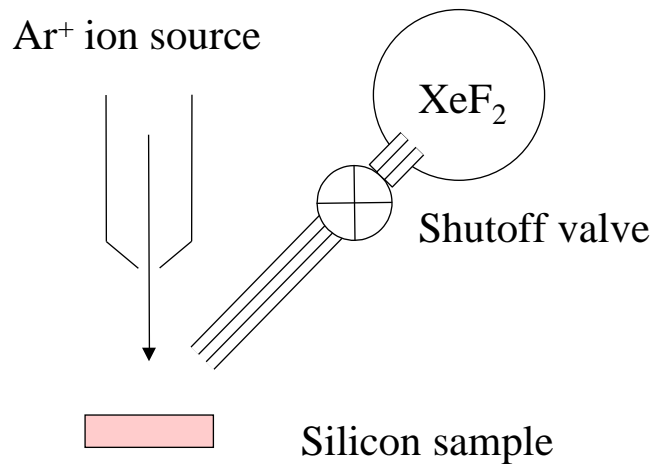
DC Bias of Etch Chamber Plasma

- $I = JA$, when A decreases, J increases, slope is high.

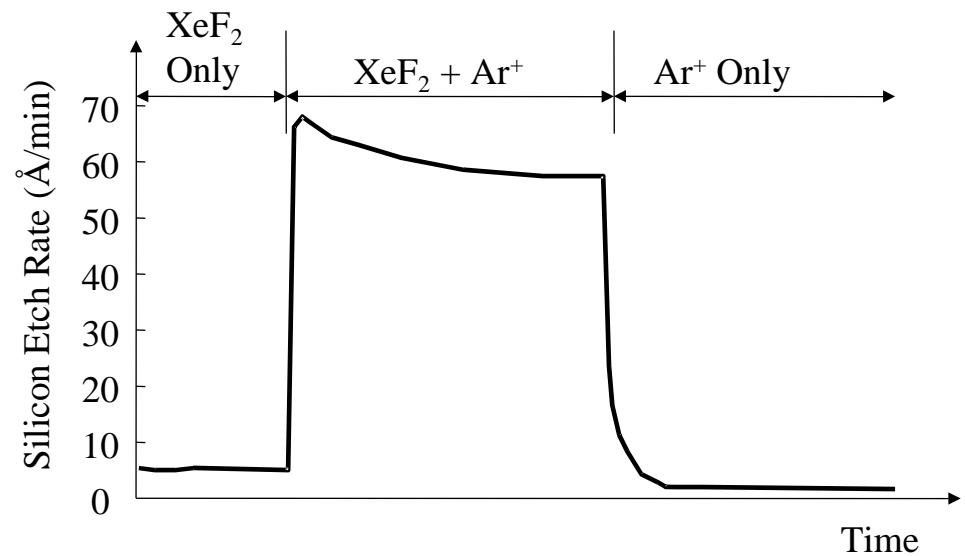


- **Current continuity** induces so call self-bias, which is the negative bias voltage build up on the smaller electrode.

RIE Experiment



Experiment arrangement



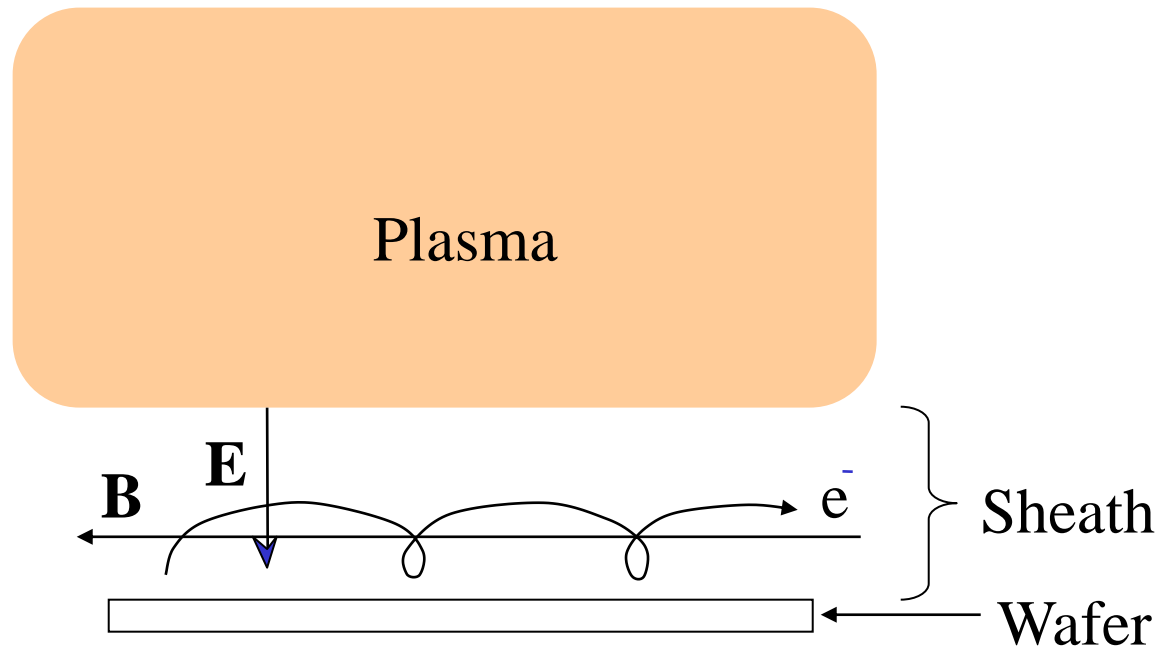
Experiment results

High Density Plasma Etcher

- High density plasma etch with single-wafer processing in a cluster tool is the most **predominant** dry etching methodology in use for critical layers
- Standard plasma ~ **a few hundred mtorr**, it has **difficult** to get etchant ion into and etch by products out of high aspect ratio feature (ionization rate 0.01~ 0.1%)
- Solution is lower the pressure (**1-10 mtorr**) to **increase the mean free path** lengths of gas molecules and ions
- Lower pressure results in lower etching rate
- Solution is to increase ionization rate to **10%** in the high density plasma etcher using **magnetic field**

Effect of Magnetic Field on DC Bias

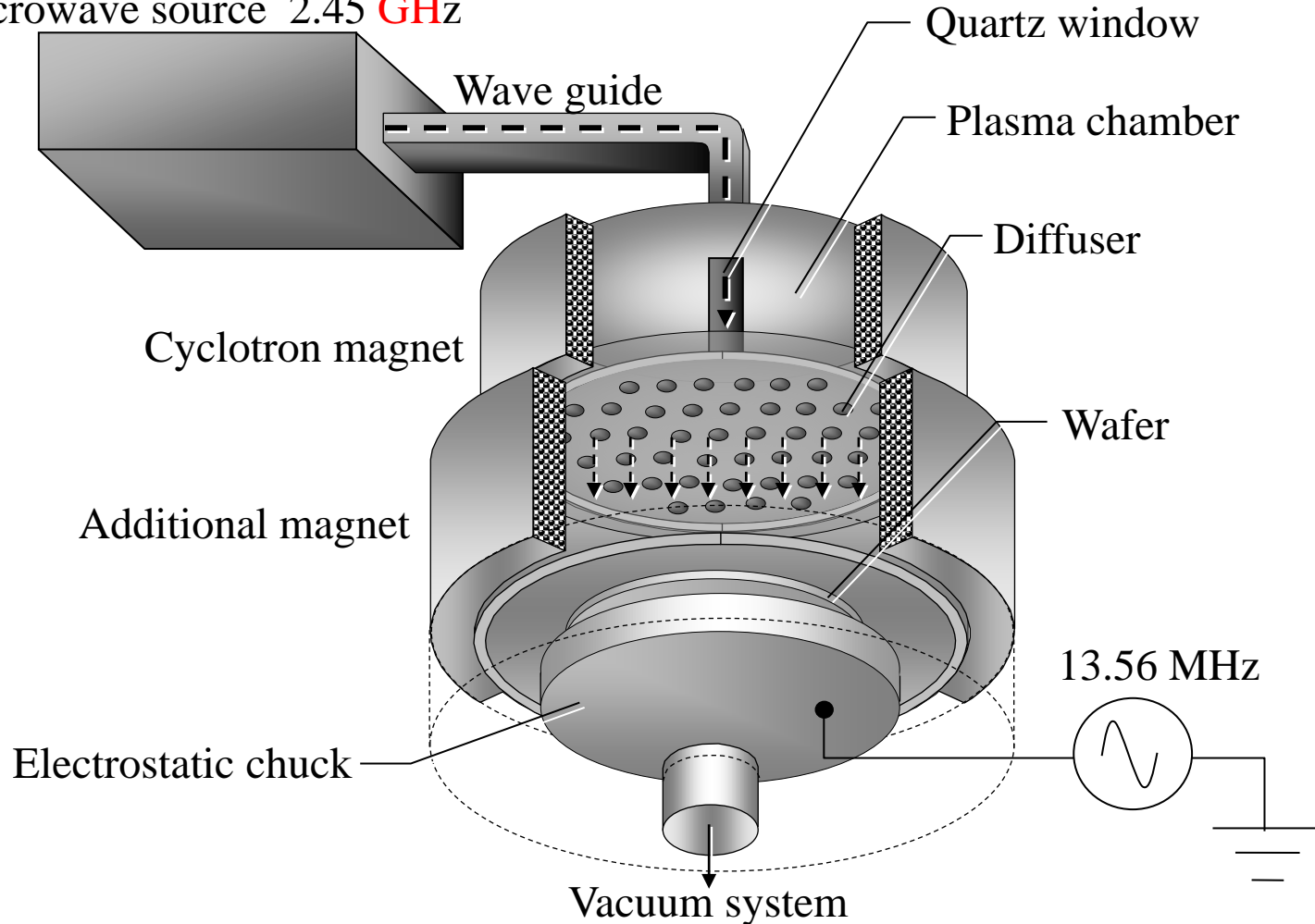
- Reasons: (a) more efficient for creating highly-directional, low-energy ions entering high-aspect ratio openings, yet causes **less wafer damage**. (b) plasma is denser, and higher etching rate. (c) low **DC-bias**, low damage



Schematic of Electron Cyclotron Reactor

- **Magnetic** field parallel to the direction of reactant flow that causes free electrons to move in a spiral path
- An efficient transfer of energy: the electric field to the electrons orbit frequency equals the frequency of the applied electric microwave field (**resonance**)

Microwave source 2.45 GHz



Inductively Coupled Plasma Etch

- Less complicated and less expensive than **ECR** and widely used
- Like a transformer, also called **TCP**

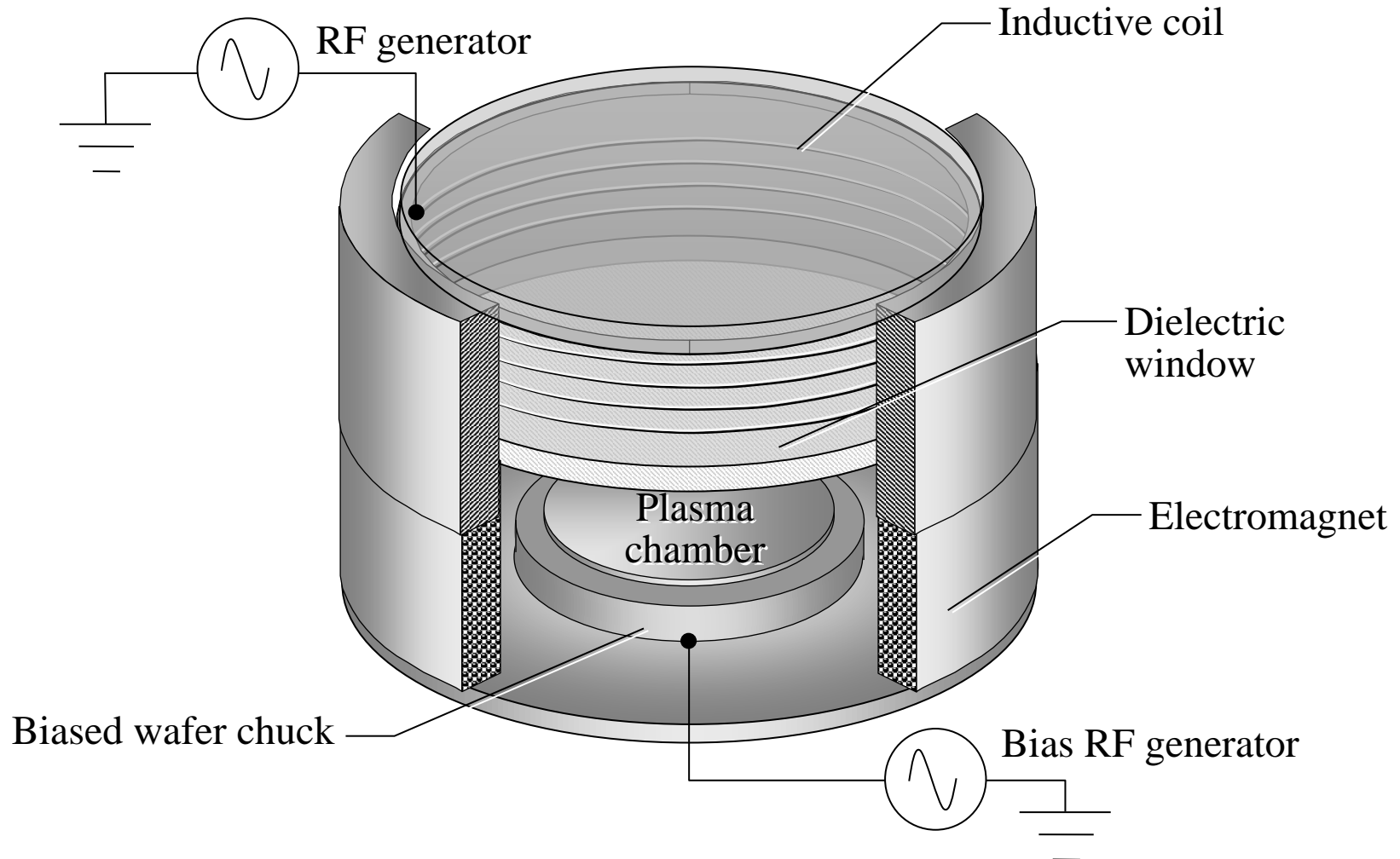
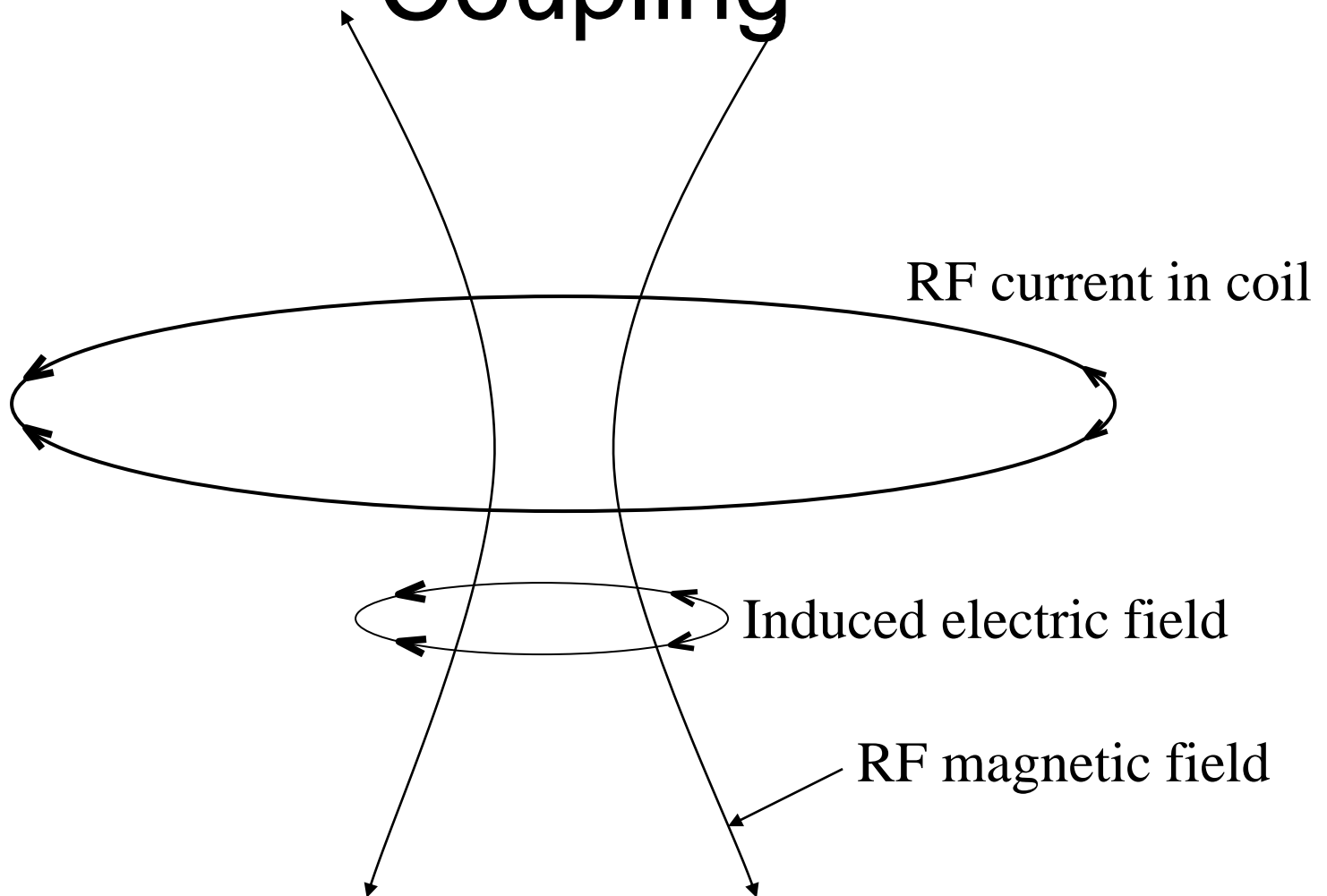
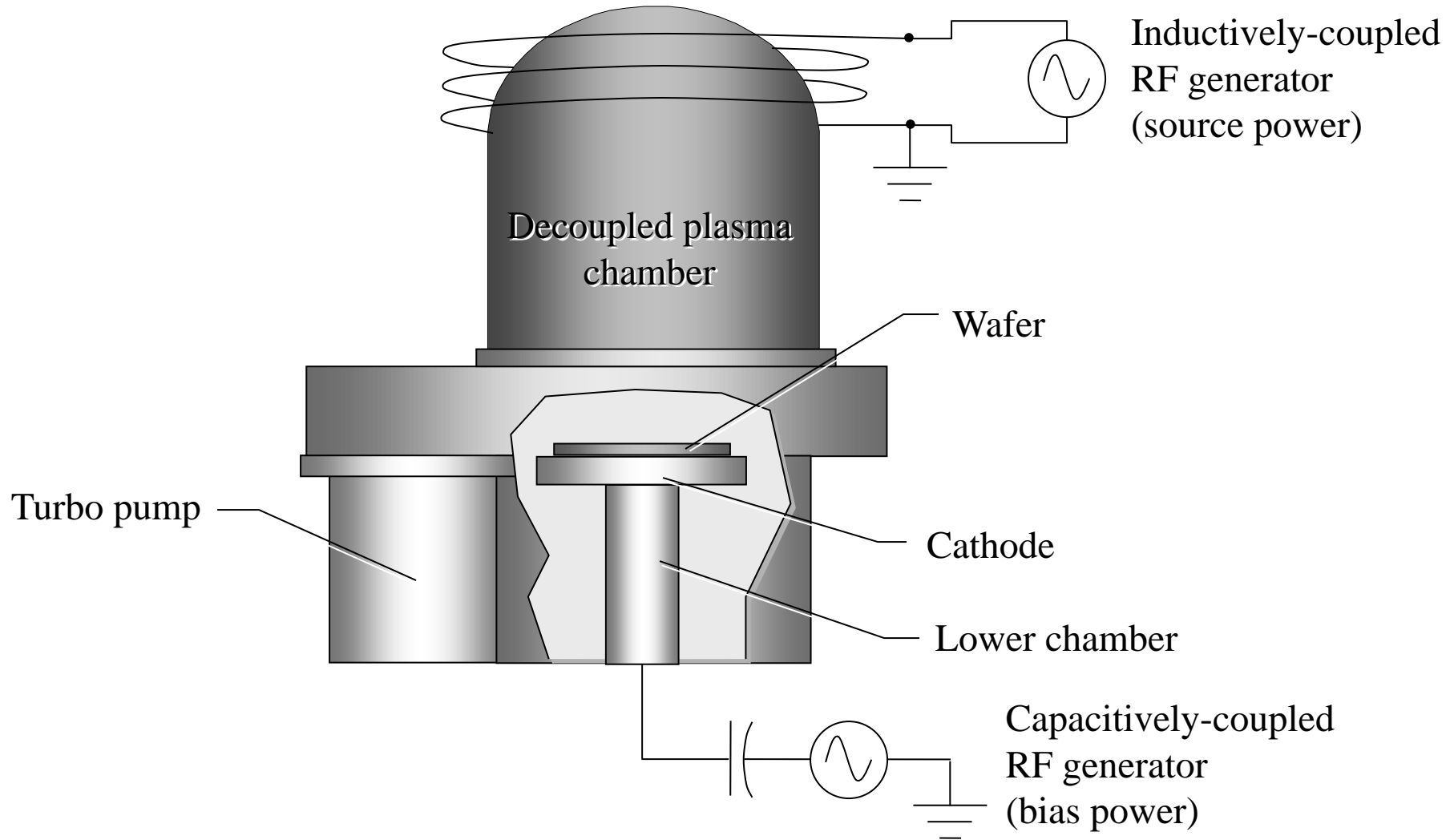


Illustration of Inductive Coupling

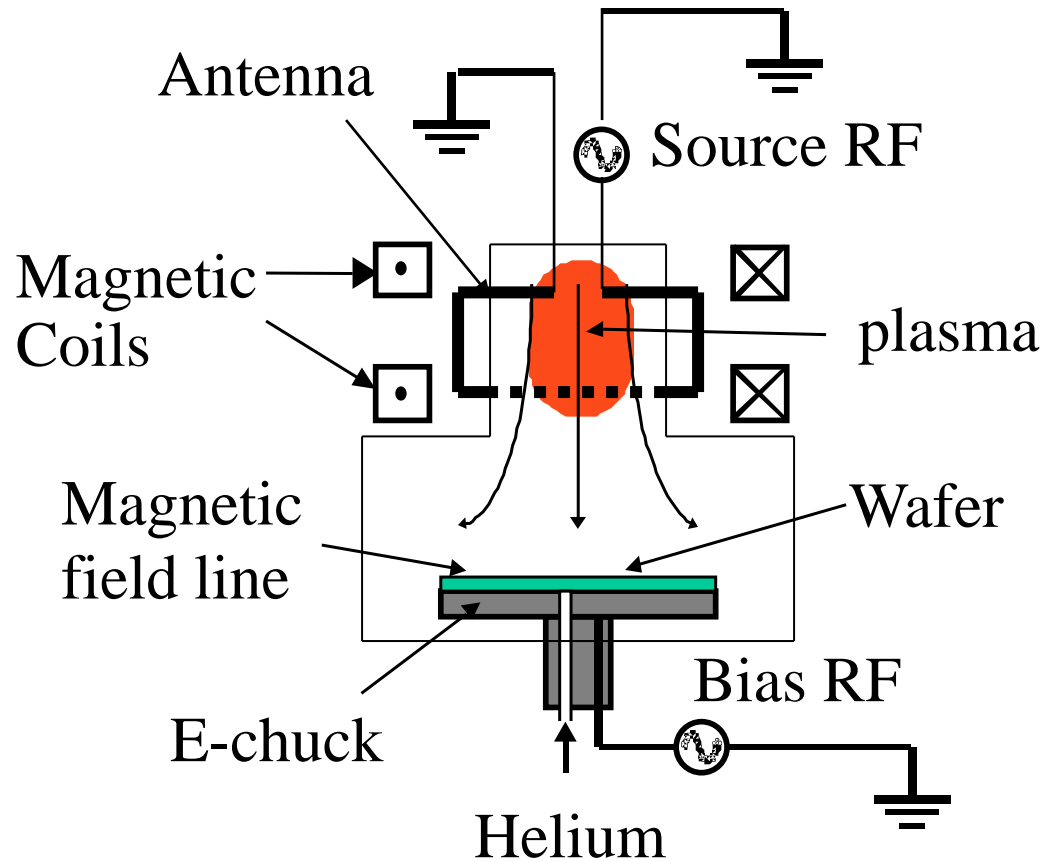


Dual Plasma Source (DPS)



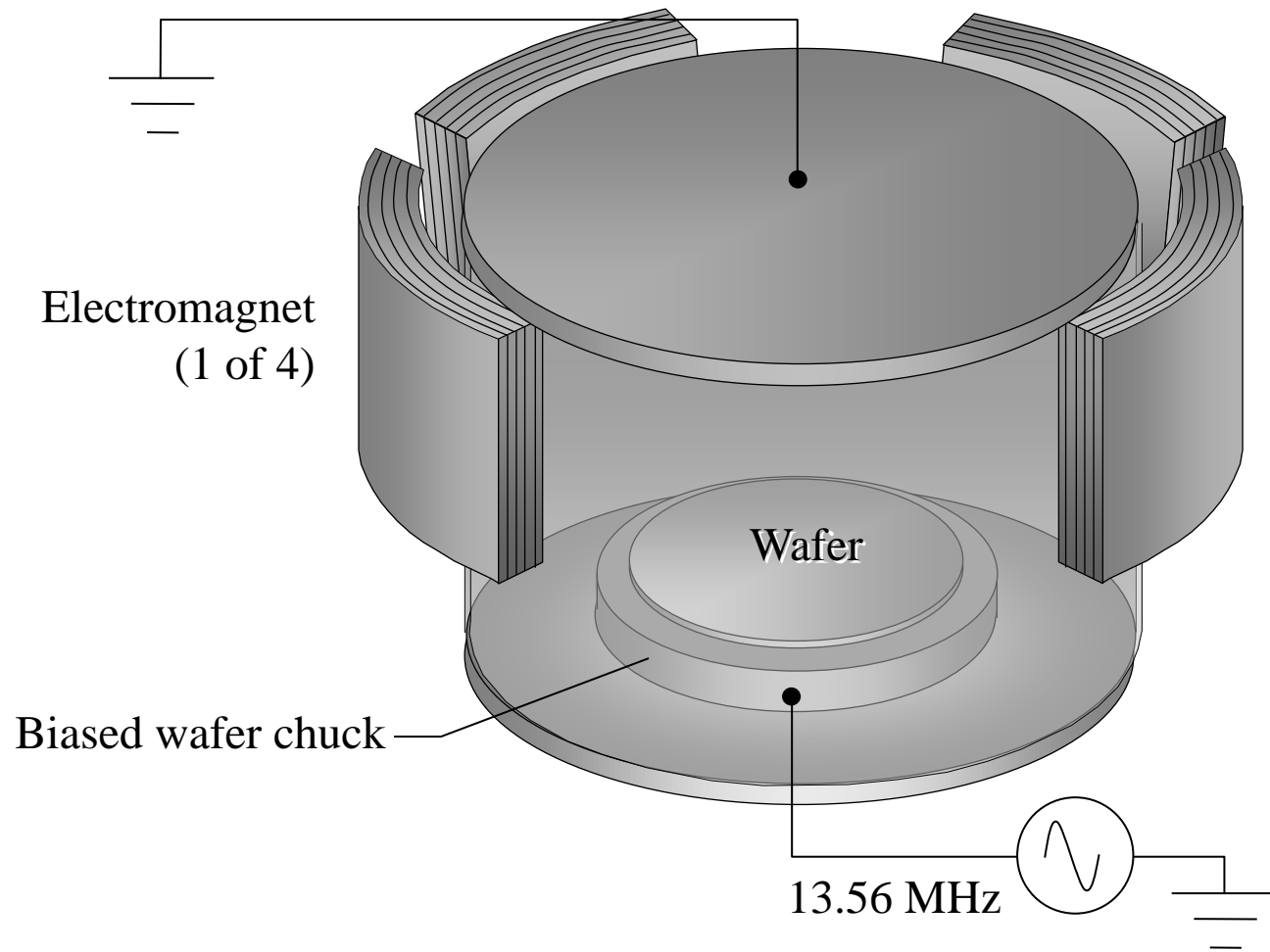
- The wafer cathode is movable in the vertical direction
- keeps the lower chamber clean and makes it much easier to maintain

Helicon Plasma Source



- The system receives power from an RF signal (13.56 MHz) that is inductively coupled into the plasma from a double-loop antenna located outside a quartz source tube. (100% ionization)

Magnetically Enhanced Reactive Ion Etch (MERIE)



Redrawn from *Wet/Dry Etch* (College Station, TX: Texas Engineering Extension Service, 1996), p. 165.

Figure 16.23

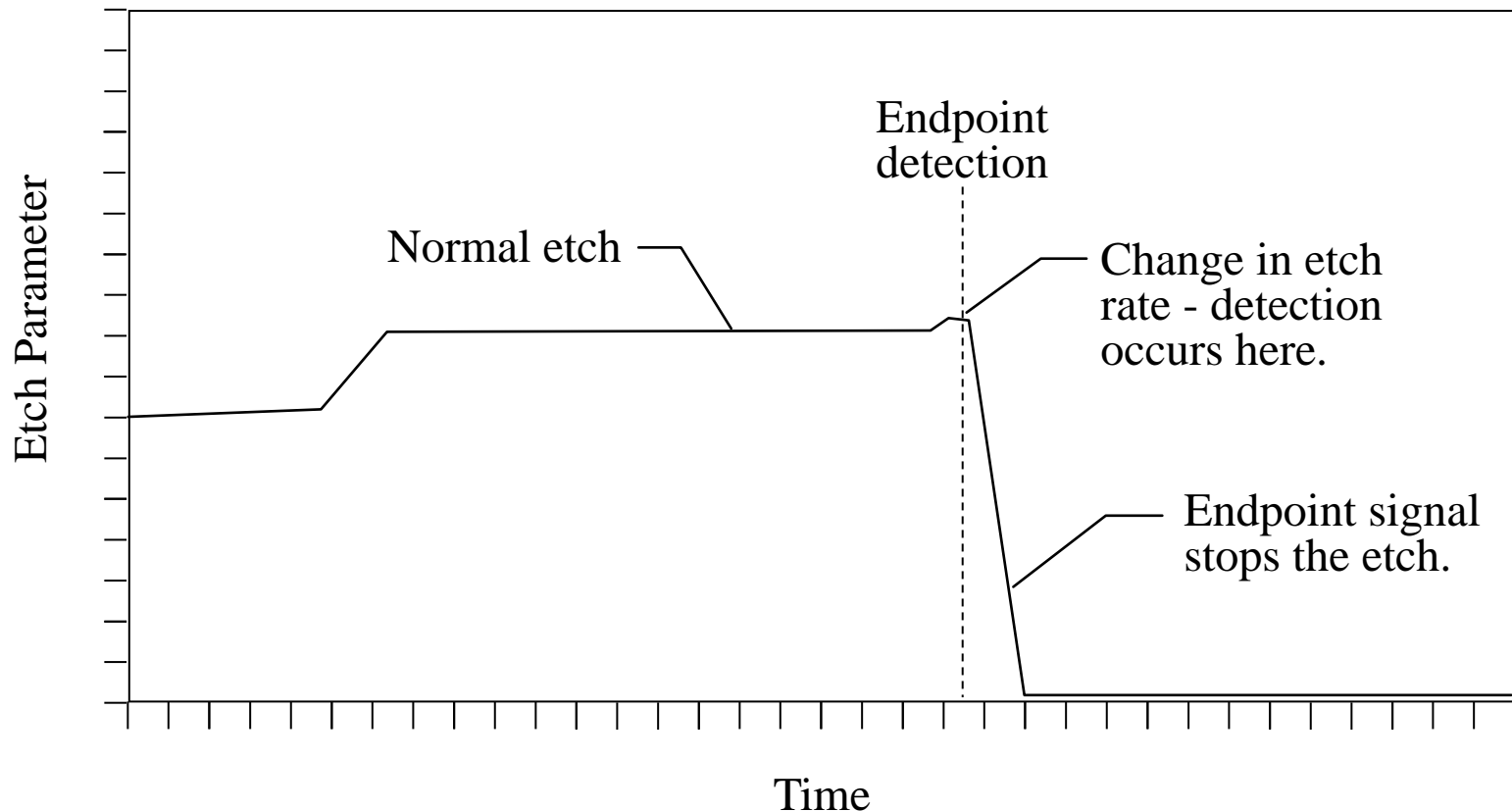
Dry Etcher Configurations

Configurations	Activity	Pressure (Torr)	Arrangement	High Density Plasma	Biasing	Bias Source	Profile
Barrel	Reactive	10^{-1} to 1	Coil or electrodes outside vessel	No	In cassette (bulk)	RF	Isotropic
Parallel Plate (Plasma)	Reactive	10^{-1} to 1	Planar diode (two electrodes)	No	On powered electrode (anode)	RF	Anisotropic
Downstream Plasma	Reactive	10^{-1} to 1	Coil or electrodes outside vessel	No	In cassette (bulk) downstream of plasma	RF or Microwave	Isotropic
Triode Planar	Reactive	10^{-3}	Triode (three electrodes)	No	On platform electrode		Anisotropic
Ion Beam Milling	Inert	10^{-4}	Planar triode	No	On powered electrode (anode)		Anisotropic
Reactive Ion Etch (RIE)	Reactive	< 0.1	Planar or cylindrical diode	No	On cathode		Anisotropic
Electron Cyclotron Resonance (ECR)	Reactive	10^{-4} to 10^{-3} (low)	Magnetic field in parallel with plasma flow	Yes	On cathode	RF or DC	Anisotropic
Distributed ECR	Reactive	(low)	Magnets distributed around central plasma	Yes	On cathode	RF or DC	Anisotropic
Inductively Coupled Plasma (ICP)	Reactive	(low)	Spiral coil separated from plasma by dielectric plate	Yes	On cathode	RF or DC	Anisotropic
Helicon Wave	Reactive	(low)	Plasma generated by electromagnets and plasma density maintained at wafer by magnetic field	Yes	On cathode	RF or DC	Anisotropic
Dual Plasma Source	Reactive	(low)	Independent plasma and wafer biasing	Yes	On cathode	RF or DC	Anisotropic
Magnetically Enhanced RIE (MERIE)	Reactive	(low)	Planar diode with magnetic field confining plasma	Yes	On cathode	RF or DC	Anisotropic

Table 16.5

Endpoint Detection for Plasma Etching

- Endpoint detection is required to monitor the etch process and stop etching to minimize over-etching of the underlying layer
- It measures: change in **etching rate**, the type of **etch product removed** from the etch process, or a change in the active reactants in **gas discharge** (following figure)
- **Optical emission spectroscopy** is used



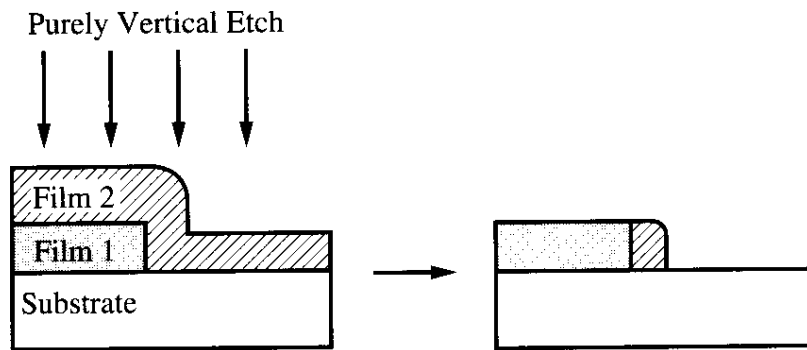


Figure 10-23 Overetching of a film over a step would be required to remove material at corner. In this example, completely anisotropic etching is assumed to emphasize this concept. This phenomenon can be used in producing self-aligned oxide spacers, in which no extra overetching is done so as to intentionally produce the structure at the right.

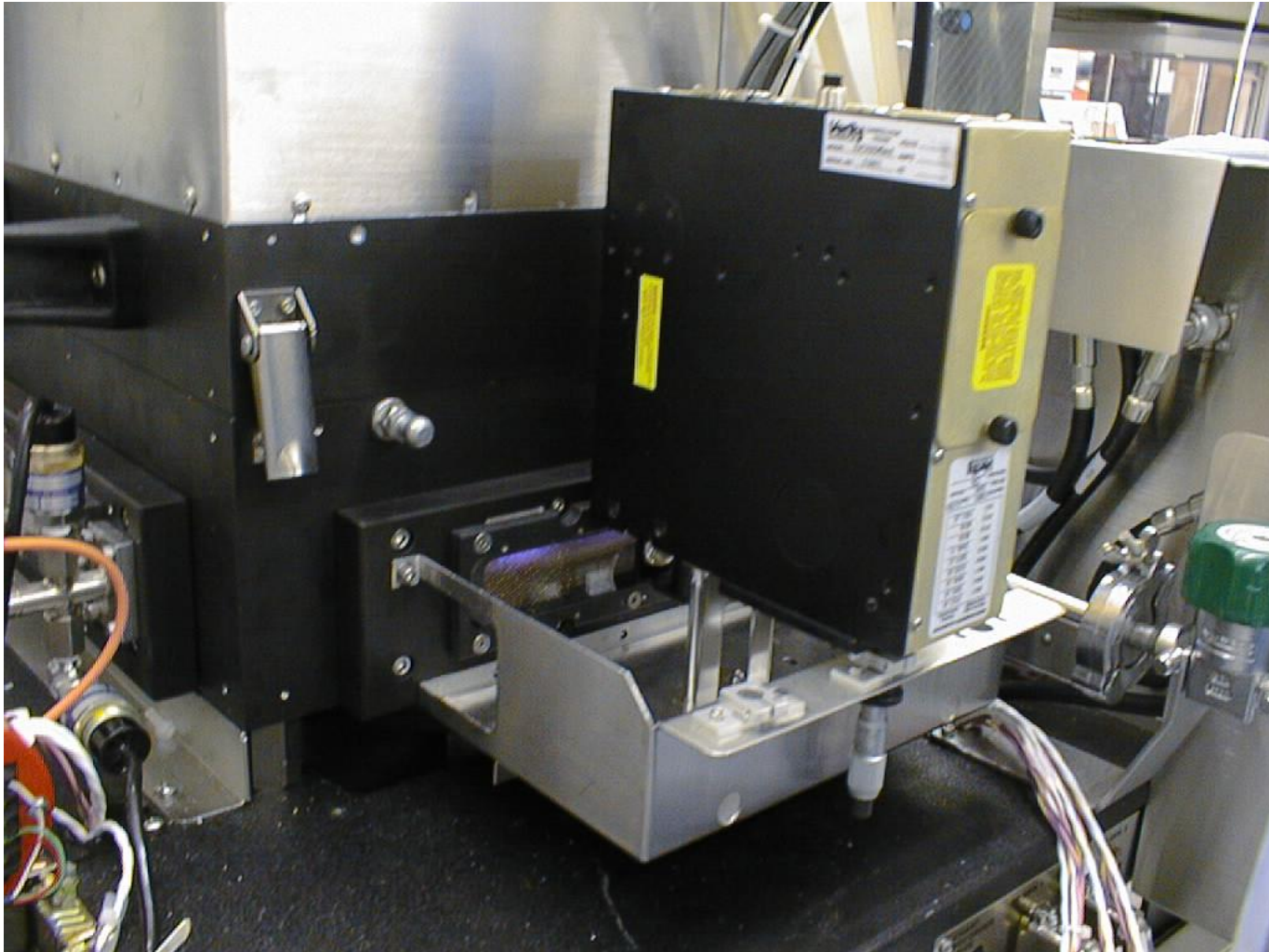
- Overetch 10-20% pass the endpoint detection is needed to avoid “stringer”

Characteristic Wavelengths of Excited Species in Plasma Etch

Material	Etchant Gas	Emitting Species of some Products	Wavelength (nm)
Silicon	CF ₄ /O ₂	SiF	440; 777
	Cl ₂	SiCl	287
SiO ₂	CHF ₃	CO	484
Aluminum	Cl ₂	Al	391; 394; 396
	BCl ₃	AlCl	261
Photoresist	O ₂	CO	484
		OH	309
		H	656
Nitrogen (indicating chamber vacuum leak)		N ₂	337
		NO	248

Table 16.6

Endpoint Detection



Photograph courtesy of Advanced Micro Devices, Lam Rainbow etcher

Dry Etch Applications

- Dielectric Dry Etch
 - Oxide
 - Silicon Nitride
- Silicon Dry Etch
 - Polysilicon
 - Single-Crystal Silicon
- Metal Dry Etch
 - Aluminum and Metal Stacks
 - Tungsten Etchback
 - Contact Metal Etch

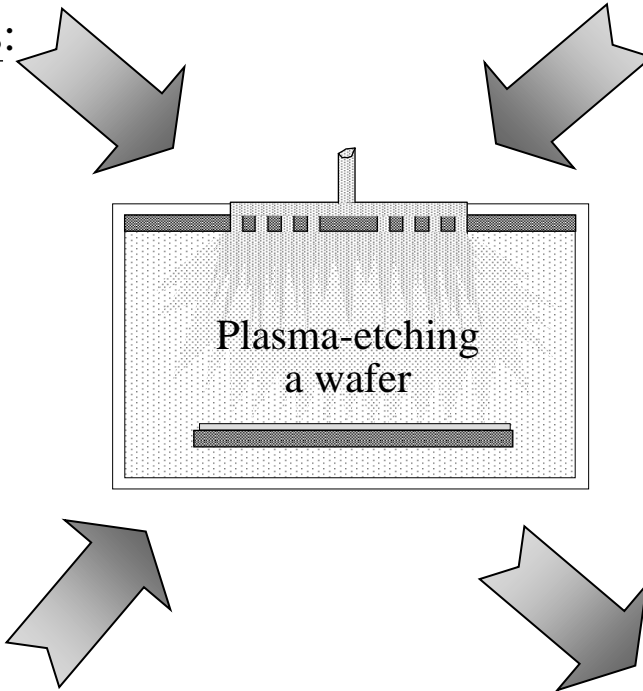
Requirements for Successful Dry Etch

1. **High selectivity** to avoid etching materials that are not to be etched (primarily photoresist and underlying materials).
2. **Fast etch** rate to achieve an acceptable throughput of wafers.
3. Good sidewall **profile** control.
4. Good etch uniformity across the wafer.
5. Low device damage.
6. Wide process latitude for manufacturing.

Dry Etch Critical Parameters

Equipment Parameters:

- Equipment design
- Source power
- Source frequency
- Pressure
- Temperature
- Gas-flow rate
- Vacuum conditions
- Process recipe



Process Parameters:

- Plasma-surface interaction:
 - Surface material
 - Material stack of different layers
 - Surface temperature
 - Surface charge
 - Surface topography
- Chemical and physical requirements
- Time

Other Contributing Factors:

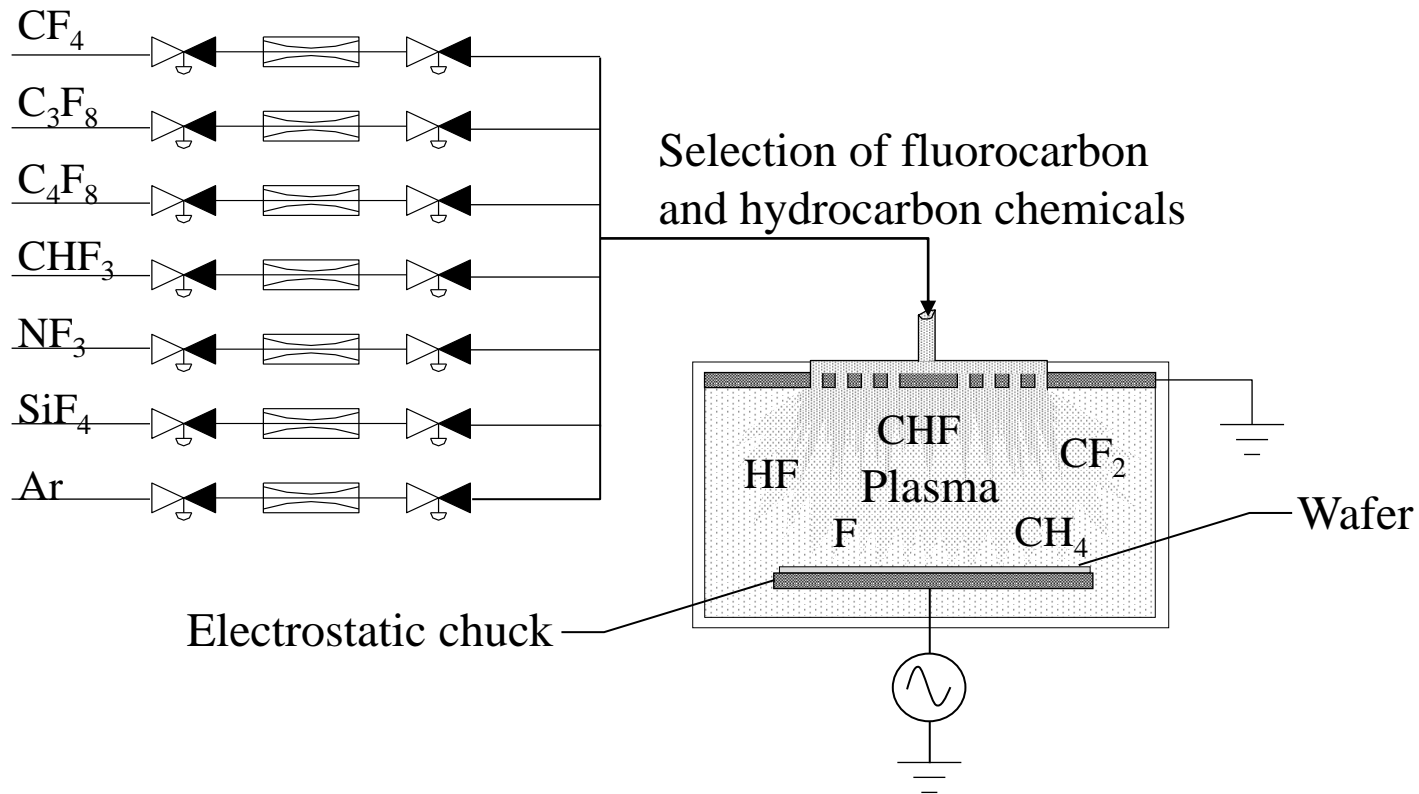
- Cleanroom protocol
- Operating procedures
- Maintenance procedures
- Preventive maintenance schedule

Quality Measures:

- Etch rate
- Selectivity
- Uniformity
- Feature profile
- Critical dimensions
- Residue

Figure 16.25

Oxide Etch Reactor



Oxide Etching

- Etching oxide are forming contact holes and vias, their features are **critical** applications
- Aspect ratio for DRAM 6:1 for 0.18 μm , **selective** etching to underlying silicon and polycide is about 50:1
- Based on **CF** chemistry: $4\text{F} + \text{SiO}_2 \rightarrow \text{SiF}_4 + 2\text{O}$
- It is radical **F** species that attacks the oxide and causes etching
- CF_x radicals also serve to passivate the sidewall surfaces with a polymer
- A high C/F ratio generally means polymer formation, lower etch rate, and **high oxide-to-Silicon selectivity**
- In some cases, a silicon source is used to getter excess F atoms, increasing the ratio of C/F

Etch Stop Hard Mask Layer

Example: Silicon nitride, Si_3N_4 , serves as etch-stop during LI oxide etch.

Note: The numbers show the order of the five operations.

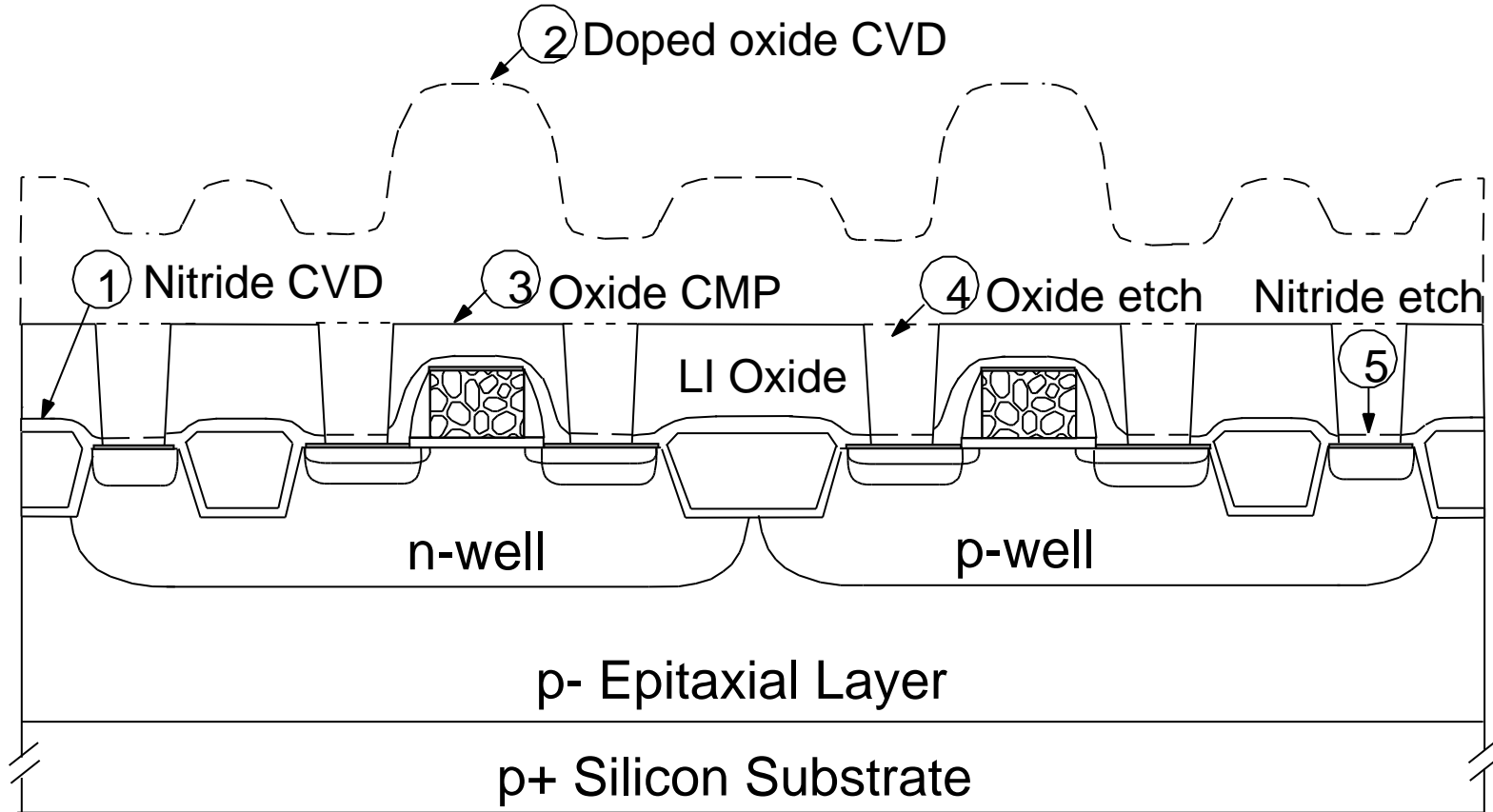


Figure 16.27

Contact Etching to Varying Depths

- High selectivity to silicon is critical during contact etch through the LI oxide dielectric to avoid etching into source/drain region
- Adding O_2 to 20% (more CO or CO_2 , then more F) can increase **oxide** etching rate, improve the selectivity
- Adding H_2 to 40% (more HF, less F) can reduce **silicon** etching rate, improve the selectivity

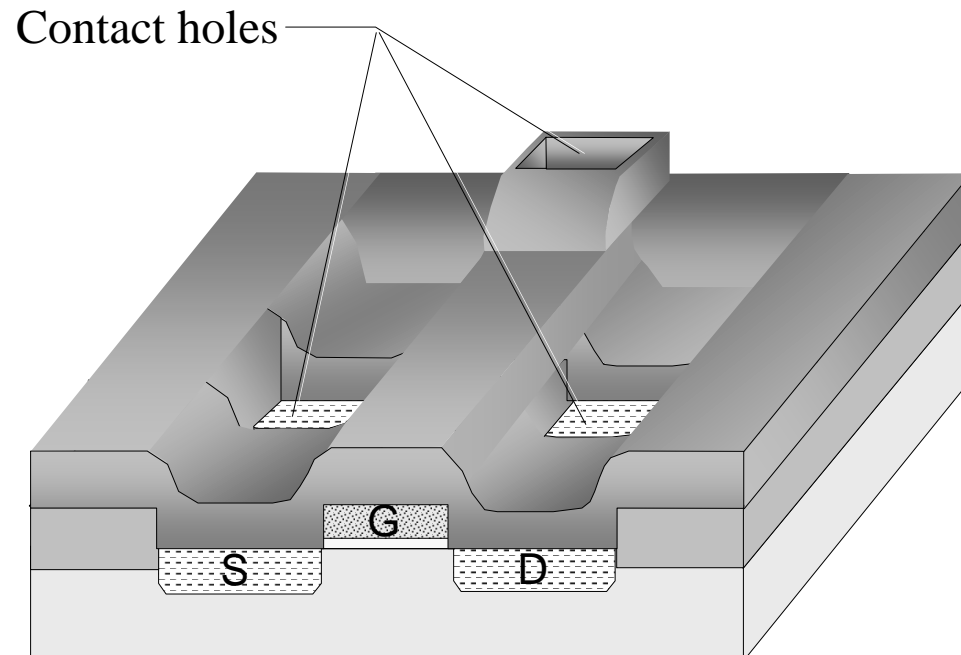


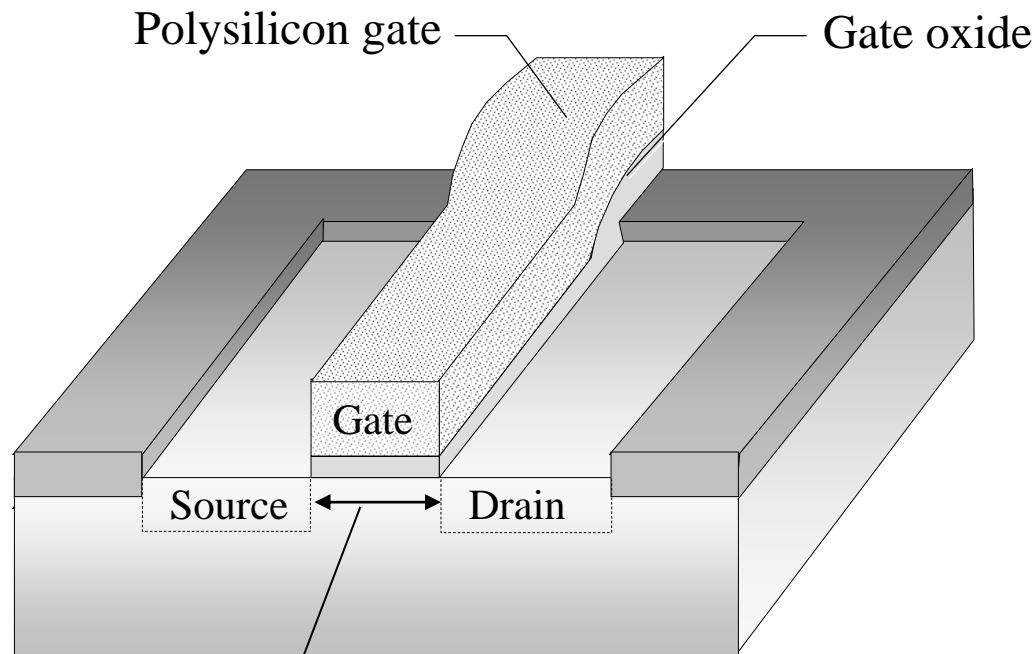
Figure 16.28

Contact Etch

- F/C ratio $F/C > 3$, etch dominant
 $F/C < 2$, polymerization
- When etching oxide, **oxygen** byproduct can react with **C to free more fluorine**
- When etching silicon or silicide, no oxygen releasing, fluorine is consumed, F/C ratio drop below 2 and **start** polymer deposition
- Polymer blocks further etch process
- High BPSG-to-TiSi₂ selectivity

Polysilicon Conductor Length

- F-based produce a fast etch reaction but with an isotropic profile and average resist selectivity
- High energy ion bombardment increases sidewall profile, but damage to oxide
- Cl_2 is used (selectivity > 10), Br_2 or HBr (> 100)
- Add O_2 in HBr or Cl_2 to increase the etch rate and the selectivity to oxide



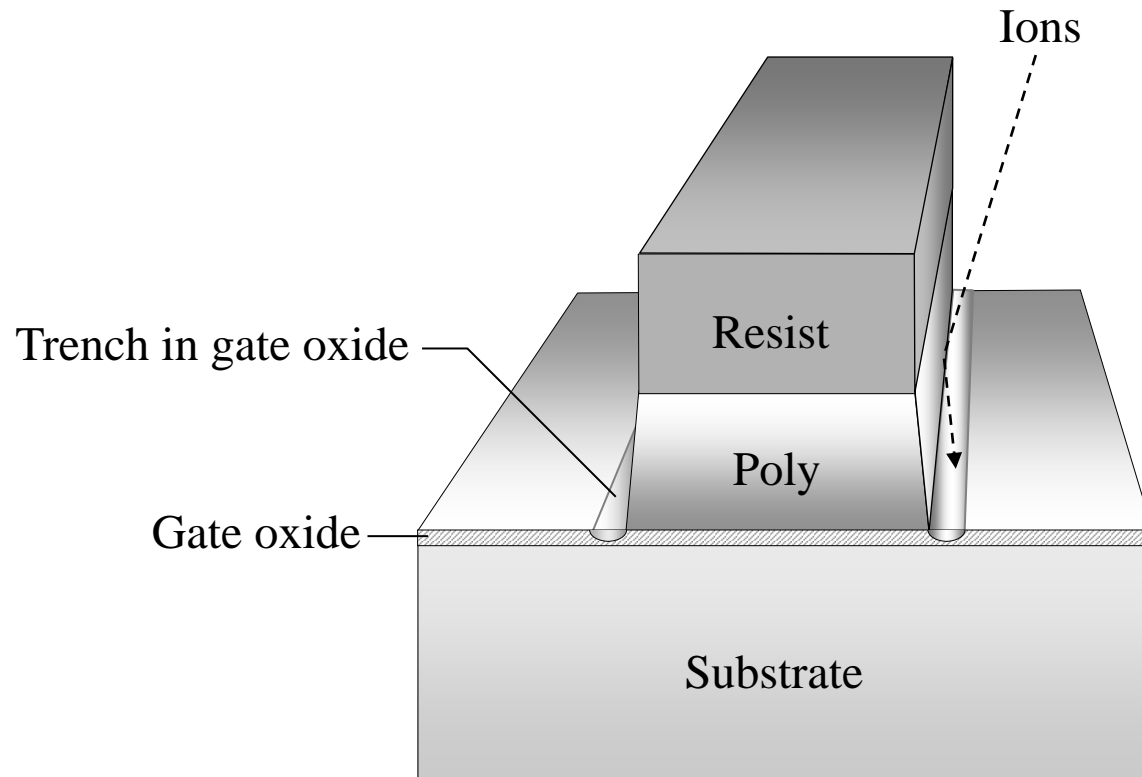
The gate length determines channel length and defines boundaries for source and drain electrodes.

Polysilicon Gate Etch Process Steps

1. Breakthrough step to remove native oxide and surface contaminants
2. Main-etch step to remove most polysilicon without damage to gate oxide
3. Overetch step to remove remaining residues and poly stringers while maintaining high selectivity to gate oxide

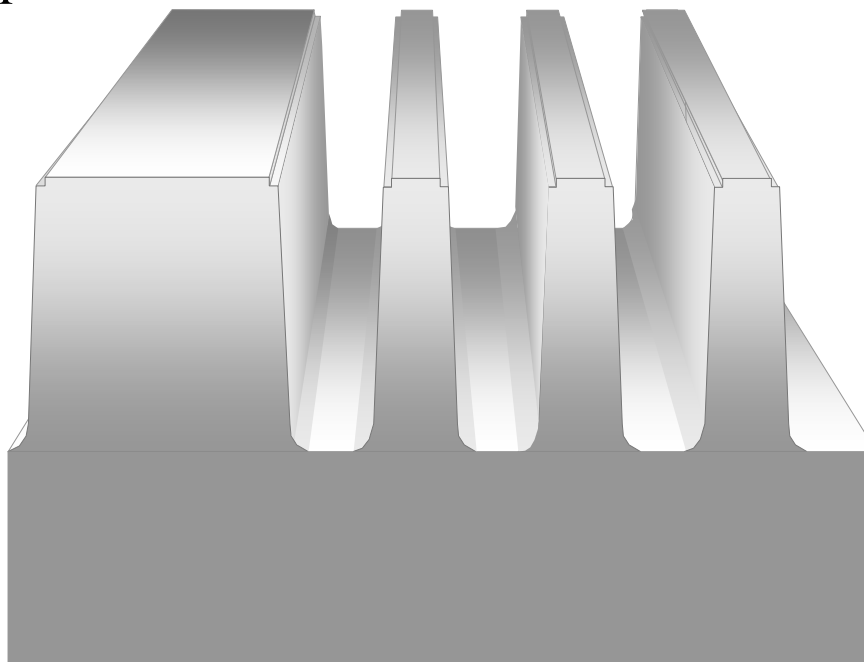
Undesirable **Microtrenching** during Polysilicon Gate Etching

- Device will have 10-20Å gate oxide, require a selectivity > 150:1
- Volatile etch by-products for F, Cl, and Br are SiF_4 , SiCl_4 , and SiBr_4



Silicon Trench Etching

- Applications of Si trench etching: shallow trench isolation [STI] ($< 1\mu\text{m}$) and vertical trench capacitor DRAM ($> 5\mu\text{m}$)
- A **multistep** etch process is needed with a modification for the final step where the bottom of the trench is **rounded** to remove any silicon damage
- STI: **F** is used for because its high etch rate with adequate selectivity to PR
- Deep trench: Cl^- or **Br-based** is used for high Si etching rate and high selectivity to oxide mask
- **Br** is common, no use of carbon [low contamination], it is **corrosive** to the gas delivery system and reactor



Major Requirements for Metal Etching

1. High etch rates (>1000 nm/min).
2. High selectivity to the masking layer ($>4:1$), interlayer dielectric ($>20:1$) and to underlying layers.
3. High uniformity with excellent CD control and no microloading ($<8\%$ at any location on the wafer).
4. No device damage from plasma-induced electrical **charging**.
5. Low residue contamination (e.g., copper residue, developer attack and surface defects).
6. Fast resist strip, often in a dedicated cluster tool chamber, with no residual contamination.
7. No **corrosion**.

Metal Stack for VLSI/ULSI Integration

- Cl-based is used for Aluminum, add CHF_3 to improve the sidewall passivation
- **AlF_3 is non-volatile**
- Al oxidizes almost instantly when exposed to air and the resulting Al_2O_3 inhibits the Cl etch reactions

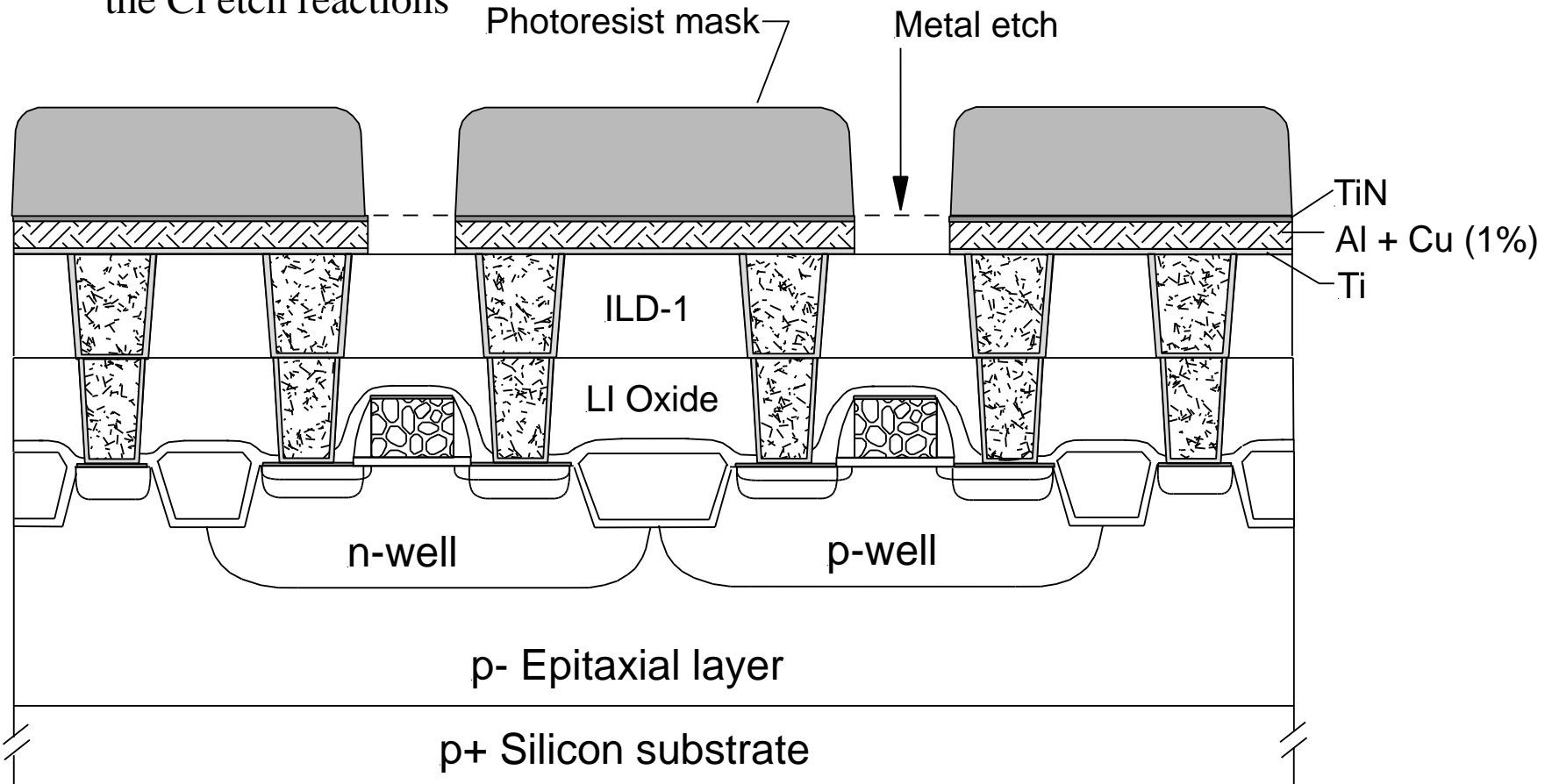


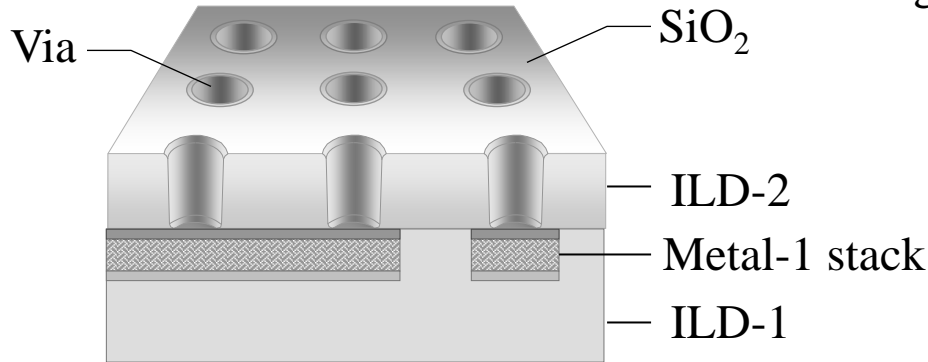
Figure 16.32

Typical Steps for Etching Metal Stacks

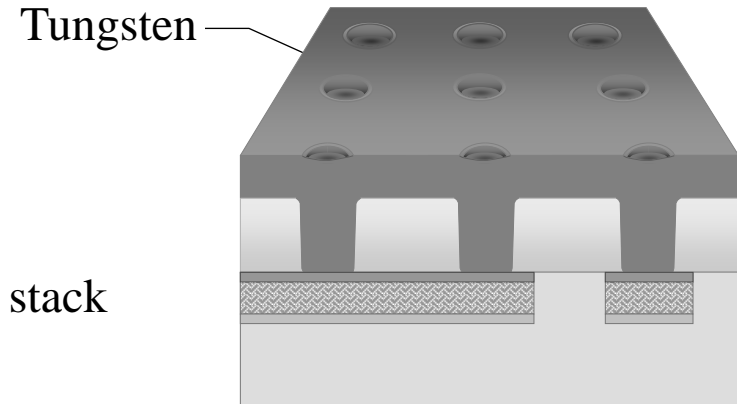
1. Breakthrough step to remove native oxide.
2. ARC layer etch (may be combined with above step).
3. Main etch step of aluminum.
4. Overetch step to remove residue. It may be a continuation of the main etch step.
5. Barrier layer etch.
6. Optional residue removal process to prevent corrosion. (AlCl_3 or AlBr_3 react with **water** to form highly corrosive HCl or HBr)
7. Resist removal. [**cluster**]

Tungsten Etchback

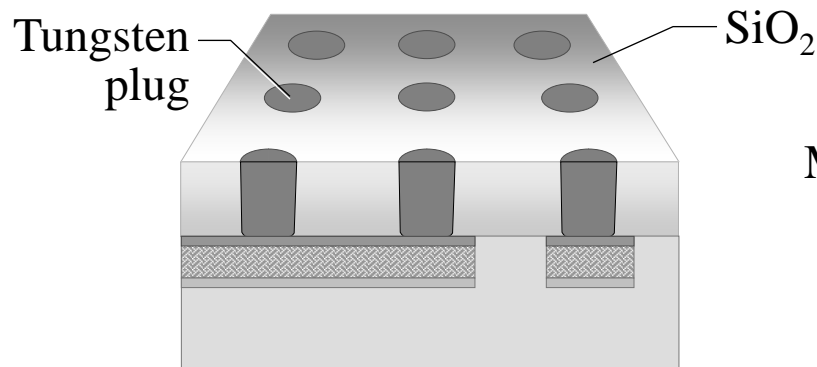
- Two-step etching: (1) 90% W is etched at a high rate with excellent uniformity, (2) etching rate is reduced with a high selectivity to TiN barrier layer
- Replaced by CMP



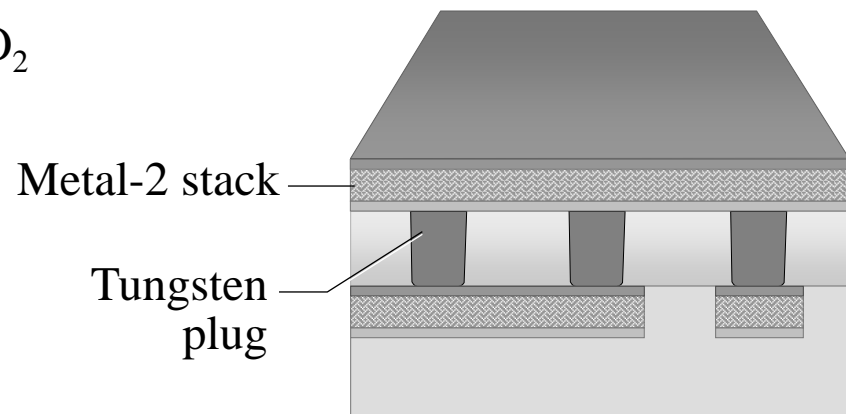
(a) Via etch through ILD-2 (SiO_2)



(b) Tungsten CVD via fill



(c) Tungsten etchback



(d) Metal-2 deposition

Figure 16.33

Wet Etch

- Replaced by dry etching
 - Still plays an **important** role in oxide **cleaning**, residue removal, stripping of surface layers, and etching for larger geometry
 - Compared to dry etching: good selectivity, no plasma damage, simple equipment
- Wet Etch Parameters
- Types of Wet Etch
 - Wet Oxide Etch
 - Wet Chemical Strips

Wet Etch Parameters

Parameter	Explanation	Difficulty to Control
Concentration	Solution concentration (e.g., ratio of $\text{NH}_4\text{F}:\text{HF}$ for etch an oxide).	Most difficult parameter to control because the bath concentration is continually changing.
Time	Time of wafer immersion in the wet chemical bath.	Relatively easy to control.
Temperature	Temperature of wet chemical bath.	Relatively easy to control.
Agitation	Agitation of the solution bath.	Moderate difficulty to properly control.

Approximate **Oxide Etch** Rates in **BHF** Solution at 25° C

- Oxide can be wet etched by hydrofluoric acid (**HF**)
- A chemical **buffer** is a solution that resist changes in pH when small amounts of strong acid or base are added
- **Buffering** the HF and NH₄F (BOE) provides a well-controlled etch solution that allows and stabilizes the etch and does not appreciably attack the PR

Table 16.8¹ Approximate Oxide Etch Rates in BHF Solution at 25°C ^a		
Type of Oxide	Density (g/cm³)	Etch Rate (nm/s)
Dry grown	2.24 – 2.27	1
Wet grown	2.18 – 2.21	1.5
CVD deposited	< 2.00	1.5 ^b – 5 ^c
Sputtered	< 2.00	10 – 20

a) 10 parts of 454 g NH₄F in 680 ml H₂O and one part 48% HF

b) Annealed at approximately 1000°C for 10 minutes

c) Not annealed

¹ B. El-Kareh, ibid, p. 277.

Wet Chemical Strips

- Due to the high selectivity, wet strips are sometimes used to remove surface layers, including **PR**, and **masking** layer
- Si_3N_4 is widely used as a mask layer in STI, LOCOS and self-aligned contact
- Hot phosphoric acid (H_3PO_4) at 160°C has the desirable property of high selectivity to exposed oxide layer
- Some oxy-nitride formed on the exposed nitride, using a short HF deglaze before nitride removal is required, reducing nonuniform nitride removal
- $\text{NH}_4\text{OH} + \text{H}_2\text{O}_2 + \text{H}_2\text{O}$ is used to remove the Ti layer on TiSi_2

Historical Perspective - Polysilicon Etch Technology Evolution

Geometry Requirements	Time Frame and Reactor Design	Chemistries	Strengths	Limitations and Problems	Controls
4 to 5 μm , isotropic etch	Pre-1977: wet etch	HF/HNO ₃ buffered with acetic acid or H ₂ O	Batch Process	Resist lift; bath aging; temperature sensitive	Operator judgement for endpoint
3 μm	1977: barrel etcher	CF ₄ /O ₂	Batch Process	Non-uniformity, isotropic etch, large undercut	Manometer and timer
2 μm	1981: single wafer etch	CF ₄ /O ₂	Single wafer; individual etch endpoint, improvement in repeatability	Low oxide selectivity; isotropic process	Endpoint detection
1.5 μm	1982: single wafer RIE	SF ₆ /Freon 11, SF ₆ /He	MFCs; independent pressure and gas flow control, improvement in repeatability	Low oxide selectivity; profile control	MFCs; separate gas flow and pressure control
To 0.5 μm	1983: variable gap; load-locked	CCl ₄ /He, Cl ₂ /He, Cl ₂ /HBr	Load-locked chamber; variable gap, improvement in repeatability	Microloading in high aspect ratios; profile control	Control of electrode gap; computer controls
To 0.25 μm and below	1991: inductively coupled plasma (ICP)	Cl ₂ , HBr	High-density plasma; low pressure; simple gas mixtures, improvement in repeatability	Complex tool; many variables	Independent RF control for plasma generation and wafer bias

Table 16.9

Photoresist Removal

Plasma Ashing

- Asher Overview
 - $\text{O} + \text{CH} \rightarrow \text{CO} + \text{CO}_2 + \text{H}_2\text{O}$
- Plasma Damage
- Residue Removal

Atomic Oxygen Reaction with Resist in Asher

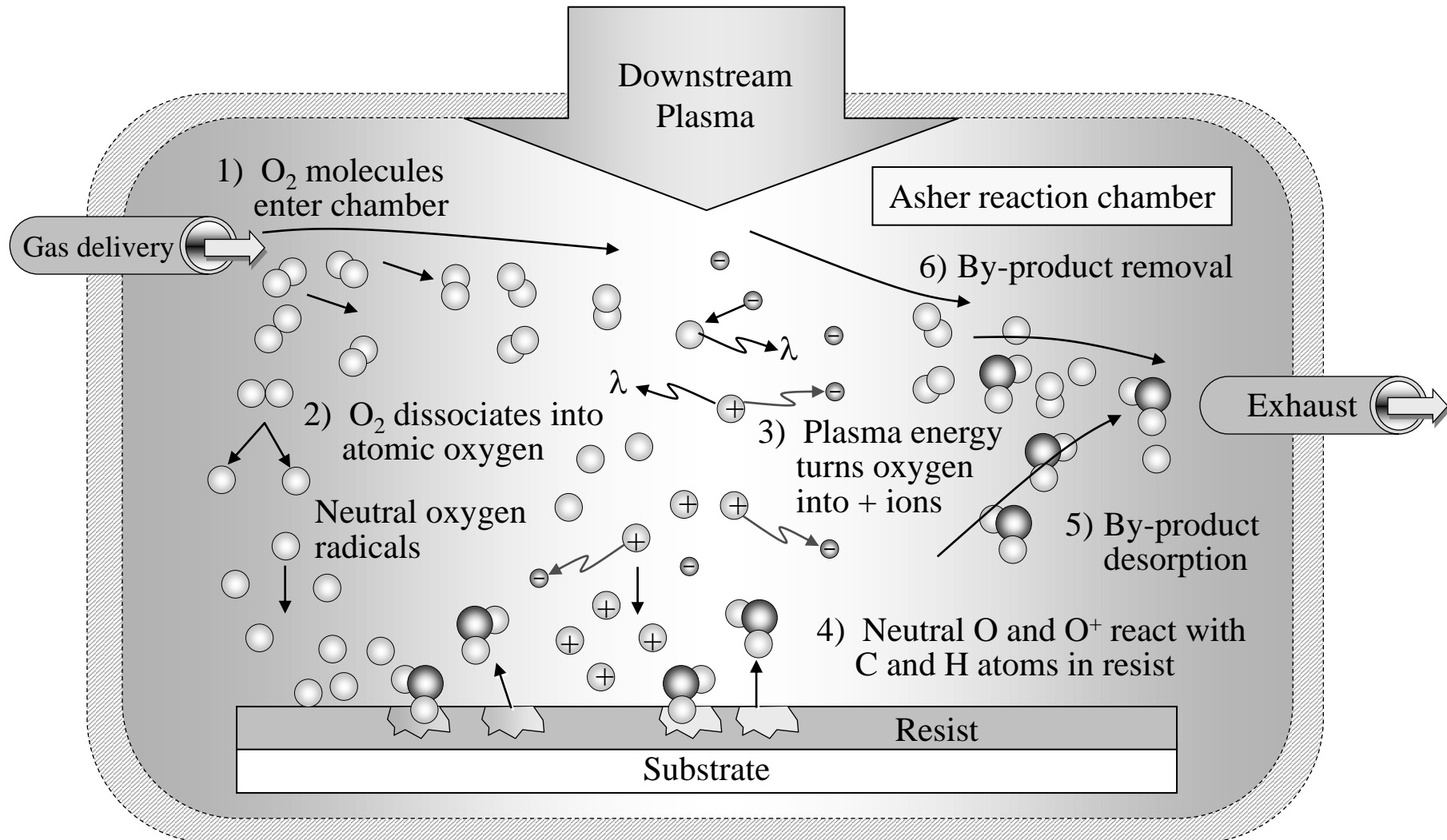


Figure 16.34

Post Etch Via Veil Residue

- Residues are **complex** and can contain by products such as Al, Ti, O, and Si
- **Inorganic residue is hard to remove**
- Adding NO, or CF₄
- Dry ashing alone is not sufficient to strip and clean residue because of inorganic materials present
- Wet chemistry residue **stripper** is used to dissolve inorganic residues at low temperature with no corrosion

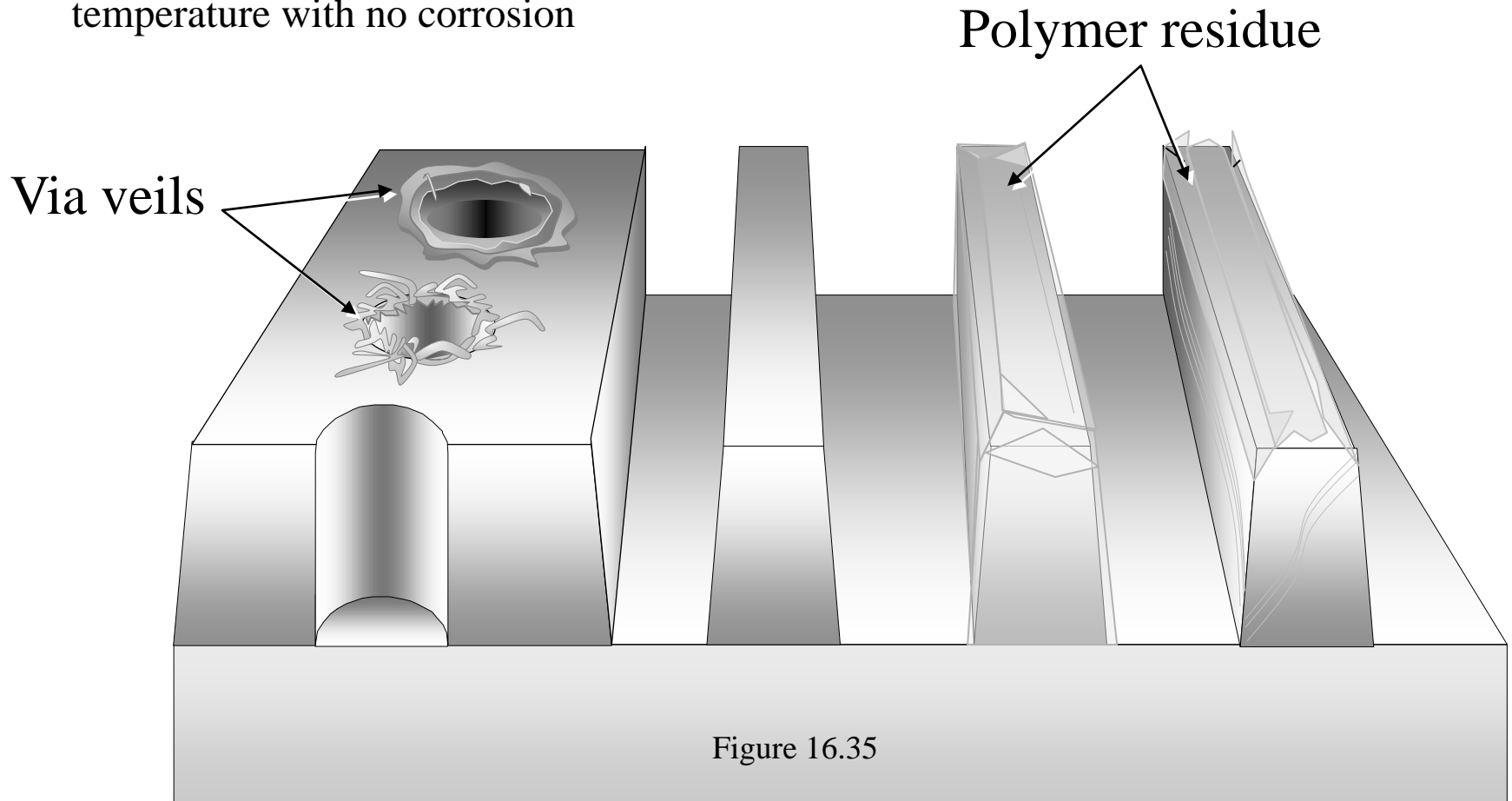
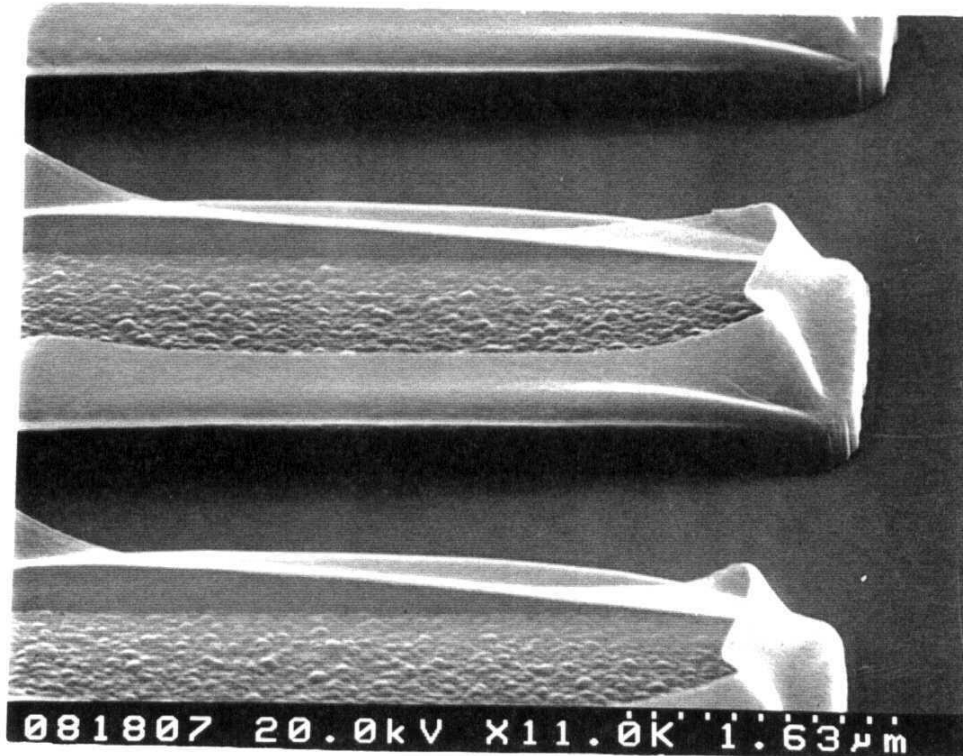


Figure 16.35



- After oxide etching, the polymer should be removed, especially in contact holes. The polymer can be removed by an O₂ and CF₄ plasma treatment CF₄ is better at removing all the polymer and even some damaged substrate.