Semiconductor Manufacturing Technology

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Chapter 12

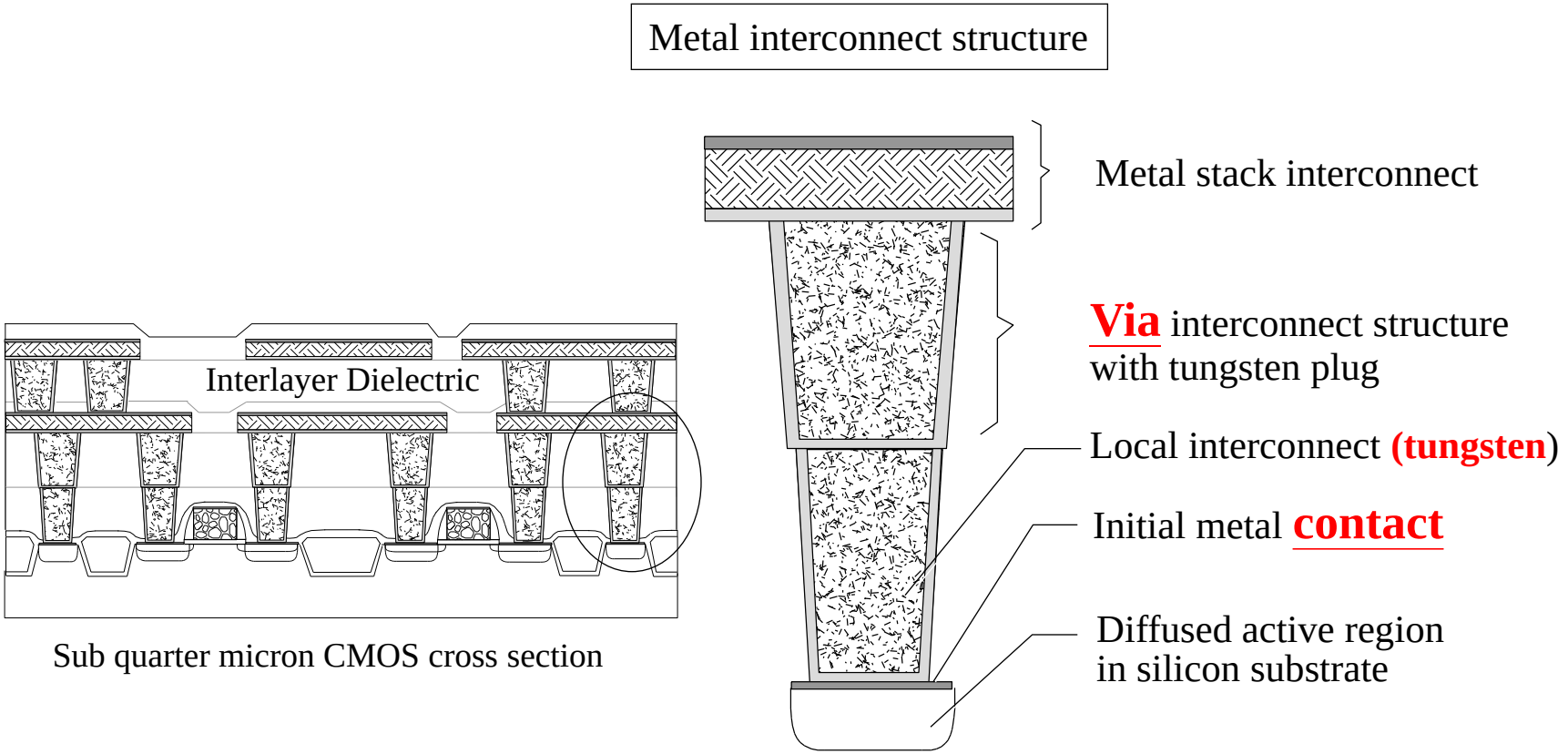
Metallization

Objectives

After studying the material in this chapter, you will be able to:

1. Explain the terminology for metallization.
2. List and describe the six categories of metals used in wafer fabrication. Discuss the performance requirements and give applications for each metal category.
3. Explain the benefits for using copper metallization in wafer fabrication. Describe the challenges for implementing copper.
4. State the advantages and disadvantages to sputtering.
5. Describe the physics of sputtering. Discuss different sputtering tools and applications.
6. Describe the benefits and applications for metal **CVD**.
7. Explain the fundamentals of copper electroplating.
8. Describe a process flow for dual Damascene processing.

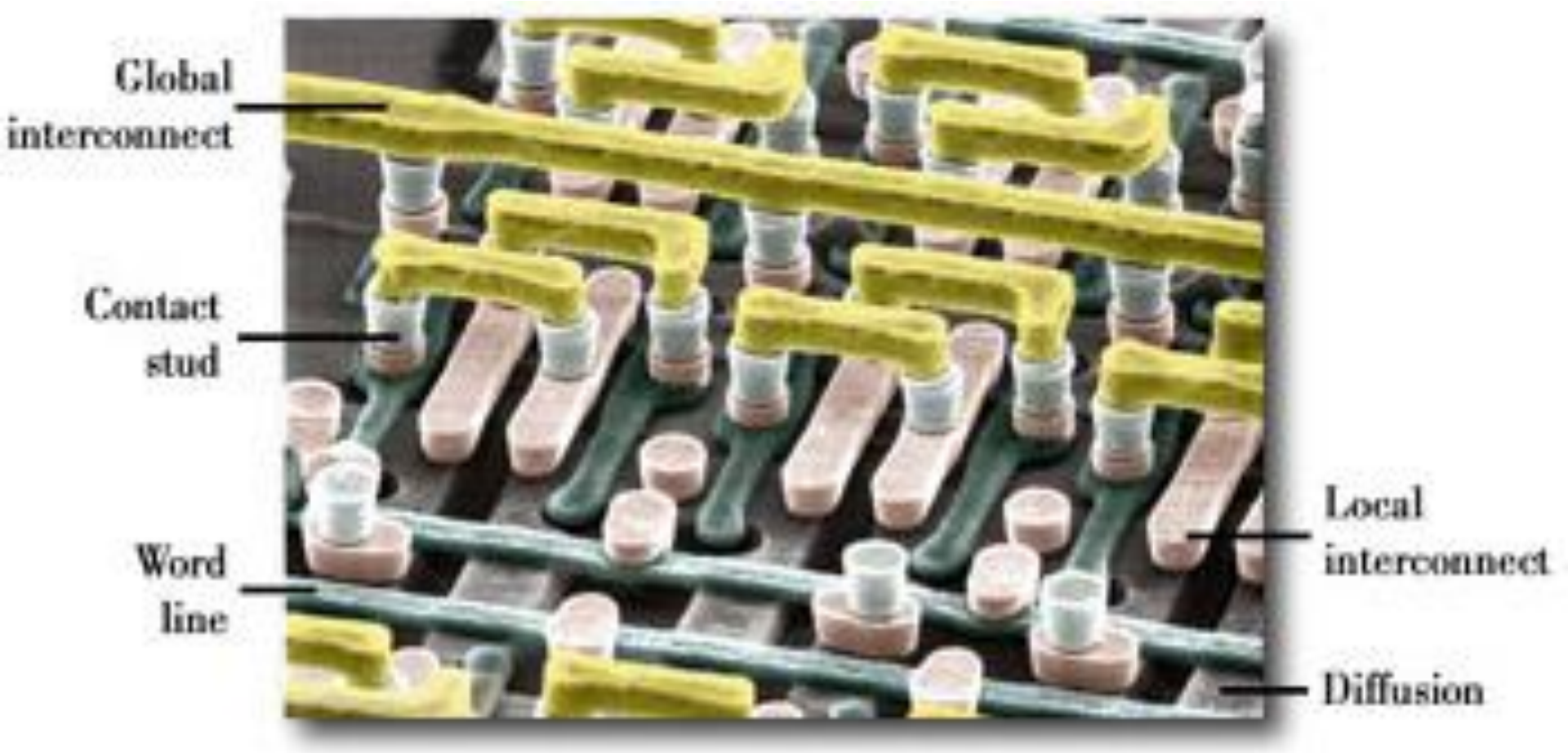
Overview of Multilevel Metallization



- **Interconnection (wiring) is to conduct the signal**
- **ILD electrically separates the metal line**
- **ILD is patterned and etched to form via pathways for metal interconnection**

Figure 12.1

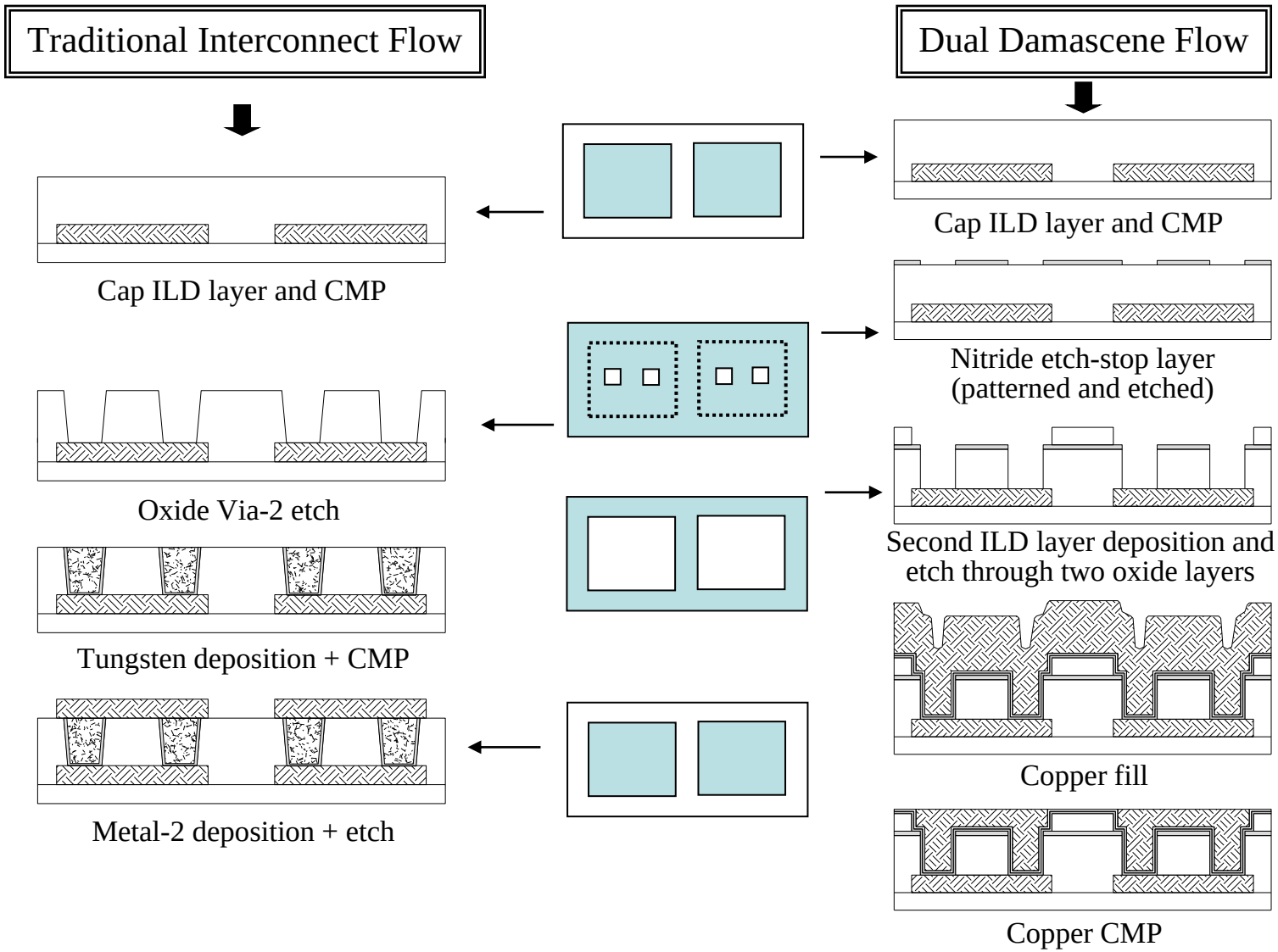
Applications: Interconnection



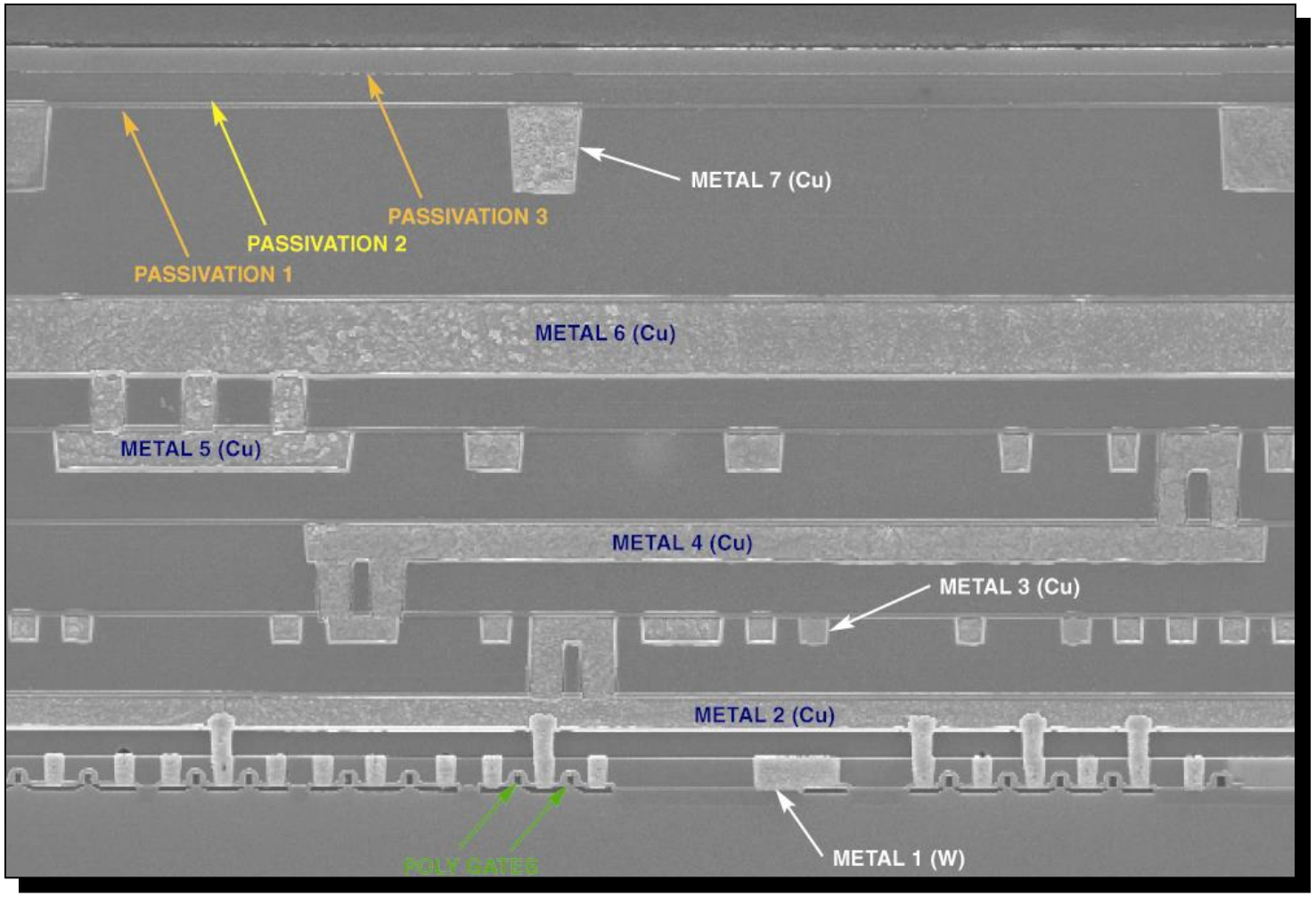
Performance in Advanced IC

- Reducing chip performance signal delay caused by interconnect lines was not a significant concern for older IC technology
- The dominant signal delay caused by the devices
- For advanced IC: denser wiring, signal delay due to interconnect becomes a larger portion of the clock time.

Traditional vs. Damascene Metallization



Copper Metallization



Photograph courtesy of Integrated Circuit Engineering

Photo 12.1

Requirements for Successful Metal Material

1. Conductivity: highly conductive and capable of handling high current density while maintaining electrical integrity
2. Adhesion: adhere to substrate, low contact resistance
3. Deposition: uniform structure and composition (for alloys) by a relatively low-temperature process, deposition into high-aspect ratio gaps
4. Patterning/Planarization: high-resolution patterning, ease of planarization
5. Reliability: withstand cyclic temperature
6. Corrosion: high resistance to corrosion with minimal chemical interactions with adjacent layers and underlying device regions
7. Stress: resistance to mechanical stress to reduce wafer distortion and material failures (cracking, void, corrosion)

Silicon and Select Wafer Fab Metals (at 20°C)

Material	Melting Temperature (°C)	Resistivity (μΩ-cm)
Silicon (Si)	1412	$\approx 10^9$
Doped Polysilicon (Doped Poly)	1412	≈ 500 – 525
Aluminum (Al)	660	2.65
Copper (Cu)	1083	1.678
Tungsten (W)	3417	8
Titanium (Ti)	1670	60
Tantalum (Ta)	2996	13 – 16
Molybdenum (Mo)	2620	5
Platinum (Pt)	1772	10

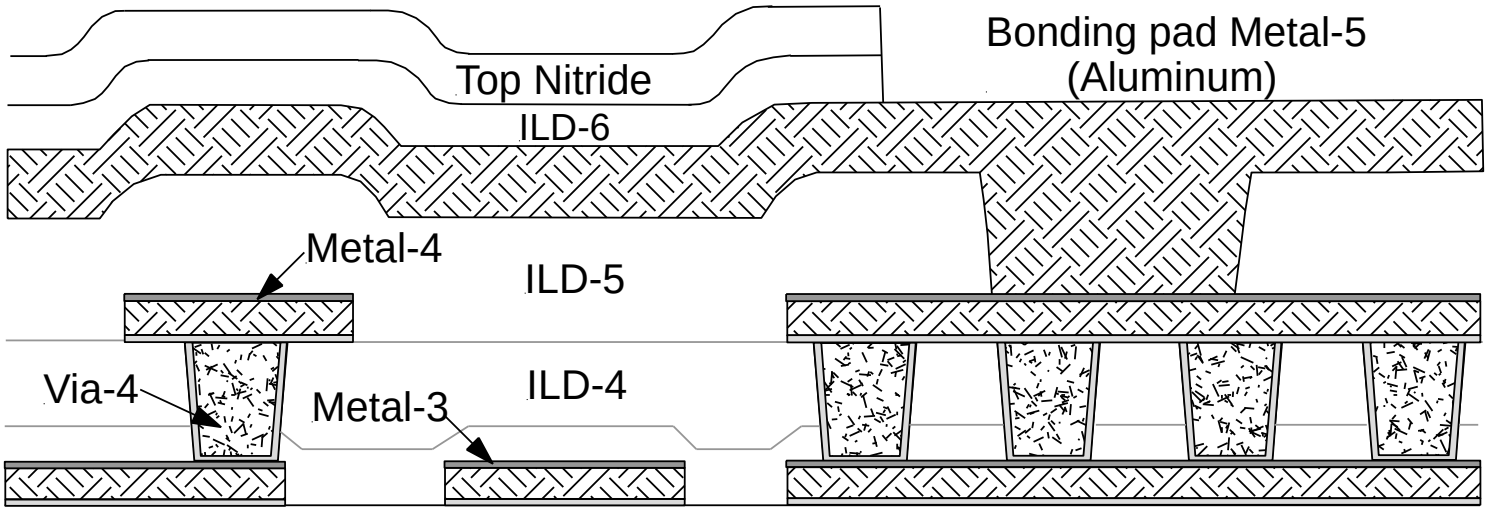
Table 12.1

Metals and Metal Alloys used in Wafer Fab

- Aluminum
- Aluminum-copper alloys
- Copper
- Barrier metals
- Silicides
- Metal plugs

Aluminum Interconnect

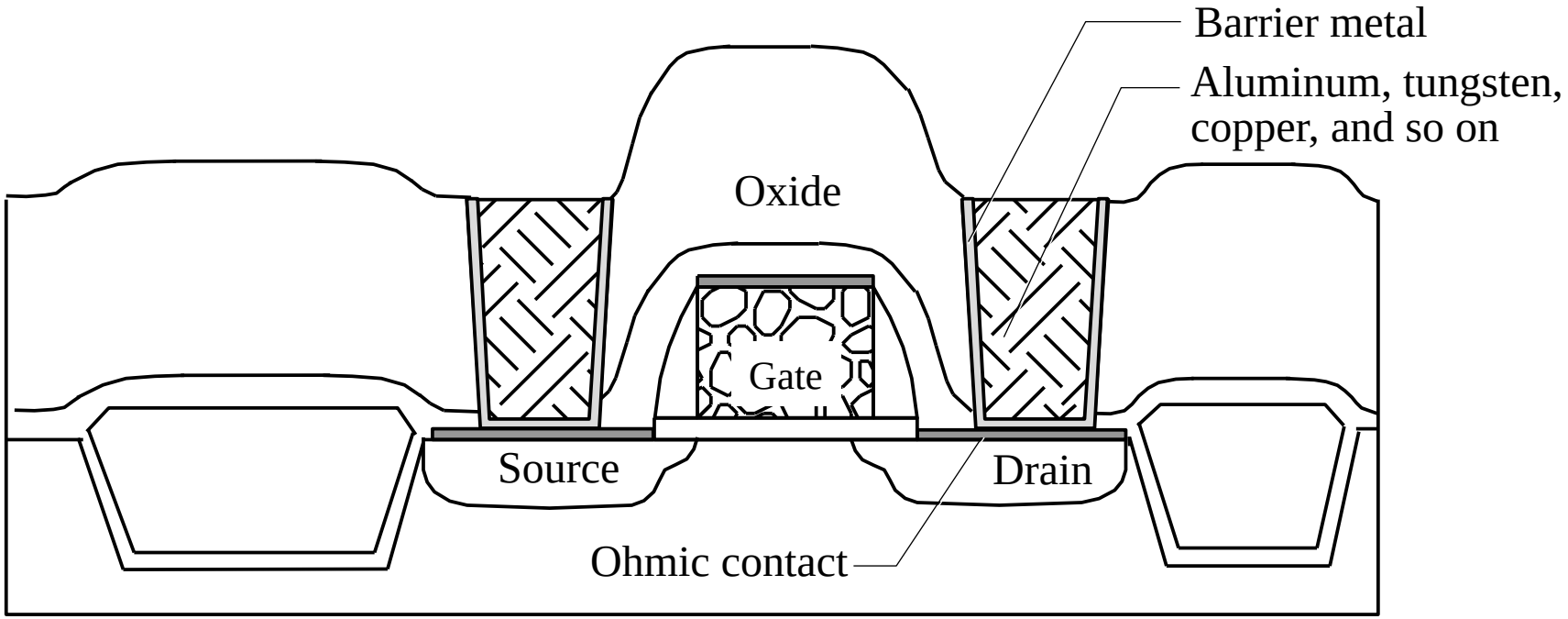
- Earliest metal, is still the most common one
- Good adhesion with Si and SiO_2, inexpensive (Au and Ag), easy etching, low contact resistance (break oxide)
- First Al ~ 500nm, the top Al ~ 2000nm



Metal-4 is preceded by other vias, interlayer dielectric, and metal layers.

Figure 12.3

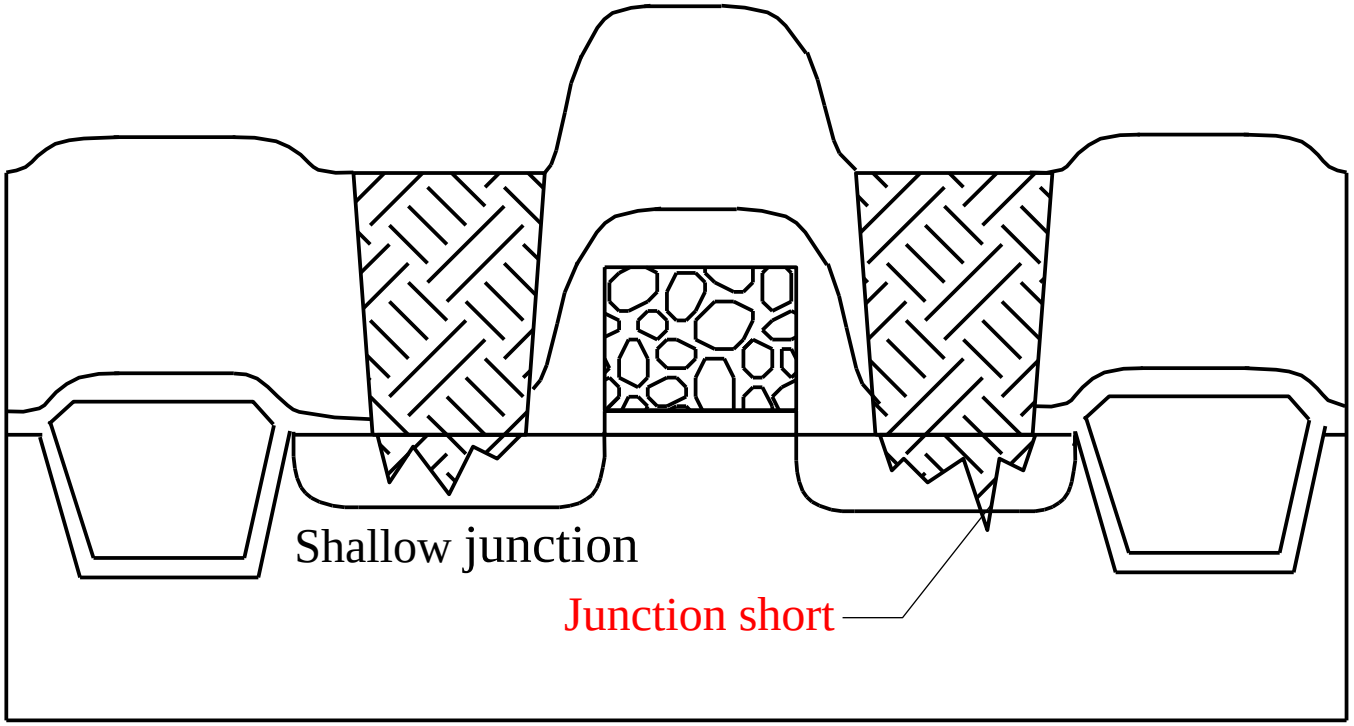
Ohmic Contact Structure



- Pure Al melts at 660°C
- Smaller contacts have higher resistance, inversely proportional to the area of the contact area
- Ohmic contacts are fabricated with a silicide above S/D
- Heat (400~ 450°C) to form ohmic contact (anneal or sinter)

Figure 12.4

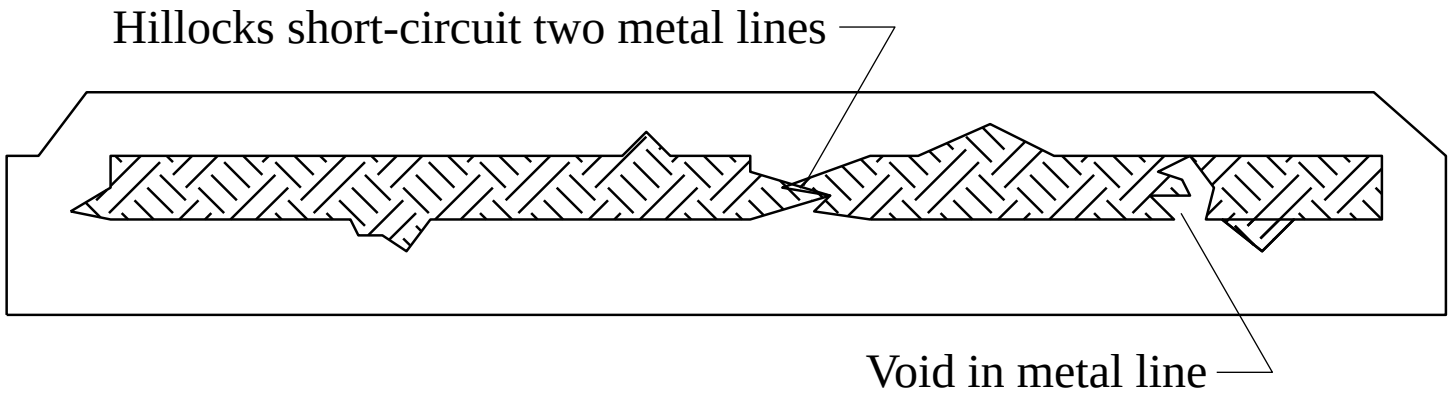
Junction Spiking



- If no barrier in-between Al-Si, Si diffuses into Al, causing Al spikes into silicon (non-uniform)
- The second method is using Al(1%Si) to over saturate Al with Si. This causes Si nodule increasing contact resistance
- Before Al deposition, HF-dip to remove native oxide

Figure 12.5

Hillock on a Metal Line due to Electromigration



- Electromigration: movement of Al atoms due to **momentum transfer** from electrons carrying the current
- Negative side: depletion of Al, forming void and open, down stream piles up Al, causing hillocks and causing short
- Add Cu (0.5 ~ 4%) to reduce EM, but Cu can't etch, care about residual Cu (promote corrosion)
- EM occurs during customer usage !

Figure 12.6

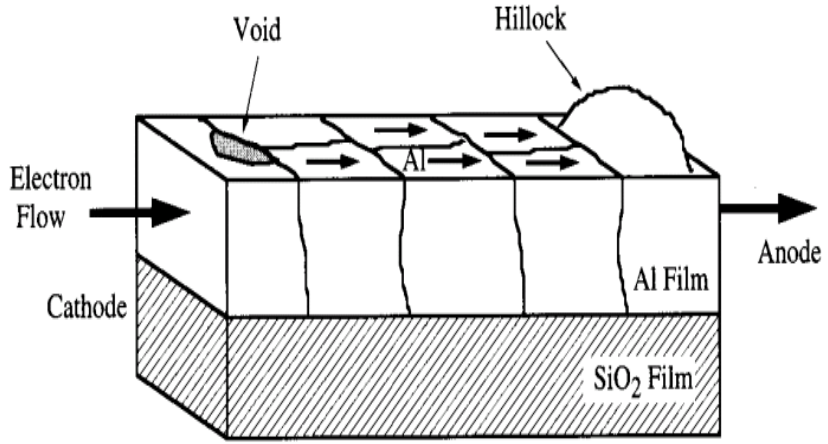


Figure 11–11 Schematic illustration of electromigration with resultant hillock and void formation. Diffusion of Al through grain boundaries is indicated.

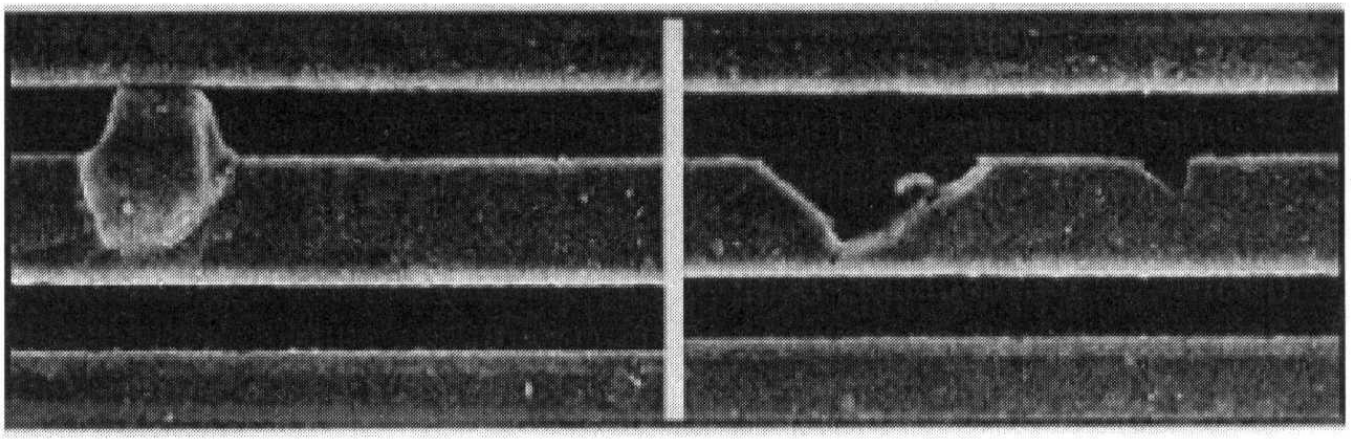


Figure 11–12 SEM top view of hillock and voids that have formed due to electromigration in an Al line [11.16]. Reprinted by permission of Materials Research Society.

The Benefits of Copper Interconnect

1. Reduction in resistivity
   - 1.678 μΩ-cm vs. 2.65 μΩ-cm for Aluminum
2. Reduction in power consumption
3. Tighter packing density (narrow line)
4. Superior resistance to electromigration
5. Fewer process steps
   - 20 to 30 % fewer steps with damascene technique

Change in Interconnect Delay Compared to 0.25-μm Device Generation

Technology	0.25 μm	0.18 μm	0.13 μm
Conventional Interconnect Technology: • Al/Cu Interconnect Alloy and TiN Barrier Metal	0	+21%	+93%
New Technology Introduced by Generation: • Reduced Barrier Thickness • Low-*k* (3.0) dielectric • Dual Damascene Cu Interconnect and plugs	-10%	-27%	-16%

- Narrow line increases R, dense line-space increases C. Both degrades speed
- Cu used to reduce R, low-k used to reduce C
- Same Cu line width can carry high I, get a tighter package density

Table 12.2

Comparison of Properties/Processes Between Al and Cu

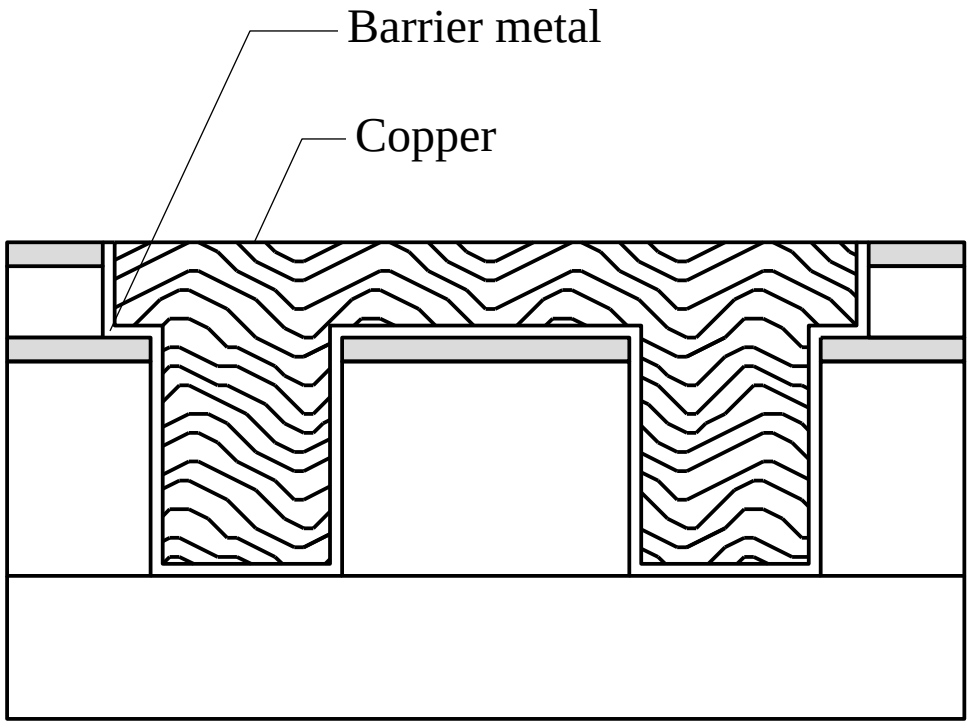
Property/Process	Al	Cu
Resistivity (μΩ-cm)	2.65 (3.2 for Al-0.5%Cu)	1.678
Electromigration resistance	Low	High
Corrosion resistance (in air)	High	Low
CVD processing	Yes	No
CMP (chemical mechanical planarization) processing	Yes	Yes

Table 12.3

Three Major Challenges to Using Copper Interconnects in Semiconductor Products

1. Copper diffuses quickly into oxides and silicon, junction leakage and oxide reliability
   - Tungsten plugs used as the first metal
2. Copper cannot be easily patterned using regular plasma etching techniques, no volatile by-product
   - Damascene
3. Copper oxidizes quickly in air at low temperatures (<200°C) and does not form a protective layer to stop further oxidation.
   - Barrier metal

Barrier Layer for Copper Interconnect Structure



Prevent intermixing of metal (~ 23 nm or less for 0.18 node)

Figure 12.7

The Essential Properties of Barrier Metal

1. Good diffusion barrier properties so that the diffusivity of the two interface materials (e.g., tungsten and silicon) is low at the sintering temperature (sintering refers to joining of the materials by thermal means).
2. High electrical conductivity with low ohmic contact resistance.
3. Good adhesion between the semiconductor and metal.
4. Resistance to electromigration.
5. Stability when thin and at high temperature.
6. Resistance to corrosion and oxidation.

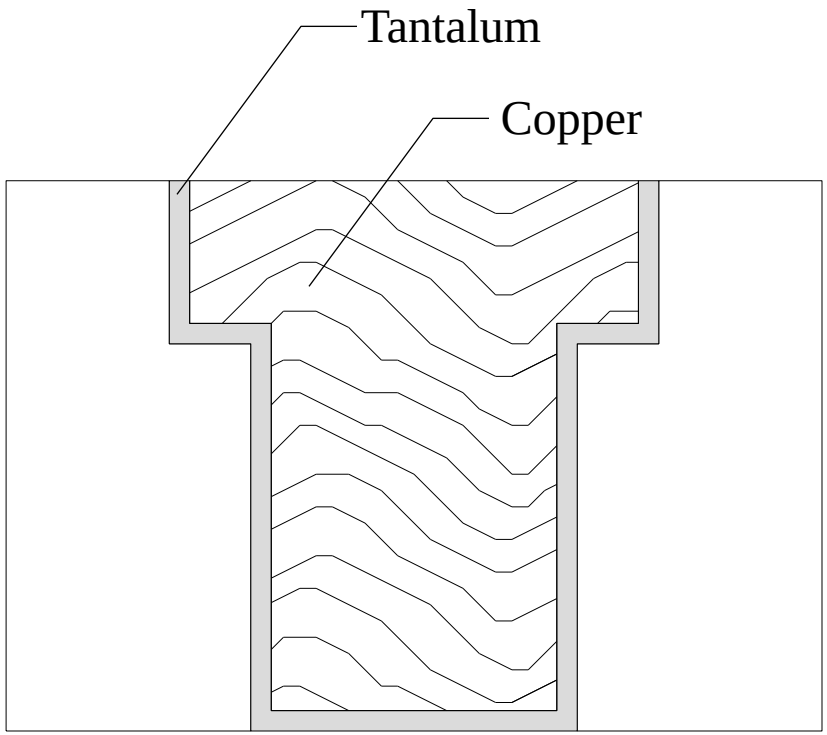
Barrier Metals

- Metals commonly used for barrier metals are a class of high melting point metals known as refractory metals.
- Common refractory metals: Ti, W, Mo, Co, and Pt
- Ti is used for its improved adhesion, reduced contact resistance, reduced stress and controlled electromigration
- TiN, and TiW are candidates for inhibit diffusion between Si and Al
- Ti and TiN are typically deposited in a cluster tool to keep oxides from forming between the two layers

Requirements for Copper Barrier Metal

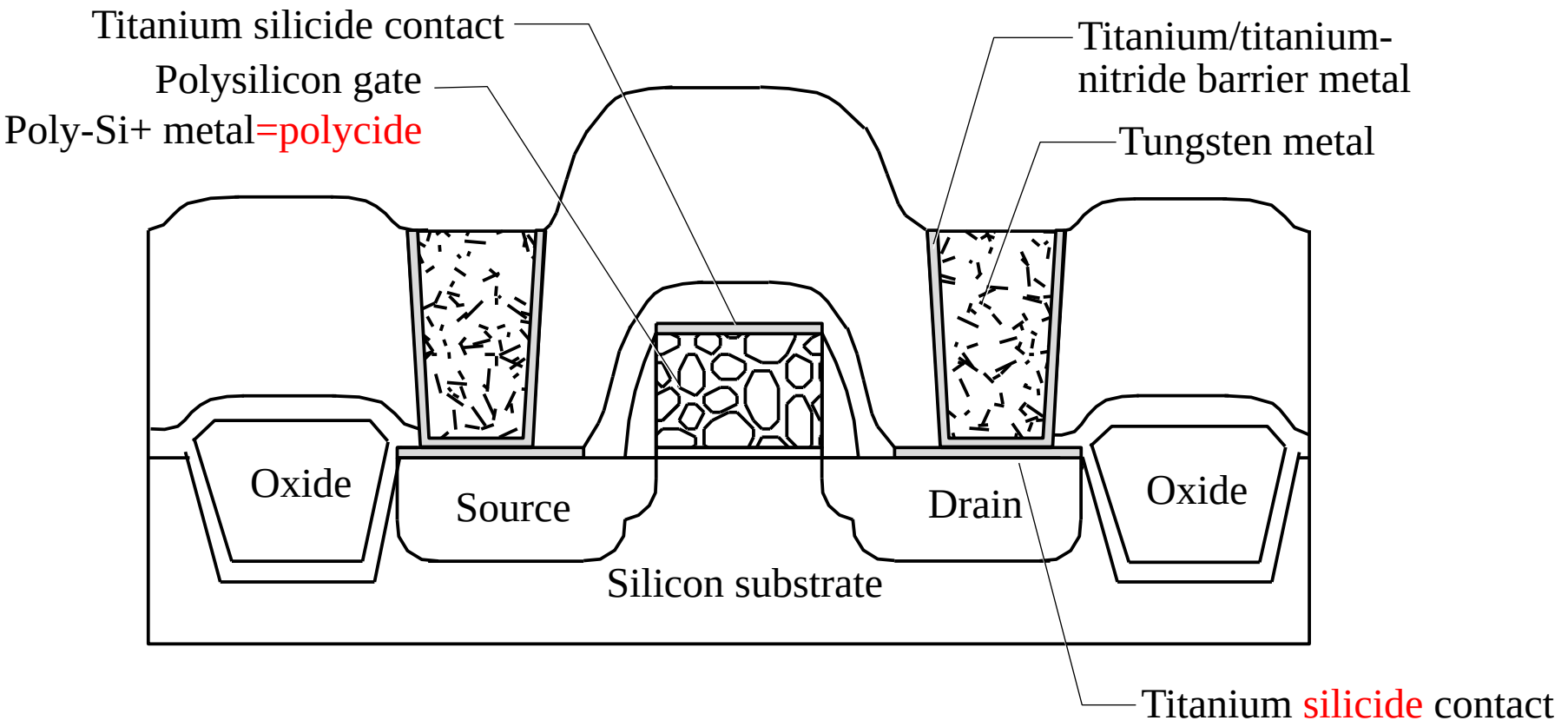
1. Prevent copper diffusion.
2. Low film resistivity.
3. Good adhesion to both dielectric material and copper.
4. Compatible with chemical-mechanical polish (CMP).
5. Metal layer is continuous and conformal with good step coverage and deposition in high aspect ratio gaps.
6. Minimal thickness to allow the copper to occupy the maximum cross-sectional area.

Ta for Copper Barrier Metal



- For Cu interconnect, Ta, TaN, WN and TaSiN are candidate materials for barrier metals
- The diffusion barrier must remain thin (~ 75Å) so that it does not affect the resistivity of the high-aspect ratio plug while still acting as a barrier metal

Refractory Metal Silicide at a Silicon Contact



- Refractory metals react with silicon when alloyed together to form a silicide
- A silicide is a metal compound that is thermally stable and provides for low electrical resistivity at the Si/refractory metal interface
- Ti, Co, Ni are common refractory metal used for contacts in aluminum interconnect technology

Figure 12.9

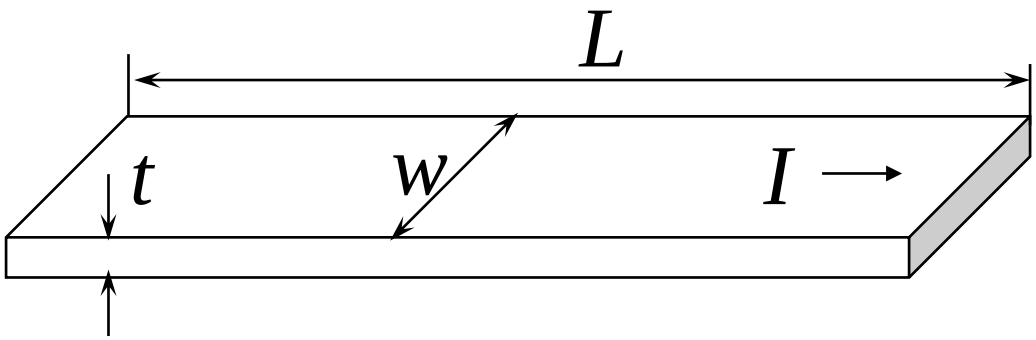
Some Properties of Select Silicides

- Doped poly-Si is used as the gate electrode and has a relatively high resistivity (~ 500 μΩ –cm)
- It leads to an undersirable RC signal delay
- Polycide: reduced resistance and good interfacial to oxide

Silicide	Lowest Eutectic Temperature (°C)	Typical Forming Temperature1 (°C)	Resistivity (μΩ-cm)
Cobalt/silicon ($CoSi_2$)	900	550 – 700	10 – 18
Molybdenum/silicon ($MoSi_2$)	1410	900 – 1100	100
Platinum/silicon (PtSi)	830	700 – 800	28 – 35
Tantalum/silicon ($TaSi_2$)	1385	900 – 1100	35 – 45
Titanium/silicon ($TiSi_2$)	1330	600 – 800	13 – 25
Tungsten/silicon (WSi_2)	1440	900 – 1100	70

1 B. El-Kareh, *Fundamentals of Semiconductor Processing Technologies*, Kluwer Academic Publishing, Boston, MA, 1995**, p. 537.**

Sheet Resistance Concepts



Apply current I and measure voltage V,

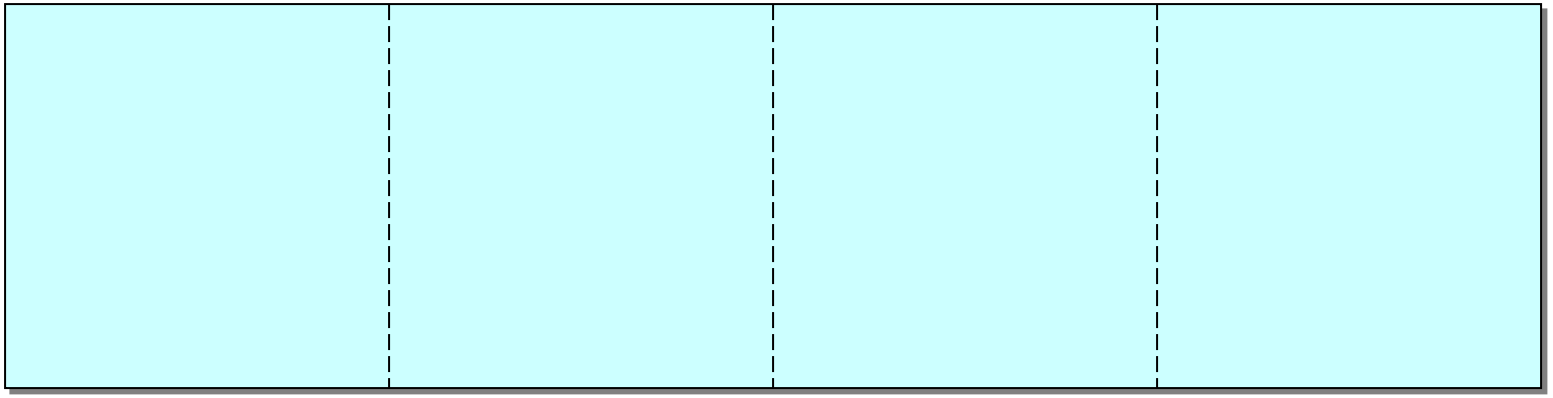
Resistance: $R = V/I = \rho L/(wt)$

For a square sheet, $L = w$, so $R = \rho/t = R_s$

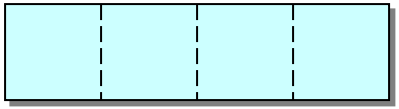
Unit of R_s: ohms per square ($\Omega/\square$)

Sheet Resistance

For this two conducting lines patterned from the same metal thin film with the same length-to-width ratios, are their line resistance the same?



Yes.



Polycide on Polysilicon

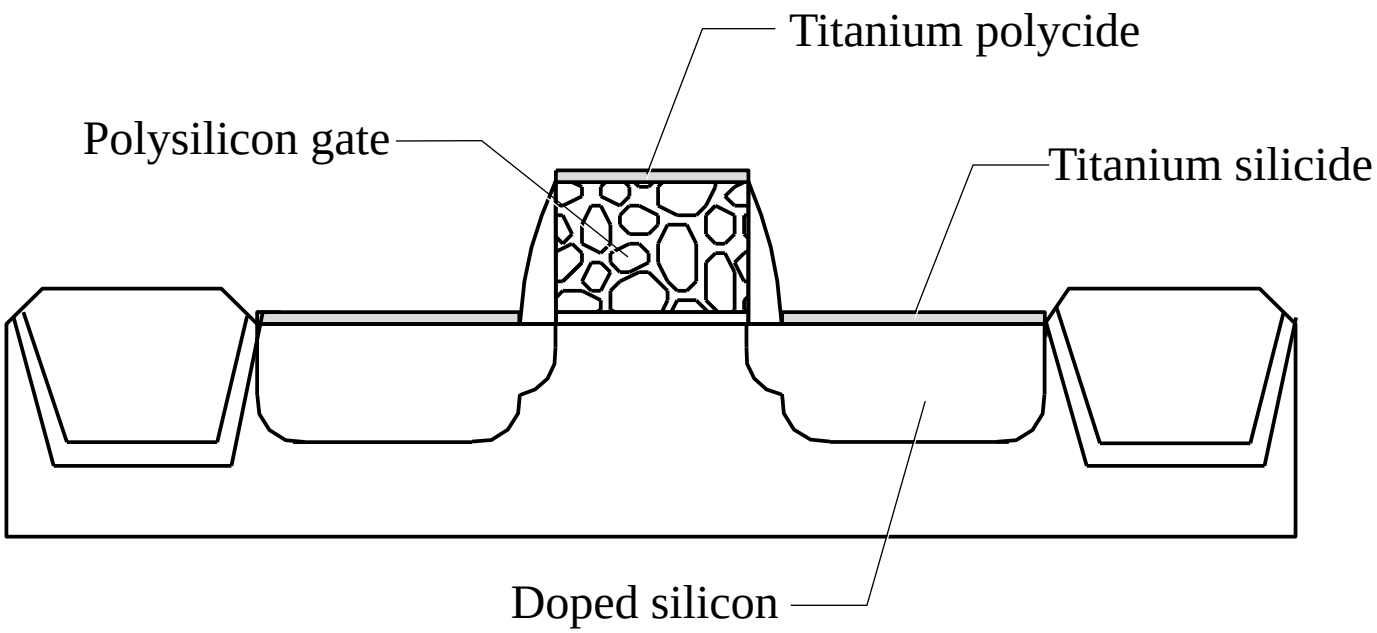
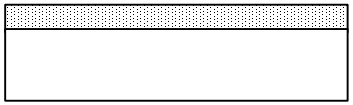
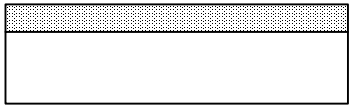


Figure 12.10

Anneal Phases of $TiSi_2$

	Sintering Temperature	Resistivity
$TiSi_2$ – C49 	625 – 675°C	60 – 65 μΩ-cm
$TiSi_2$ – C54 	800°C	10 – 15 μΩ-cm

- $CoSi_2$ replace $TiSi_2$ for 0.18 μm due to reduced resistivity
- Silicide is not barrier, so it needs barrier layer (TiN) with W or Al

Figure 12.11

Chip Performance Issues Related to a Salicide Structure

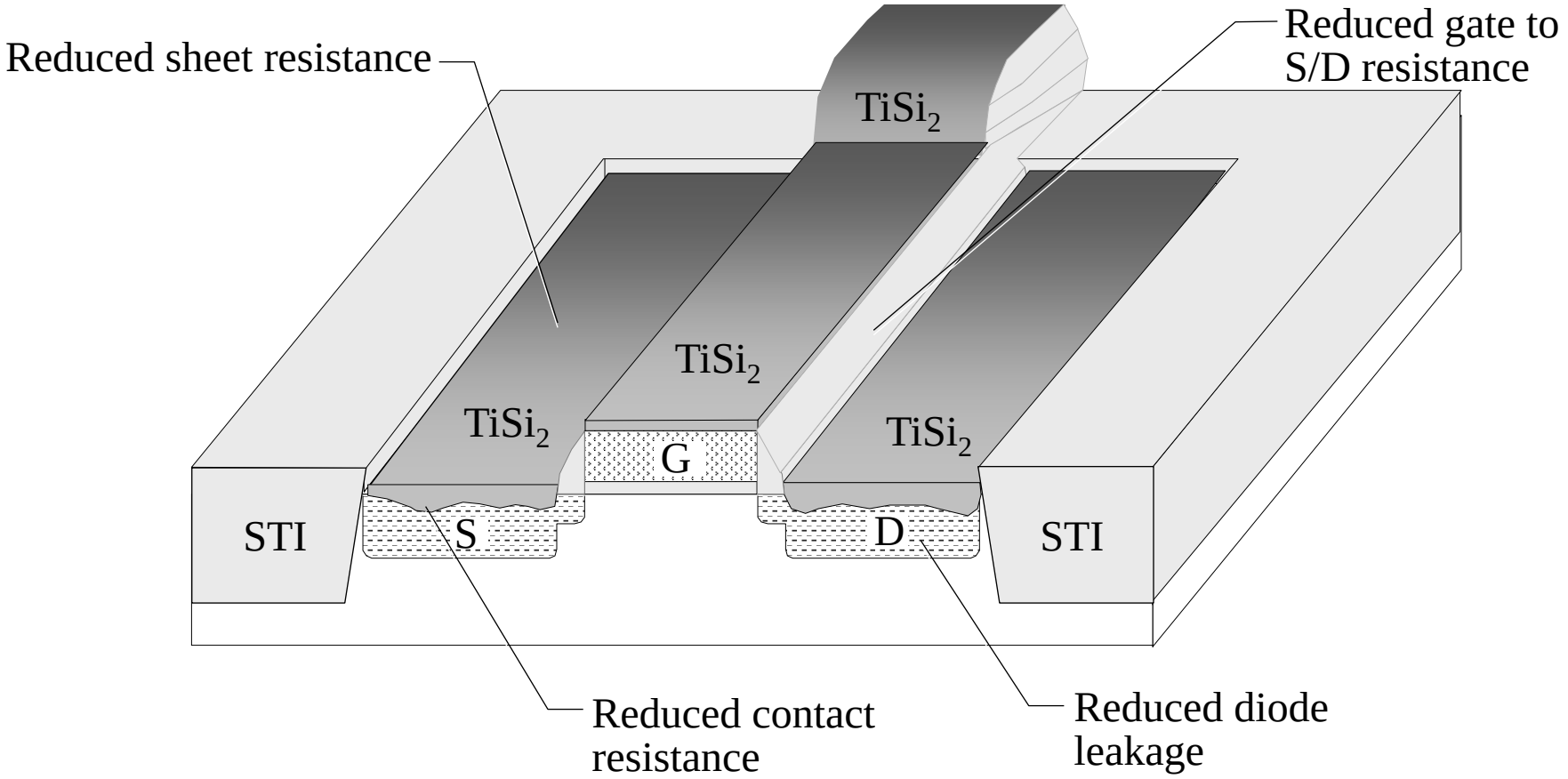
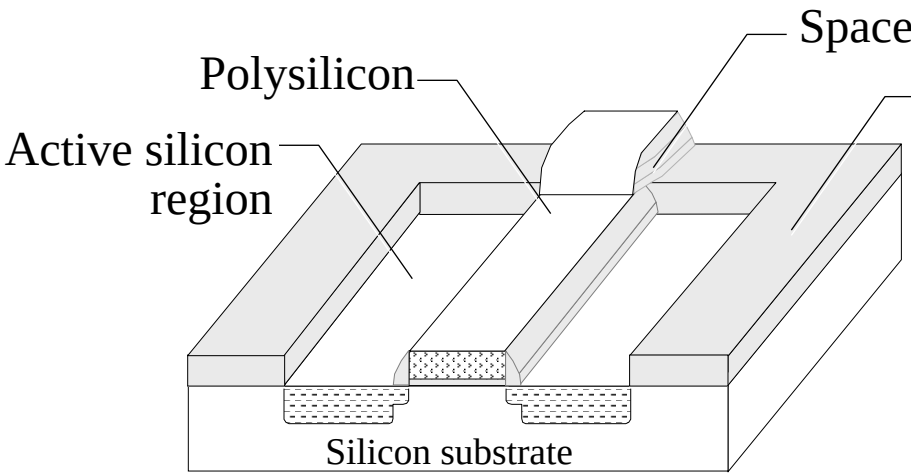
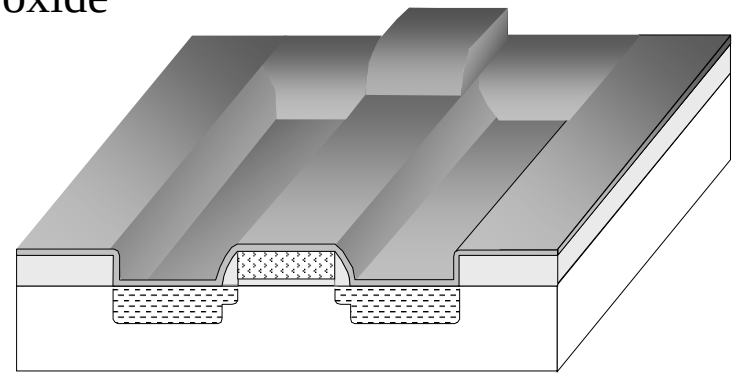


Figure 12.12

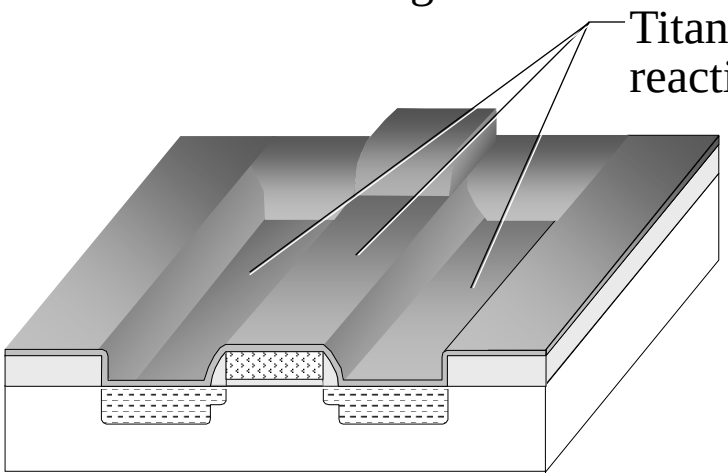
Formation of Self-Aligned Metal Silicide (Salicide)



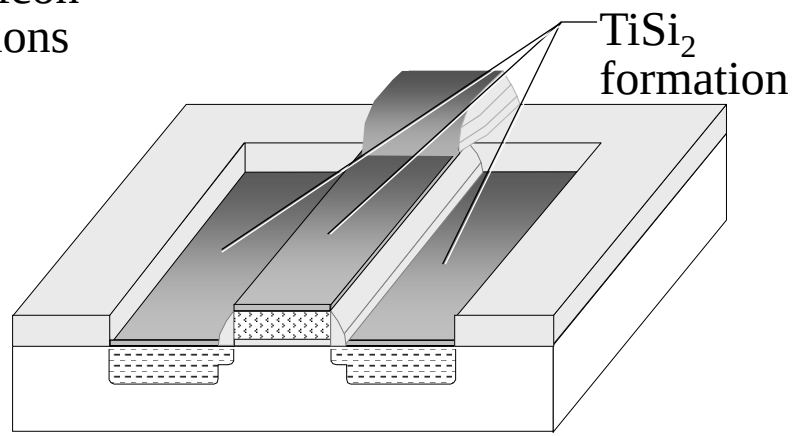
1. Active silicon regions



2. Titanium deposition

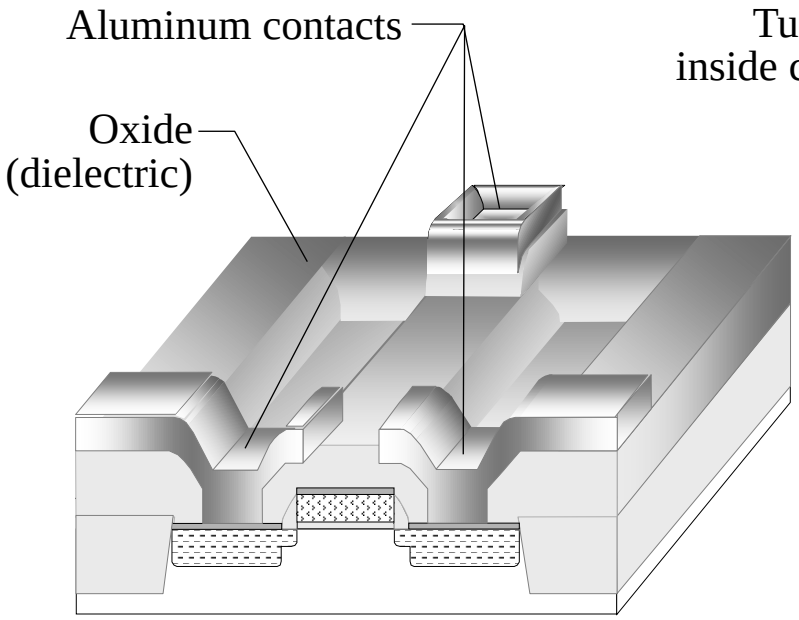


3. Rapid thermal anneal treatment (1st RTA, C49) 600-800C



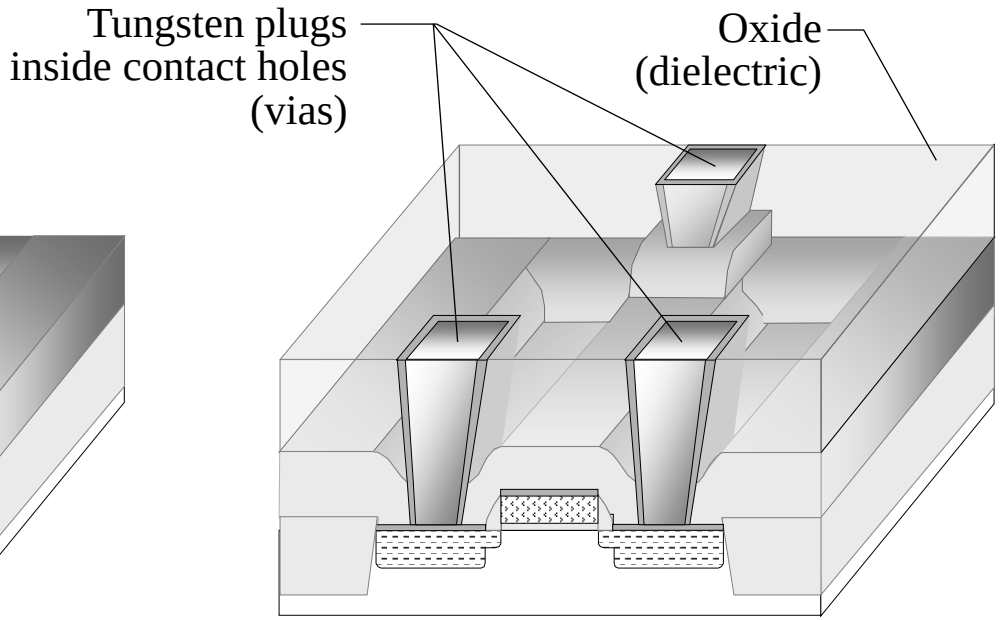
4. Titanium strip (NH4OH: H2O2) and 2nd RTA, C54 ~ 800-900C

Tungsten Plug for Multilevel Metal Layers



Early metallization technique

1. Contact etch through oxide
2. Aluminum deposition
3. Aluminum etch



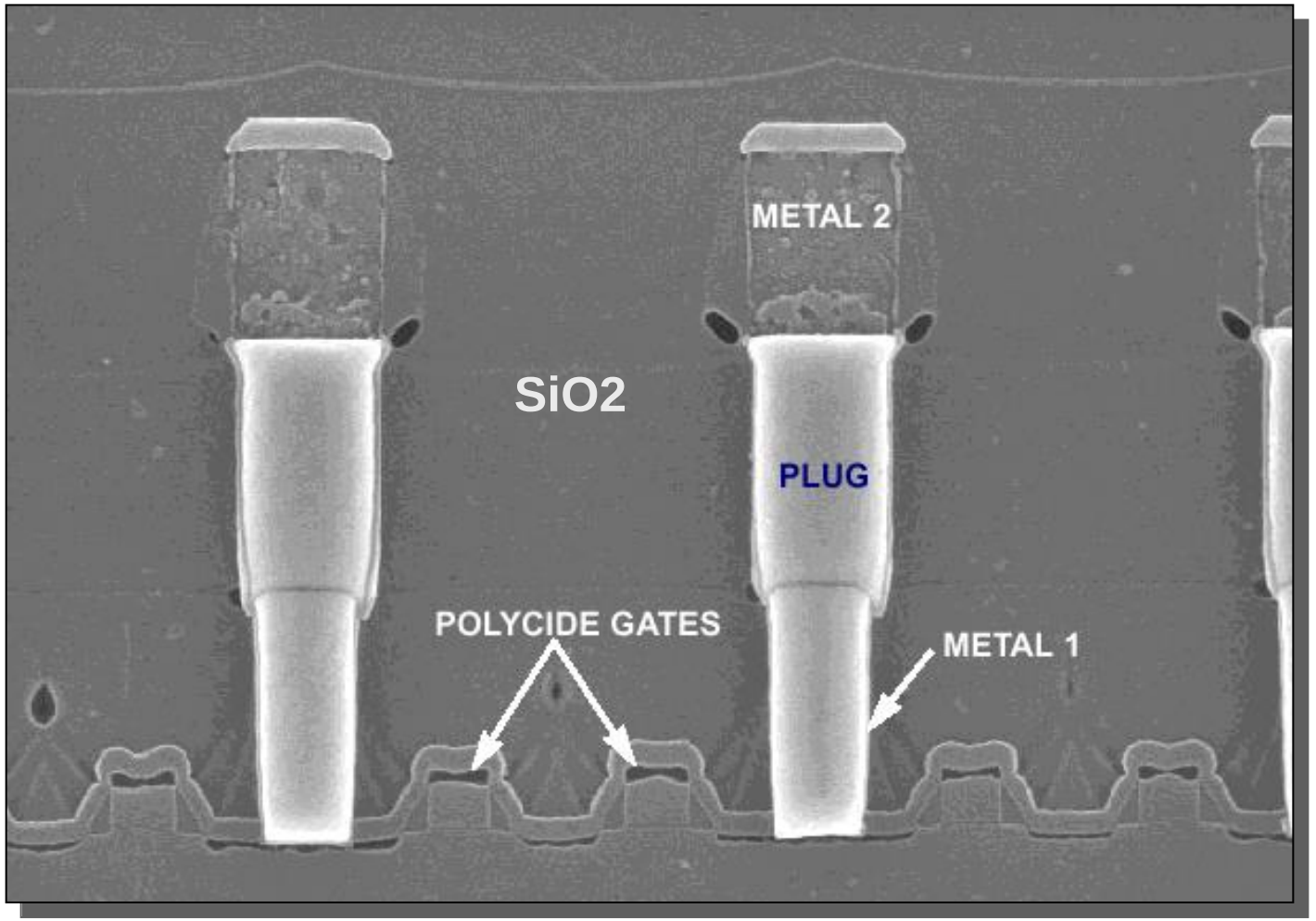
Current metallization technique

1. Thick oxide deposition
2. Oxide planarization
3. Contact etch through oxide
4. Barrier metal deposition
5. Tungsten deposition (CVD)
6. Tungsten planarization

W-plug

- Multilevel metallization creates the need for billions of vias filled with metal plugs to form electrical pathways between two metal layers
- A contact plug is also used to connect the silicon devices in the wafer to the first level of metallization
- Tungsten has been traditionally used as a plug because of its ability to uniformly fill the high-aspect ratio vias using CVD
- W is resistant to electromigration failure, can be used between Si and first metal layer
- W is a refractory material with a melting point of 3417°C and a bulk resistivity of 52.8 $\mu\Omega$ –cm

Metal Plugs in IC



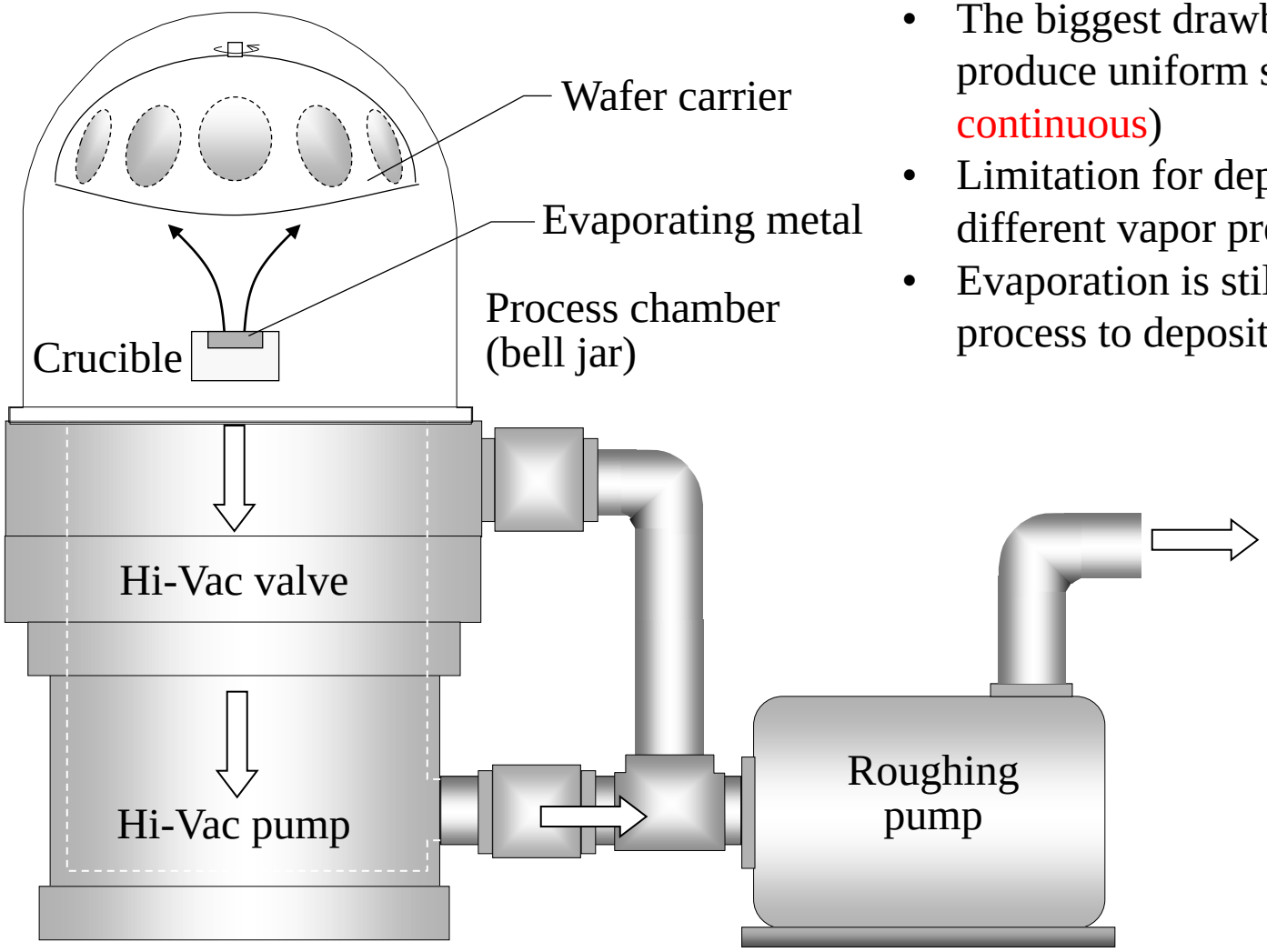
Photograph courtesy of Integrated Circuit Engineering

Photo 12.2

Metal Deposition Systems
Physical Vapor Deposition (PVD)

- Evaporation
- Sputtering
- Metal CVD
- Copper electroplating

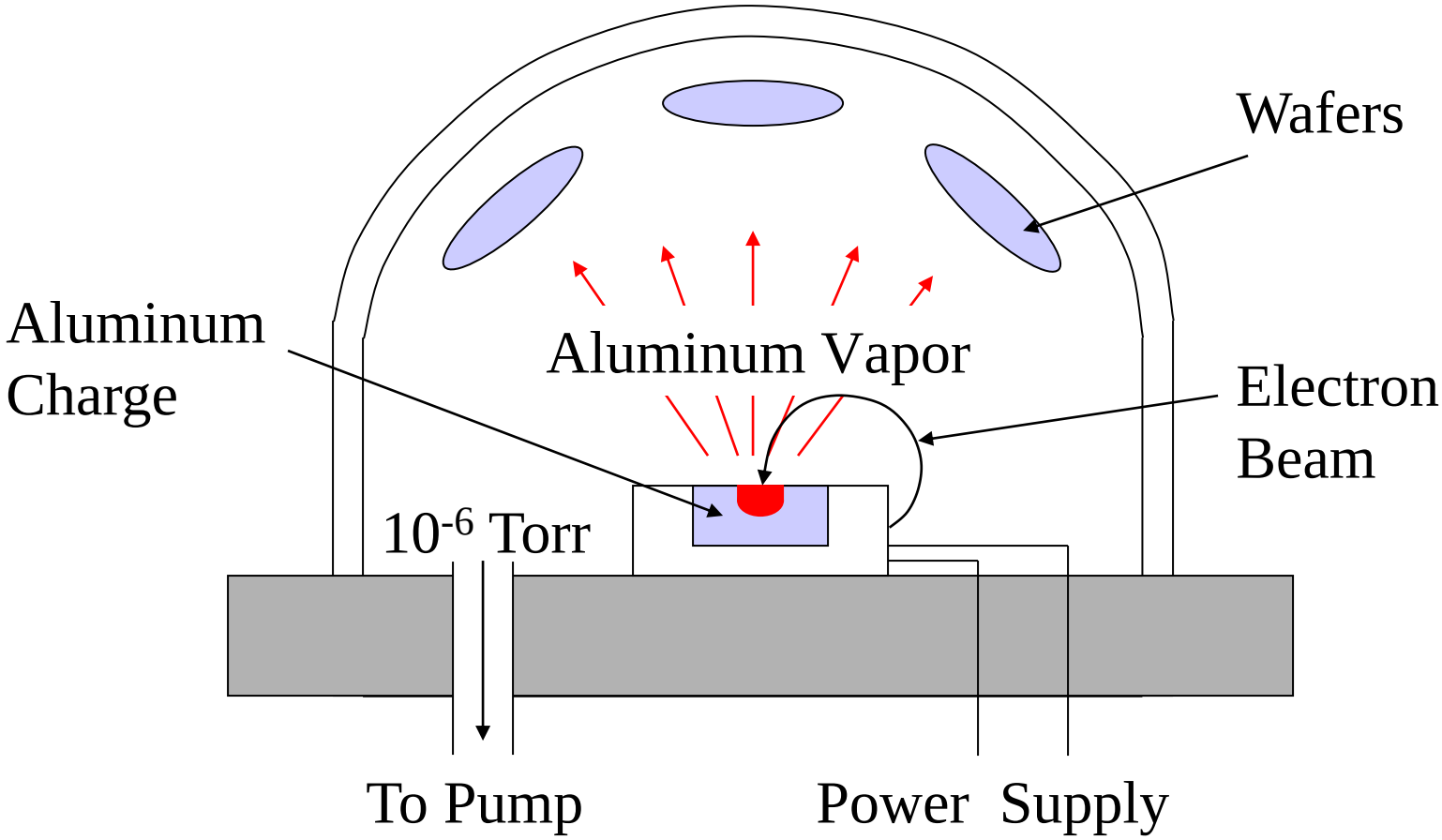
Simple Evaporator



- The biggest drawback is the inability to produce uniform step coverage (not continuous)
- Limitation for depositing alloys because of different vapor pressure
- Evaporation is still used in chip package process to deposit solder bumps

Figure 12.15

Electron Beam Evaporator



Some Advantages of Sputtering

- Using high energy particles strike a solid slab of high-purity target material and physically dislodge atoms
- Ability to deposit and maintain complex alloys.
- Ability to deposit high-temperature and refractory metals.
- Ability to deposit controlled, uniform films on large wafers (200 mm and larger).
- Ability of multichamber cluster tools to clean the wafer surface for contamination and native oxides before depositing metal (referred to as in situ sputter etch).

Simple Parallel Plate DC Diode Sputtering System

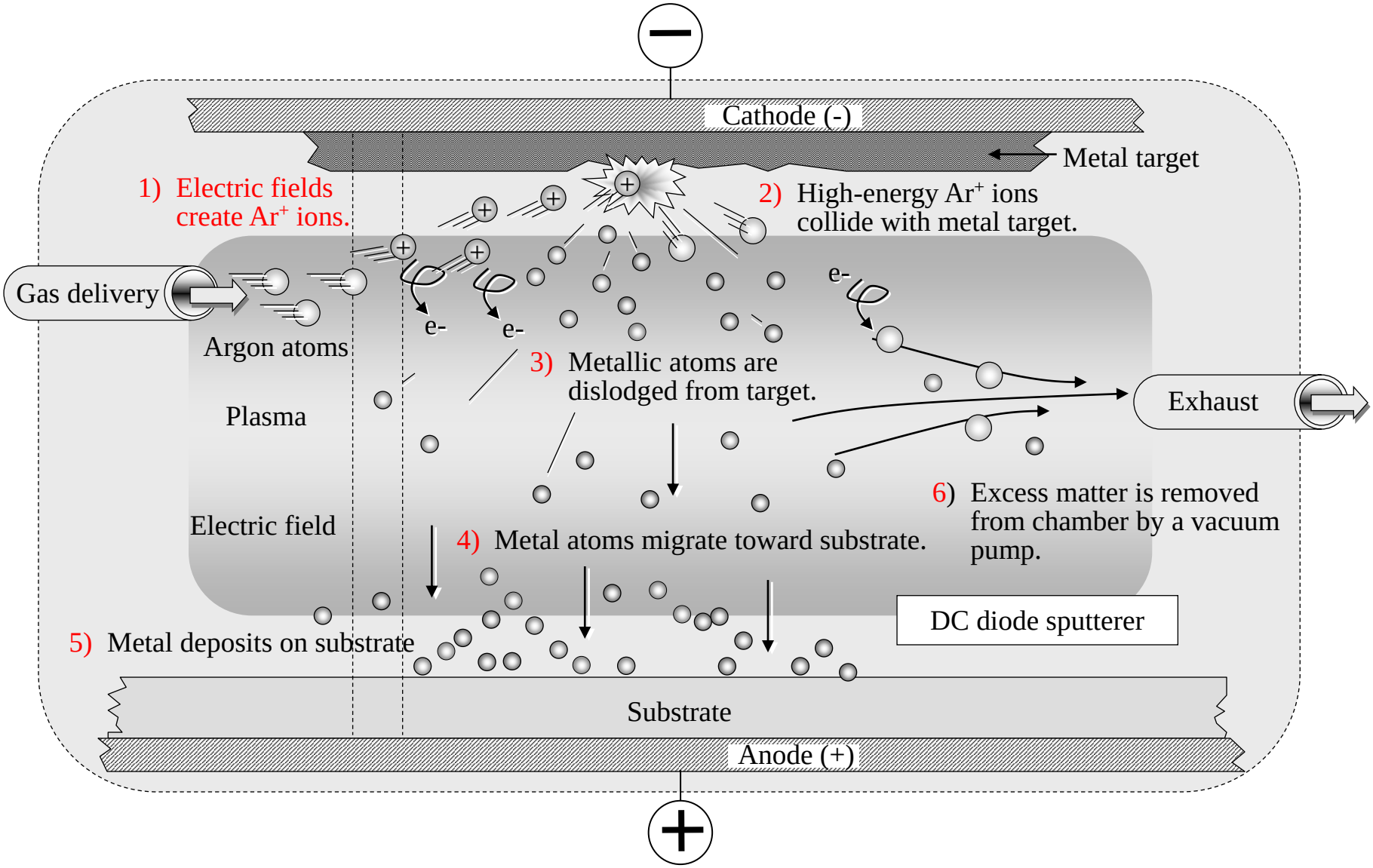


Figure 12.16

Dislodging Metal Atoms from Surface of Sputtering Target

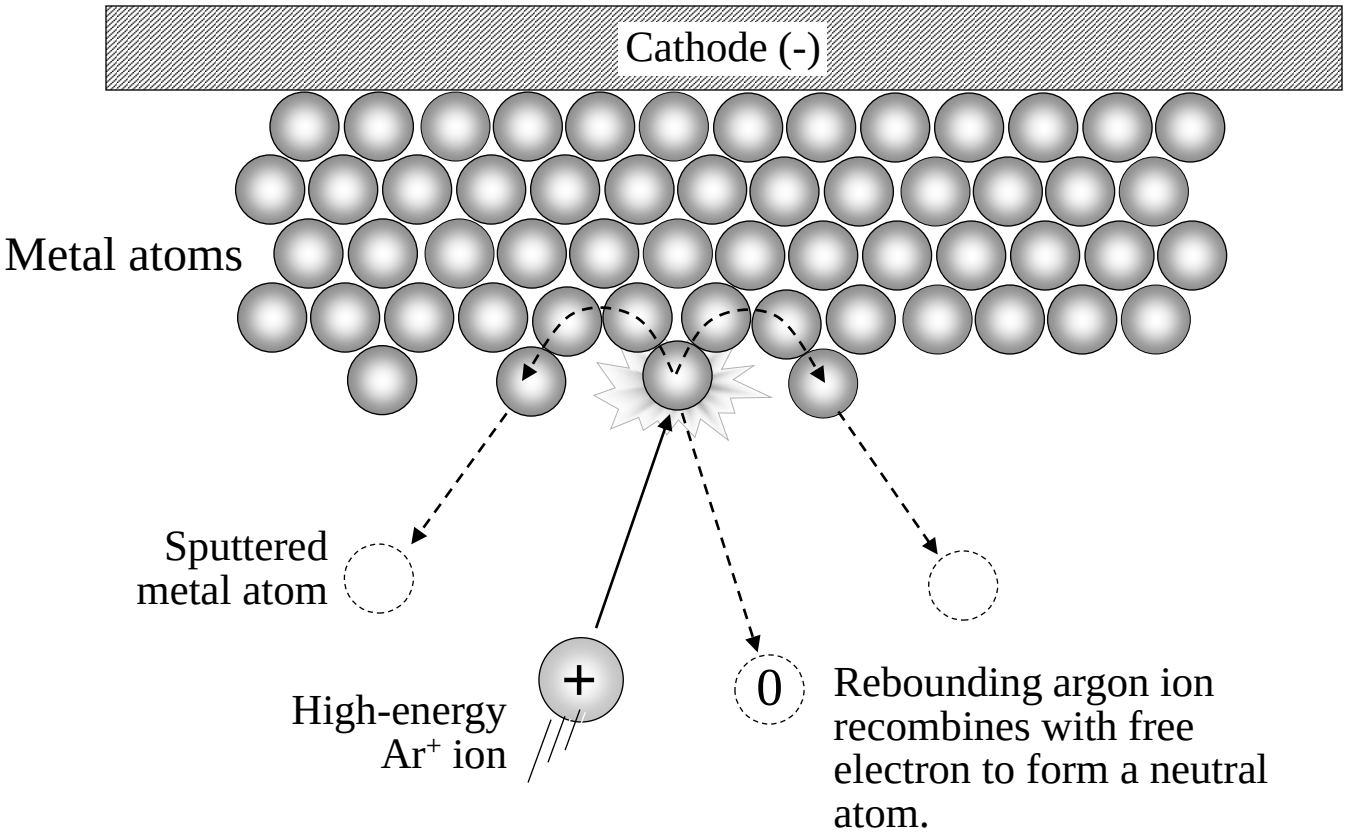


Figure 12.17

Factors that Affect Sputter Yield

- The sputtering yield is defined as the number of atoms ejected by the target per incident ion that strikes it, 4-fact affect the yield

1. Incident angle of the bombarding ions.
2. Composition and geometry of the target material.
3. Mass of bombarding ions.
4. Energy of the bombarding ions.

Different Species Landing on Substrate

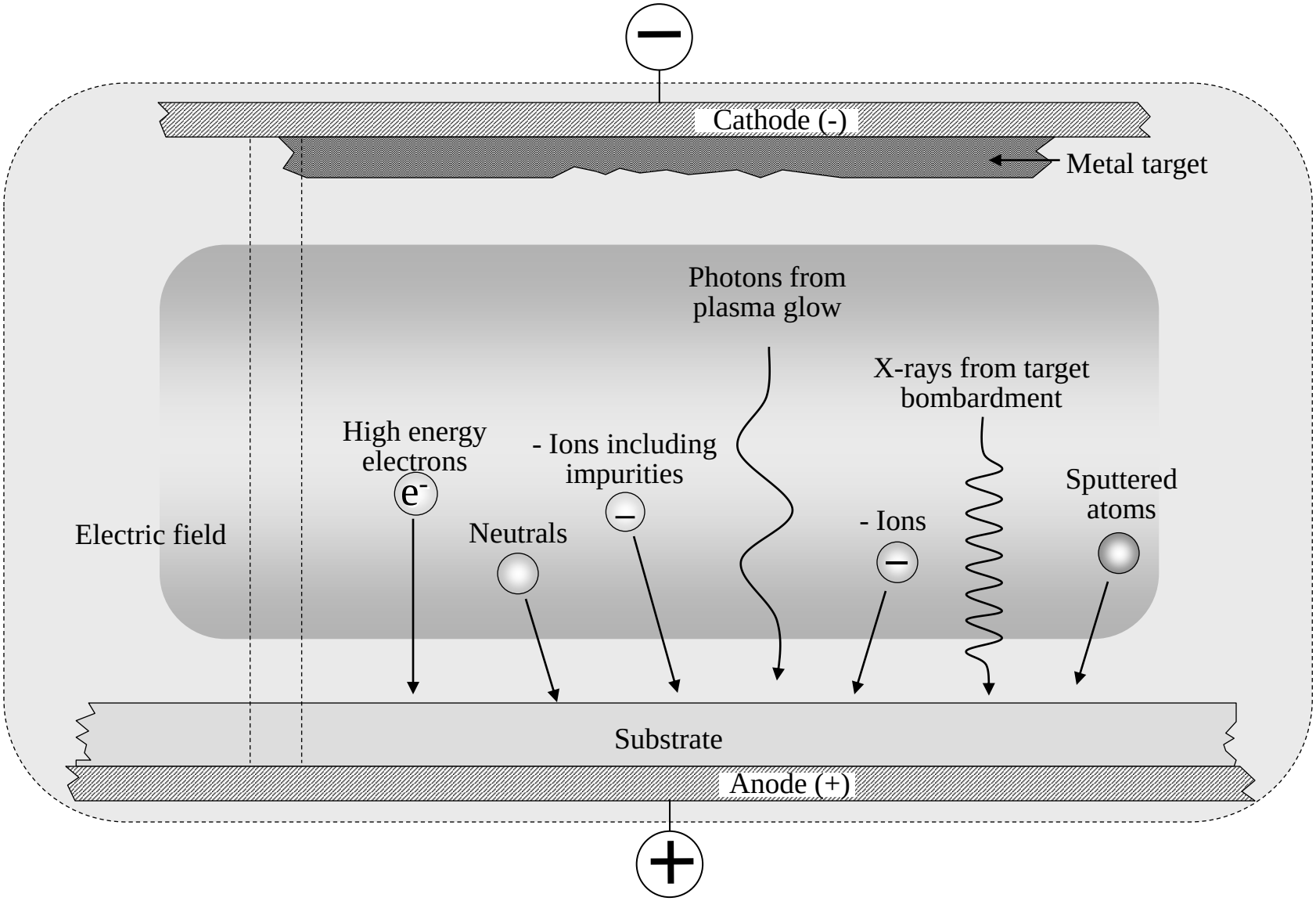
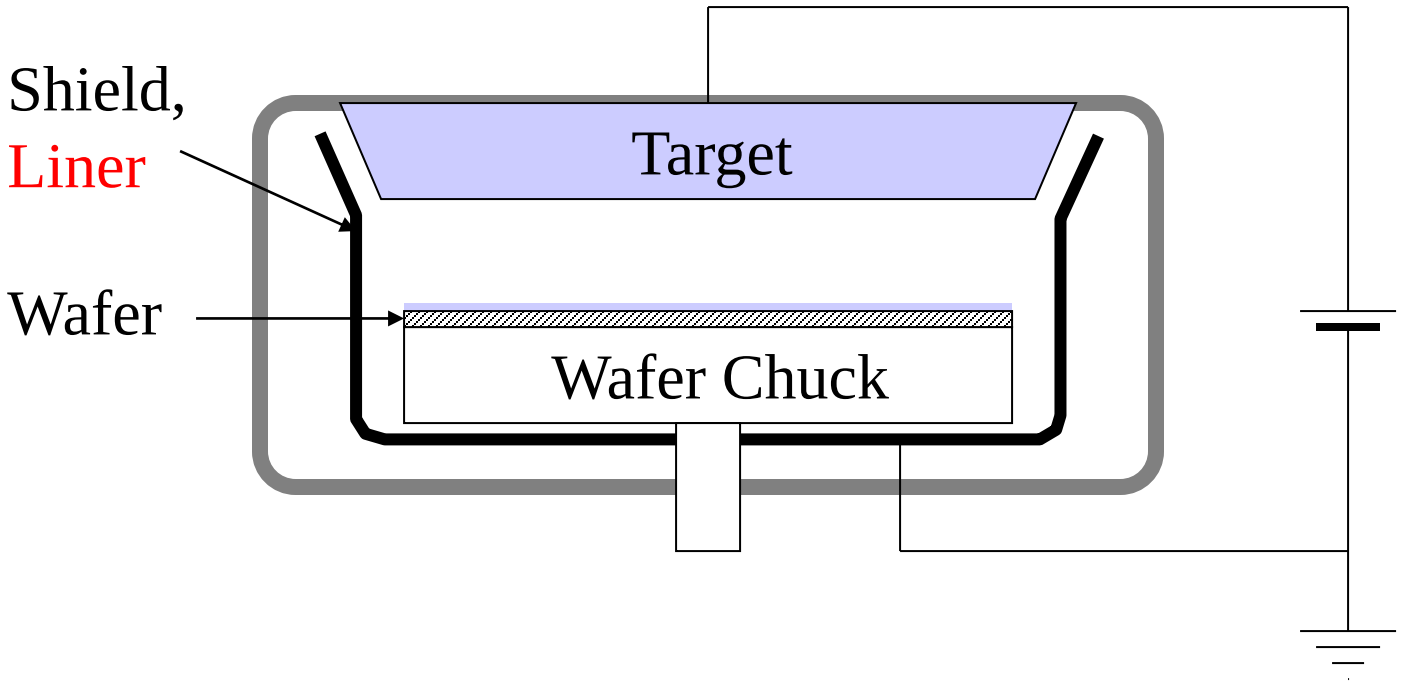


Figure 12.18

PVD Chamber with Shield

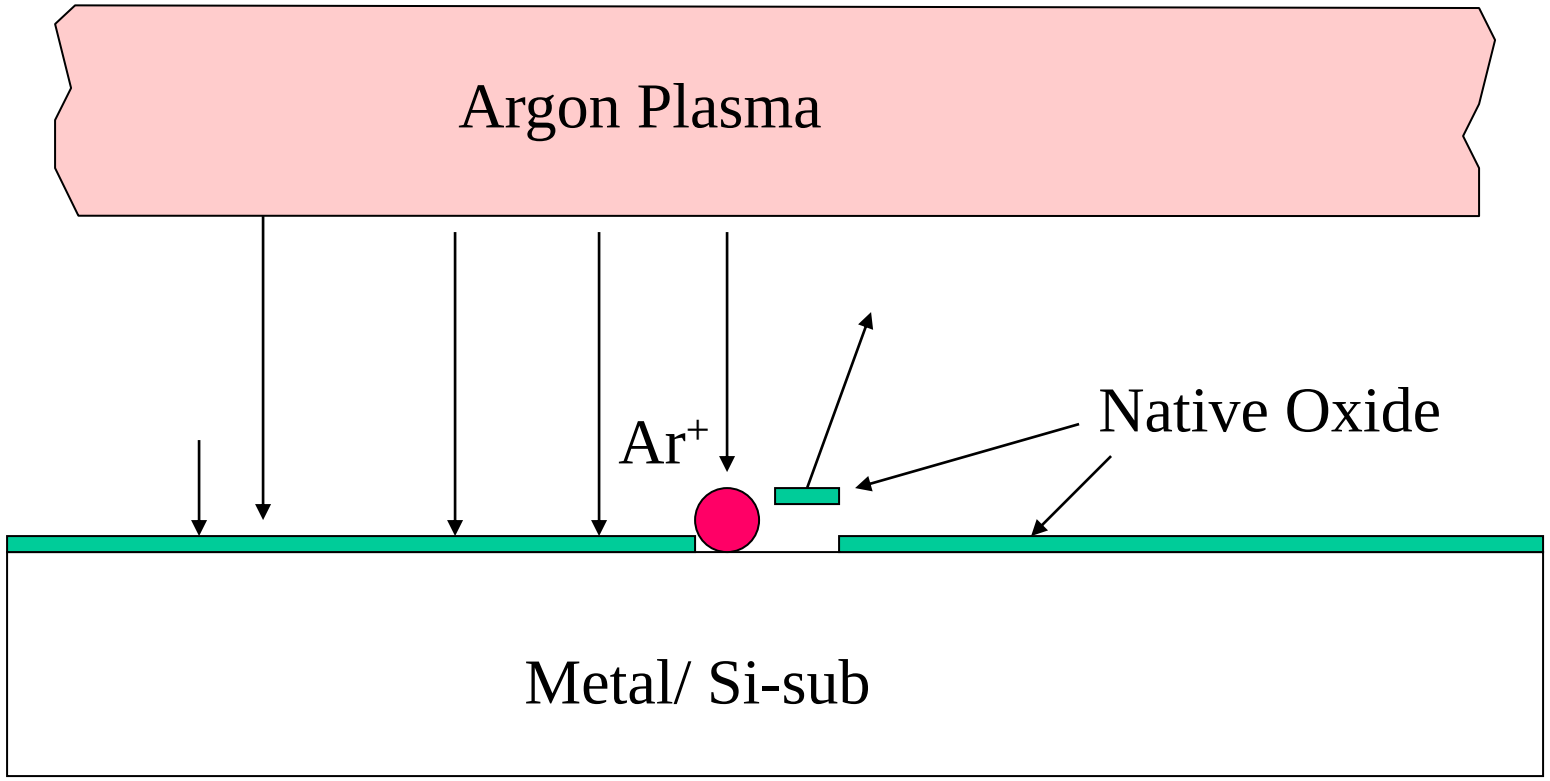


- A method of increasing the sputtering deposition rate is to confine the plasma to the region between the target and wafers
- A shield liner is used

DC Diode System

- It has a DC voltage applied between two electrode
- It cannot be used to sputter dielectrics because the target rapidly builds up a positive charge, which repels incoming positive ions
- It is also not capable of performing a sputter etch, it is a pre-clean step where the sputter process is reversed and argon atoms are used to remove thin native-oxide layers and remaining etch residues and contaminate contacts and vias

Pre-clean Process



Three Types of Sputtering Systems

- RF (radio frequency)
  - Use for dielectrics
- Magnetron
- IMP (ionized metal plasma)

RF Sputtering System

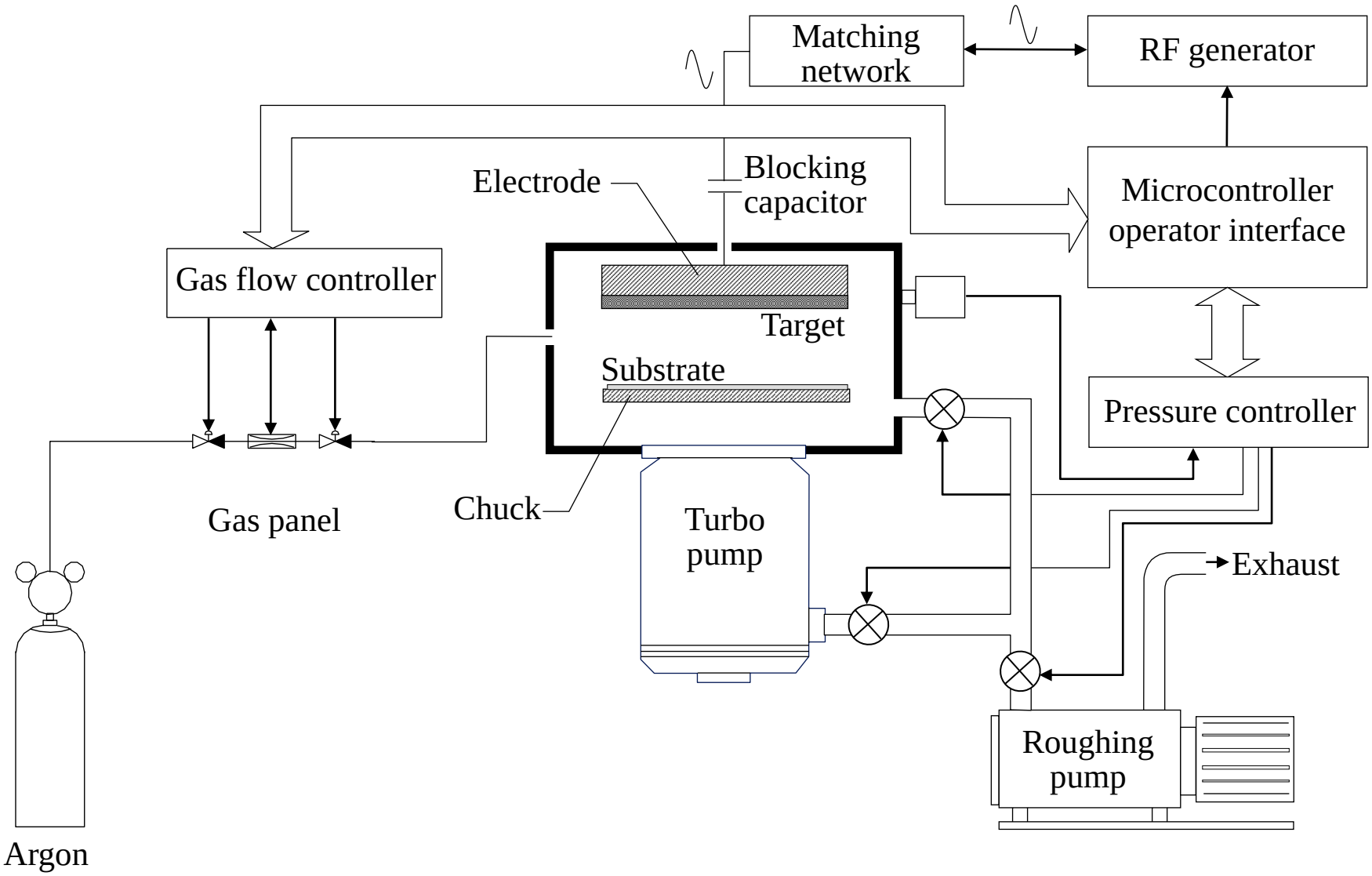


Figure 12.19

RF Sputtering

- 13.56 MHz is used
- Due to the high frequency, the electrons respond most strongly
- The chamber and electrode behave like a diode, creating a high amount of electron flow and resulting in a negative charge on the target electrode
- Thus self-bias attracts positive argon ions, which sputter materials from the insulator or non-insulator target

Magnetron Sputtering

- An RF sputtering system is limited because it doesn't have a high sputtering yield, low secondary electrons, leading to a low deposition rate.
- Magnet increase the ionization rate in the plasma, needs cooling

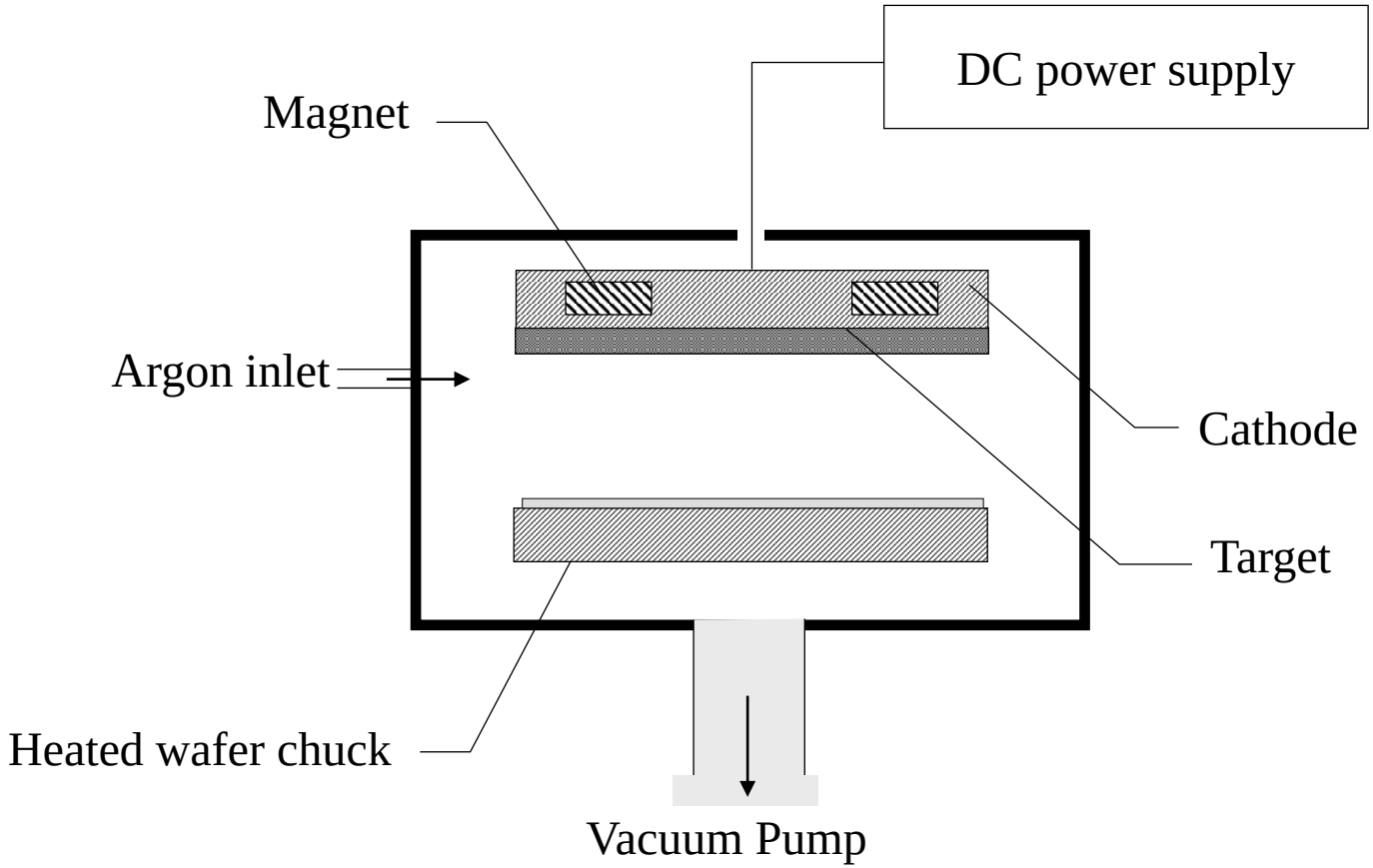


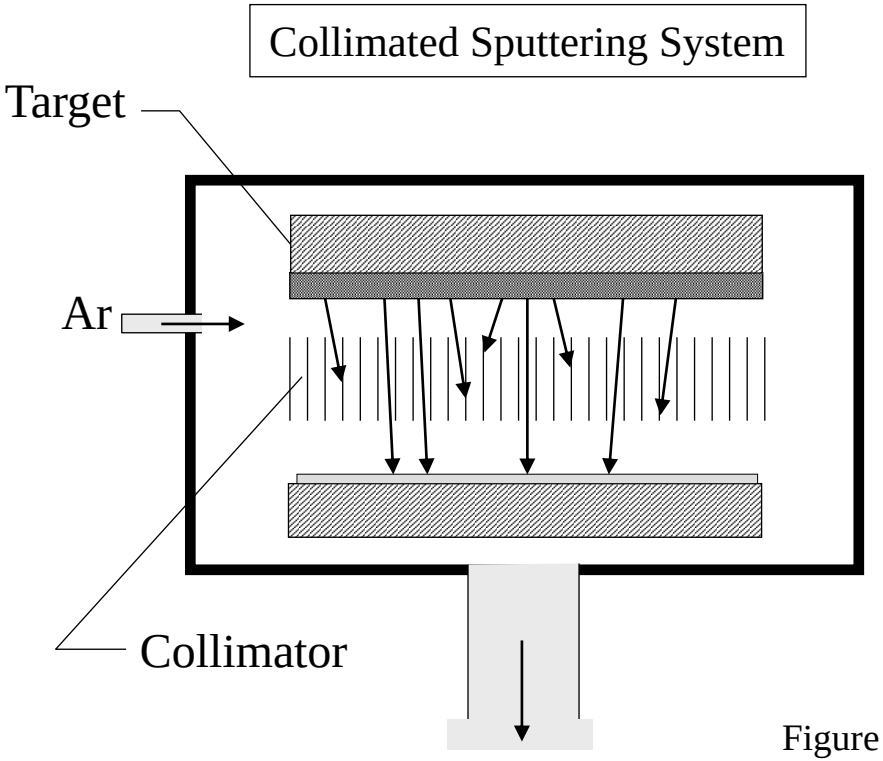
Figure 12.20

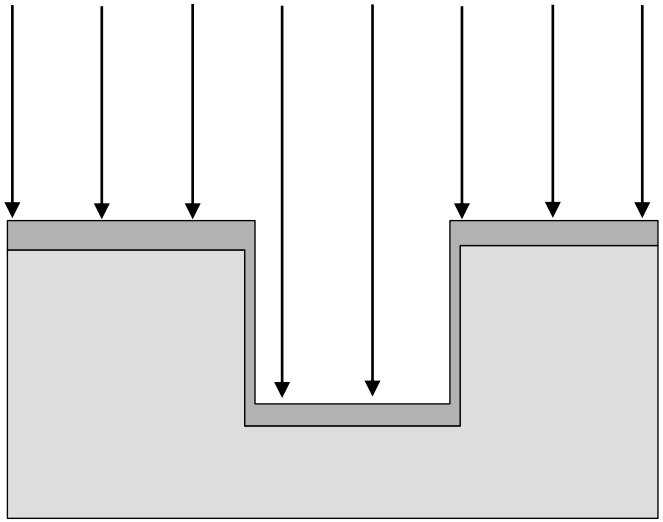
Step Coverage

- The vacuum during the sputtering process is around 1 m-torr, with a mean free path of several centimeters
- This is the distance between the target and wafer, following a line-of-sight path
- Many different angles from the target causes poor coverage on steps and sidewall in contacts and vias

Collimated Sputtering

- The collimator is configured so that it appears as the electrical ground for the plasma
- Any neutral species sputtered from the target at a high angle is intercepted and deposited on the collimator
- Other atoms pass the collimator and deposit on the bottom of the contact hole, lowers the sputter yield, maintenance costs increase





Cross section of via showing coverage of resulting sputtered film.

Figure 12.21

Concept of Ionized Metal Plasma PVD

- The positive metal ions travel in a highly directional, vertical path toward a wafer configured with a negative voltage bias
- Ionized PVD achieves good hole-fill for Ti and TiN with 0.25 μm contact and 6:1 aspect ratio with 70% bottom coverage and 10% sidewall coverage

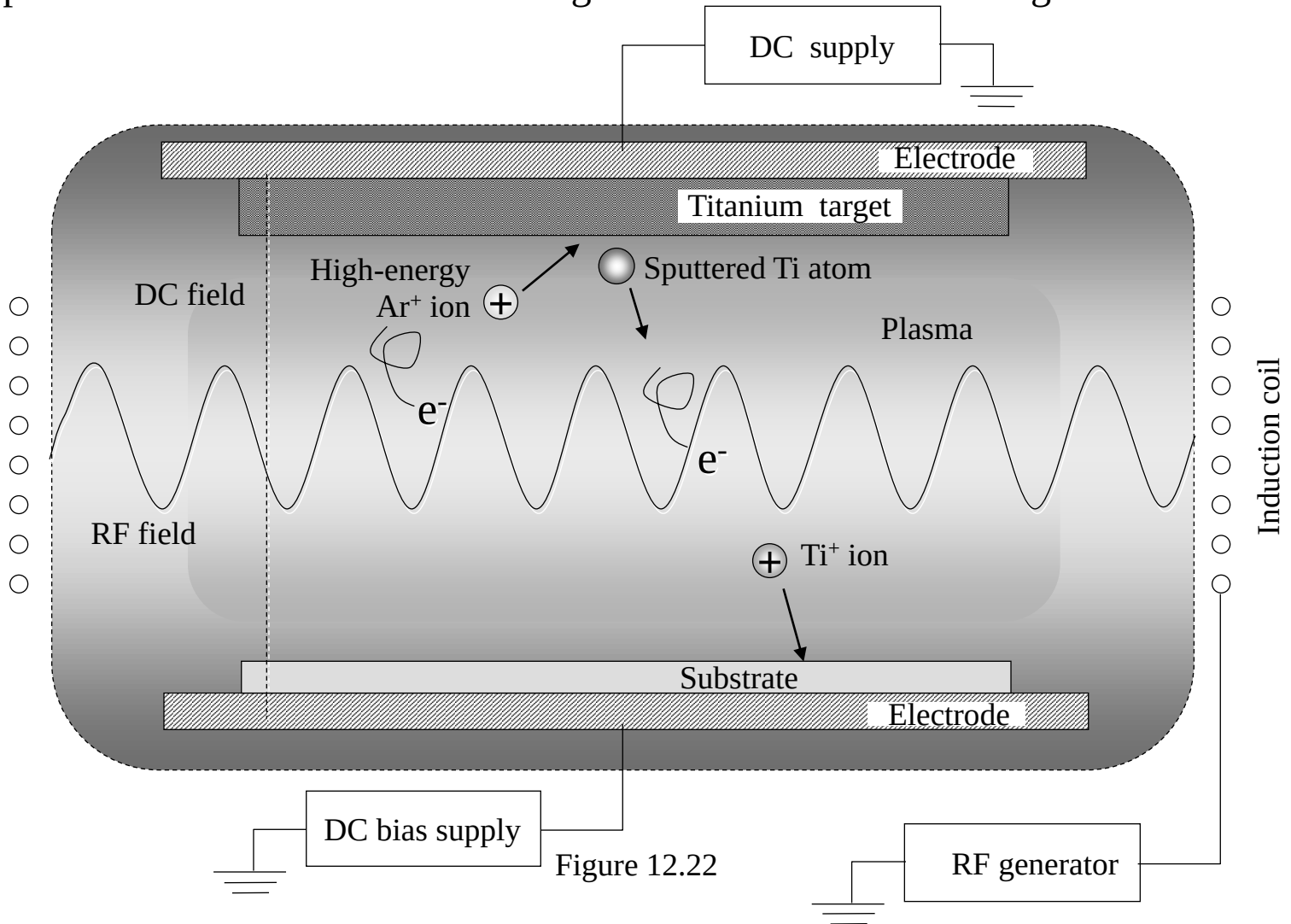
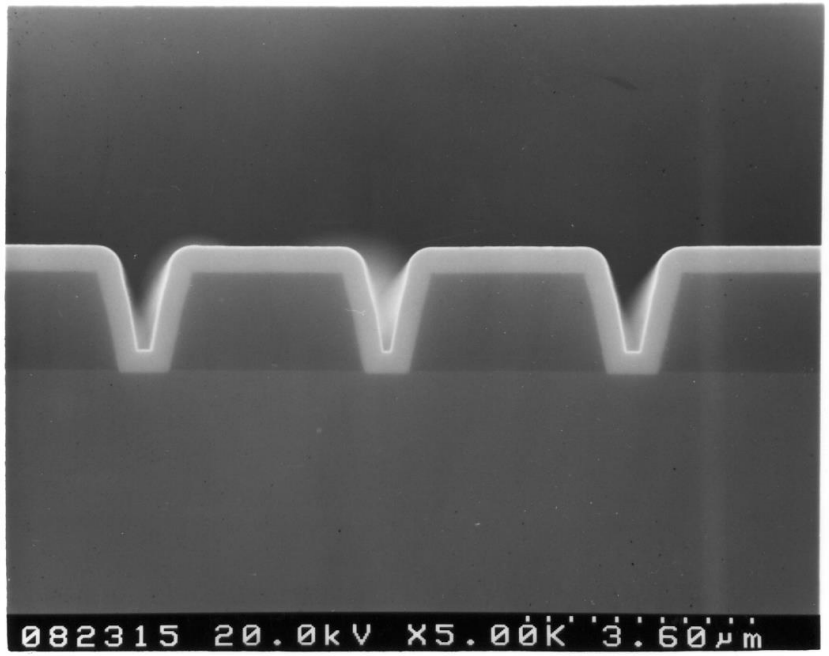


Figure 12.22

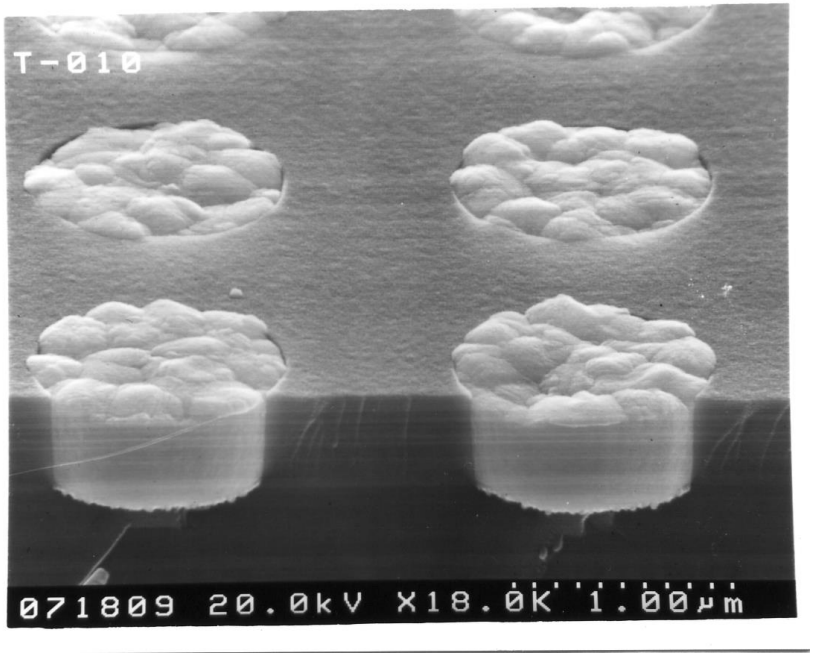
Metal CVD

- Tungsten CVD
  - Excellent step coverage and gap fill
  - High electromigration resistance
- Copper CVD
  - Excellent conformality

TaN CVD



Selective T-plug

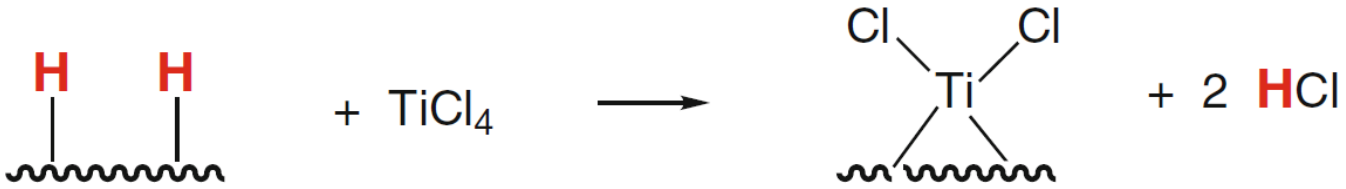


- @ 450˚C

	氮化鉭(TaN)阻障層(Barrier)	氮化鈦(TiN) 阻障層
電阻係數	200 ~ 350 mΩ-cm	22 mΩ-cm

Atomic Layer CVD

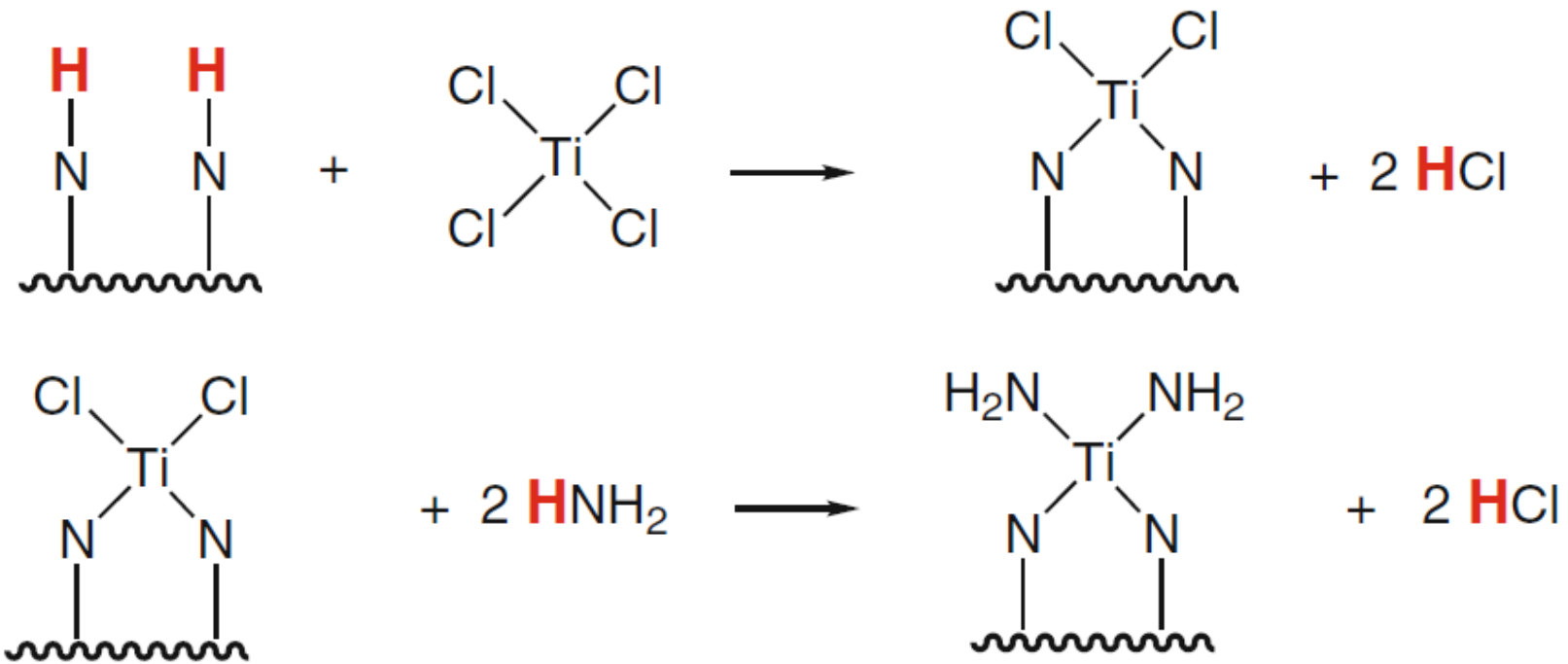
Remote hydrogen plasma has been used to deposit very reactive metals, such as titanium and tantalum from their chlorides. Assuming that the plasma has already provided hydrogen atoms to the surface, the next reaction step would be the following:



The surface is now returned to the state in which it is ready for the first reaction to begin the ALD cycle again.

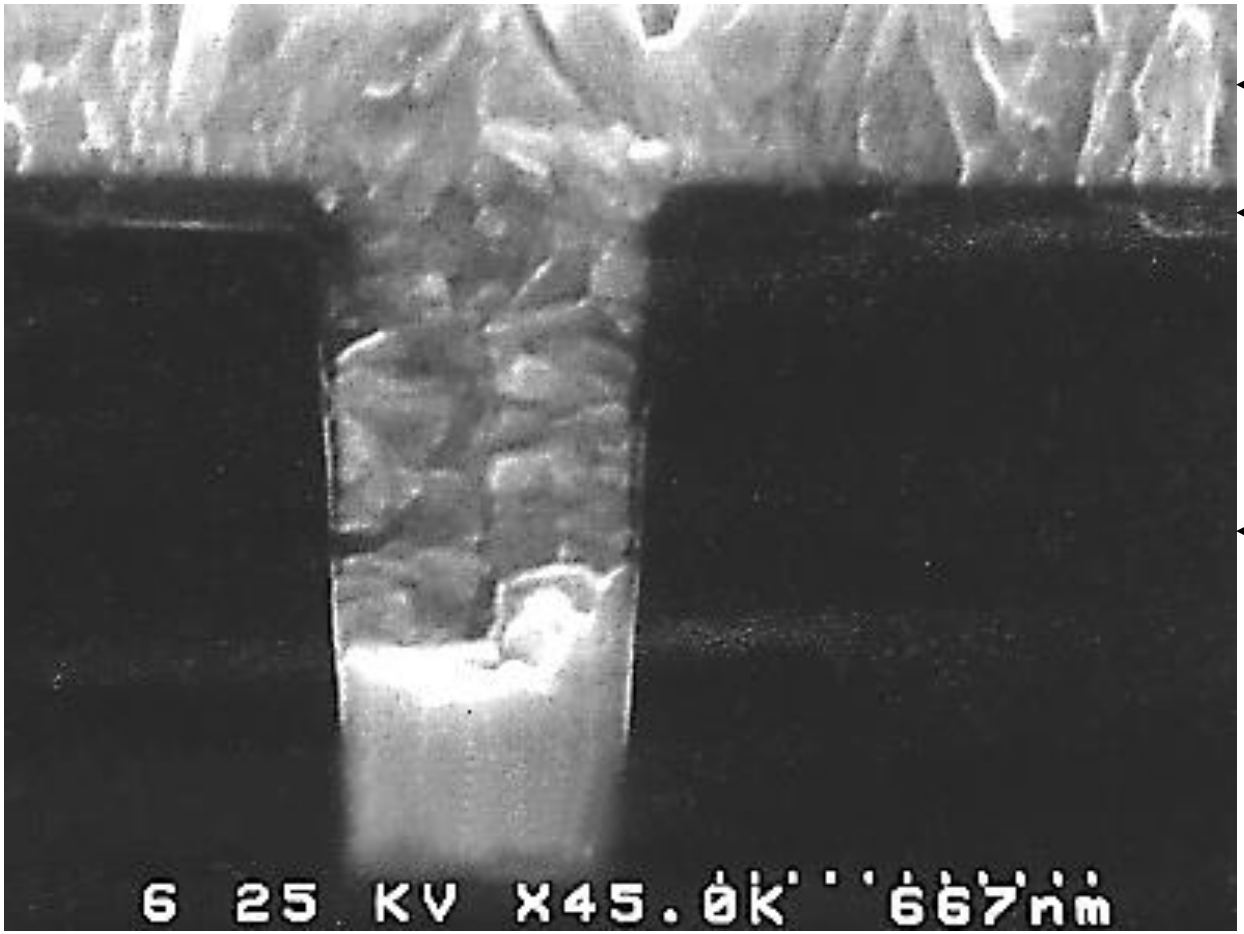
Atomic Layer CVD

$$TiCl_4 + NH_3 => TiN + \text{gaseous products}$$

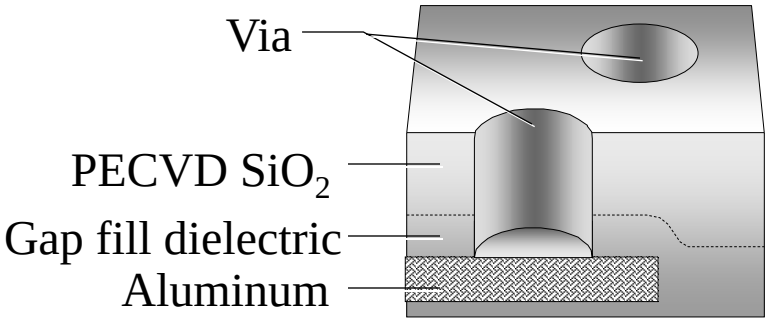


After this step, the titanium remains in the +4 oxidation state, corresponding to a product Ti_3N_4.

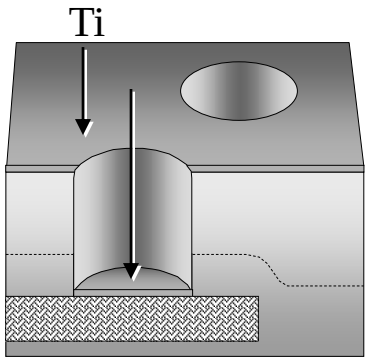
W Plug and TiN/Ti Barrier/Adhesion Layer



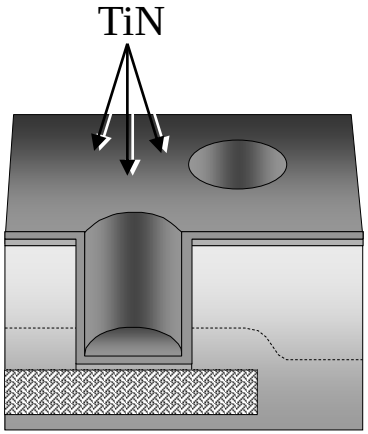
Blanket Tungsten CVD with Ti/TiN Barrier Metal



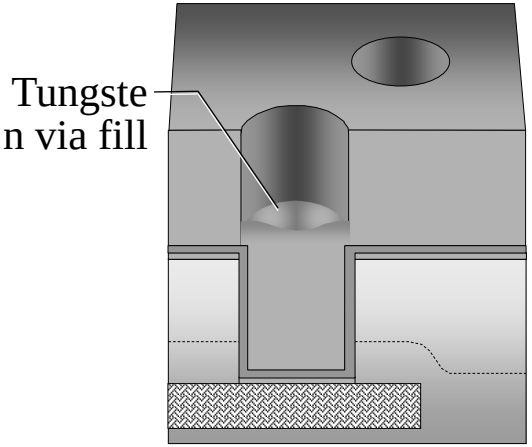
1. Interlayer dielectric via etch



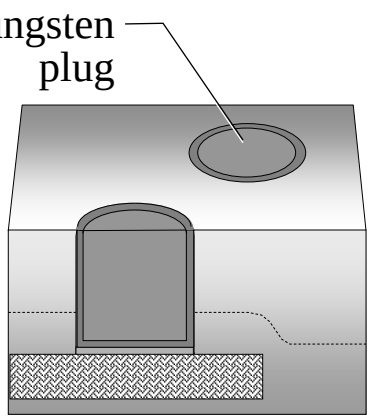
2. Collimated Ti deposition covers bottom of via



3. CVD TiN conformal deposition



4. CVD tungsten deposition



5. Tungsten planarization

$WF_6 + 3H_2 \rightarrow W + 6HF$

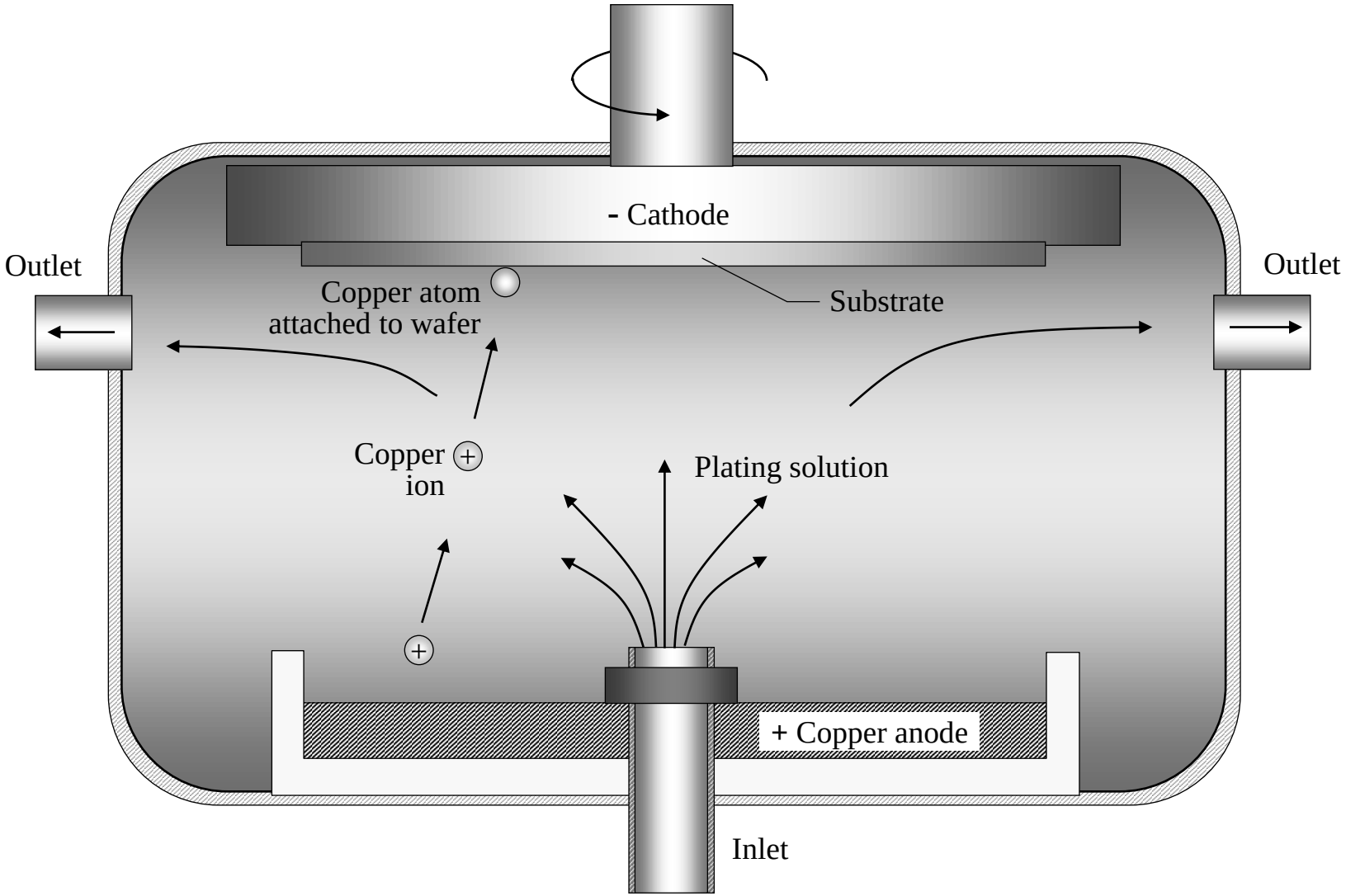
Figure 12.23

PVD Cluster Tool

Photo Courtesy of Applied Materials, Inc.

Photo 12.3

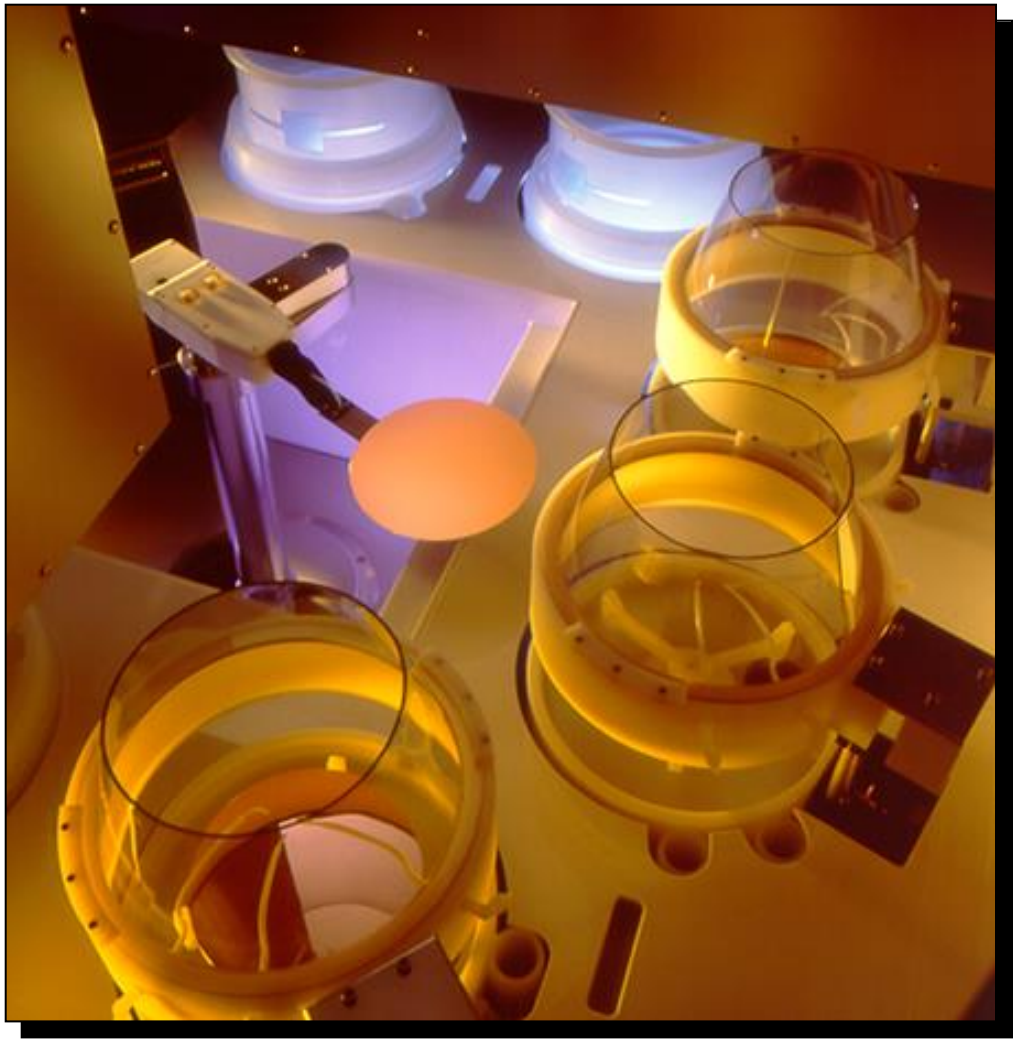
Copper Electroplating



Copper Electroplating

- The basic principle of electroplating copper metal is to immerse a wafer with a conductive surface into a solution of copper sulfate ($Cu(SO_4)$) which contains copper ions to be deposited
- $Cu^{2+} + 2e^- \rightarrow Cu^0$
- Plating rate is a direct function of current density, if there is a high current density at the top of hole and a lower current density at the bottom of the hole, then copper will plate faster at the top
- Applying an oscillating electric field and controlling the amplitude of the waveform, a deposition/etch sequence is obtained
- So, the copper can be slightly removed (etched) in the high-density current regions to balance the copper gap-fill capability

Electroplating Tool

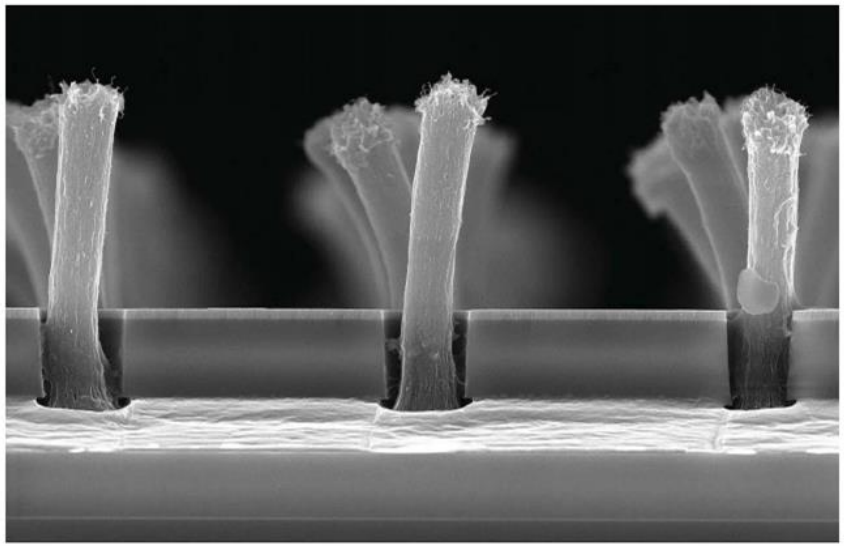


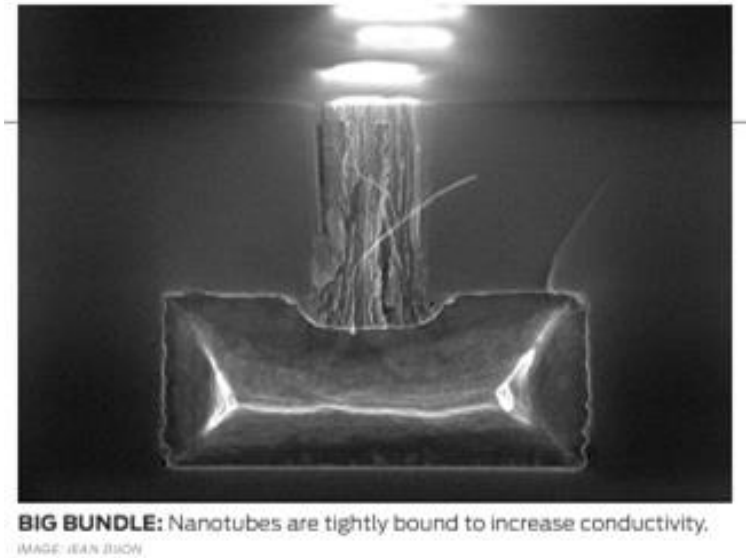
Used with permission from Novellus Systems, Inc.

Photo 12.4

Can carbon put copper down for the counter (ieee, spectrum 2010/12)

- CNT bundle vias can greatly reduce interconnect temperature rise, offering at least 30% performance improvement and 2 order of magnitude in lifetime improvement over Cu interconnect



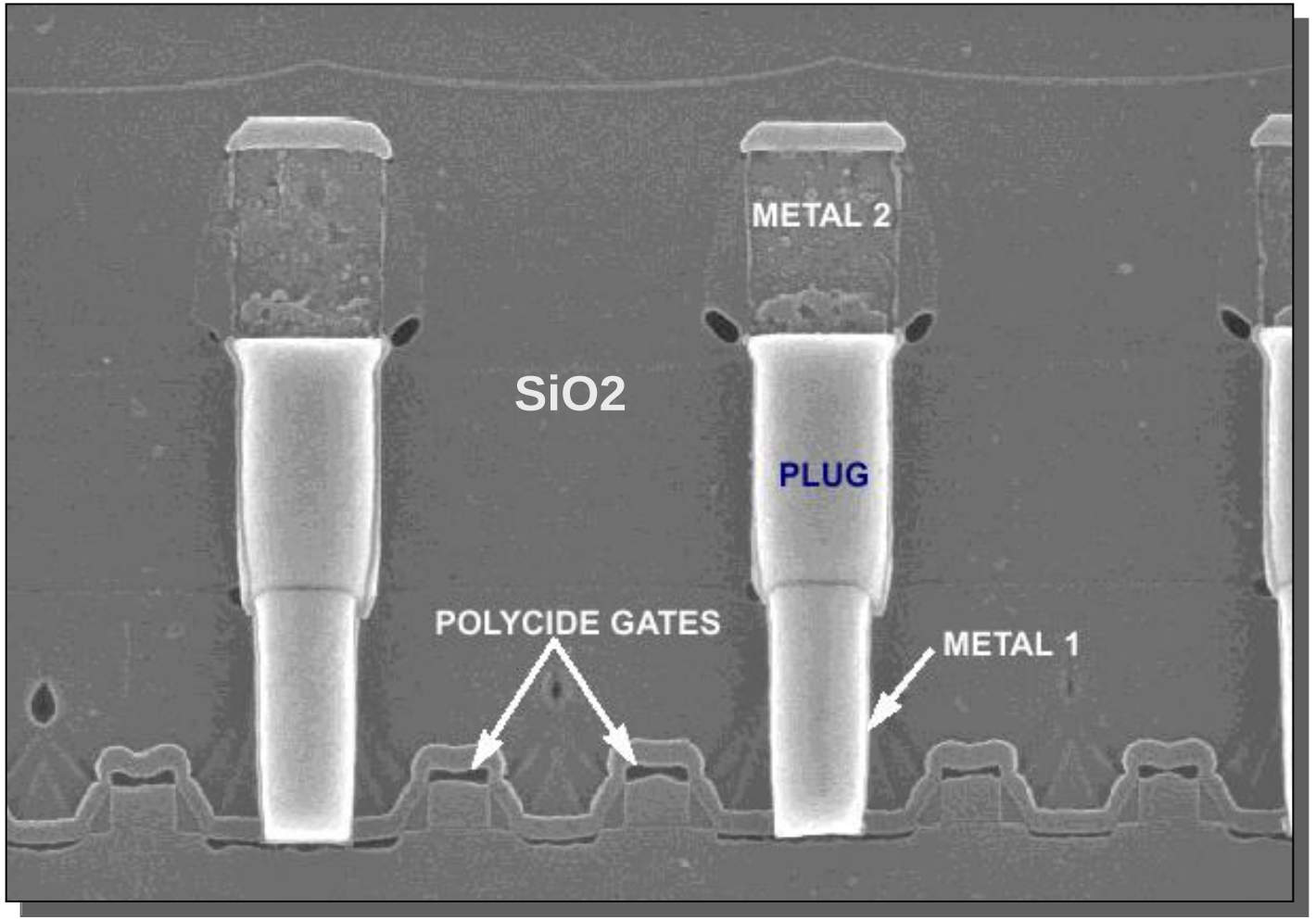


BIG BUNDLE: Nanotubes are tightly bound to increase conductivity.

IMAGE: JEAN BIJON

J: A billion ampere /cm^2 , 100 times than copper.

Traditional Aluminum Structure

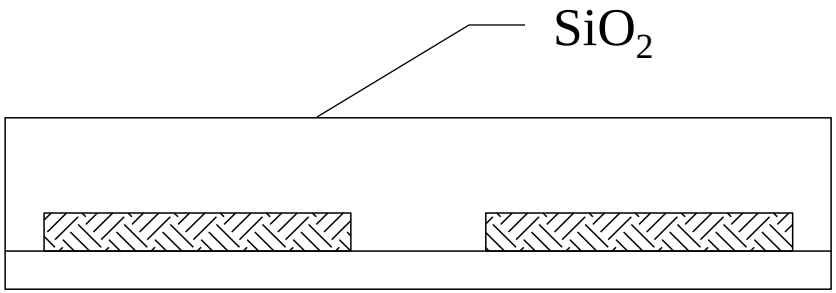


Photograph courtesy of Integrated Circuit Engineering

Photo 12.4

Table 12.5.1 [55]
Copper Metallization using Dual Damascene

Process Step: SiO_2 deposition



Description: ILD oxide deposition with PECVD to desired thickness for via There is no critical gap fill therefore PECVD is acceptable.

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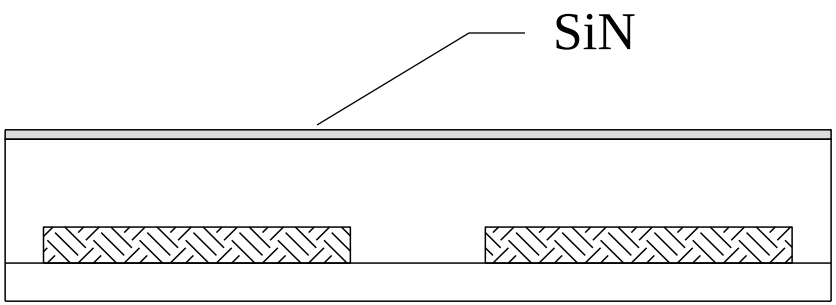
Table 12.5.2
Copper Metallization using Dual Damascene

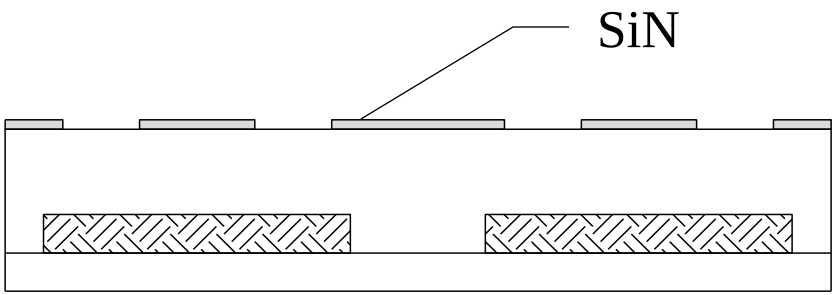
Process Step: SiN etch stop deposition



Description: Thin (250 Å) SiN etch stop is deposited on ILD oxide. The SiN needs to be dense and pinhole-free; therefore HDPCVD is used.

Table 12.5.3
Copper Metallization using Dual Damascene

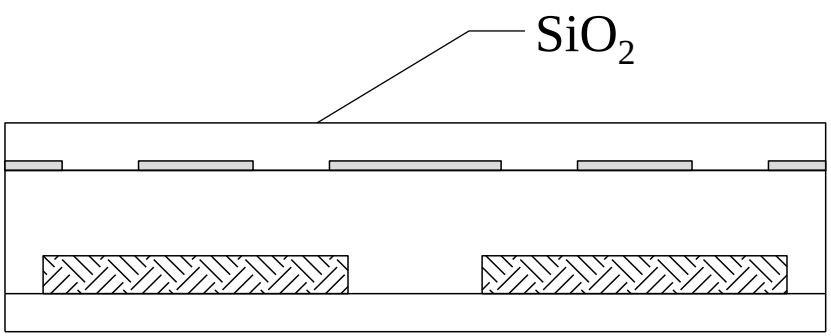
Process Step: Via patterning and etch



Description: Photolithography to pattern and dry etch via openings into SiN. Strip photoresist after completion of etch.

Table 12.5.4
Copper Metallization using Dual Damascene

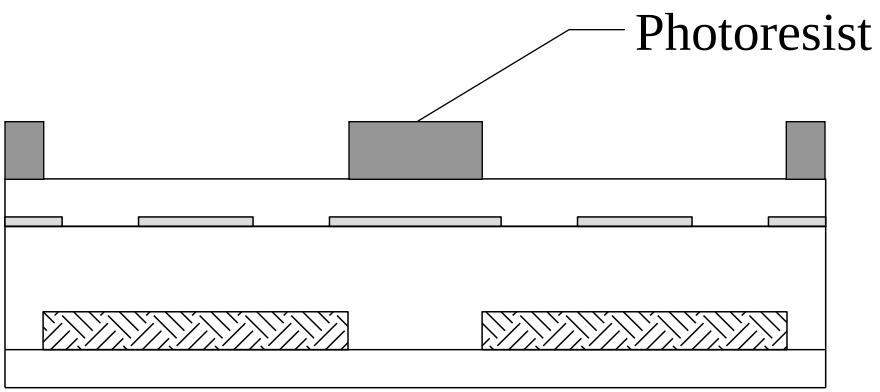
Process Step: Deposit remaining SiO_2



Description: PECVD oxide deposition for remaining ILD oxide.

Table 12.5.5
Copper Metallization using Dual Damascene

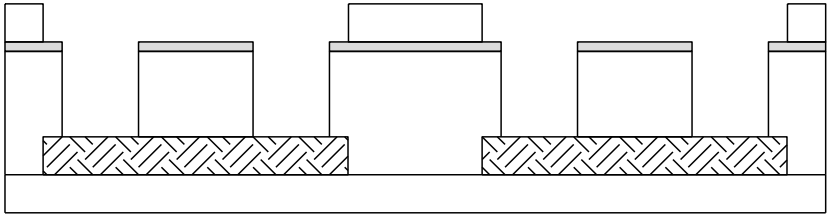
Process Step: Interconnect patterning



Description: Photolithography to pattern SiO_2 trench with resist. Previously patterned via openings are located in trench.

Table 12.5.6
Copper Metallization using Dual Damascene

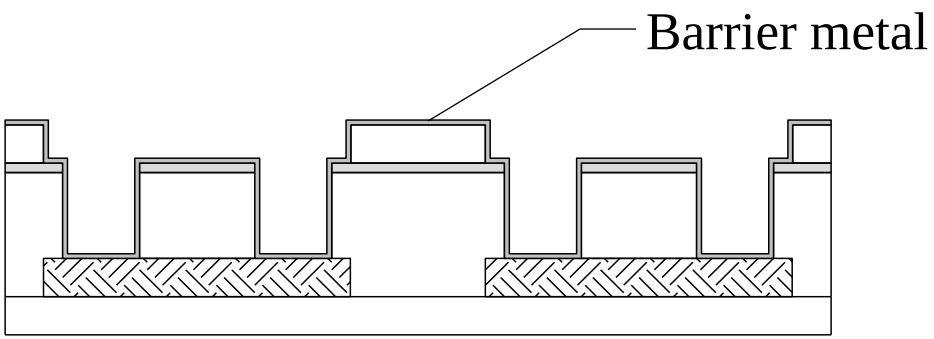
Process Step: Etch trench for interconnect and hole for via



Description: Dry etch trench in ILD oxide, stopping on the SiN layer. Etch continues to form via opening by passing through opening in SiN.

Table 12.5.7
Copper Metallization using Dual Damascene

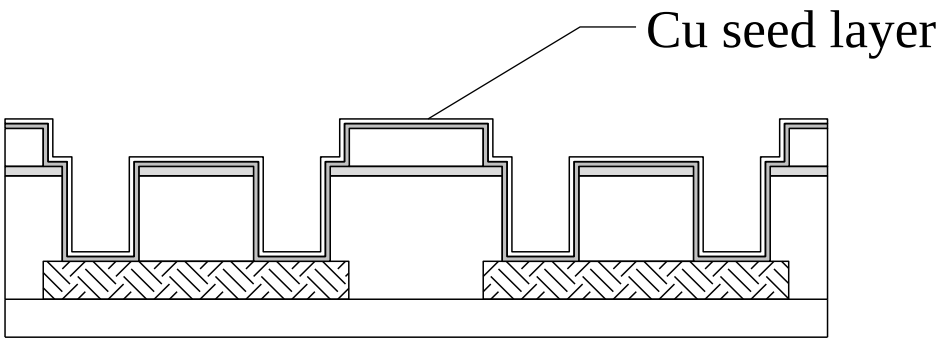
Process Step: Deposit Barrier Metal



Description: Deposit Ta or TaN diffusion layer with ionized PVD on bottom and sidewalls of trench and via.

Table 12.5.8
Copper Metallization using Dual Damascene

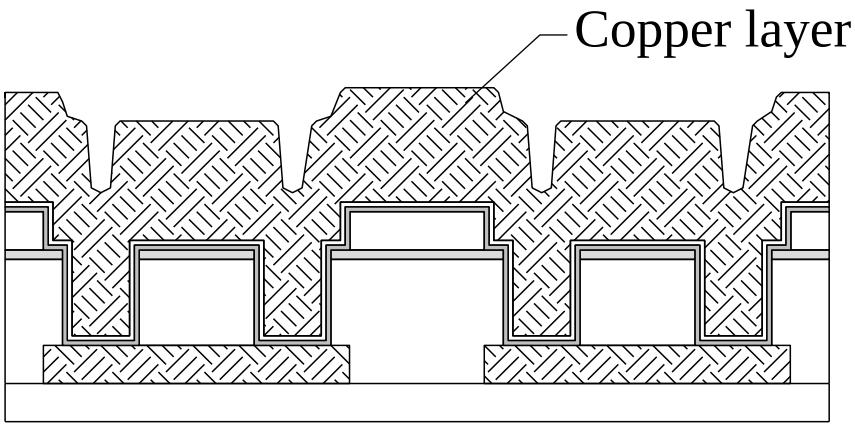
Process Step: Deposit Cu seed layer



Description: Deposit continuous Cu seed layer with CVD. The layer must be uniform and free of pinholes

Table 12.5.9
Copper Metallization using Dual Damascene

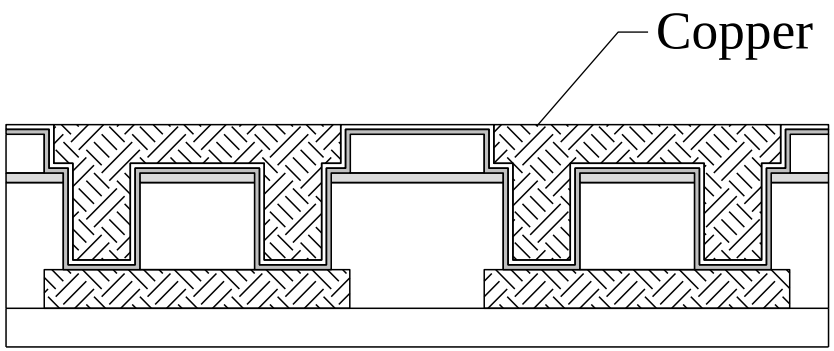
Process Step: Deposit Cu fill



Description: Deposit Cu fill with electrochemical deposition (ECD). Fill both via opening and trench.

Copper Metallization using Dual Damascene

Process Step: Remove excess Cu with

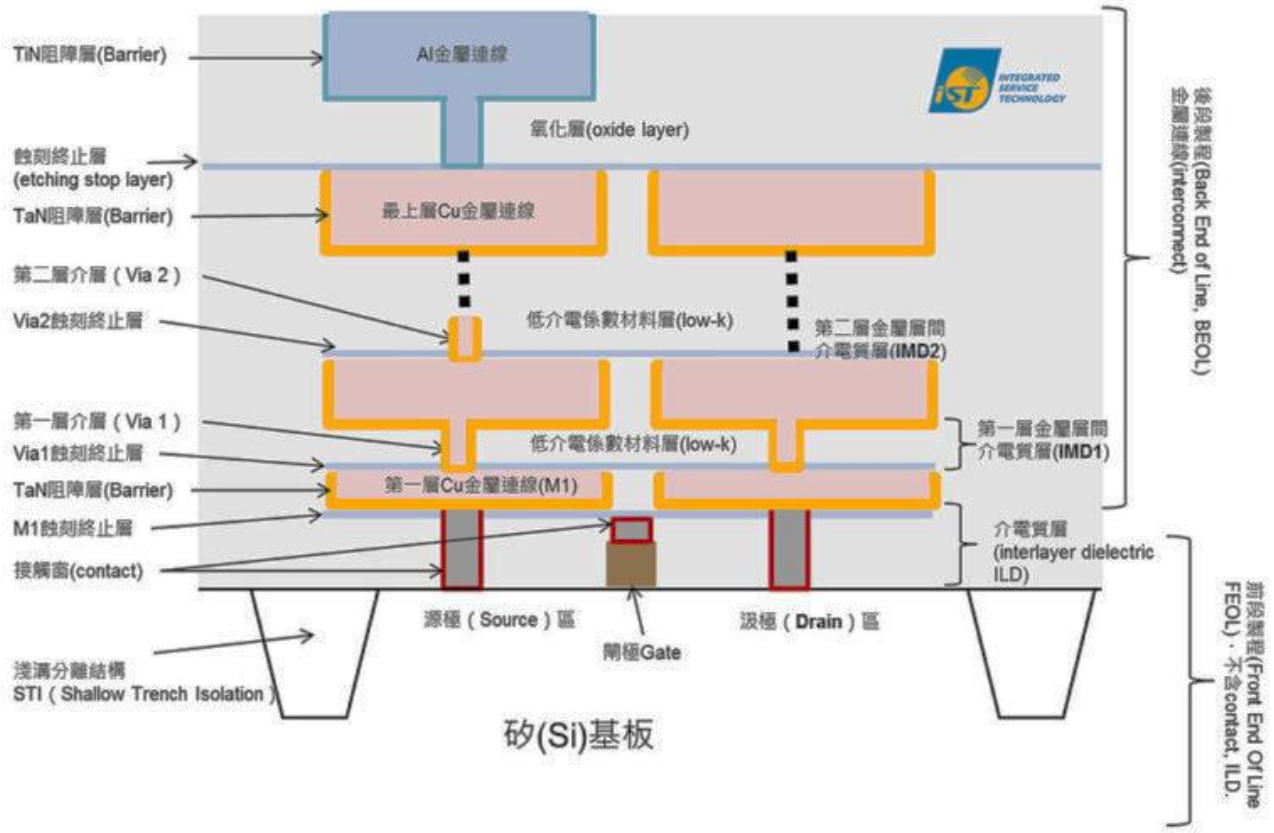


Description: CMP remove excess Cu using chemical mechanical planarization (CMP).This planarizes the surface and prepares for next level. The resulting surface is a planar structure with metal inlays in the dielectric to form the circuitry.

Dual Damascene Structure

- The dual-damascene process became the consensus process for copper metallurgy
- It creates both the vias and lines for each metal layer by etching holes and trenches in the ILD, depositing copper in the etched features and using chemical mechanical planarization to remove the excess copper
- The most important reason for using a damascene approach to copper metallization is to avoid metal etch
- The second advantage is there is no further need for dielectric gap fill between etched metal lines, since the dielectric is applied as a blanket and then etched

@ 7nm node, Can Co replaces Cu ? *



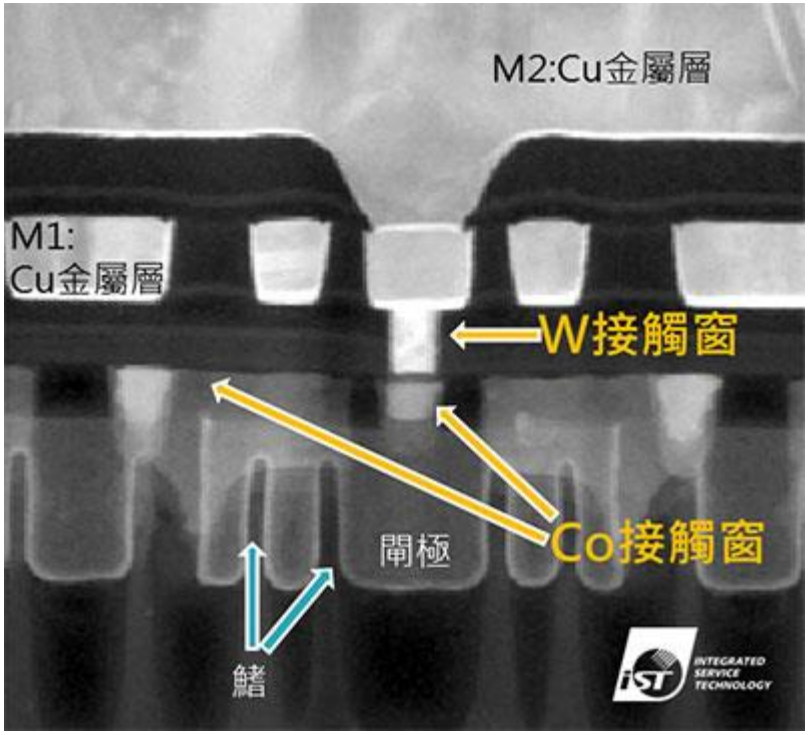
- Cu has low resistivity than Al, but high diffusibity
- Need diffusion barrier layer TaN, instead of TiN (column)

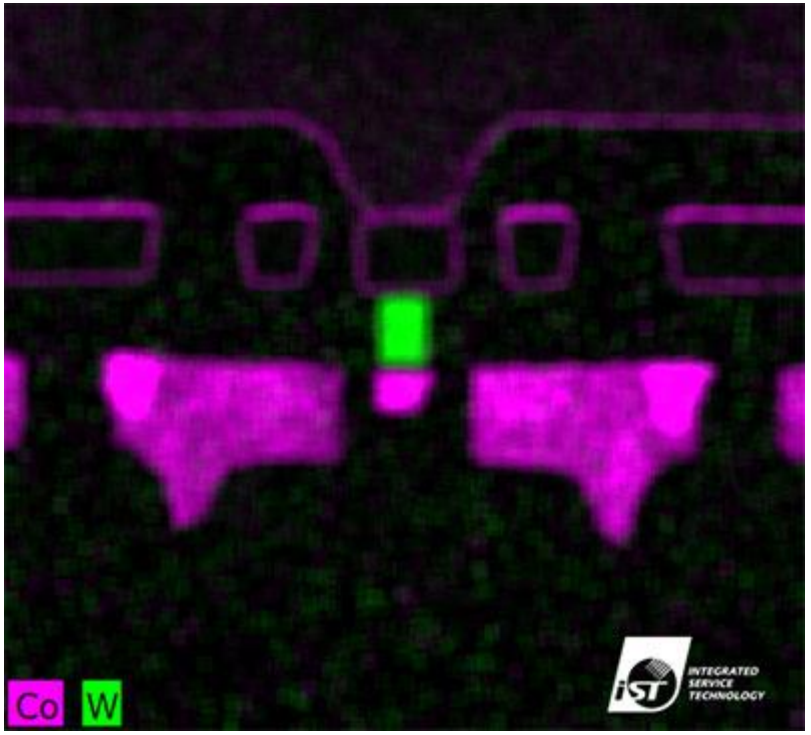
* https://technews.tw/2019/10/15/istgroup-7nm-wafer-analysis/

金屬線上的電阻= 銅線電阻+氮化鉭層電阻			
既有製程	銅線尺寸	氮化鉭層尺寸	氮化鉭層電阻貢獻度
	200nm	5nm	1 (定義為參考值)
7奈米先進製程	銅線尺寸	氮化鉭層尺寸	
	20nm	5nm	> 40

- But TaN is not easy to scaled
- Add Co into TaN is the best candidate
- Co can reduce barrier resistivity, and also the thickness of barrier metal

Kirin 980 CPU





1. But pure Co reacts with Cu, resulting in electro-migration
2. It cannot replace W/TiN at contact hole
3. We need double contact hole [W and Co]