Semiconductor Manufacturing Technology

Michael Quirk & Julian Serda

Chapter 11

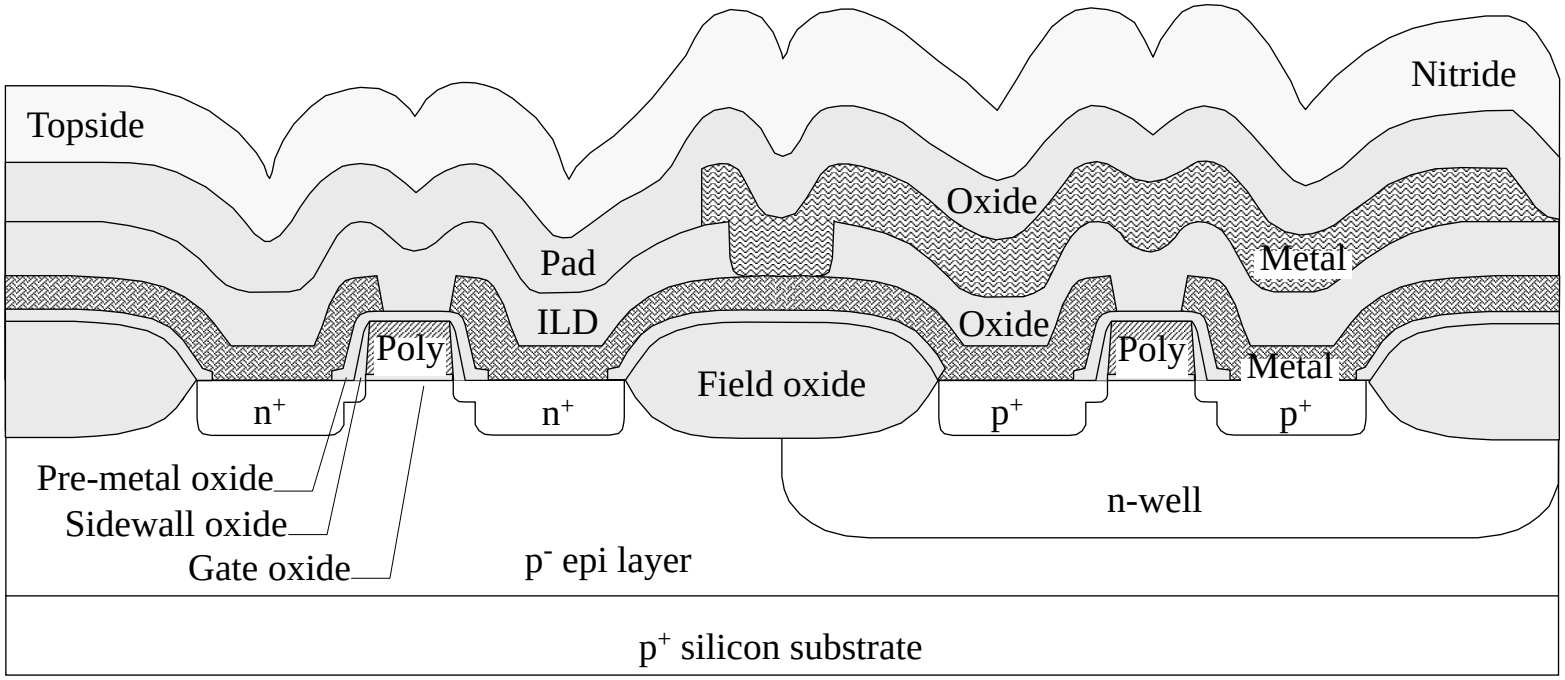
Deposition

Objectives

After studying the material in this chapter, you will be able to:

1. Describe multilayer metallization. Discuss the acceptable characteristics of a thin film. State and explain the three stages of film growth.
2. Provide an overview of the different film deposition techniques.
3. List and discuss the ***8*** basic steps to a chemical vapor deposition (CVD) reaction, including the different types of chemical reactions.
4. Describe how CVD reactions are limited, reaction dynamics and the effect of dopant addition to CVD films.
5. Describe the different types of CVD deposition systems, how the equipment functions and the benefits/limitations of a particular tool for film applications.
6. Explain the importance of dielectric materials for chip technology, with applications.
7. Discuss epitaxy and three different epi-layer deposition methods
8. Explain spin on dielectrics.

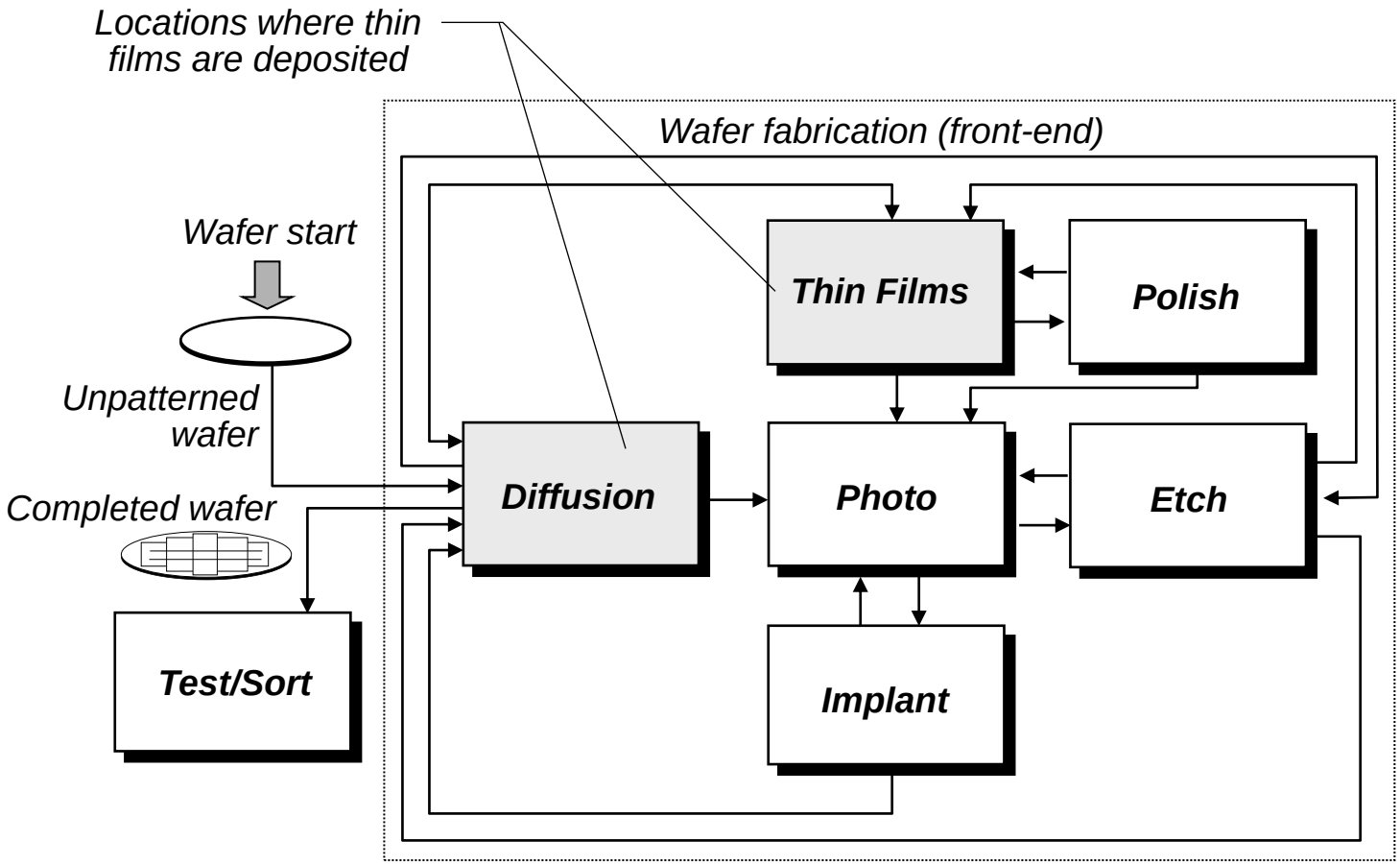
Film Layers for an MSI Era NMOS Transistor



IC is a thin film engineering

Figure 11.1

Process Flow in a Wafer Fab



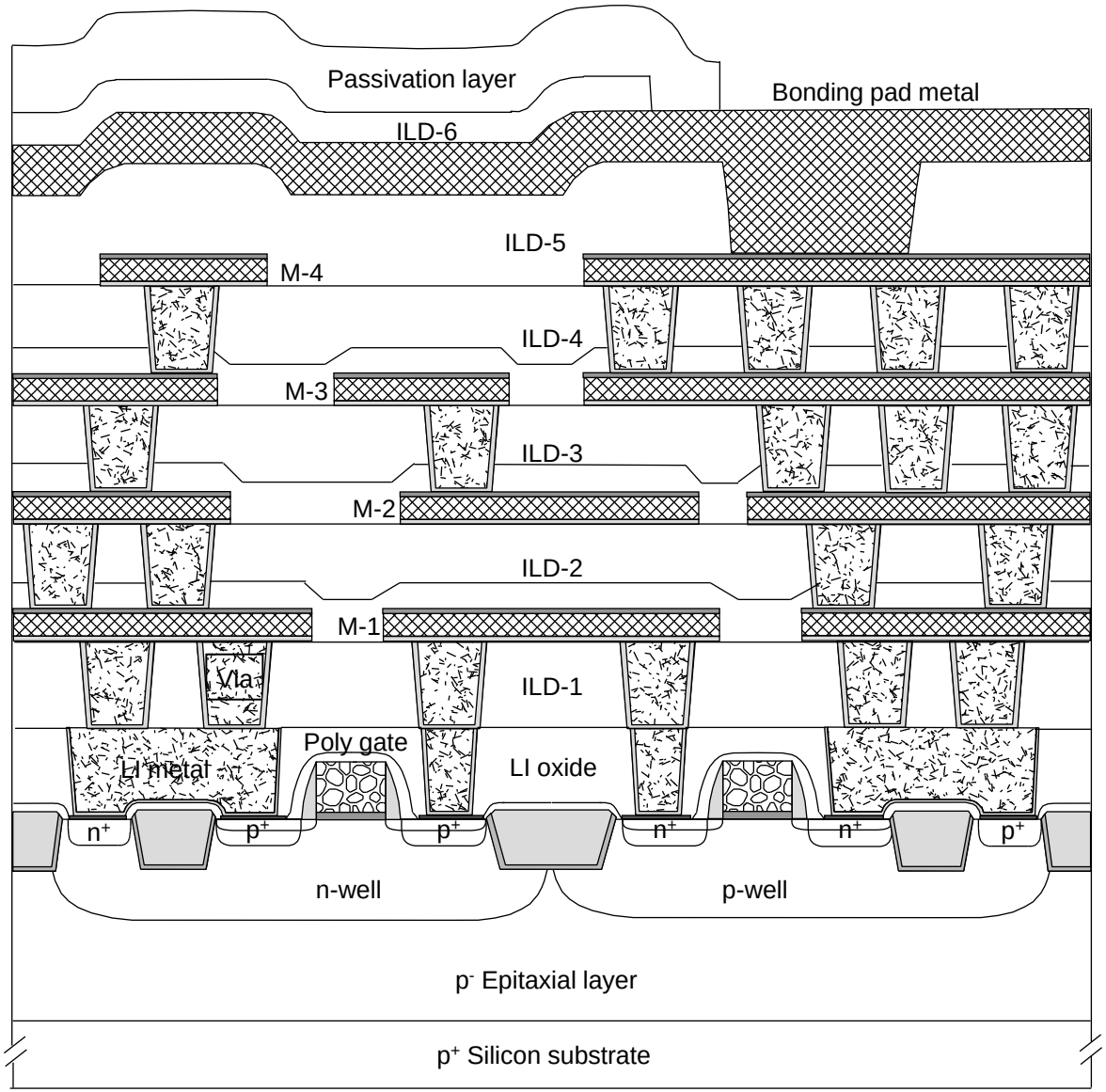
Used with permission of Advanced Micro Devices

Figure 11.2

Introduction

- Film Layering in Wafer Fab
  - Diffusion
  - Thin Films
- Film Layering Terminology
- Multilayer Metallization
  - Metal Layers
  - Dielectric Layers

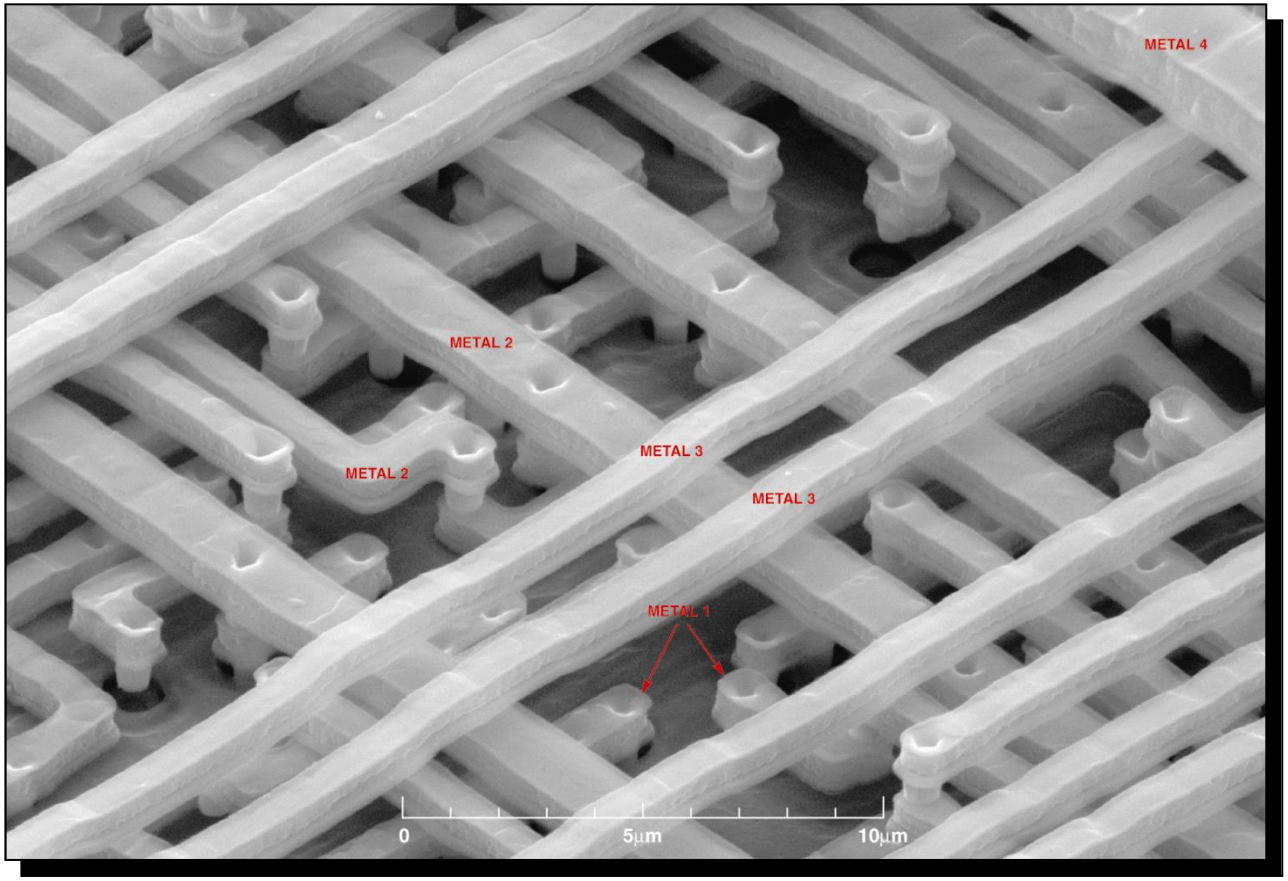
Multilevel Metallization on a ULSI Wafer



- Designer should **tradeoff** cost, complexity, and performance
- One metal layer needs **2** mask, adds 15% cost
- ILD: interlayer dielectric (oxide)
- ILD: electrically isolate from the metal interconnect layers, and physically isolate from mobile ions by doped-P (p-glass)
- **Low-k** materials is used today to reduce delay

Figure 11.3

Metal Layers in a Chip



- **Al is used, which is deposited on whole wafer and etched**
- **Transition to Cu for low R and high speed**
- **CD layers: poly-Si, contact hole and metal 1 (very sensitive to contamination)**

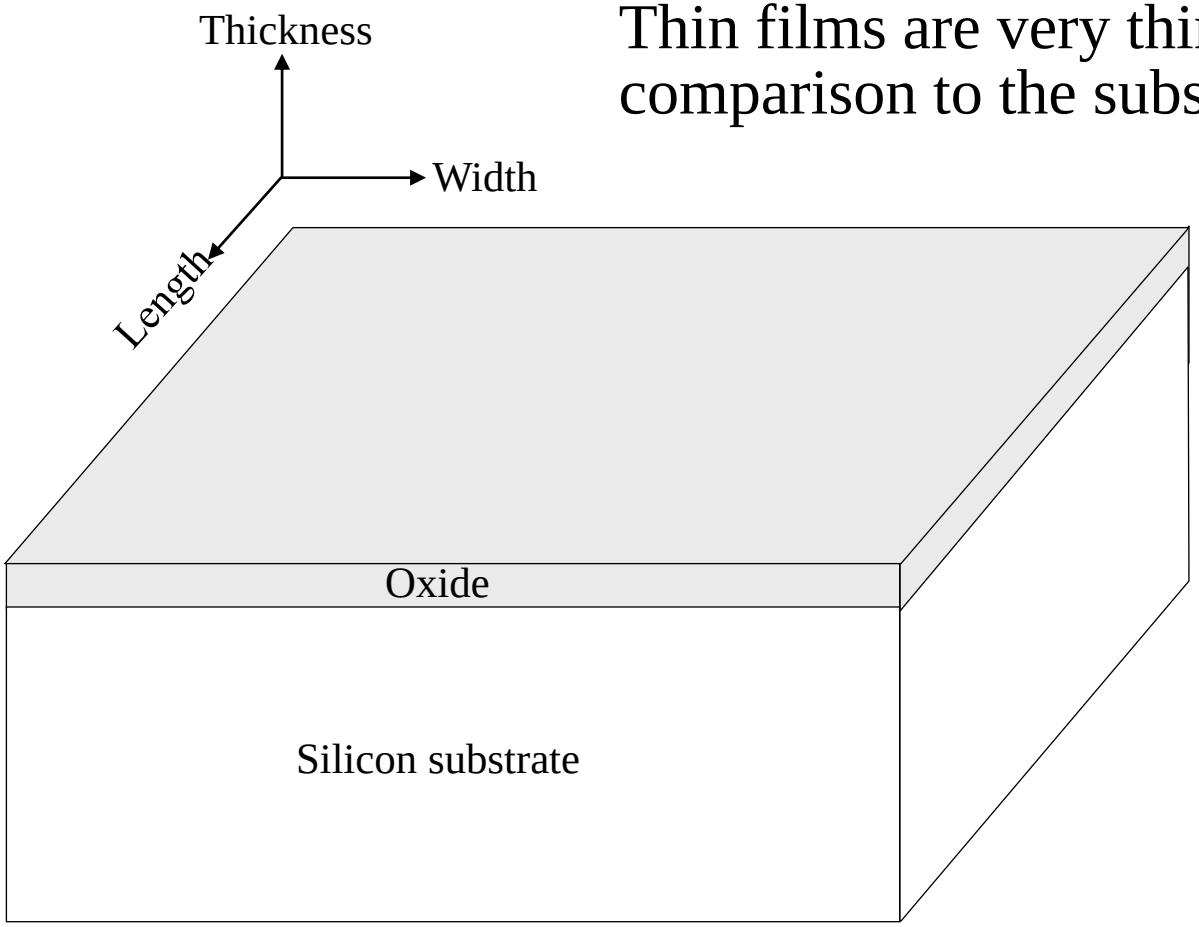
Photo 11.1

Film Deposition

Thin Film Characteristics

- Good **step coverage**
- Ability to **fill** high aspect ratio **gaps** (conformality)
- Good thickness **uniformity (no pinholes)**
- High purity and density (Mobile ion or particle)
- Controlled **stoichiometry ($Si_xN_yH_z$)**
- High degree of structural **perfection** with low film **stress**
- Good **electrical properties**
- Excellent **adhesion** to the substrate material and subsequent films

Solid Thin Film



Thin films are very thin in comparison to the substrate.

Figure 11.4

Film Coverage over Steps

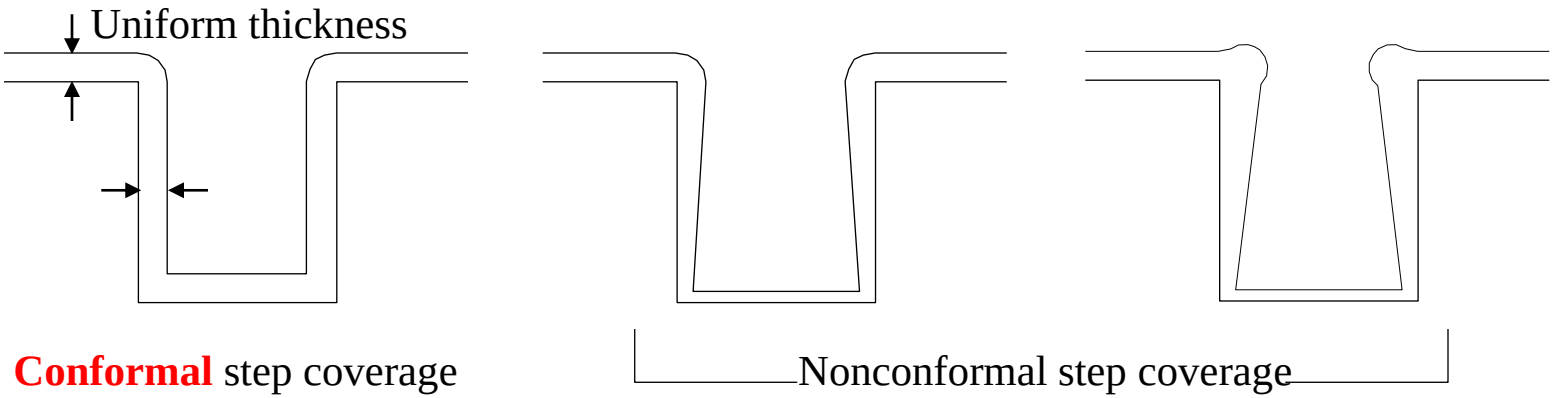
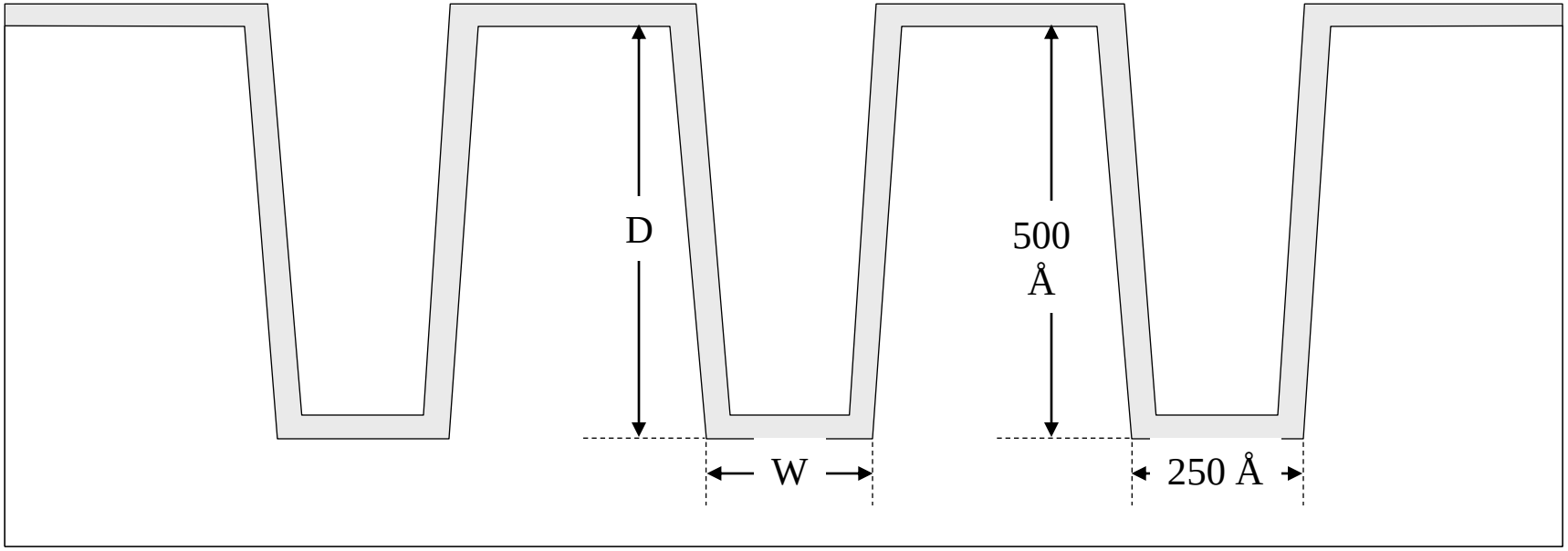


Figure 11.5

Aspect Ratio for Film Deposition

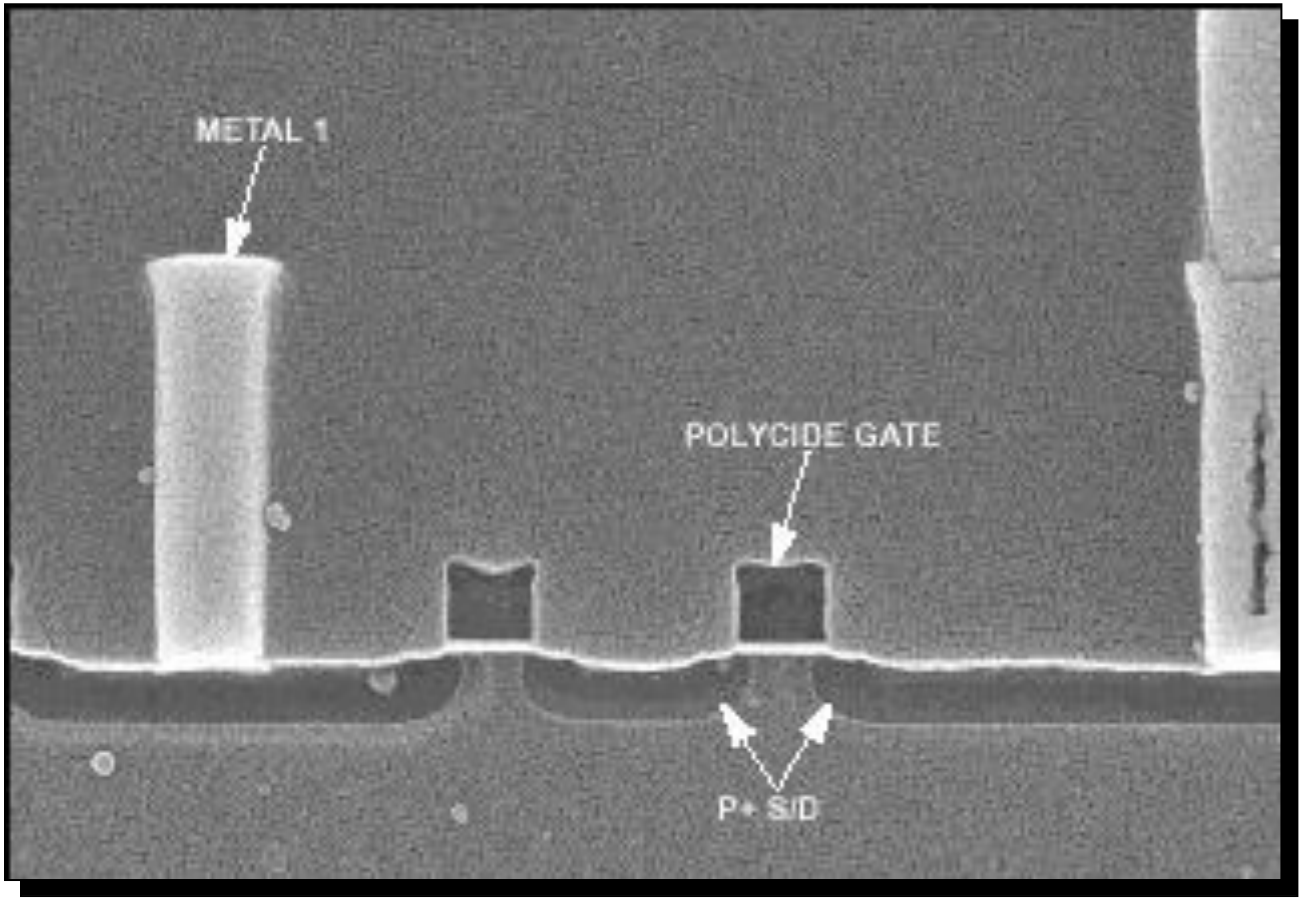
$$\text{Aspect Ratio} = \frac{\text{Depth}}{\text{Width}} \qquad \text{Aspect Ratio} = \frac{500\ \text{Å}}{250\ \text{Å}} = \frac{2}{1}$$



- **CD decreases, aspect ratio increases due to non-scaled film thickness**
- **The ability of filling high aspect ratio gap/via become the most important**

Figure 11.6

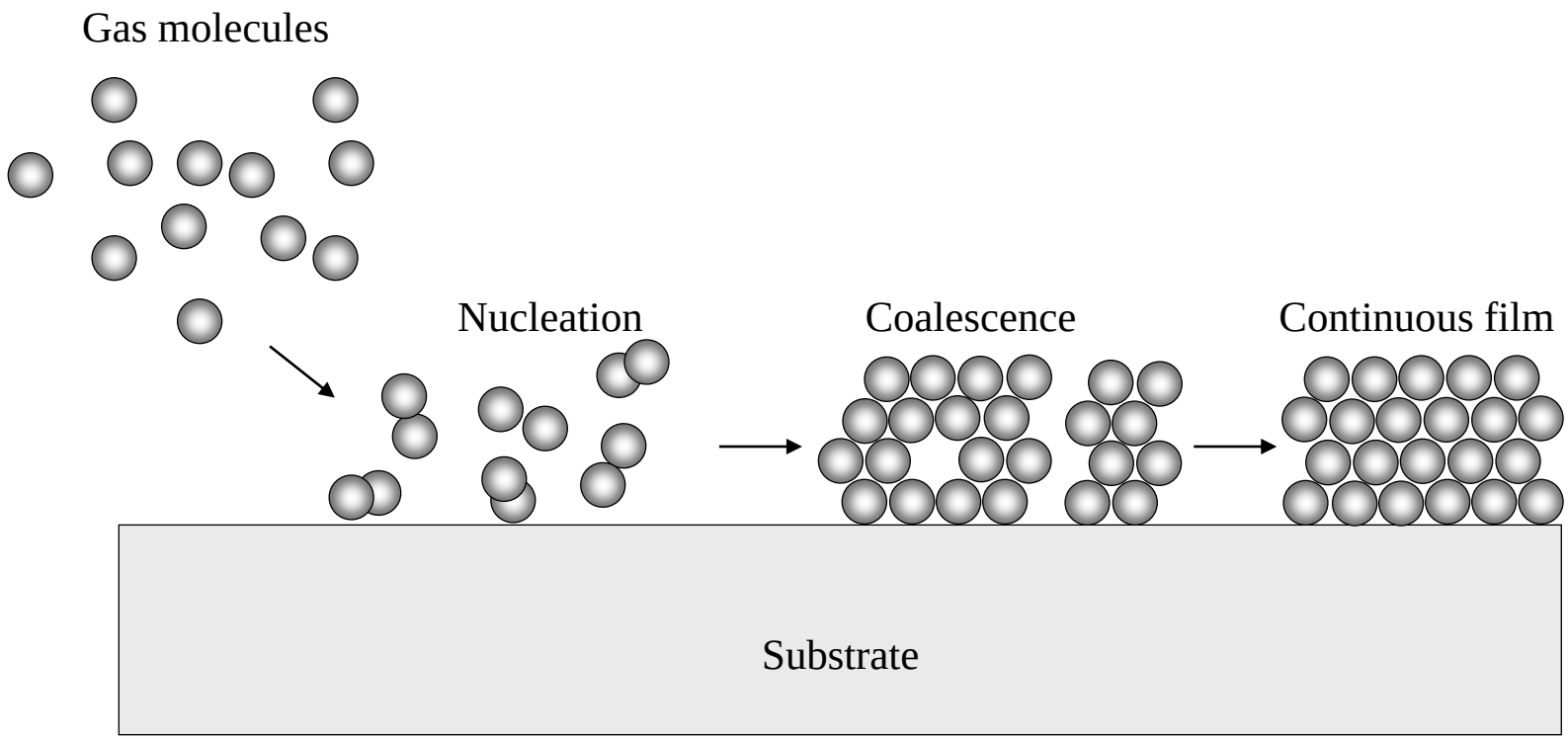
High Aspect Ratio Gap



Photograph courtesy of Integrated Circuit Engineering

Photo 11.2

Stages of Film Growth



- **A high surface mobility and/or low nucleation rate promote the formation of relatively large clusters. This leads polycrystalline.**
- **Low surface mobility leads to amorphous, normally at low deposition temperature (low surface mobility)**

Figure 11.7

Techniques of Film Deposition[13]

Chemical Processes		Physical Processes		
Chemical Vapor Deposition (CVD)	**Plating**	**Physical Vapor Deposition (PVD or Sputtering)**	**Evaporation**	**Spin On Methods**
Atmospheric Pressure CVD (APCVD) or Sub-Atmospheric CVD (SACVD)	Electrochemical deposition (ECD), commonly referred to as electroplating	DC Diode	Filament and Electron Beam	Spin on glass (SOG)
Low Pressure CVD (LPCVD)	Electroless Plating	Radio Frequency (RF)	Molecular Beam Epitaxy (MBE)	Spin on dielectric (SOD)
Plasma Assisted CVD: ▪ Plasma Enhanced CVD (PECVD) ▪ High Density Plasma CVD (HDPCVD)		DC Magnetron		
Vapor Phase Epitaxy (VPE) and Metal-organic CVD (MOCVD)		Ionized metal plasma (IMP)		
Dielectrics: Chapter 11 Metals: Chapter 12	Chapter 12	Chapter 12	Chapter 12	Chapter 11

Table 11.1

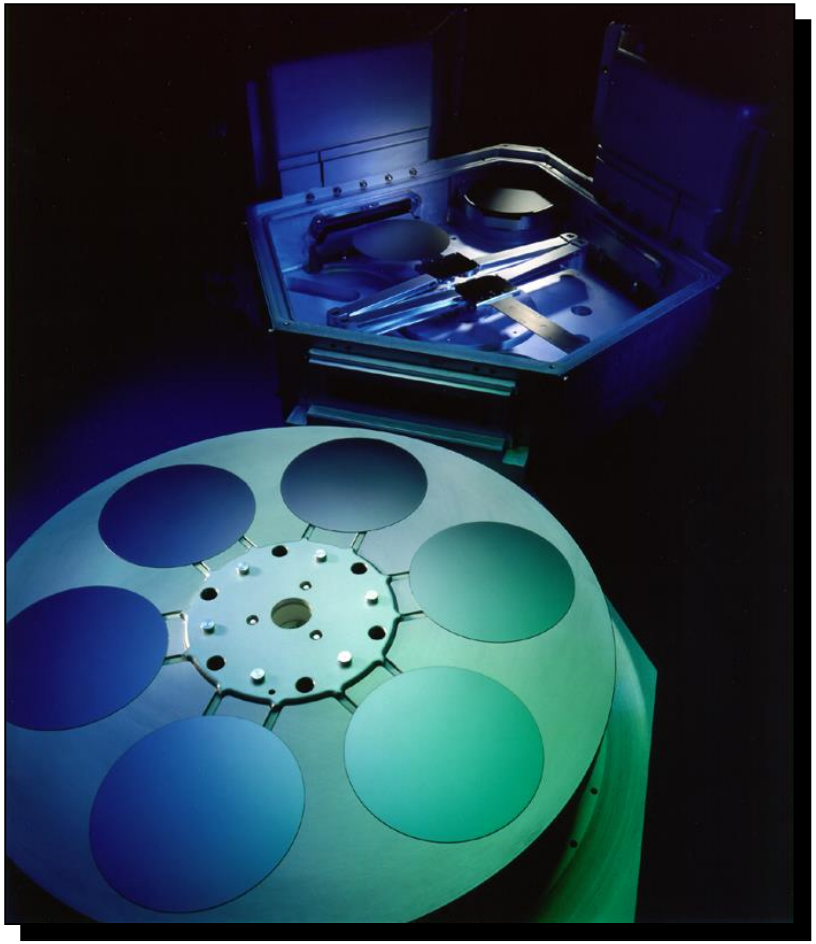
Chemical Vapor Deposition

CVD: deposited a solid film on surface through a chemical reaction of a gas mixture

The Essential Aspects of CVD

1. **Chemical** action is involved, either through chemical reaction or by thermal decomposition (referred to as pyrolysis).
2. All material for the thin film is supplied by an **external** source.
3. The reactants in a CVD process must start out in the **vapor phase** (as a gas).

Chemical Vapor Deposition Tool



Deposited chamber : reactor

Photo 11.3

CVD Chemical Processes

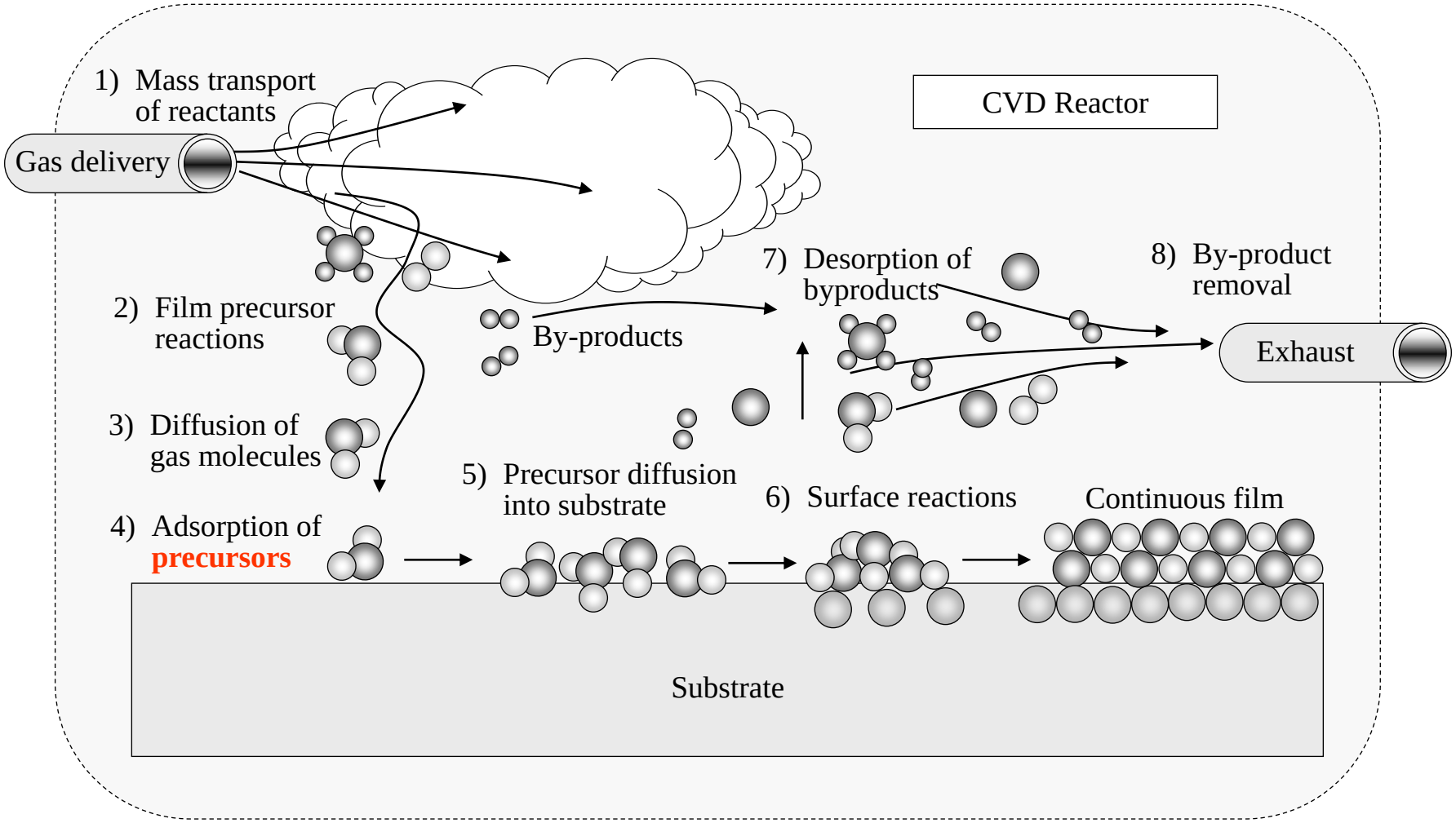
1. **Pyrolysis**: a compound dissociates (breaks bonds, or decomposes) with the application of heat, usually without oxygen.
2. **Photolysis**: a compound dissociates with the application of radiant energy that breaks bonds.
3. **Reduction**: a chemical reaction occurs by reacting a molecule with hydrogen.
4. **Oxidation**: a chemical reaction of an atom or molecule with oxygen.
5. **Reduction-oxidation (redox)**: a combination of reactions 3 and 4 with the formation of two new compounds.

- $SiH_4 + 2PH_3 + O_2 \rightarrow SiO_2 + 2P + 5H_2$

CVD Reaction

- CVD Reaction Steps
- Rate Limiting Step
- CVD Gas Flow Dynamics
- Pressure in CVD
- Doping During CVD
  - PSG
  - BSG
  - FSG

Schematic of CVD Transport and Reaction **8 Steps**



CVD Reaction

- Take place on wafer surface: **hetero**geneous reaction (surface catalyzed).
- **Homo**geneous reaction: above surface (gas reaction), which is poor adhesion, low-density with high defects
- $SiH_4 \rightarrow SiH_2 + H_2$ (SiH_2 is precursor, it is pyrolysis)
- CVD reaction steps are sequential, the slowest step defines the **bottleneck**

Gas Flow in CVD

- Mass transport limited deposition: at high temperature and high pressure, insufficient reactant gas being supplied to surface. It is temperature independent.
- Reaction rate limited deposition: at low temperature, less energy to drive surface reaction. It is very temperature sensitive.

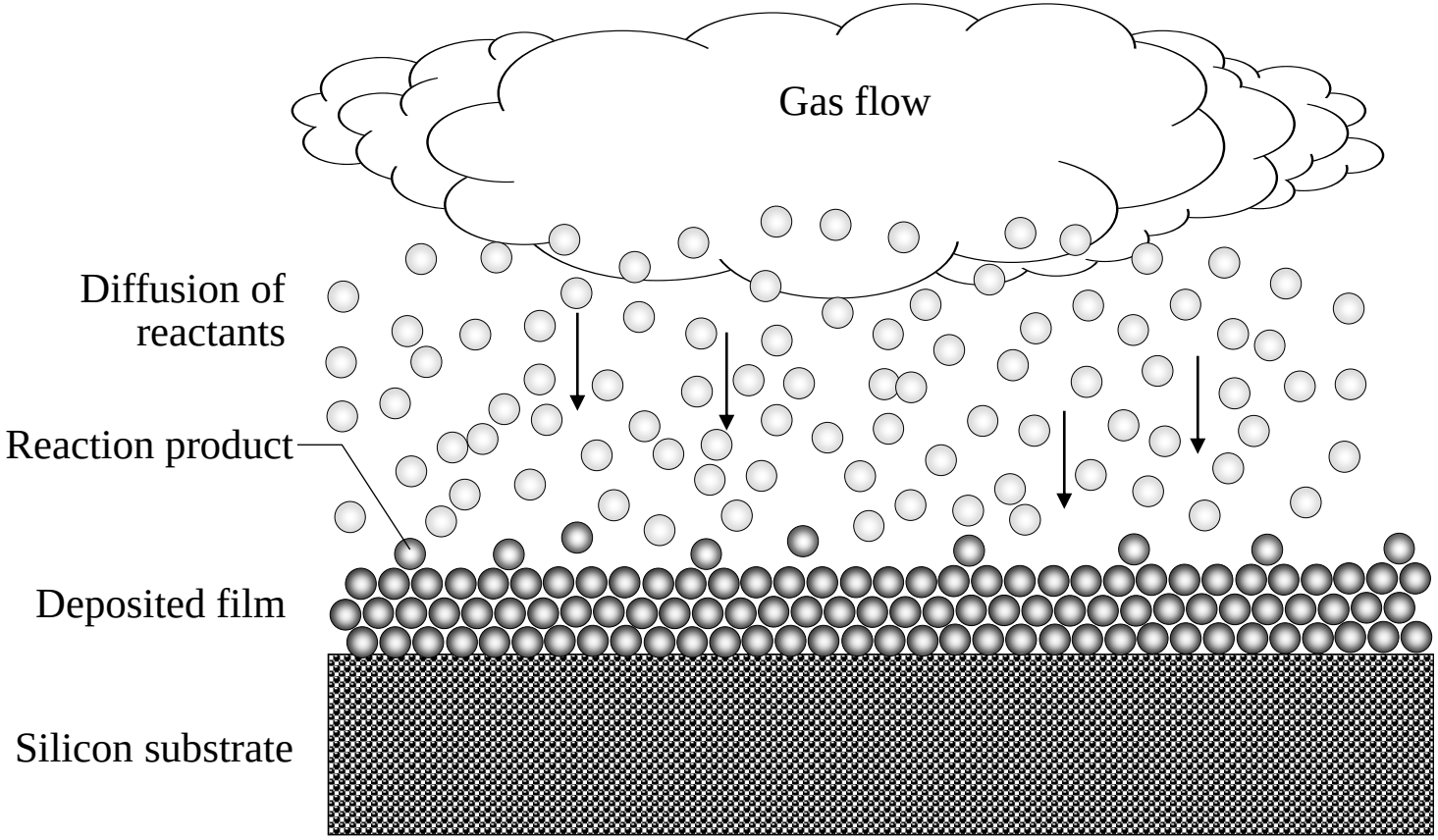
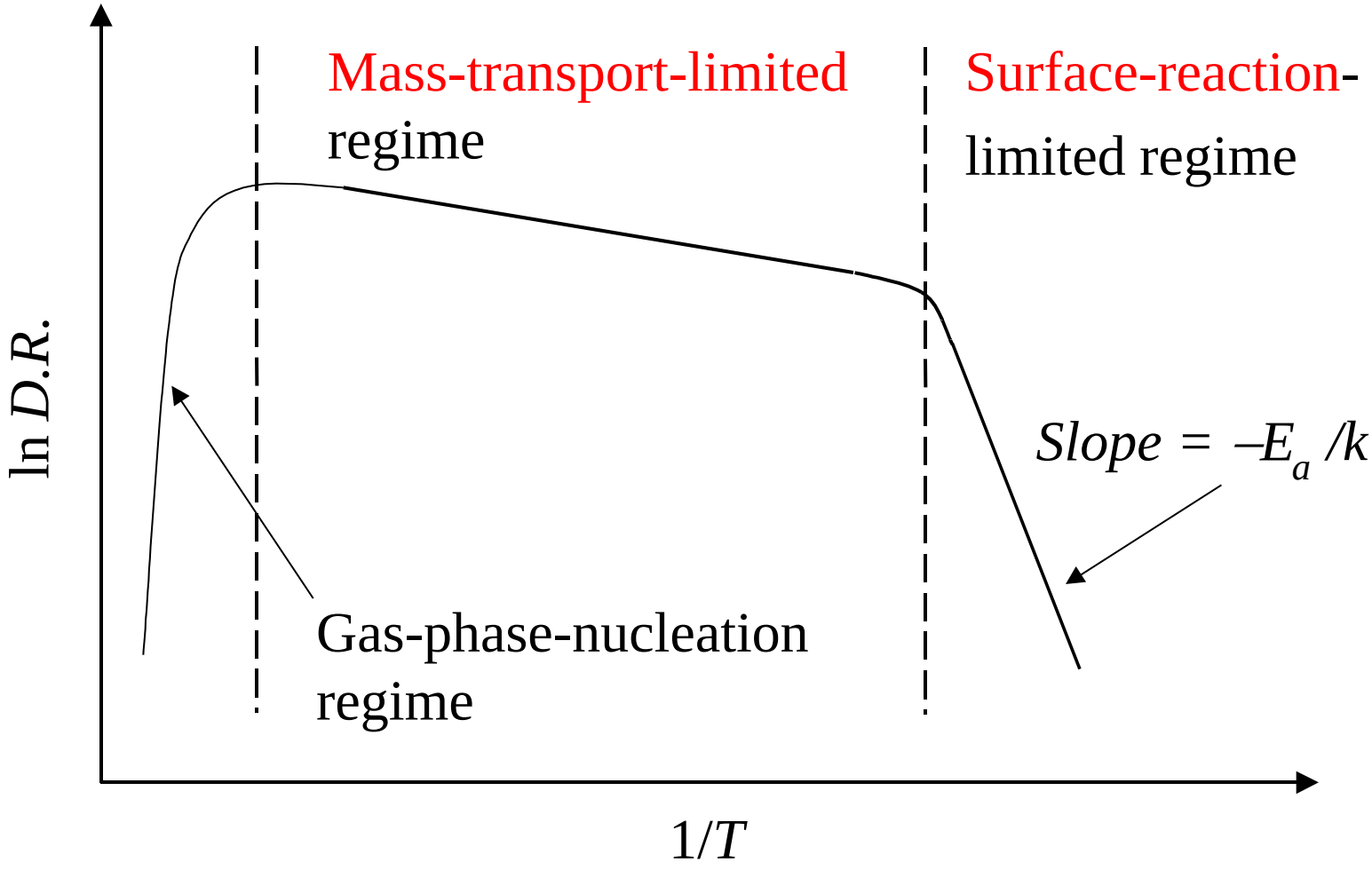
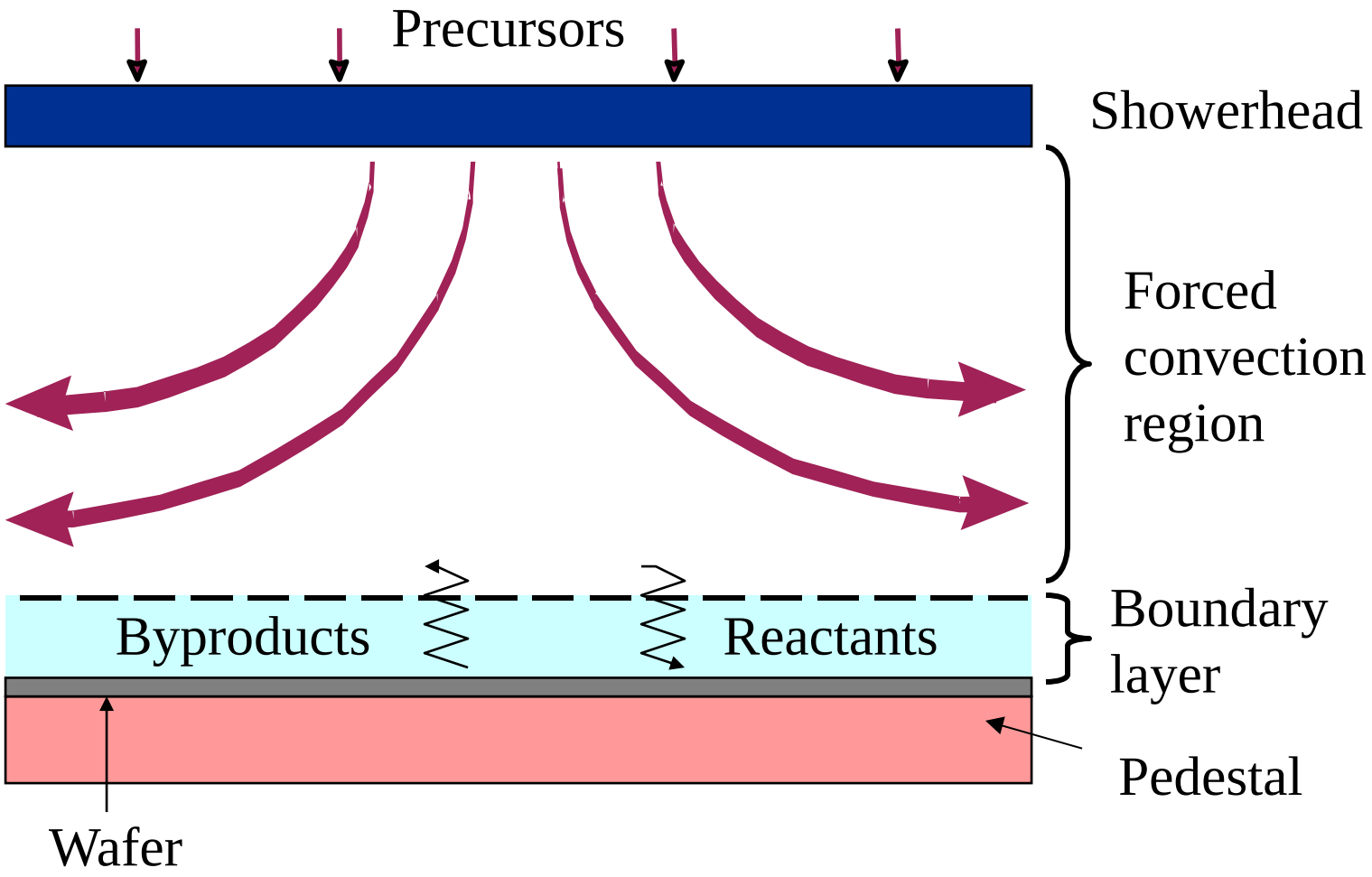


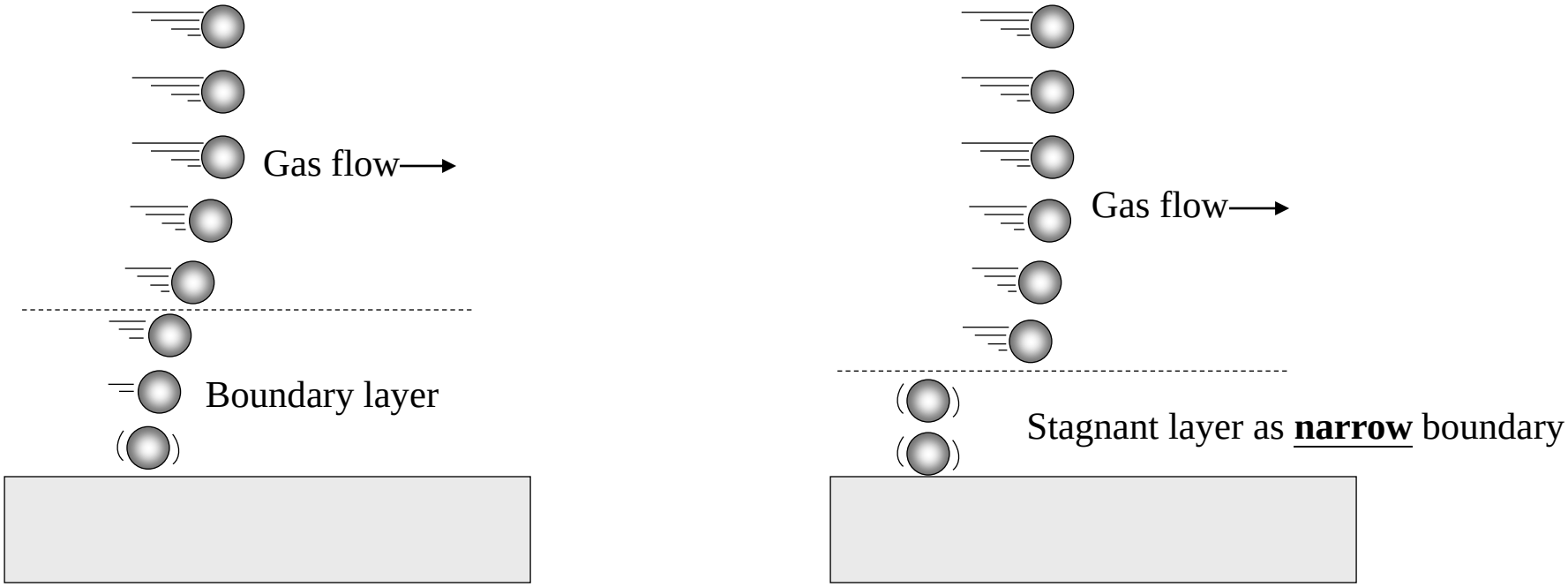
Figure 11.9

Deposition Regimes




Precursors
Showerhead
Forced convection region
Byproducts
Reactants
Boundary layer
Pedestal
Wafer

Gas Flow Dynamics at the Wafer Surface



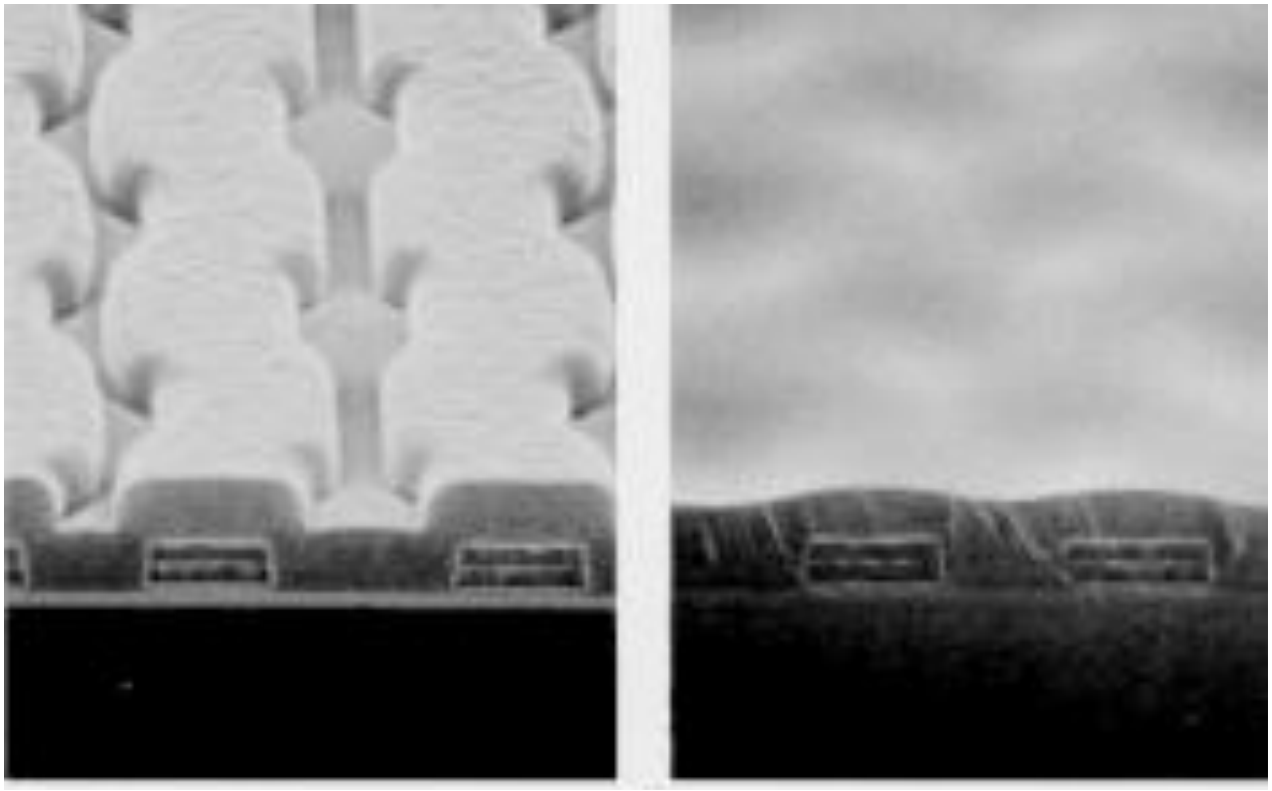
- **At low pressure, diffusion to surface increases, surface reaction becomes the limit.**
- **It means wafer can be stacked vertically and close spacing**

Figure 11.10

Doping During CVD

- Doping P as PSG (phosphosilicate glass) benefits wafer process, e.g., getter Na^+, low stress.
  - $SiH_4 + 2PH_3 + O_2 \rightarrow SiO_2 + 2P + 5H_2$
- $(P\text{-}O)^-$ getters Na^+
- P < 4%, otherwise water-absorbing
- B_2H_6 is used to form BSG, to reduce flow temperature
- BPSG (2-6%), flow temperature is still too high 800-1000C. Now is replaced by gap filling and CMP
- Fluorosilicate glass, or FSG is used for low-k (3.5), formed with SiF_4 (F< 6%), otherwise lead to corrosion (HF)
- FSG: SiF_4+SiH4+O_2

4×4 BPSG Reflow at 850 °C, 30 Minutes in N_2 Ambient



CVD Deposition Systems

- CVD Equipment Design
  - CVD reactor heating
  - CVD reactor configuration
  - CVD reactor summary
- Atmospheric Pressure CVD, APCVD
- Low Pressure CVD, LPCVD
- Plasma-Assisted CVD
- Plasma-Enhanced CVD, PECVD
- High-Density Plasma CVD, HDPCVD
- Atomic Layer CVD, ALCVD

CVD Reactor Types

- Hot wall: heat on both wafer and tube (need **cleaning**)
- Cold wall: heat on wafer and susceptor using RF or infrared lamp

CVD Reactor Types	**Atmospheric**	**Low-pressure**	**Batch**	**Single-wafer**
Hot-wall	√	√	√	
Cold-wall	√	√	√	√
Continuous motion	√		√	
Epitaxial	√		√	
Plenum	√		√	
Nozzle	√		√	
Barrel	√		√	
Cold-wall planar		√	√	√
Plasma-assisted		√	√	√
Vertical-flow Isothermal		√	√	√

Figure 11.11

Types of CVD Reactors and Principal Characteristics

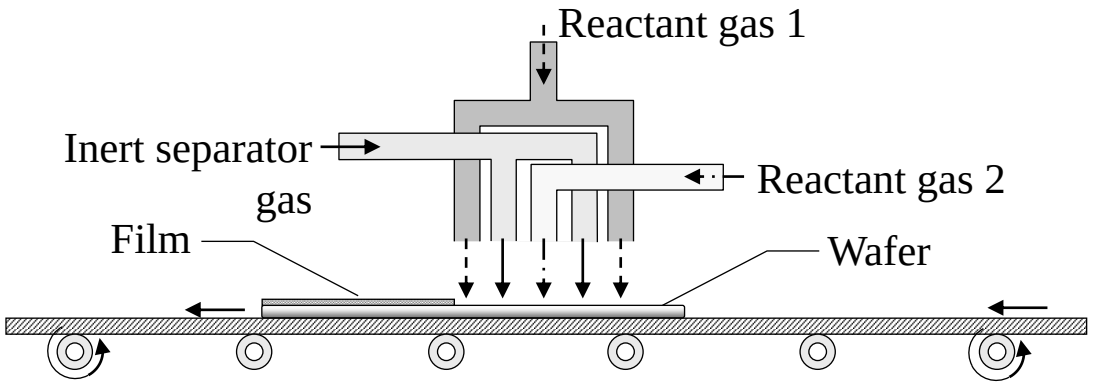
Process	Advantages	Disadvantages	Applications
APCVD (Atmospheric Pressure CVD)	Simple reactor, fast deposition, low temperature.	Poor step coverage, particle contamination, and low throughput.	Low-temperature oxides (both doped and undoped).
LPCVD (Low Pressure CVD)	Excellent purity and uniformity, conformal step coverage, large wafer capacity.	High temperature, low deposition rate, more maintenance intensive and requires vacuum system.	High-temperature oxides (both doped and undoped), silicon nitride, polysilicon, W, WSi_2.
Plasma Assisted CVD: ▪ Plasma Enhanced CVD (PECVD) ▪ High Density Plasma CVD (HDPCVD)	Low temperature, fast deposition, good step coverage, good gap fill.	Requires RF system, higher cost, stress is much higher with a tensile component, and chemical (e.g., H_2) and particle contamination.	High aspect ratio gap fill, low-temperature oxides over metals, ILD-1, ILD, copper seed layer for dual damascene, passivation (nitride).

APCVD: operate at mass-transport limited region, **equal** amount of reactant gases delivered is important
LPCVD: operate at reaction-rate limited, **temperature** control is important

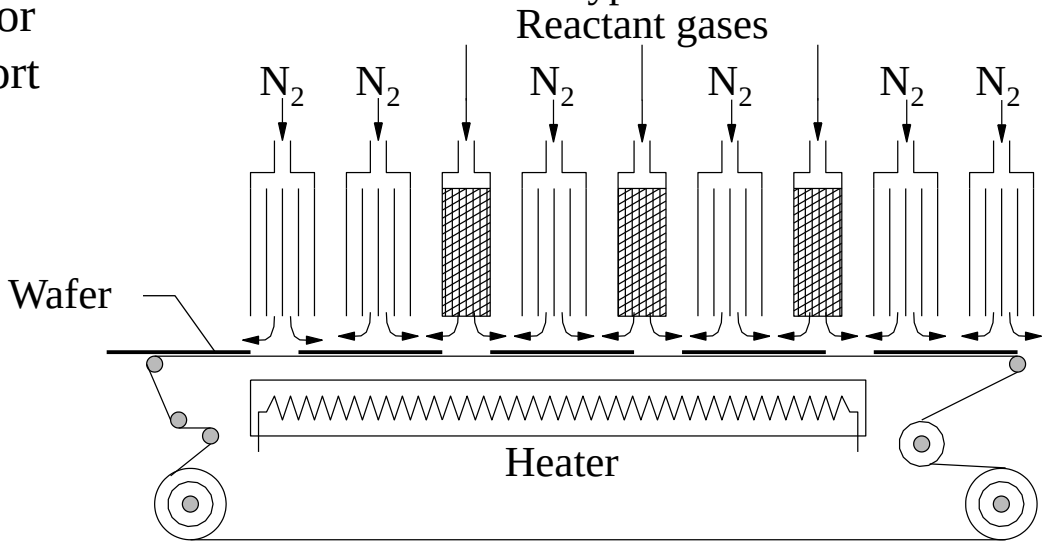
Table 11.2

Continuous-Processing APCVD Reactors

APCVD: design is **simple** with high deposition rate, for large-diameter. Belt transport system needs cleaning



(a) Gas-injection type

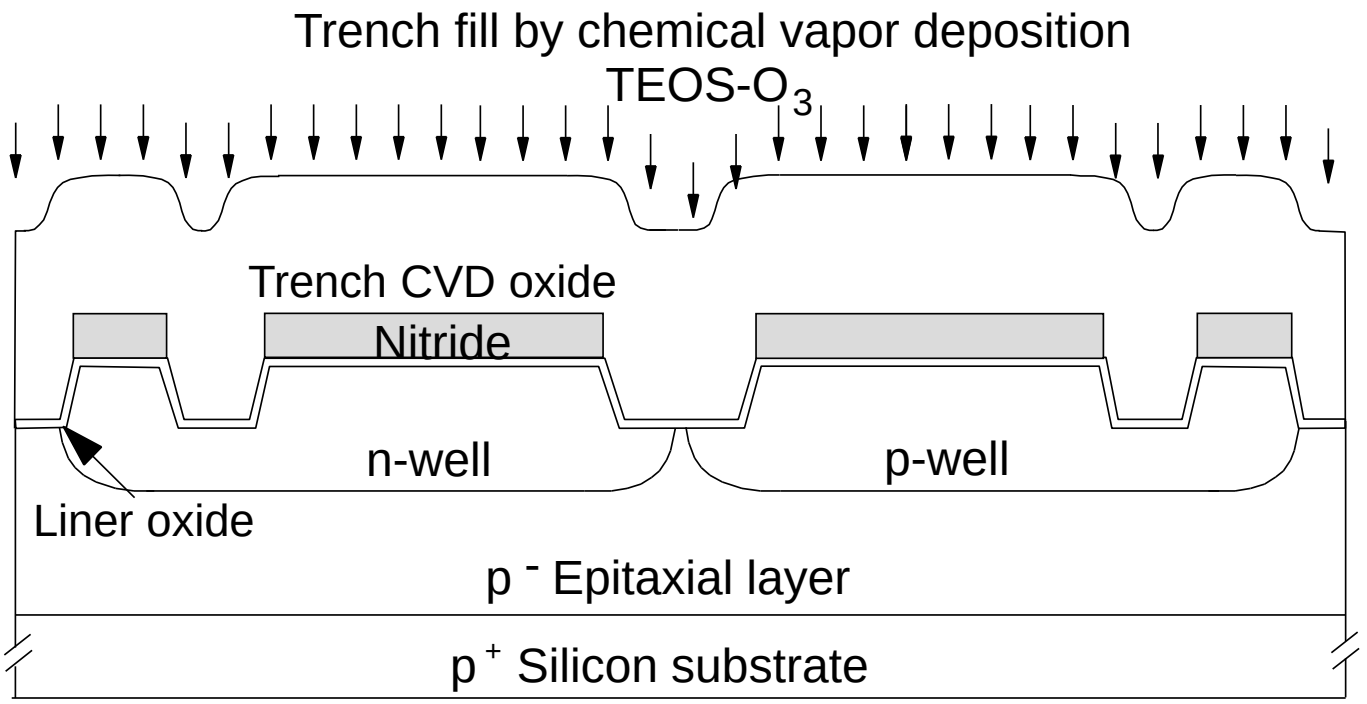


(b) Plenum type

Figure 11.12

Excellent Step Coverage of APCVD TEOS-O_3

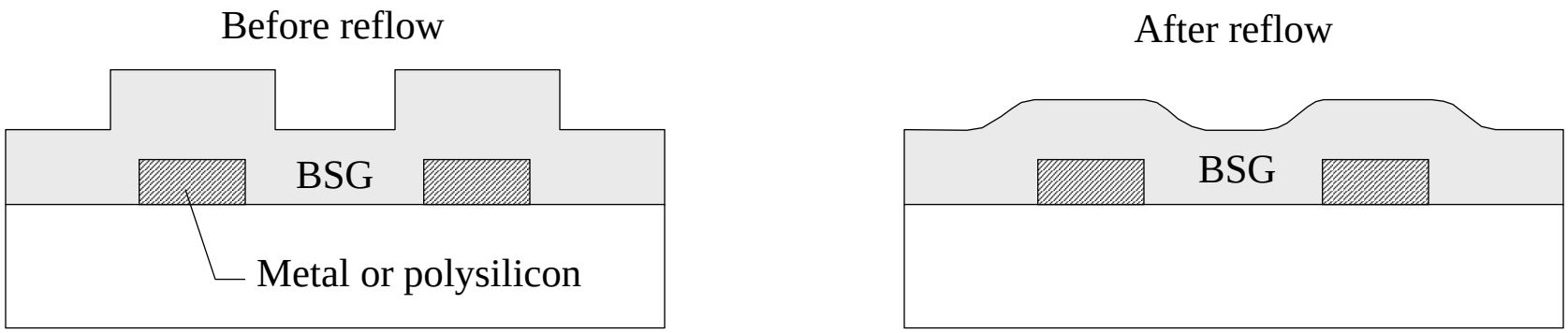
$$Si(C_2H_5O)_4 + 8O_3 \rightarrow SiO_2 + 10H_2O + 8\,CO_2$$



- SiH_4-base is not safe. Now tetraethylorthosilicate ($Si(C_2H_5O)_4$) with O_3 is commonly used
- O_3 is more reactive than O_2, hence, process can be done at low temperature without plasma
- Good at high-aspect ratio gaps filling (at STI)

Figure 11.3

Planarized Surface after Reflow of PSG



USG: undoped silicate glass
PSG: 950°C for 15-30 min
BPSG: 800°C for 60-min

Figure 11.14

Boundary Layer at Wafer Surface

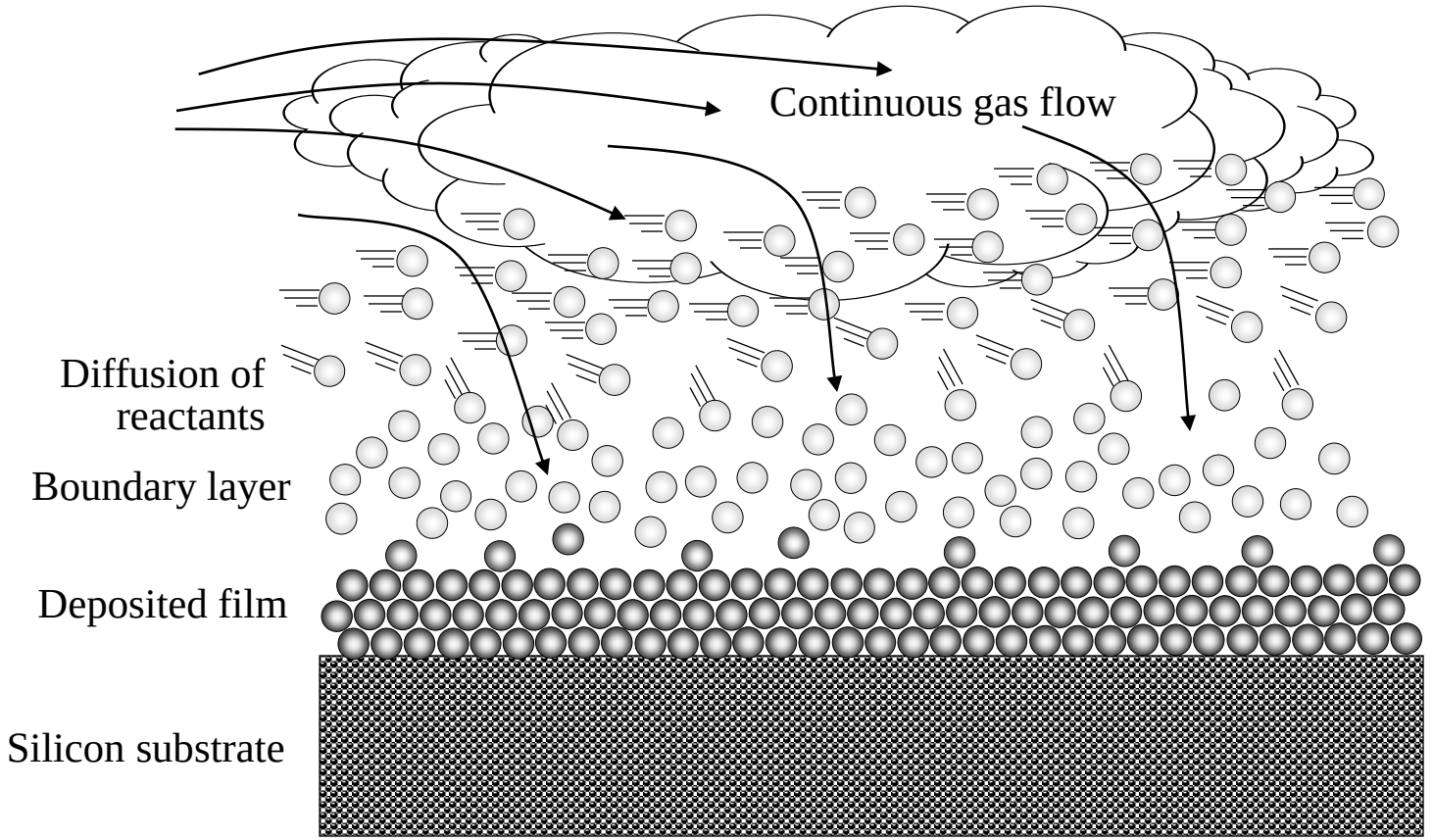
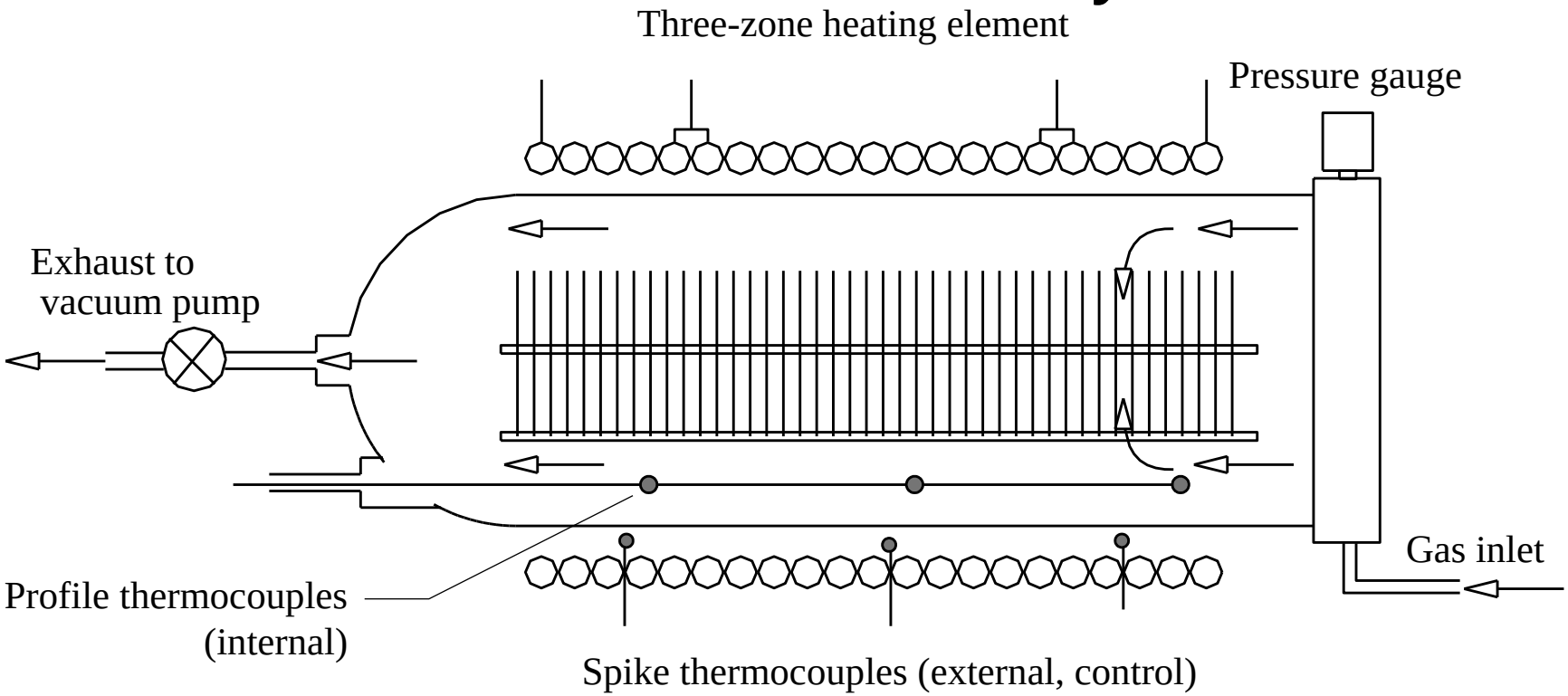


Figure 11.15

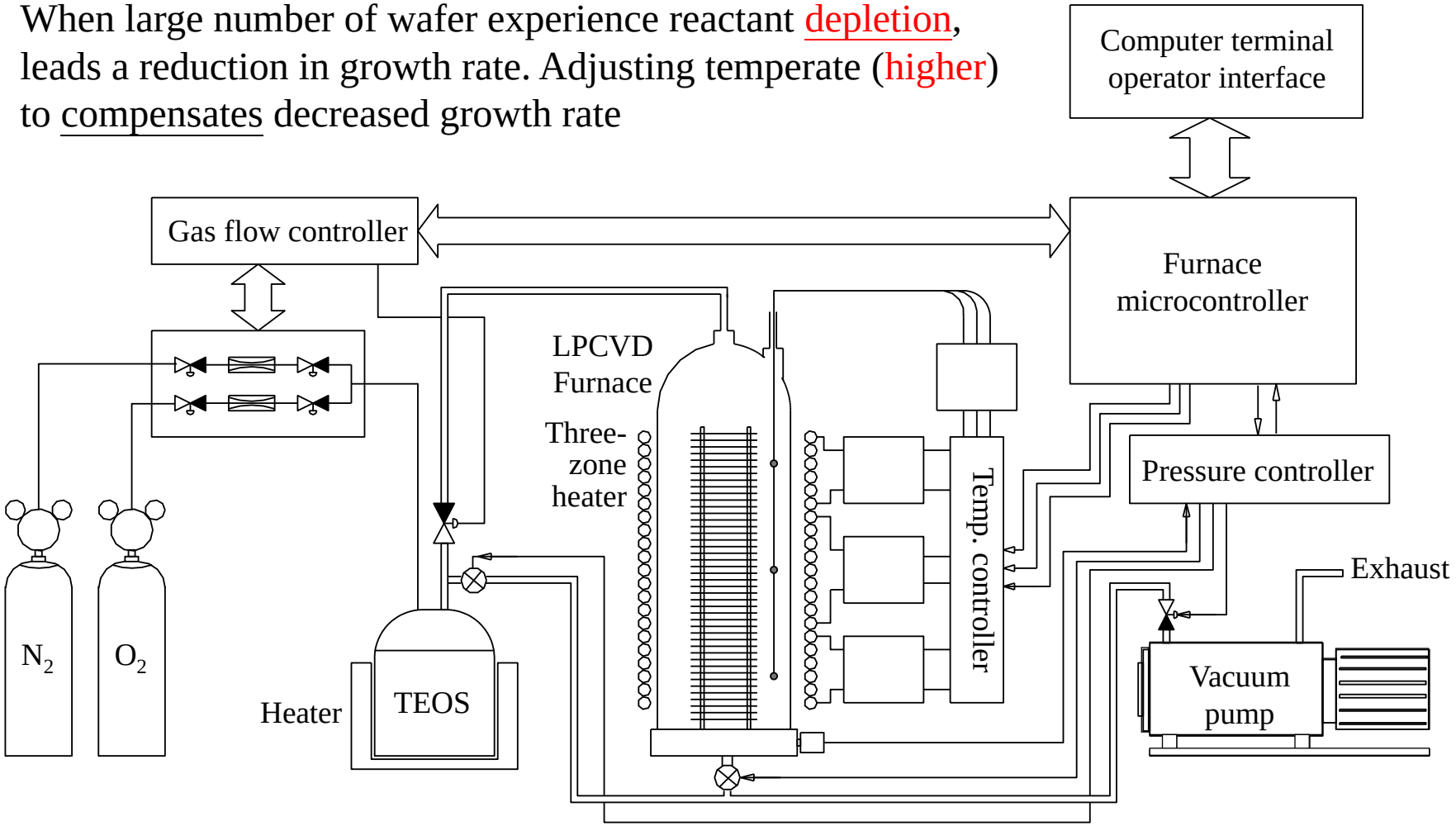
LPCVD Reaction Chamber for Deposition of Oxides, Nitrides, or Polysilicon



- Limited by surface reaction, flow condition is not important
- Films are uniformly deposited on a large number of wafer surface as long as the temperature is tightly controlled
- Conformal film coverage on the wafer
- Low growth rate than APCVD and need routine maintenance
- In-situ clean, using ClF_3 or NF_3
- $3SiCl2H2 + 4NH3 \rightarrow Si3N4 + 6HCl + 6H2$

Oxide Deposition with TEOS LPCVD

When large number of wafer experience reactant depletion, leads a reduction in growth rate. Adjusting temperate (higher) to compensates decreased growth rate



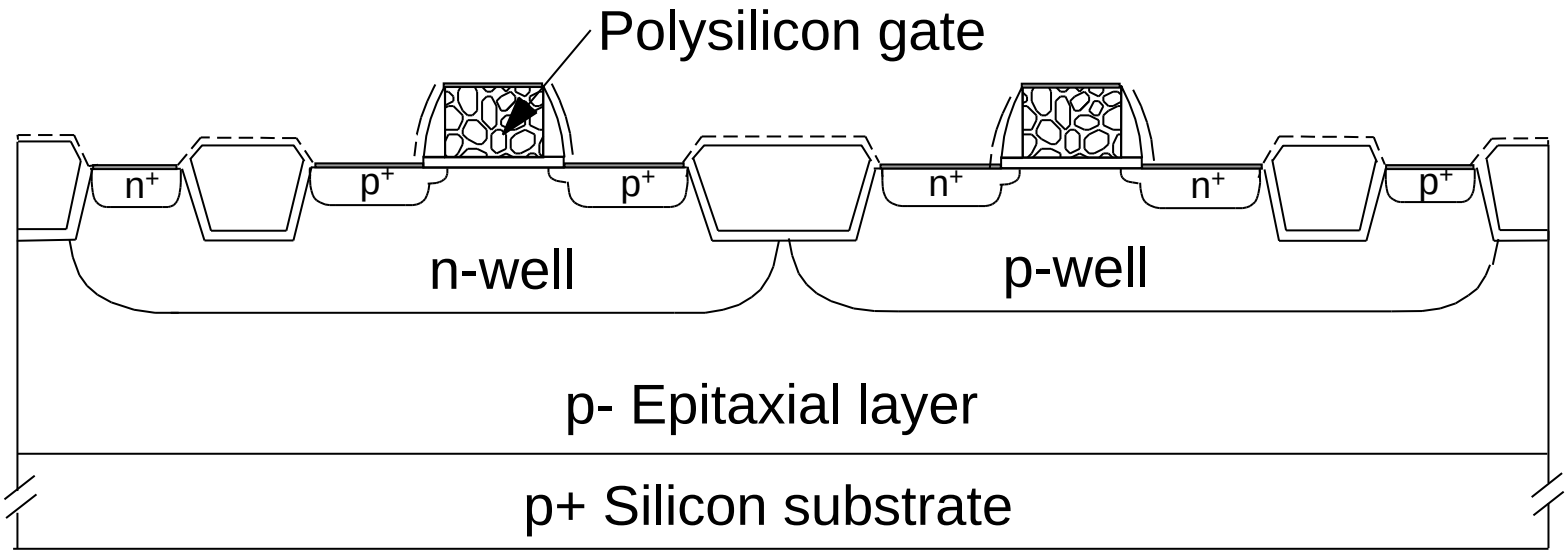
Temperature ~ 650-750°C with growth rate ~ 100-150 Å/min

Figure 11.17

Key Reasons for the Use of Doped Polysilicon in the Gate Structure

- Ability to be doped to a specific resistivity.
- Excellent interface characteristics with silicon dioxide.
- Compatibility with subsequent high temperature processing.
- Higher reliability than possible metal electrodes (e.g., Aluminum)
- Ability to be deposited conformally over steep topography.
- Allows for self-aligned gate process (see Chapter 9).

Doped Polysilicon as a Gate electrode



$SiH_4 \rightarrow Si\ (s) + 2H_2$

In situ doping using PH_3 for n^+, B_2H_6 for p^+

Figure 11.18

Advantages of Plasma Assisted CVD

- Lower processing temperature (250 – 450°C).
- Excellent gap-fill for high aspect ratio gaps (with high-density plasma).
- Good film adhesion to the wafer.
- High deposition rates.
- High film density due to low pinholes and voids.
- Low film stress due to lower processing temperature.

Film Formation during Plasma-Based CVD

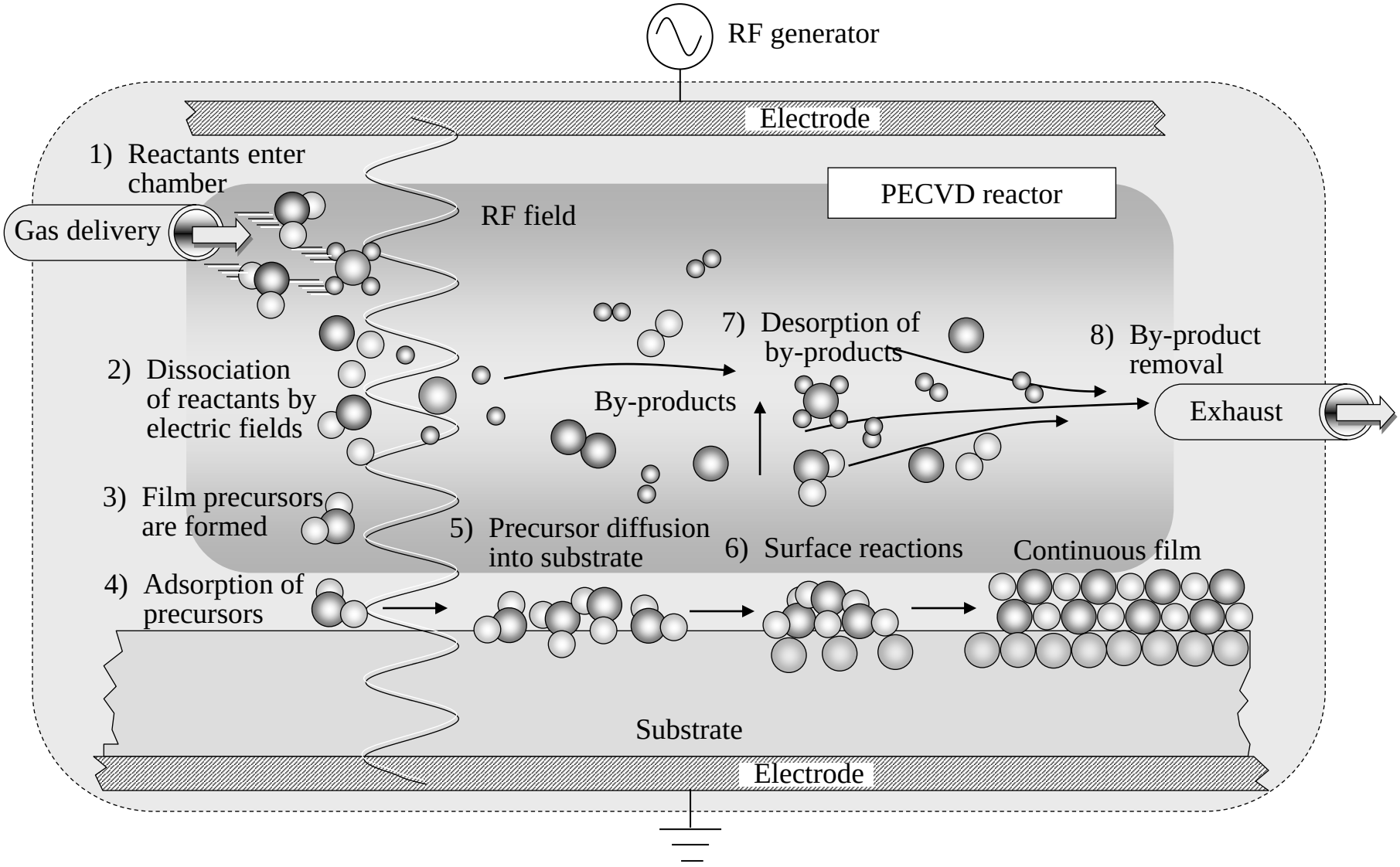


Figure 11.19

General Schematic of PECVD for Deposition of Oxides, Nitrides, Silicon Oxynitride or Tungsten

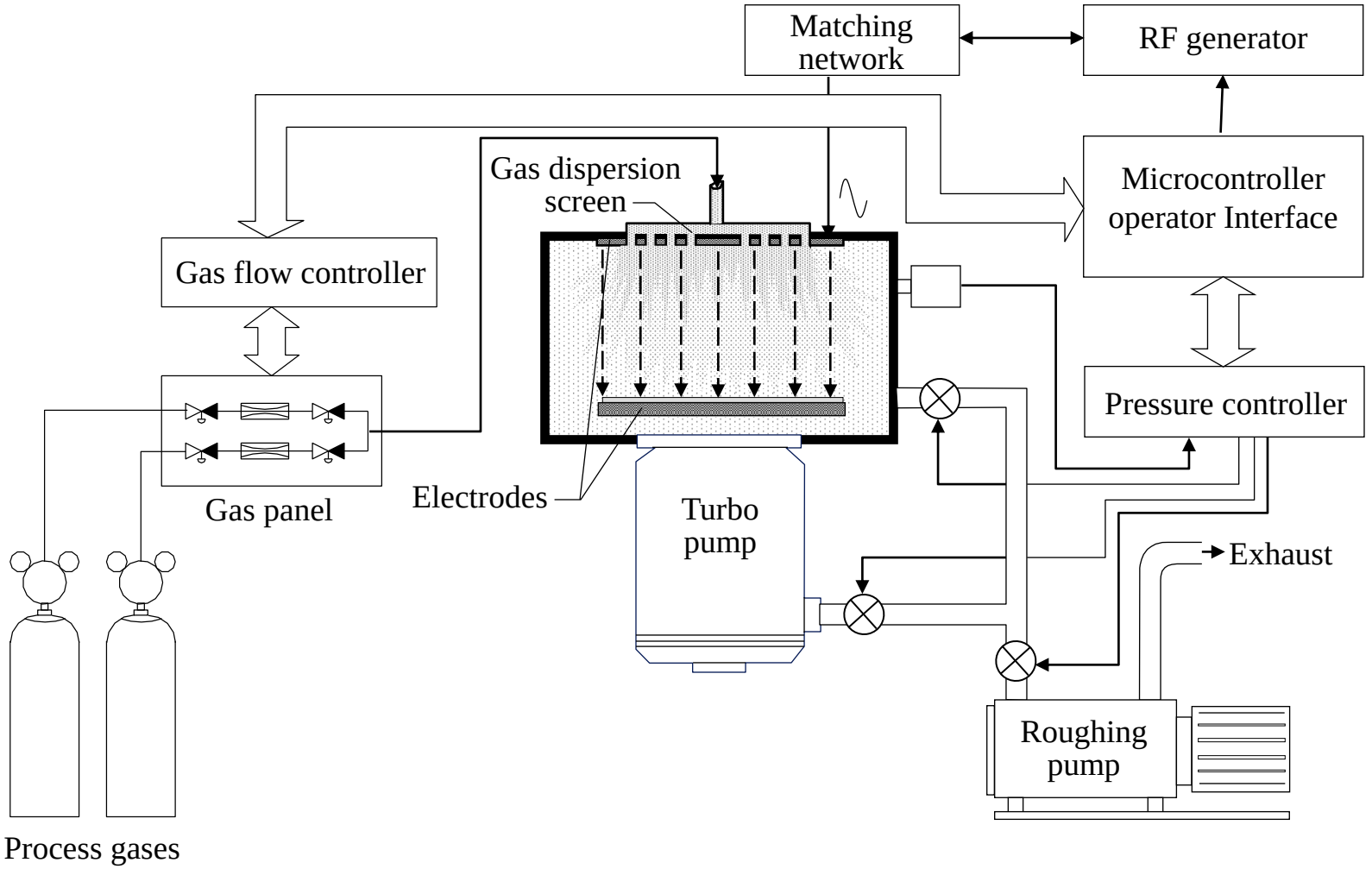


Figure 11.20

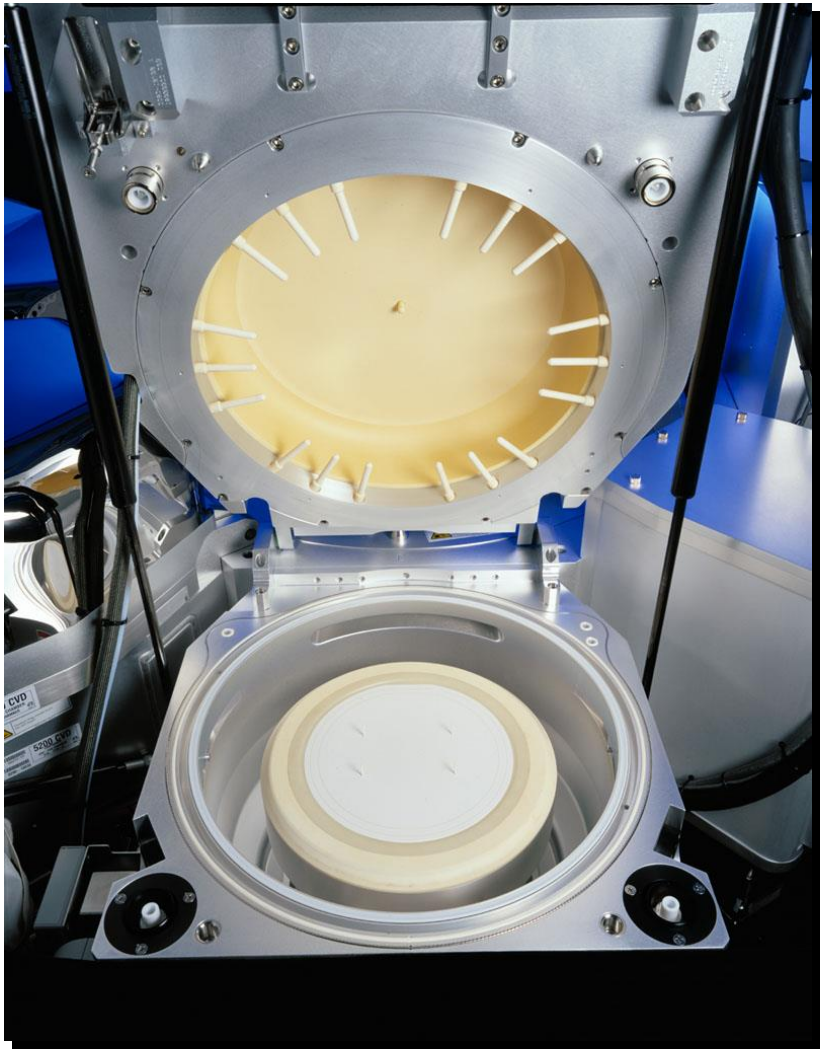
Properties of Silicon Nitride for LPCVD Versus PECVD

Property	LPCVD	PECVD
Deposition temperature (°C)	700 – 800	300 – 400
Composition	Si_3N_4	$Si_xN_yH_z$
Step coverage	Conformal	Fair
Stress at 23°C on silicon (dyn/cm^{-2})	$1.2 – 1.8 \times 10^{10}$ (tensile)	$1 – 8 \times 10^{9}$ (tensile or compressive)

Table 11.3

High Density Plasma Deposition Chamber

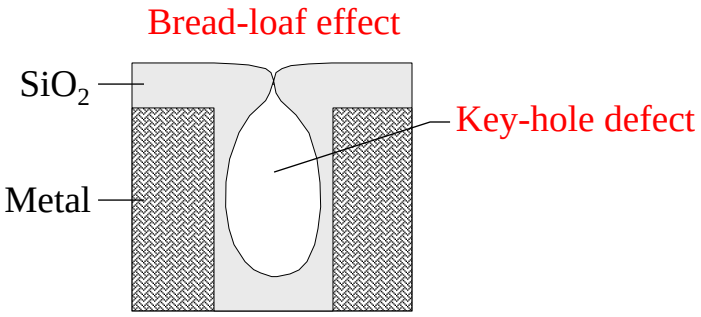
- Popular in mid-1990s
- High density plasma
- Highly directional due to wafer bias (RF)
- Fills high aspect ratio gaps (replaced PECVD)
- Backside He cooling to relieve high thermal load (high ion bombardment)
- Simultaneously deposits and etches film to prevent bread-loaf and key-hole effects



Photograph courtesy of Applied Materials, Ultima HDPCVD Centura

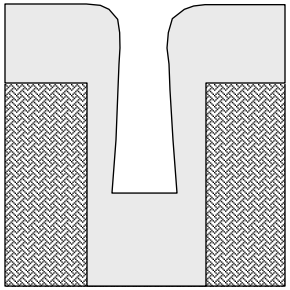
Photo 11.4

Dep-Etch-Dep Process (3:1)

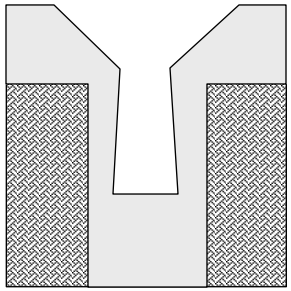


Film deposited with PECVD creates pinch-off at the entrance to a gap resulting in a void in the gap fill.

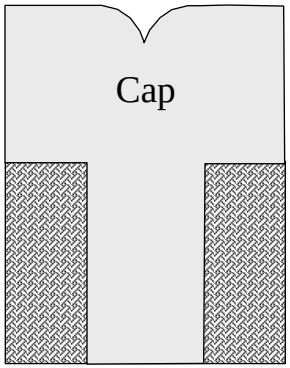
The solution begins here



1) Ion-induced deposition of film precursors



2) Argon ions sputter-etch excess film at gap entrance resulting in a beveled appearance in the film.



3) Etched material is redeposited. The process is repeated resulting in an equal “bottom-up” profile.

Figure 11.21

Five Steps of HDPCVD Process [1-3 major]

1. Ion-induced deposition
2. Sputter etch (Ar+)
3. Redeposition (from the bottom)
4. Hot neutral CVD (minor)
5. Reflection (minor contribution of ion reflecting off sidewall)

HDPCVD with Wafer at Throat of Turbo Pump

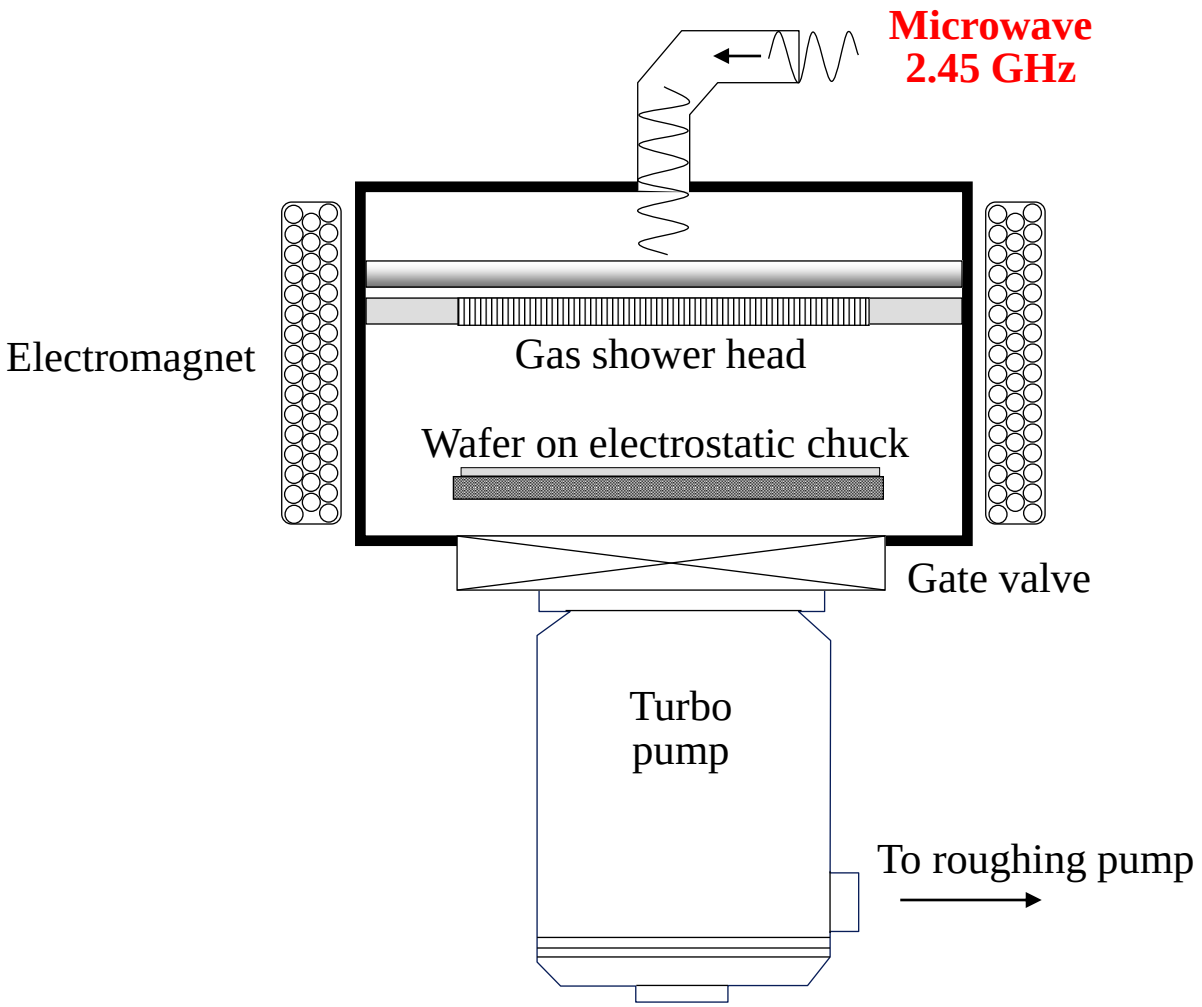
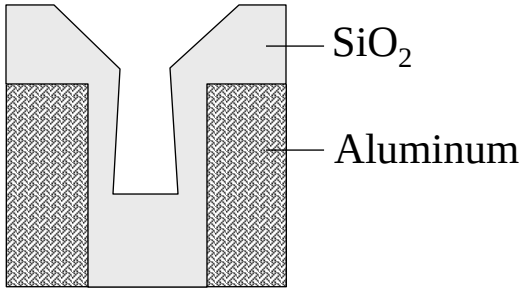


Figure 11.22

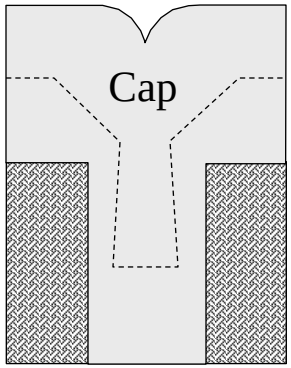
Dielectrics and Performance

- Dielectric Constant
- Gap Fill
- Chip Performance
- Low-k Dielectric
- High-k Dielectric
- Device Isolation
  - LOCOS
  - STI

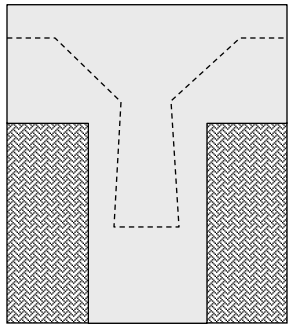
3-Part Process for Dielectric Gap Fill



1) HDPCVD gap fill



2) PECVD cap



3) Chemical mechanical planarization

Figure 11.23

Potential Low-*k* Materials for ILD of ULSI Interconnects

Potential low-*k* Dielectric	Dielectric Constant (*k*)	Gap Fill (μm)	Cure Temp. (°C)	Remarks
FSG (silicon oxyfluoride, Si_XOF_y)	3.4 – 4.1	<0.35	No issue	FSG has almost the same *k*-value as SiO_2 and reliability concern that fluorine will attack and corrode tantalum barrier metal.
HSQ (hydrogen silsesquioxane)	2.9	<0.10	350 – 450	Silicon-based resin polymer available in solution as Fox (Flowable Oxide) for spin-on coating application. May require surface passivation to reduce moisture absorption. Cure is done in nitrogen.
Nanoporous silica	1.3 – 2.5	<0.25	400	Inorganic material with tunable dielectric constant that relies on pore density. Increased porosity reduces mechanical integrity – porous material must withstand polishing, etching and heat treatments without degradation.
Poly(arylene) ether (PAE)	2.6 – 2.8	<0.15	375 – 425	Spin-on aromatic polymer with excellent adhesion and ability to be polished with CMP.
a-CF (fluorinated amorphous carbon or FLAC)[1]	2.8	<0.18	250 – 350	Leading candidate for CVD deposition with high density plasma CVD (HDPCVD) to produce film with good thermal stability and adhesion.
Parylene AF4 (aliphatic tetrafluorinated poly-p-xylylene)	2.5	<0.18	420 – 450	CVD film that meets adhesion and via resistance requirements with need to maintain gas delivery system at 200°C to control parylene precursor flow rate.

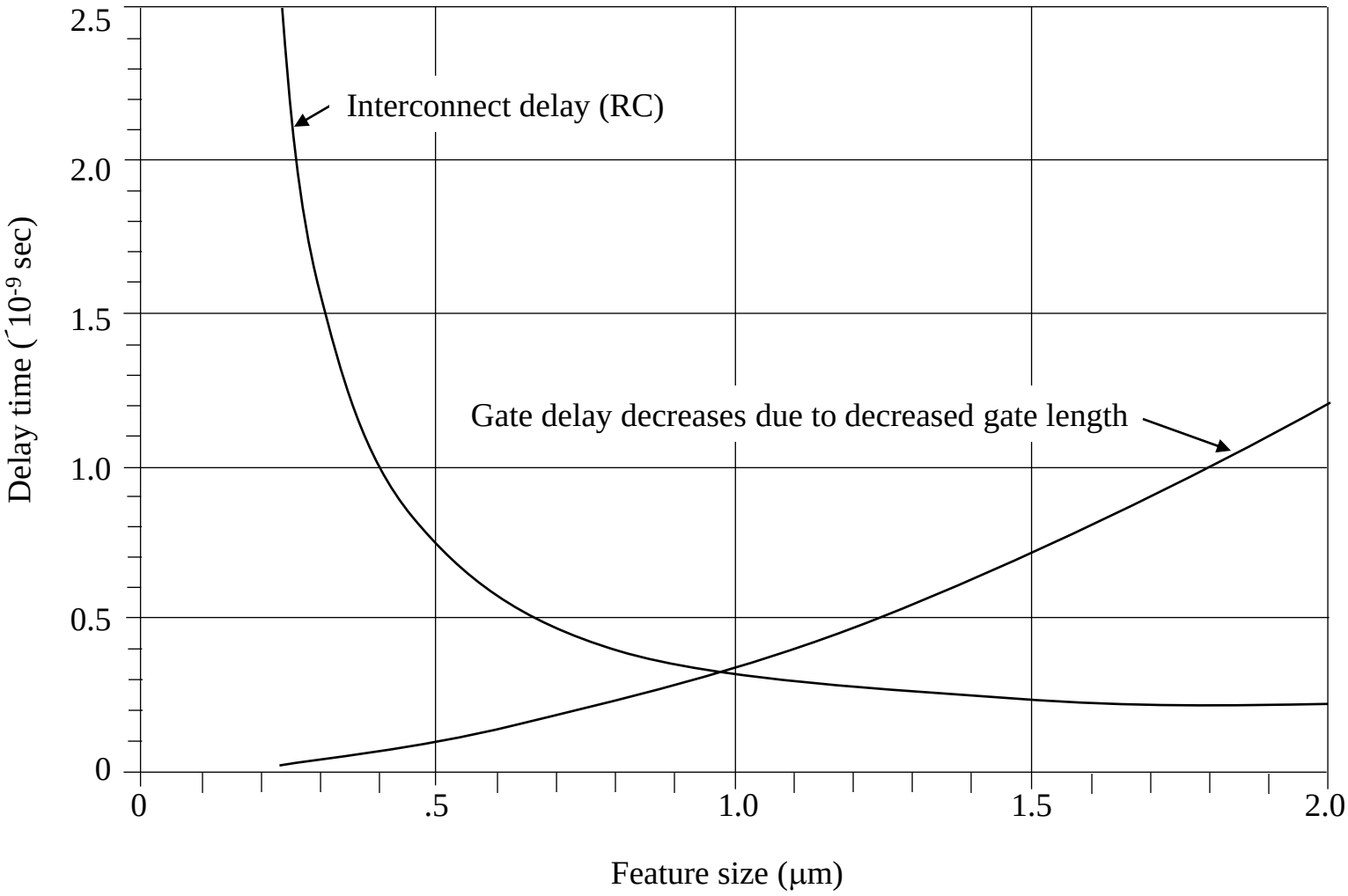
[1] P. Singer, *Technology News: Wafer Processing*, Semiconductor International, October, 1998, p. 44.

Table 11.4

Table 11–6 Materials used or considered for interlevel dielectrics (After [11.19])

Material class	Material	Dielectric constant	Deposition technique
Inorganic	SiO_2 (including PSG and BPSG)	3.9–5.0	CVD Thermal oxidation Bias-sputtering High-density plasma
	Spin-on-glass (SiO_2) (including PSG and BPSG)	3.9–5.0	SOD (spin-on-dielectric)
	Modified SiO_2 (e.g., fluorinated SiO_2 or hydrogen silsesquioxane—HSQ)	2.8–3.8	CVD/SOD
	BN (Si)	>2.9	CVD
	Si_3N_4 (only used in multilayer structure)	5.8–6.1	CVD
Organic	Polyimides	2.9–3.9	SOD/CVD
	Fluorinated polyimides	2.3–2.8	SOD/CVD
	Fluoro-polymers	1.8–2.2	SOD/CVD
	F-doped amorphous C	2.0–2.5	CVD
Inorganic/Organic Hybrids	Si-O-C hybrid polymers based on organosilsesquioxanes (e.g., MSQ)	2.0–3.8	SOD
Aerogels (Microporous)	Porous SiO_2 (with tiny free space regions)	1.2–1.8	SOD
Air bridge		1.0–1.2	

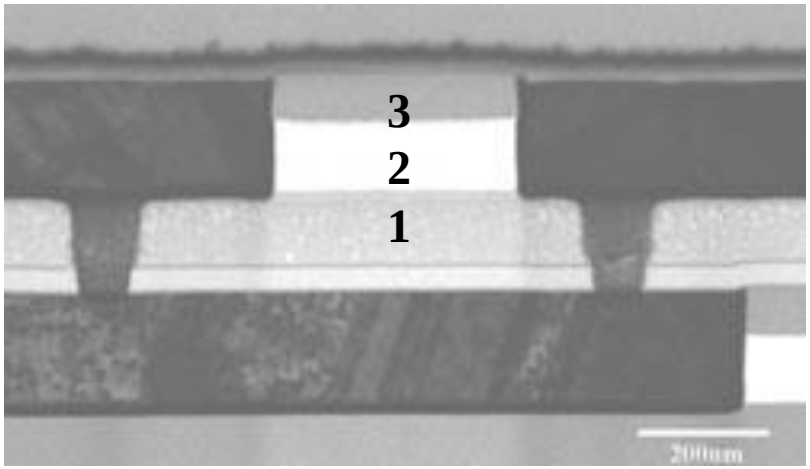
Interconnect Delay (RC) vs. Feature Size (μm)



R increases due to scaled line width, C increases due to narrow line space

Figure 11.24

Sony Demonstrates Feasibility of Copper/ULK (2.0) Interconnects 32 nm node

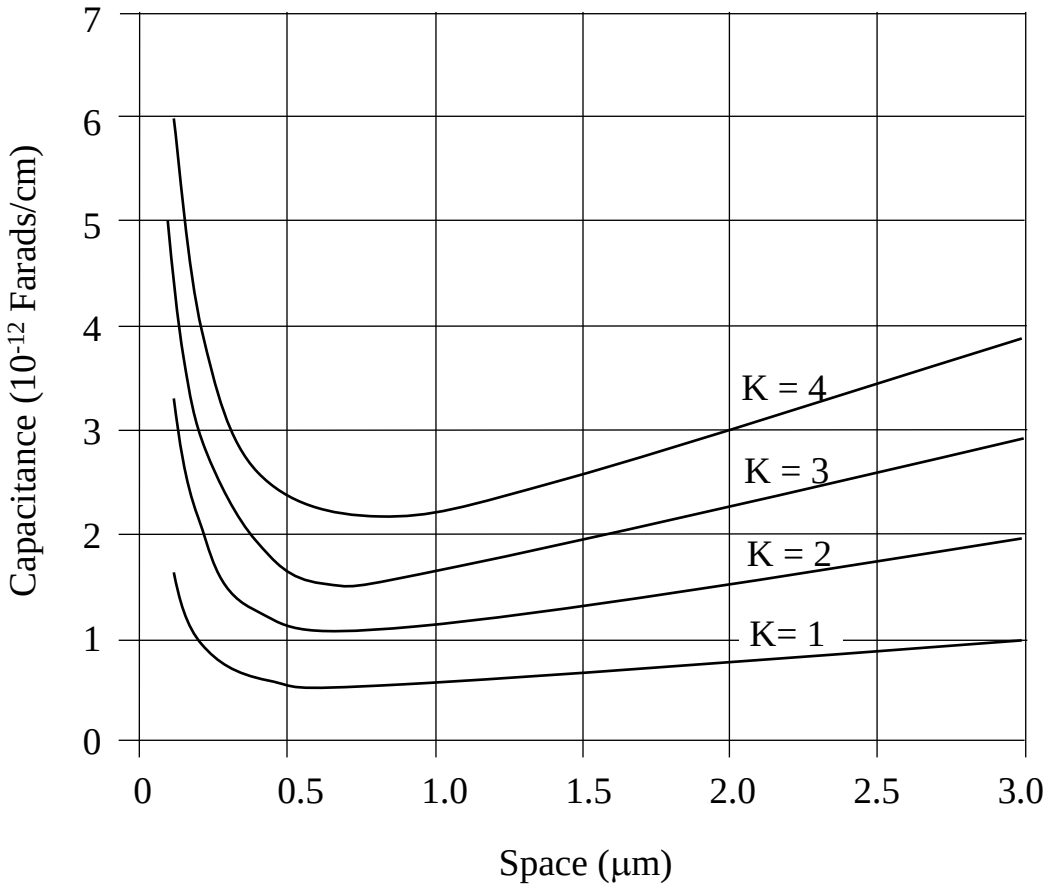


Ultralow-k (2.0) is used at the via level, while polyarylene (k=2.3) is integrated at the line level with low-k (2.65) hard mask.

- replaced a conventional triple hard mask process (TEOS/SiN/low-k) to better control the dual-damascene profile
- 2.65/PAr/ultralow-k (ULK) stack
- low-k hard mask (k=2.65) resulted in an 11% reduction in interline
- With the ULK, interlevel capacitance was reduced by 18%.

(*Semiconductor International*, 7/1/2006)

Total Interconnect Wiring Capacitance

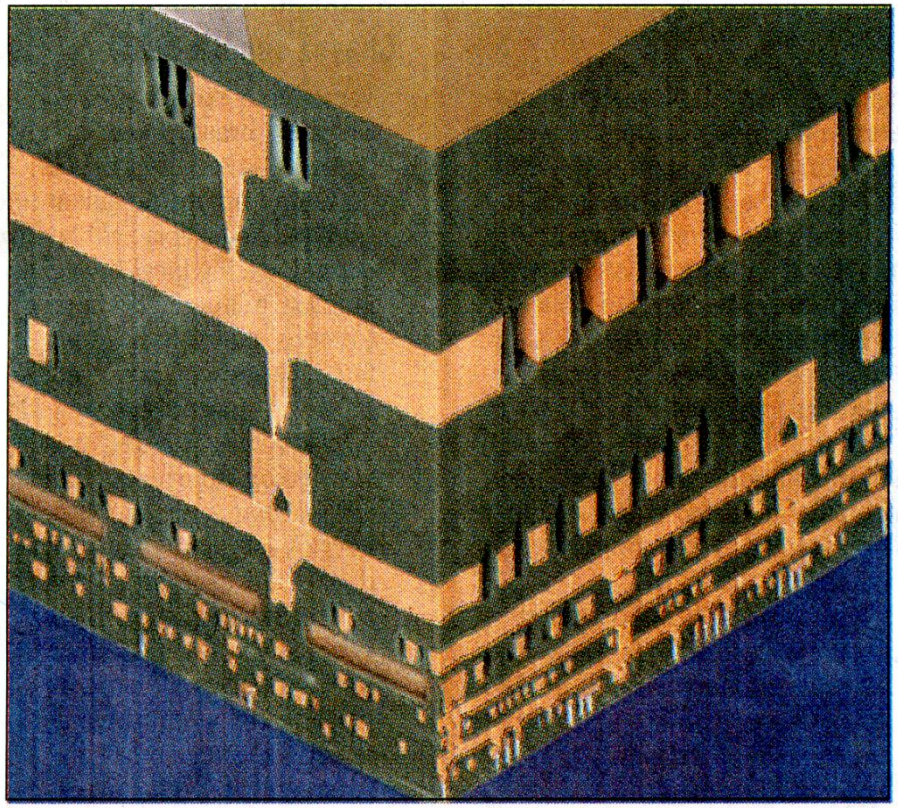


Redrawn with permission from Semiconductor International, September 1998

Figure 11.25

Nanotechnology Boots Chip Performance

(Taipei Times 2007/5/6)



A cross section of a microprocessor shows empty space in between the chip's copper wiring in this undated handout photograph. Wires are usually insulated with a glass-like material. IBM has integrated self-assembly techniques with its manufacturing lines to create test versions of its latest microprocessors that use vacuum gaps to insulate the miles of nano-scale wire that connect hundreds of millions of transistors. PHOTO: REUTERS/IBM

- For an advanced multilevel interconnect, a ~5% cost adder should provide 35% faster chips or 15% less power consumption.

- 2009 in production
- Process:
  - a self-assembling materials on top glass (mask)
  - Etching away the glass to form small holes in top surface, and larger, continuous gags between the wires
  - Another glass seals the smaller hole on the top in vacuum
- They're more like **Swiss** cheese than American cheese

Low-*k* Dielectric Film Requirements

Electrical	Mechanical	Thermal	Chemical	Processing	Metallization
Low dielectric constant	Good adhesion	Thermal stability	Resistant: acids and bases	Patternability	Low contact resistance
Low dielectric loss	Low shrinkage	Low coefficient of thermal expansion	Etch selectivity	Good gap fill	Low electromigration (corrosion)
Low leakage	Crack resistant	Low conductivity	Low impurities	Planarization	Low stress voiding
High reliability	Low stress		No corrosion	Low pin hole	Hillock (smooth surface)
	Good hardness		Low moisture uptake	Low particulate	Compatible with barrier metals (Ta, TaN, TiN, etc.)
			Storage life		

Table 11.5

General Diagram of DRAM Stacked Capacitors

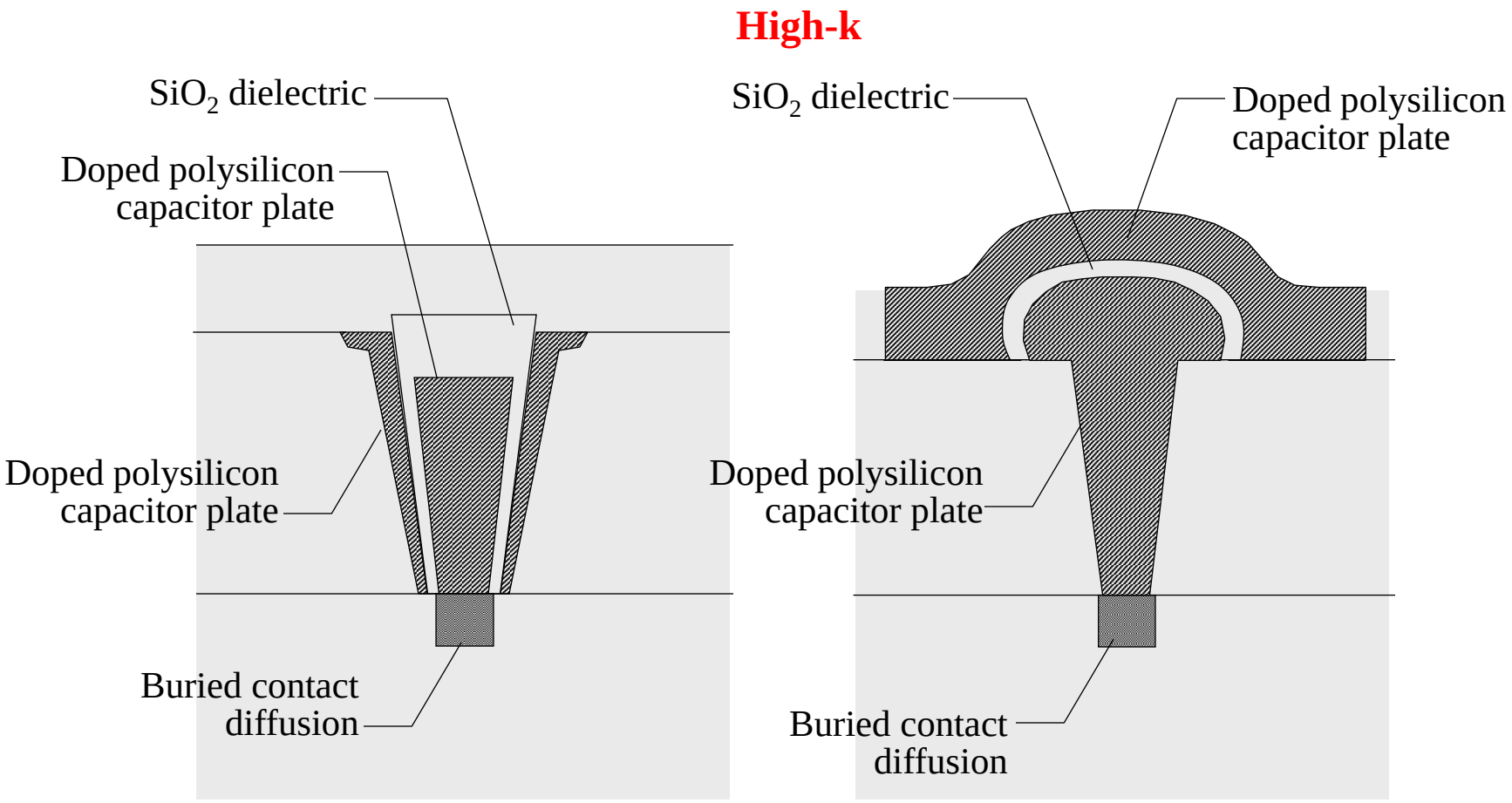
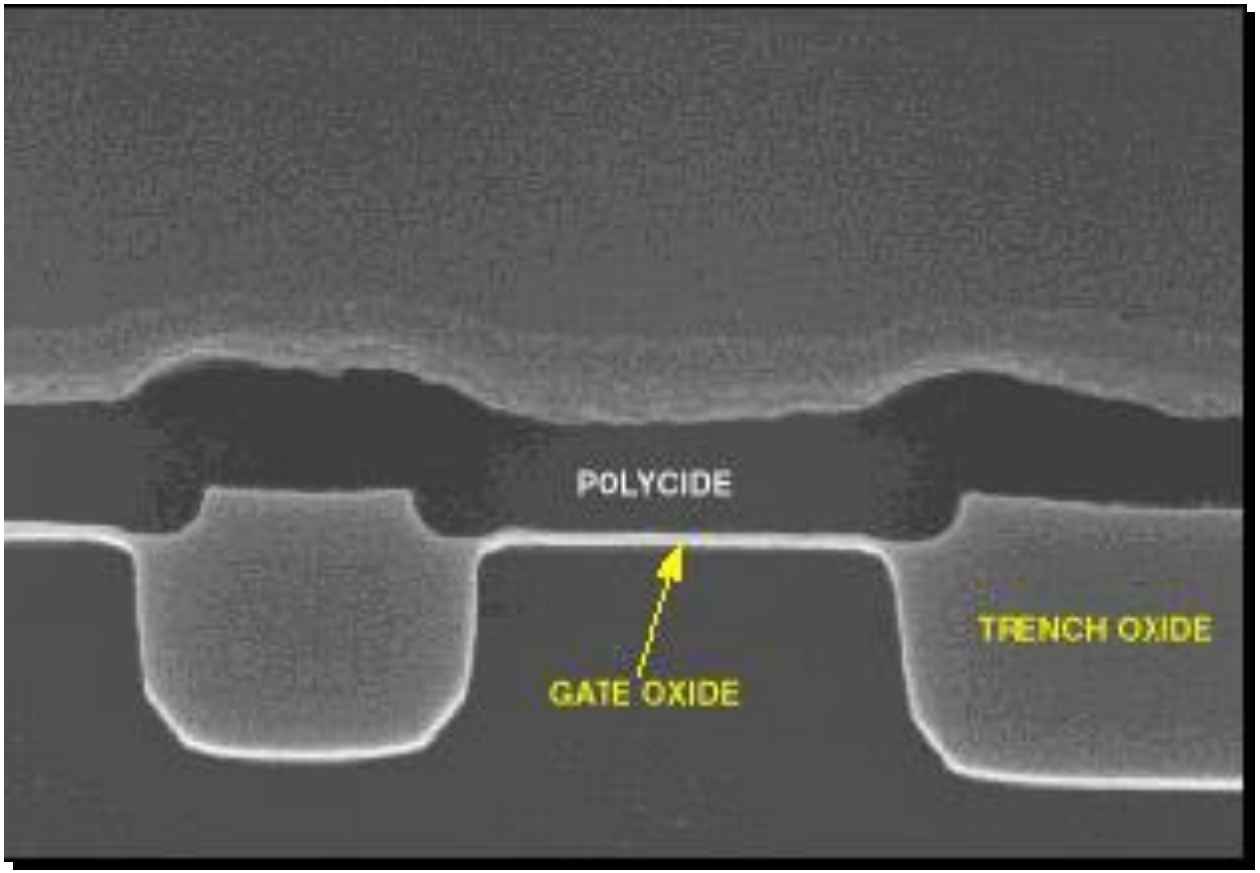


Figure 11.26

Shallow Trench Isolation (< 0.25 um)



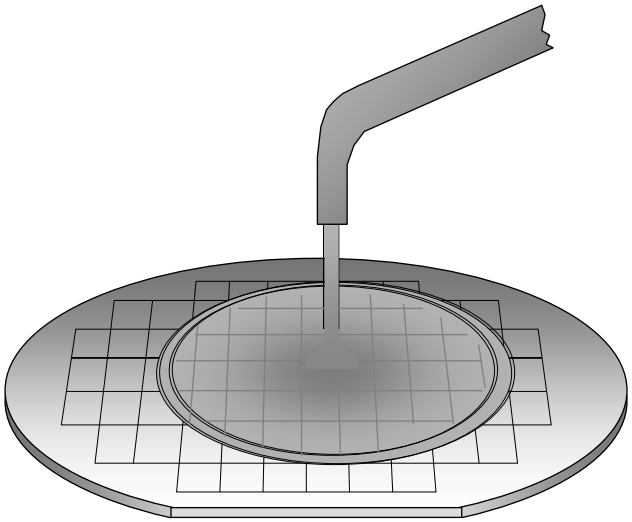
Photograph courtesy of Integrated Circuit Engineering

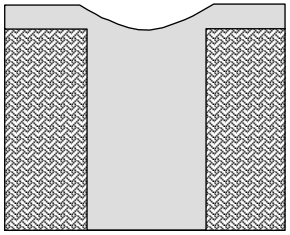
Photo 11.5

Spin-on Dielectrics

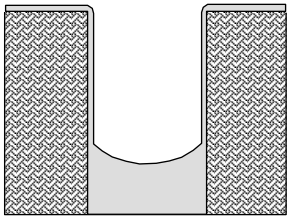
- Spin-on Glass (SOG)
- Spin-on Dielectric (SOD)
- Epitaxy
  - Epitaxy growth methods
    - Vapor-phase epitaxy
    - Metalorganic CVD
    - Molecular-beam epitaxy
- Quality Measures
- CVD Troubleshooting

Gap-Fill with Spin-On-Glass (SOG)

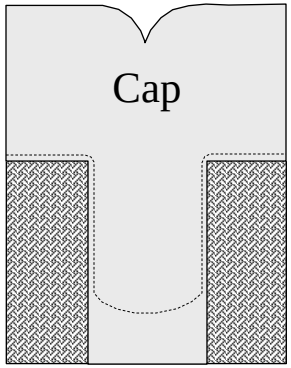




1) Initial SOG gap fill



2) SOG after curing



3) CVD oxide cap

Figure 11.27

Proposed HSQ Low-*k* Dielectric Processing Parameters

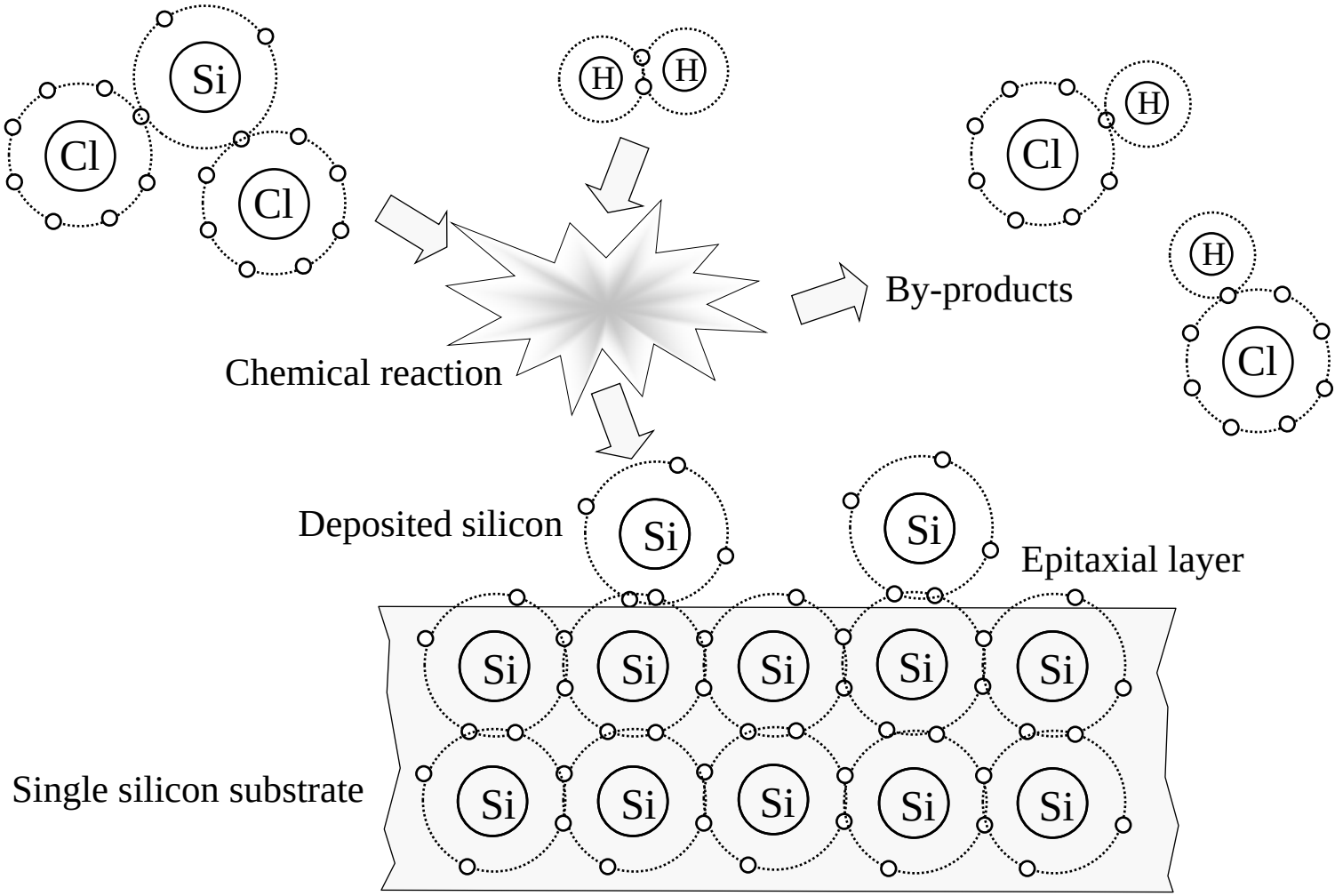
Major Operation	Process Step	Parameter
Spin coating	Apply bowl speed	50 rpm
	Maximum bowl speed	800 – 1500 rpm
	Backside rinse	800 rpm, 5 sec
	Topside edge bead removal	1000 rpm, 10 sec
	Spin Dry	1000 rpm, 5 sec
Cure	Initial soft-bake cure	200°C, 60 sec, N_2 purge
	In-line cure	475°C, 60 sec, N_2 ambient

Table 11.6

Epitaxy

- Epitaxy Growth Model
- Epitaxy Growth Methods
  - Vapor-Phase Epitaxy (VPE)
  - Metalorganic CVD (MOCVD) (for GaAs compound)
  - Molecular-Beam Epitaxy (MBE) (GaAs, using e-beam to evaporation under high vacuum)

Silicon Epitaxial Growth on a Silicon Wafer



1. Use for raised S/D to reduce contact resistance
2. When lightly doped epilayer on heavily doped: we have autodoping evaporate from the wafer, or out-diffusion from heavily doped
3. Si-epi on Si: homoepitaxy, Si-epi on Al2O3 (SOI): heteroepitaxy

Figure 11.28

Illustration of Vapor Phase Epitaxy (high T, mass-transport-limit)

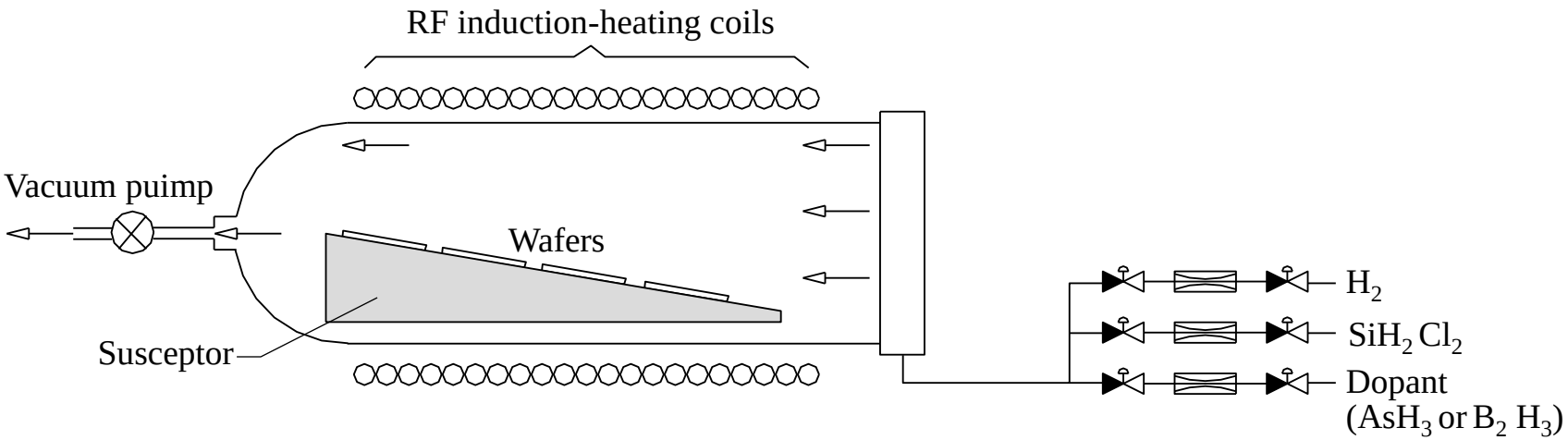


Figure 11.29

Silicon Vapor Phase Epitaxy Reactors

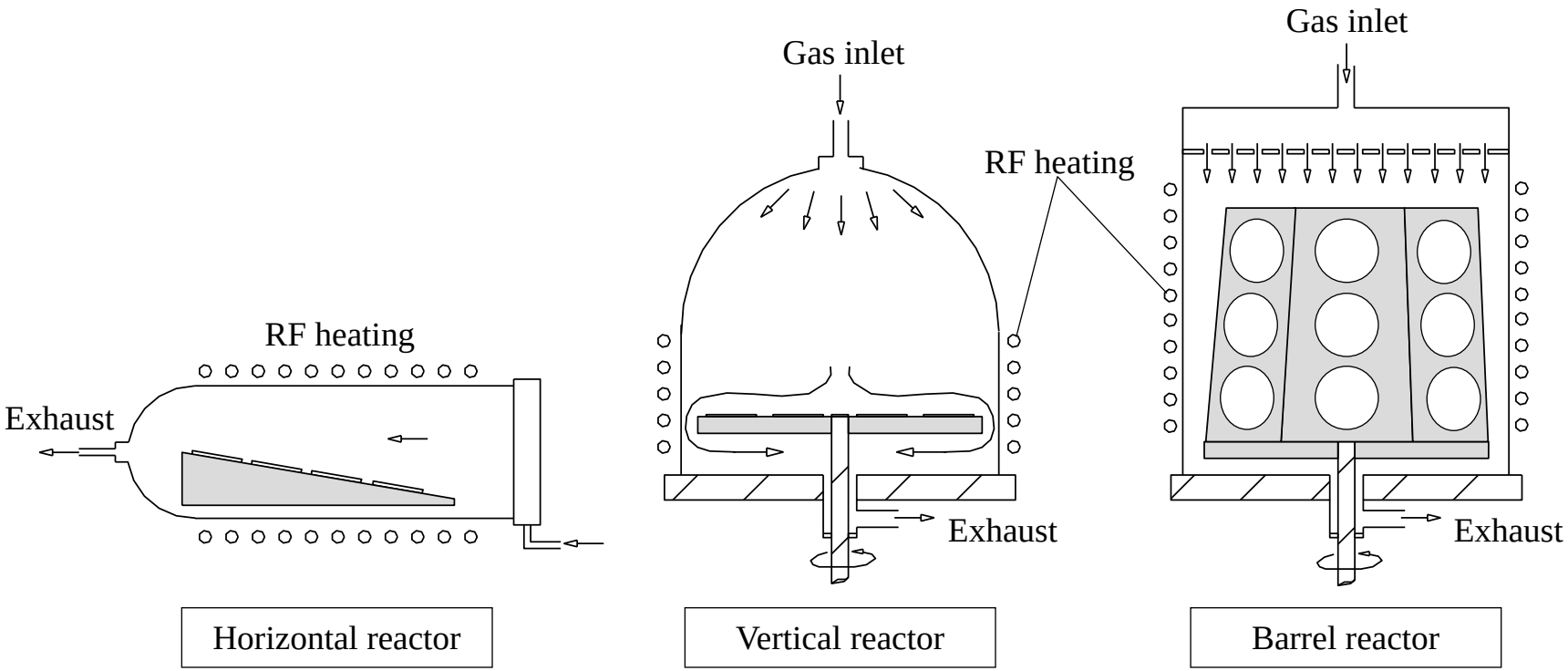


Figure 11.30

Effects of Keyholes in ILD on Metal Step Coverage

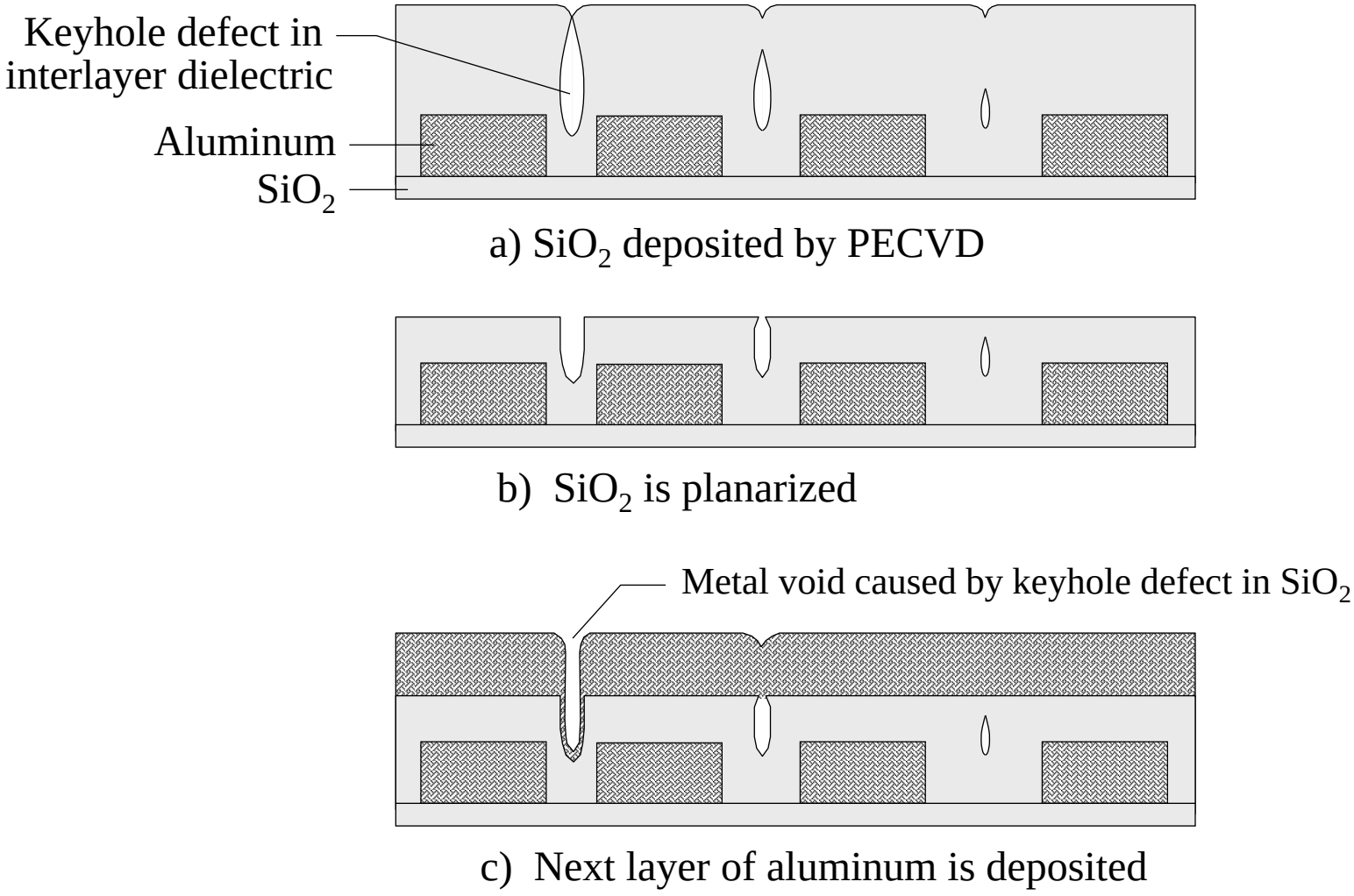
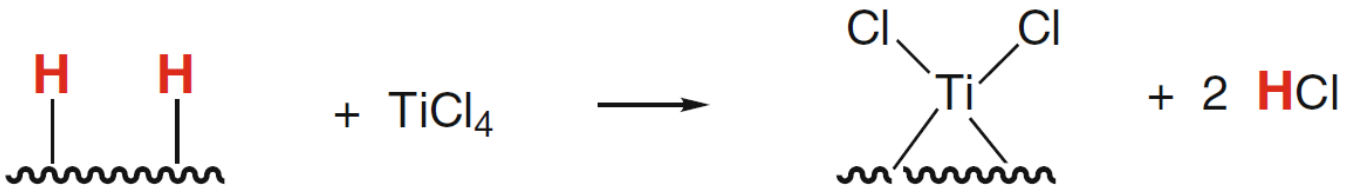


Figure 11.31

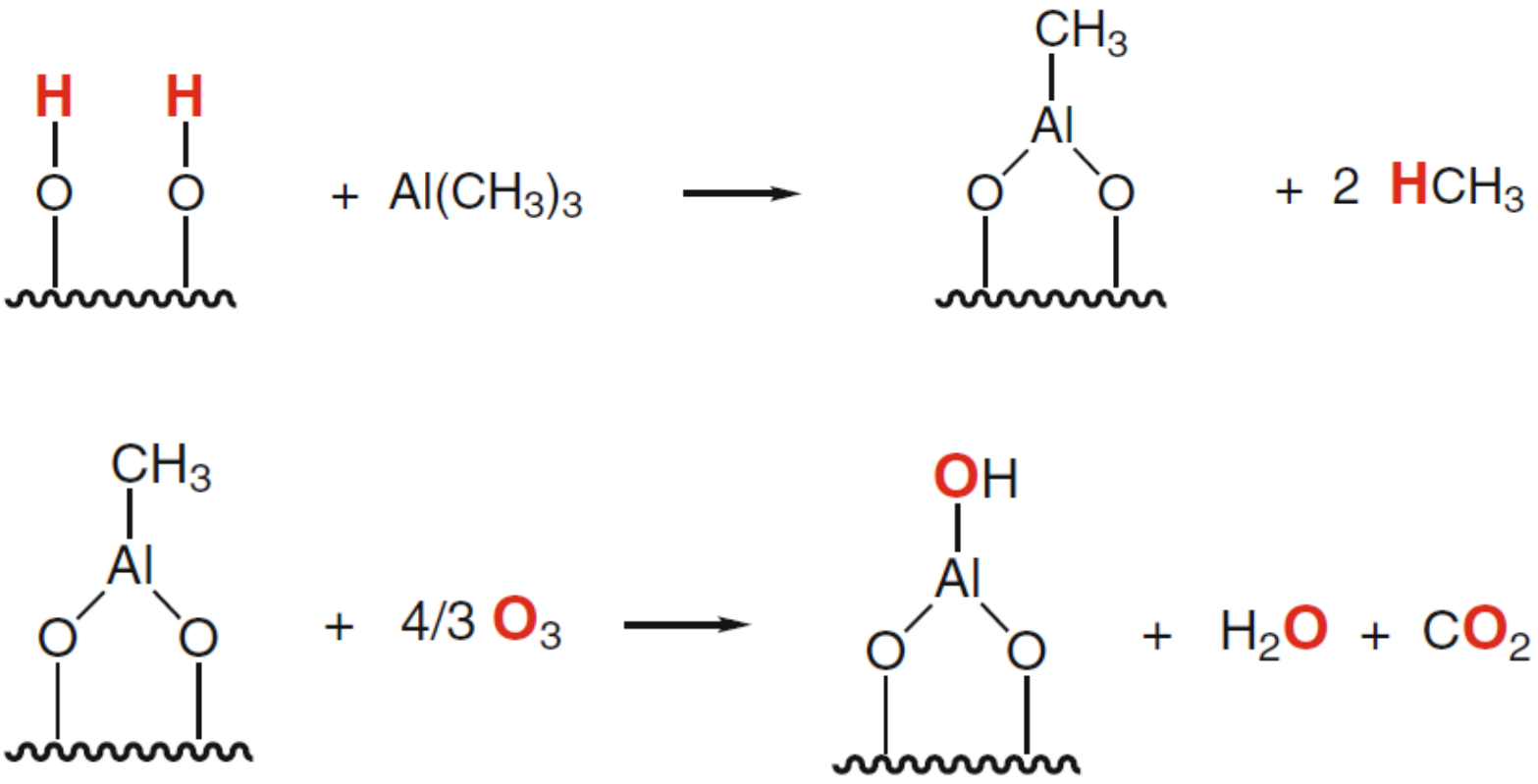
Atomic Layer CVD

Remote hydrogen plasma has been used to deposit very reactive metals, such as titanium and tantalum from their chlorides. Assuming that the plasma has already provided hydrogen atoms to the surface, the next reaction step would be the following:



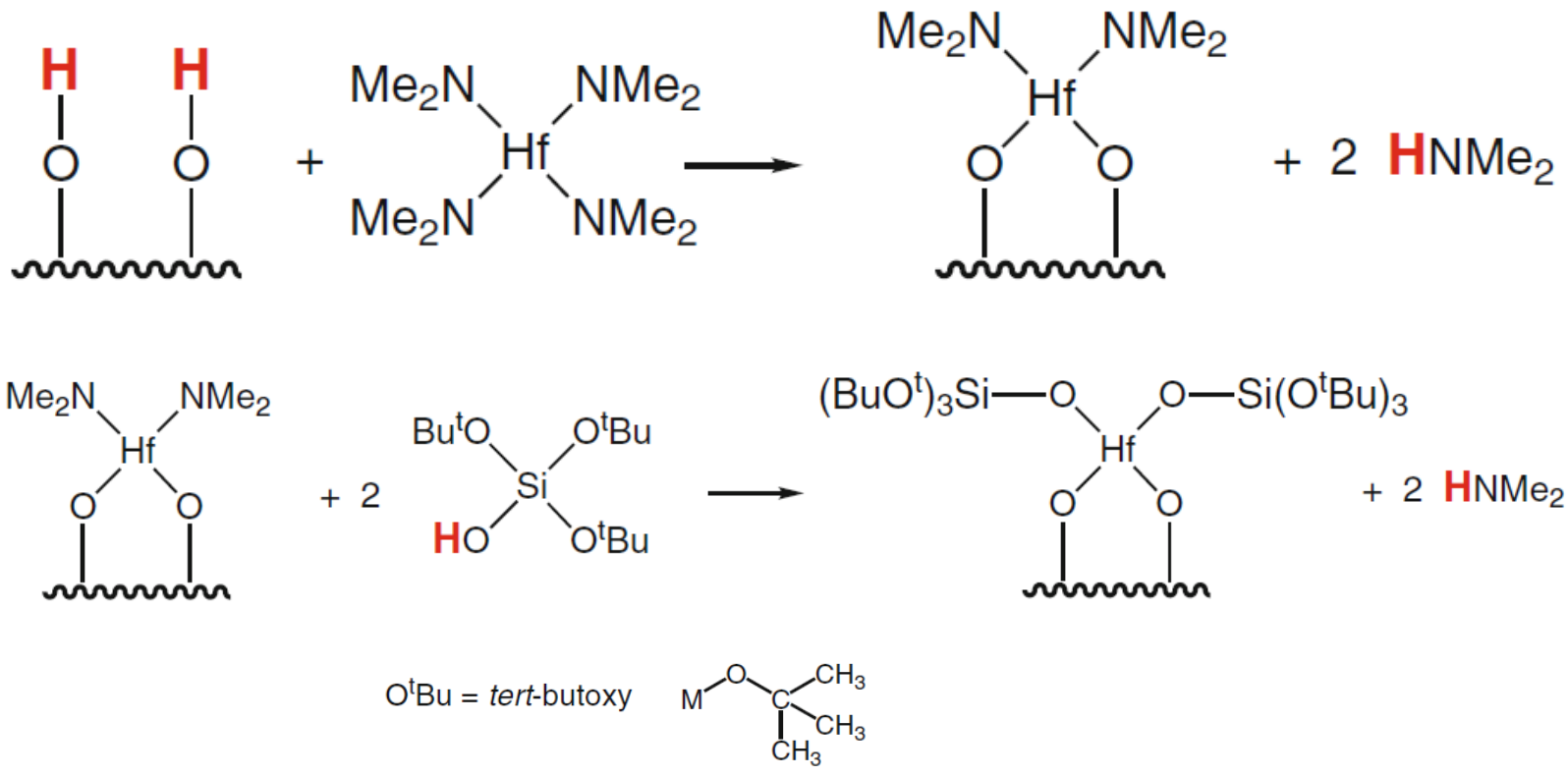
The surface is now returned to the state in which it is ready for the first reaction to begin the ALD cycle again.

Al_2O_3 Atomic Layer CVD



The surface is now returned to the state in which it is ready for the first reaction to begin the ALD cycle again.

HfSiO ALD


H H
O O
+
Me2N NMe2
Hf
Me2N NMe2
Me2N NMe2
Hf
O O
+ 2 HNMe2
Me2N NMe2
Hf
O O
+ 2
ButO OtBu
Si
HO OtBu
(BuOt)3Si—O O—Si(OtBu)3
Hf
O O
+ 2 HNMe2
OtBu = tert-butoxy
M O C CH3 CH3 CH3
(BuOt)3Si—O O—Si(OtBu)3
Hf
O O
(HO)3Si—O O—Si(OH)3
Hf
O O
+ 6
H2C=C CH3 CH3

HfO_2 ALD CVD

$$Hf(NMe_2)_4 + 2H_2O => HfO_2 + 4\ HNMe_2$$

Me: methyl