# Semiconductor Manufacturing Technology

## Chapter 1

## Introduction to the Semiconductor Industry

# Objectives

After studying the material in this chapter, you will be able to:

1. Describe the current economic state and the technical roots of the semiconductor industry.
2. Explain what is an integrated circuit (IC) and list the five circuit integration eras.
3. Describe a wafer, including how it is layered and describe the essential aspects of the five stages of wafer fabrication.
4. State and discuss the three major trends associated with improvement in wafer fabrication.
5. Explain what is a critical dimension (CD) and how Moore's law predicts future wafer fabrication improvement.
6. Describe the different eras of electronics since the invention of the transistor up to modern wafer fabrication.
7. Discuss different career paths in the semiconductor industry.

# Microprocessor Chips

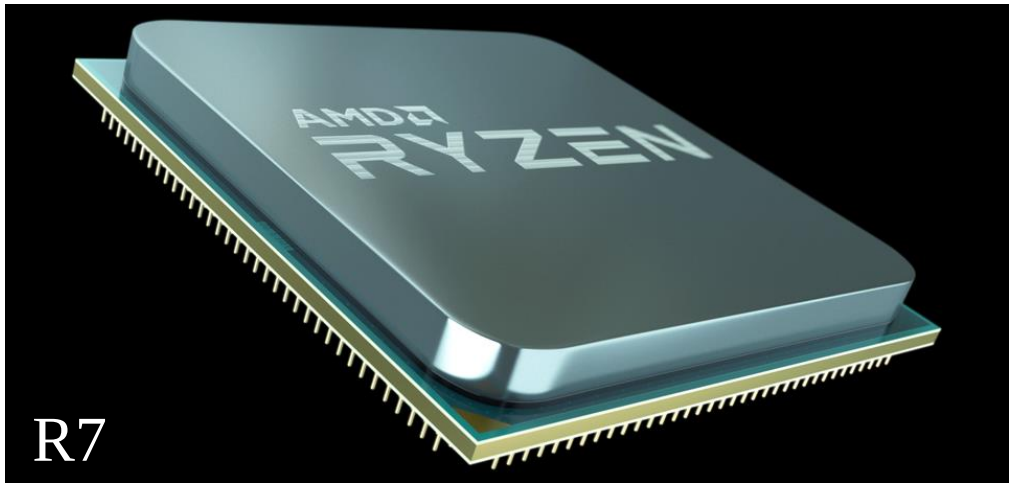



Photo courtesy of
Advanced Micro Devices


US$ 499

Photo courtesy of
Intel Corporation

Wafer: round thin crystalline disk
Wafer fab: fabrication factories
Chip account for 30%-40% of cost PC

Photo 1.1

# Development of an Industry

- Industry Roots
  - Vacuum Tubes (1906)
  - Radio Communications (silicon, 1900s)
  - Mechanical Tabulators ( movie, The Imitation Game, 2015)
  - Inventors (computer, 50 tons, 3000 $ft^2$, 19000 vacuum tubes)
  - Disadvantages (large, unreliable, more power)
- The Solid State
  - Solid State Physics (Ge)
  - The First Transistor (1947, Bell Lab.)
  - Benefits (small size, no vacuum, reliable, less power)

# The Imitation Game

Turing's machine

# Vacuum Tubes



Photo 1.2

# 《歲月憶往》交大第一部電腦


http://blog.cnyes.com/My/jmtaiwan3952/Article2573591

- 1957, 台糖 [右圖]
- 1962, IBM650 [交大]
- 台灣找不到氣墊車, 只好…找牛車
- 真空管及鍺二極體 組成
- Memory為2000字節的磁鼓(Drum)
- 220V, 100Amp
- 嚴家淦副總統前來主持剪綵
- 冷氣尚未裝好, 開機40分鐘, 換 400個二極鍺晶體，又再換了300多個真空管…沒法恢復正常運作

# The Semiconductor Industry

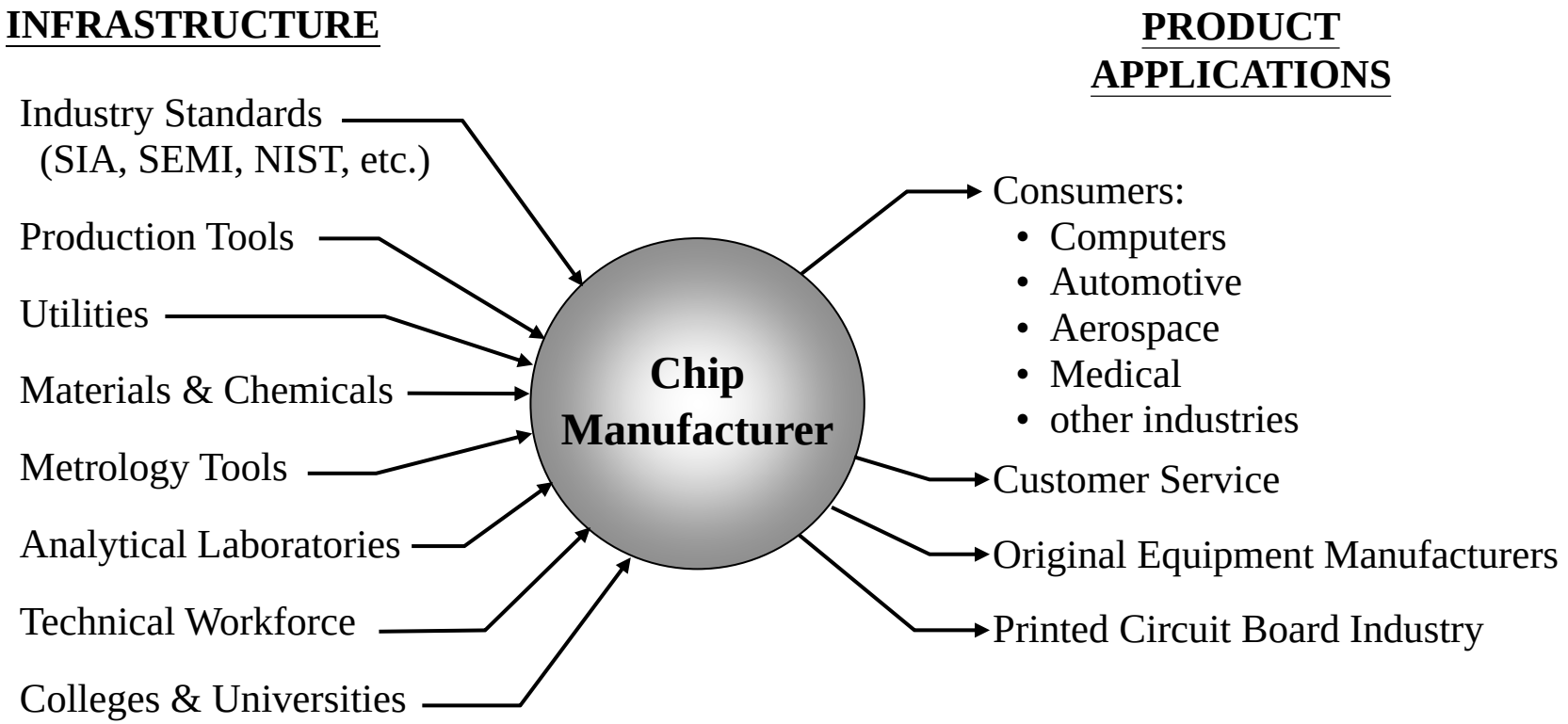



Figure 1.1

# The First Transistor from Bell Labs (1947)

- Made from poly-Ge.
- Output power > input power
- 1956: Nobel Prize
- Ge-based transistor quickly replaced vacuum tubes because of their smaller size, lower power, quicker response time

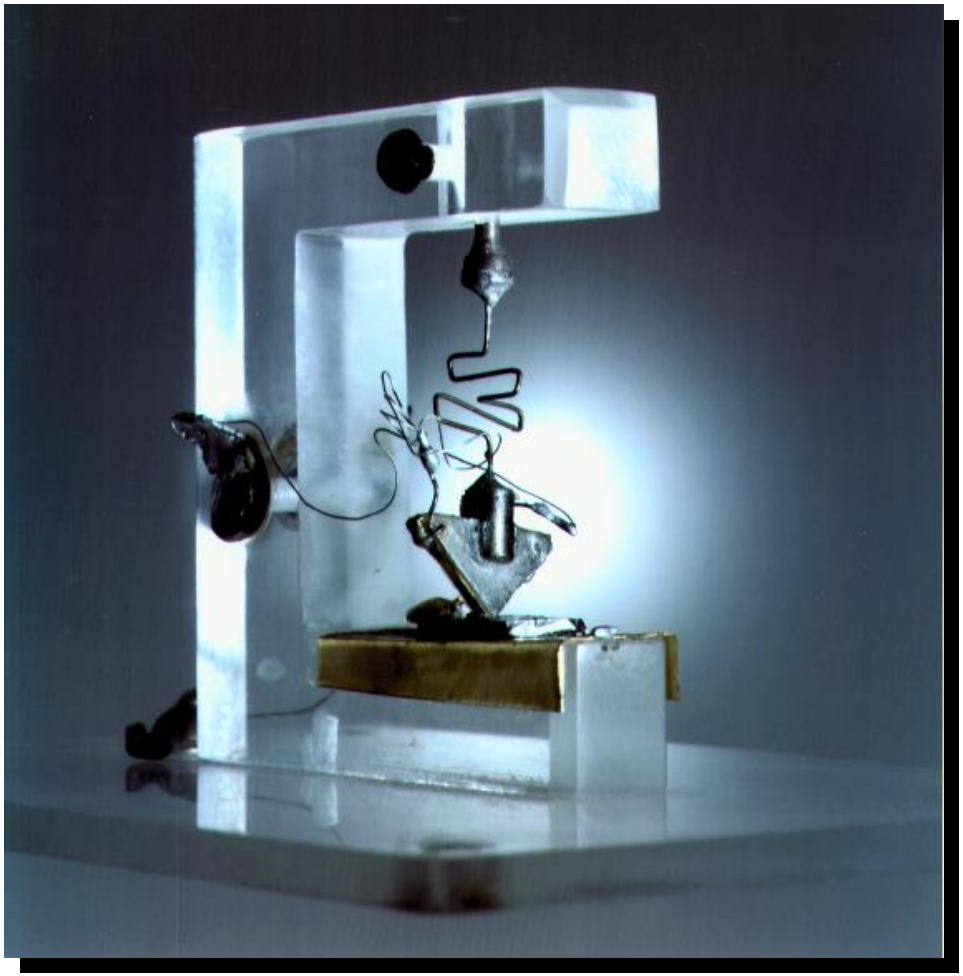


Photo courtesy of Lucent Technologies Bell Labs Innovations

Photo 1.3

# Circuit Integration: on the silicon surface: transistor, diodes, resistors, inductor and capacitors

- Integrated Circuits (IC)
  - Microchips, chips
  - Inventors : Noyce (Fairchild) and Kilby (TI) 1959
  - Benefits of IC: cost effective, reliable, and more complex circuits can be made
- Integration Eras
  - From SSI to ULSI
  - 1960 - 2000

# Jack Kilby's First Integrated Circuit

The devices were connected with individual wires.

- A discrete device is an electronic device, such as a resistor, capacitor, diode, or transistor, that contains only one device per piece
- Kilby: it would be possible make discrete devices on the same piece of semiconductor (Ge).
- In this photo, it contains Transistor: 1, Resistor: 3, C:1

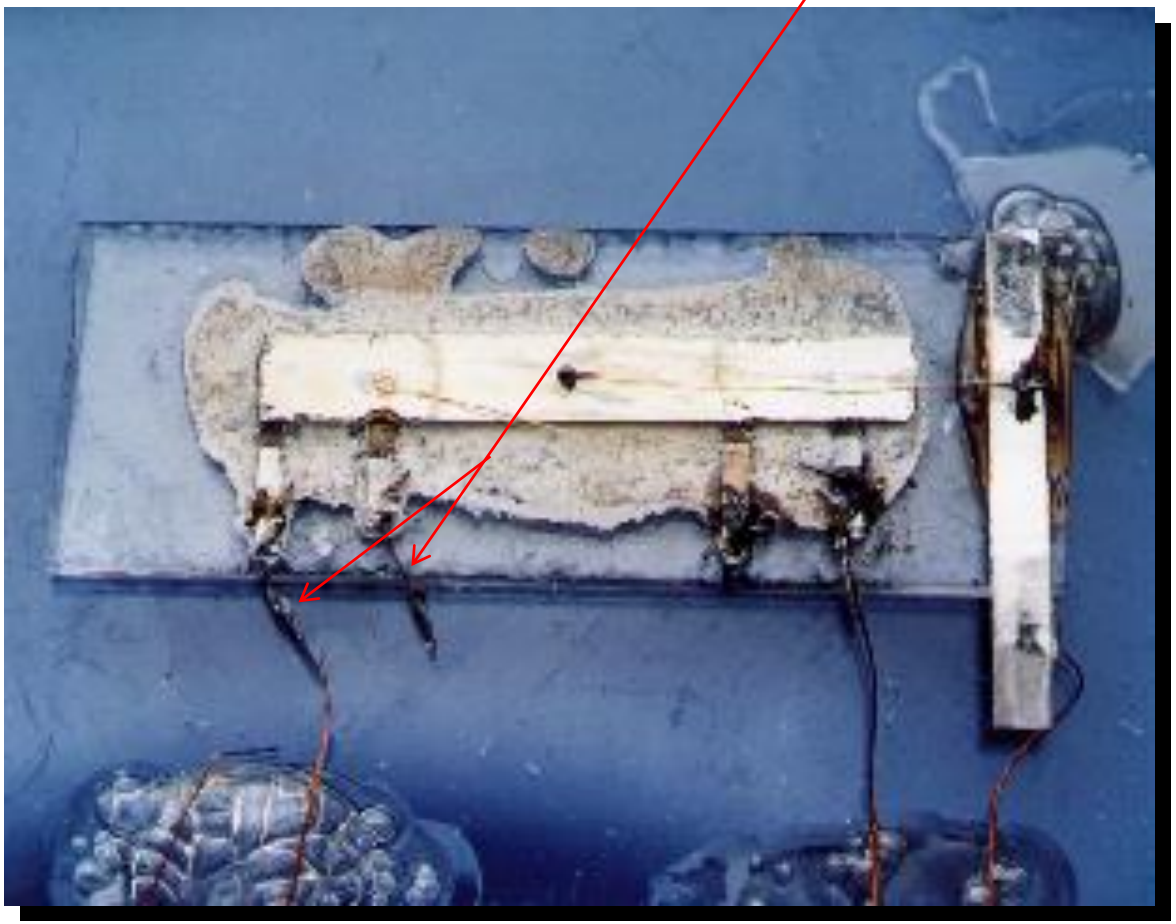
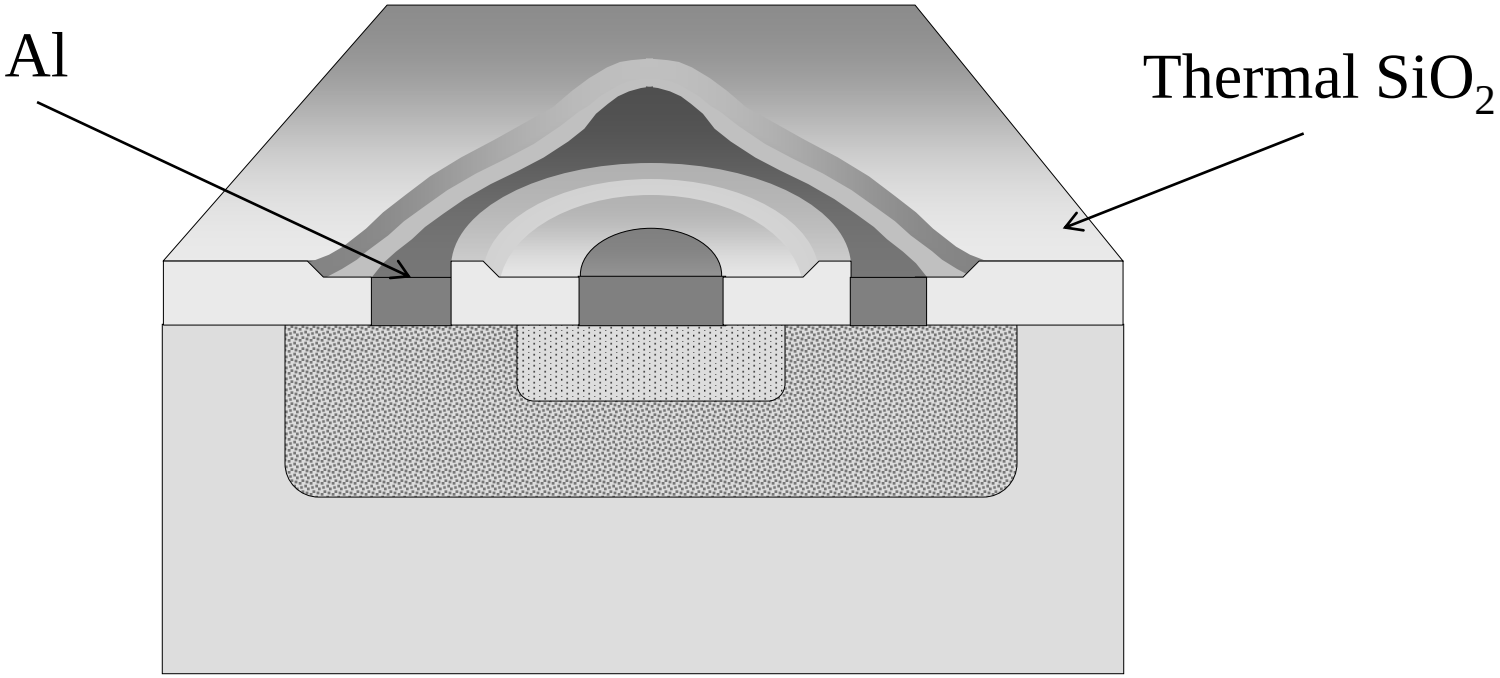


Photo courtesy of Texas Instruments, Inc.

Photo 1.4

# The First Planar Transistor (1957, Fairchild)

Planar Technology

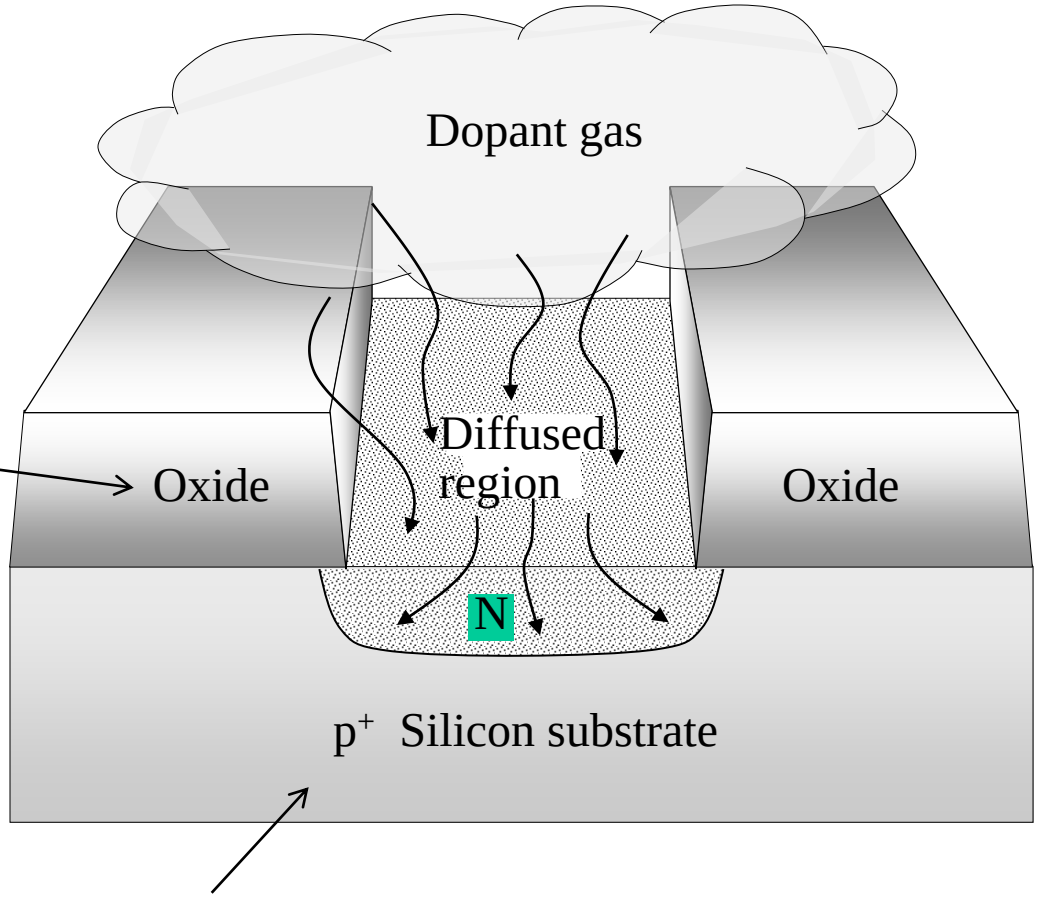



Transistor: transconductance and varistor

Figure 1.2

# Doped Region in a Silicon Wafer

The most important discovery




The most important invention

# First Silicon IC Chip Made by Robert Noyce of Fairchild Camera in 1961

- At the same time, the same idea: make more for less
- Using aluminum thin film on silicon
- Using grown oxide to isolate: planar technology
- In this photo: 4-transistor, sold for $150 (Customer: NASA)
- It has the basic process techniques of modern IC chips.
- Noyce, Grove, and Moore cofounded the Intel in 1968.

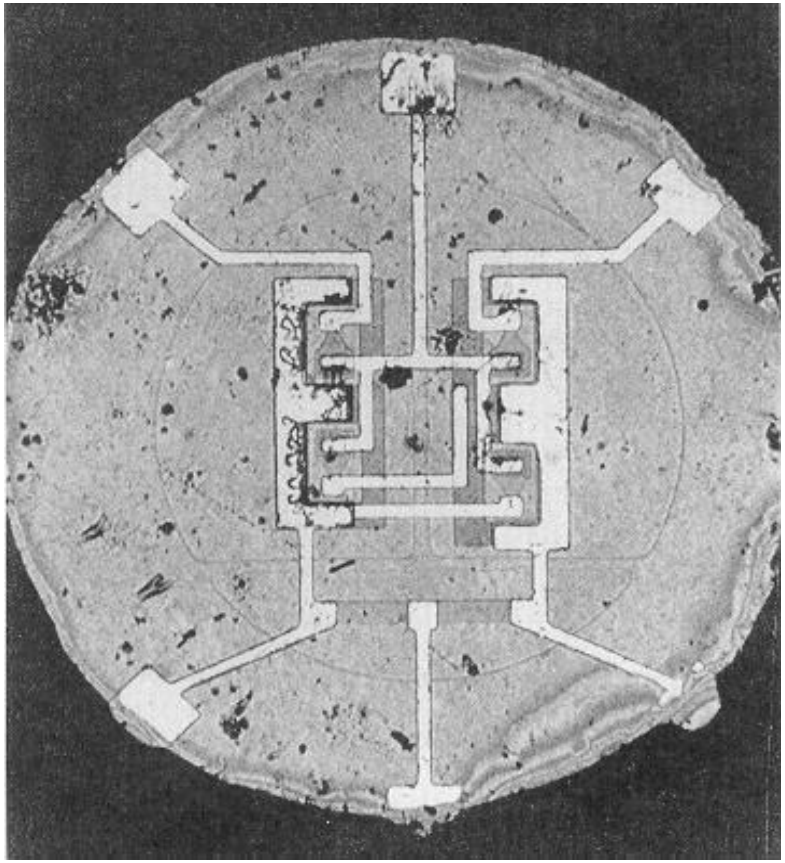
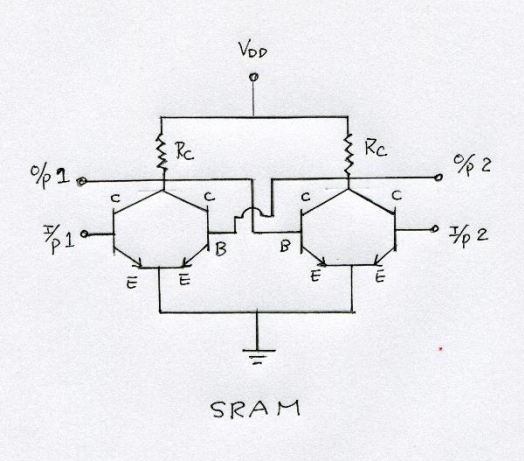
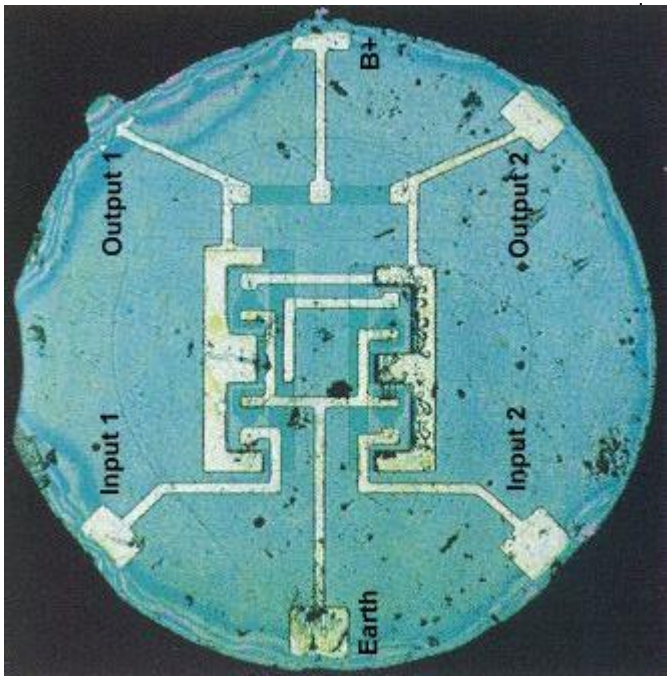


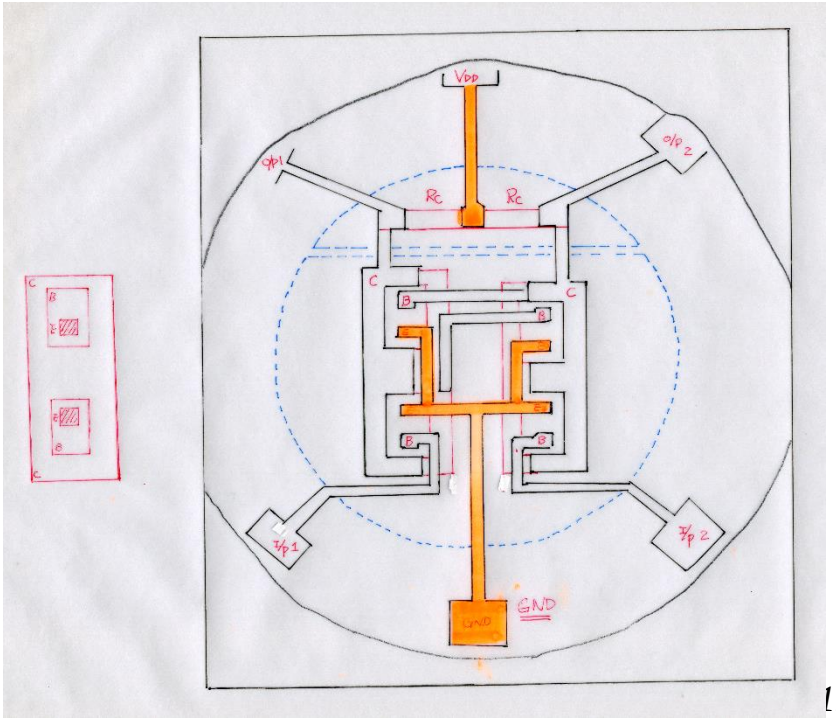
Photo courtesy: Fairchild Semiconductor International

0.4 inch

# SRAM


VDD
Rc
Rc
o/p 1
o/p 2
C
C
C
C
I/p 1
I/p 2
B
B
E
E
E
E
SRAM


B+
Output 1
Output 2
Input 1
Input 2
Earth


VDD
o/p1
o/p 2
Rc
Rc
C
C
B
B
B
B
I/p 1
I/p 2
GND

# Top View of Wafer with Chips

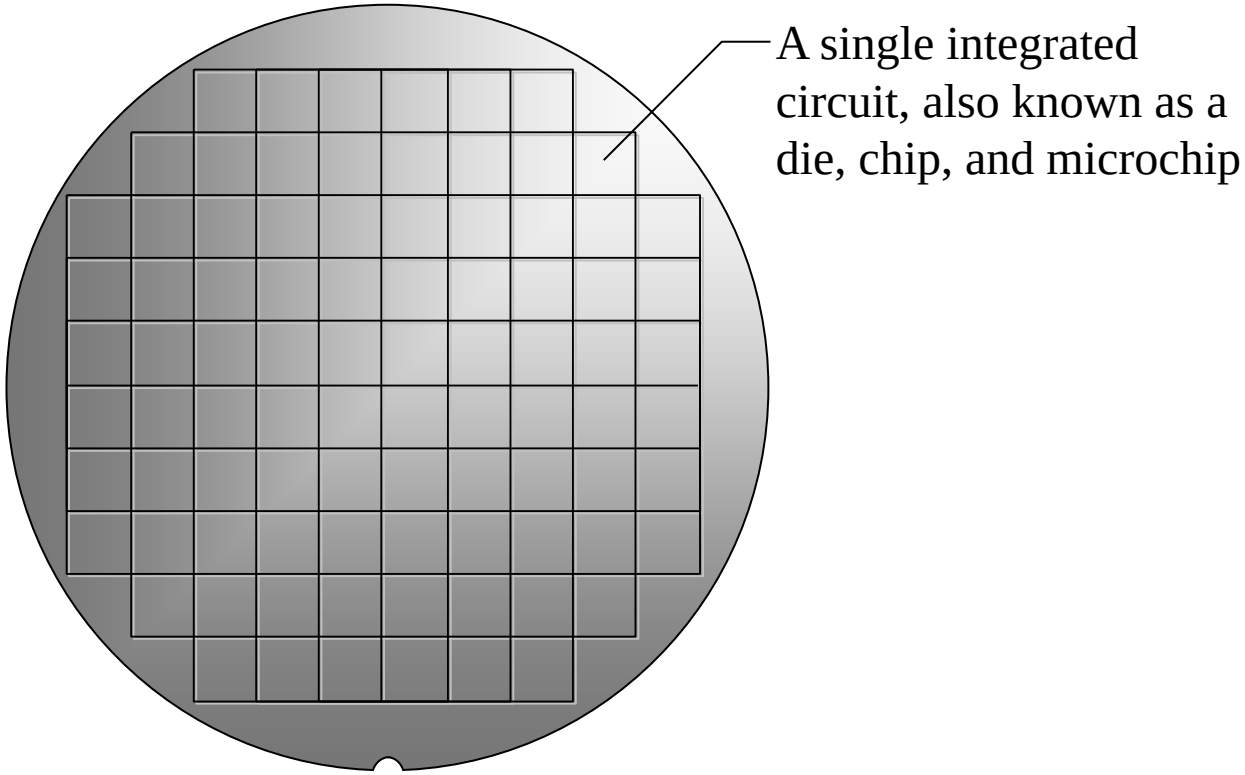



Figure 1.3

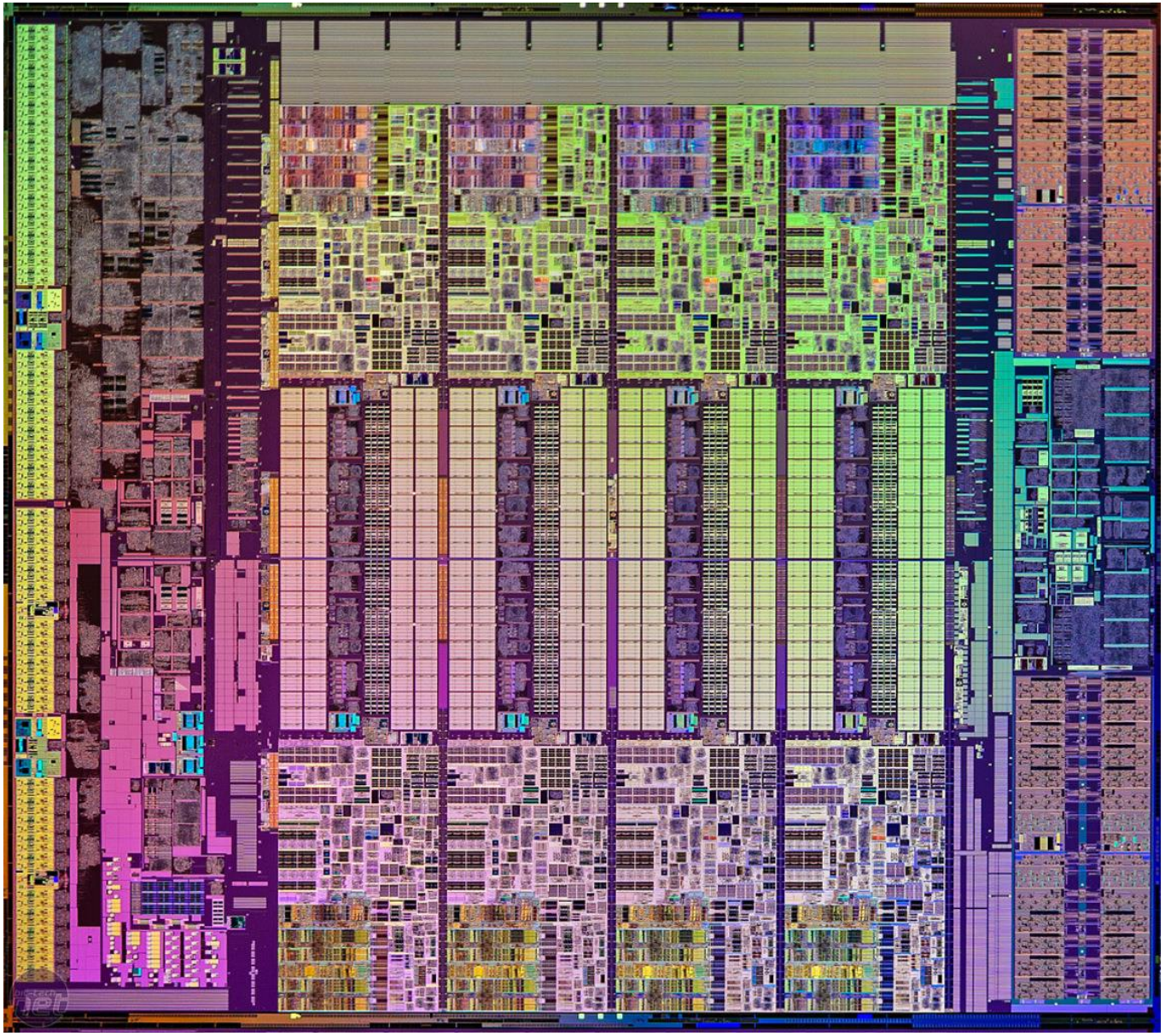
# Circuit Integration of Semiconductors

| Circuit Integration | Semiconductor Industry Time Period | Number of Components per Chip |
|---|---|---|
| No integration (discrete components) | Prior to 1960 | 1 |
| Small scale integration (SSI) | Early 1960s | 2 to 50 |
| Medium scale integration (MSI) | 1960s to Early 1970s | 50 to 5,000 |
| Large scale integration (LSI) | Early 1970s to Late 1970s | 5,000 to 100,000 |
| Very large scale integration (VLSI) | Late 1970s to Late 1980s | 100,000 to 1,000,000 |
| Ultra large scale integration (ULSI) | 1990s to present | > 1,000,000 |

The key to market success is the ability to deliver the right product at the right time.

Table 1.1

# ULSI Chip



# Advanced CPU


| | |
|---|---|
| **Series** | Intel Core i7 |
| **Codename** | Haswell |
| **Clock Rate** | 3100 - 4000 MHz |
| **Level 1 Cache** | 256 KB |
| **Level 2 Cache** | 1024 KB |
| **Level 3 Cache** | 8192 KB |
| **Number of Cores / Threads** | 4 / 8 |
| **Max. Power Consumption (TDP = Thermal Design Power)** | 57 Watt |
| **Transistor Count** | 1400 Million |
| **Manufacturing Technology** | 22 nm |
| **Die Size** | 177 mm2 |
| **Max. Temperature** | 100 °C |

2020

5.1 GHz

16 MB

8

35/45

$450.

# IC Fabrication

- Silicon
  - Wafer
  - Wafer Sizes (increase to reduce cost)
  - Devices and Layers
- Wafer Fab (clean room to reduce contaminations)
- Stages of IC Fabrication
  - Wafer preparation
  - Wafer fabrication
  - Wafer test/sort
  - Assembly and packaging
  - Final test

# Evolution of Wafer Size

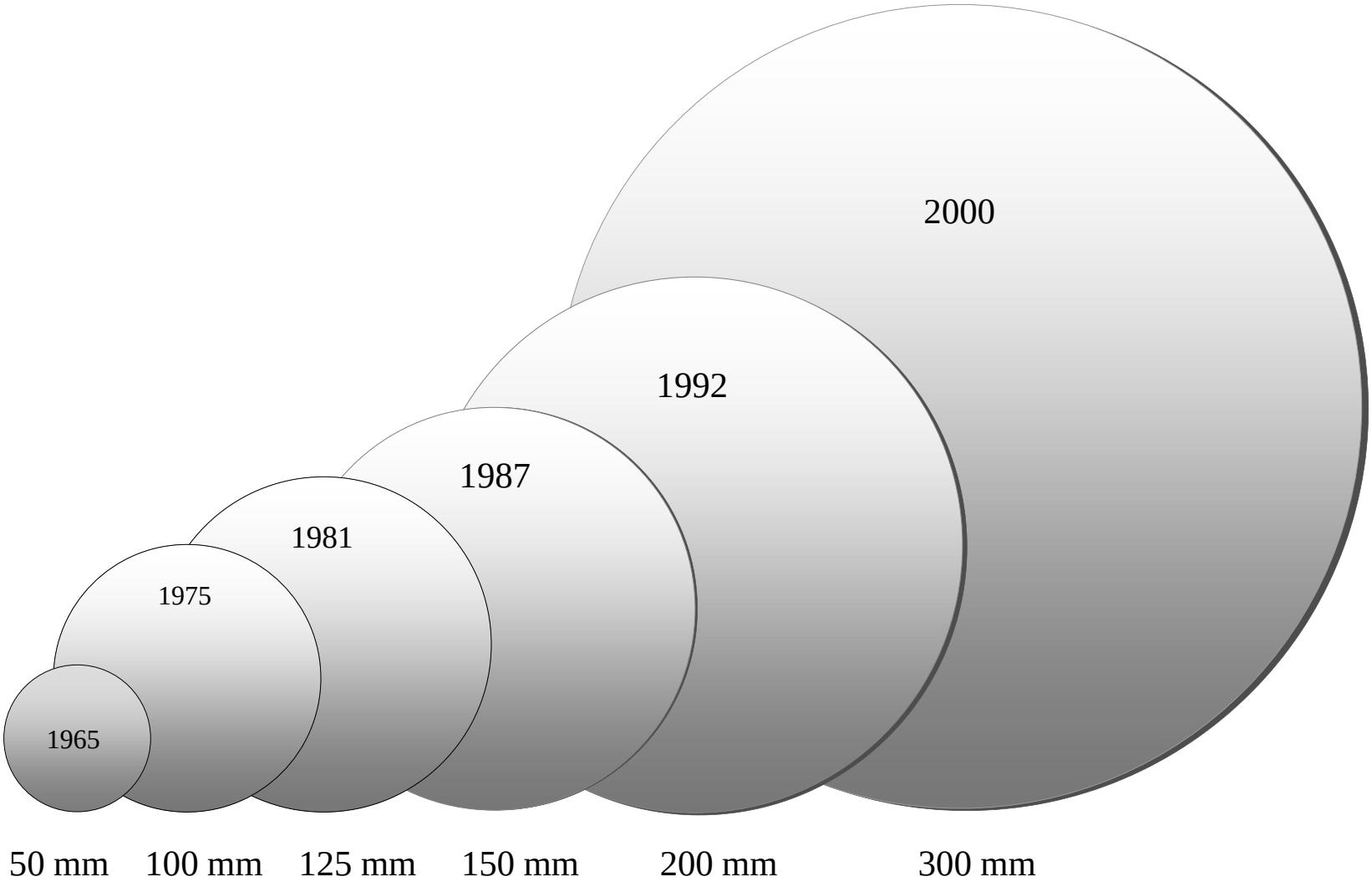
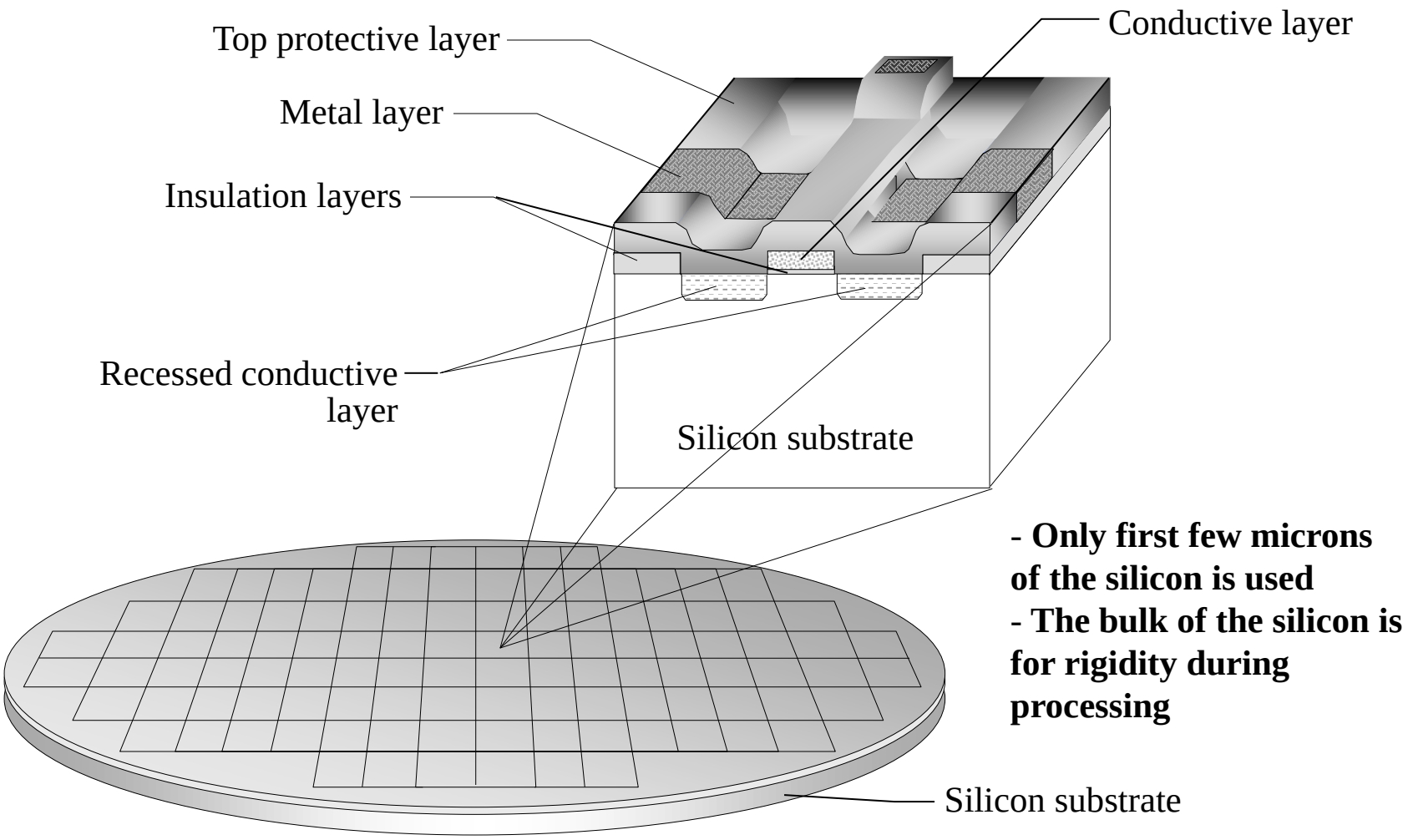



Figure 1.4

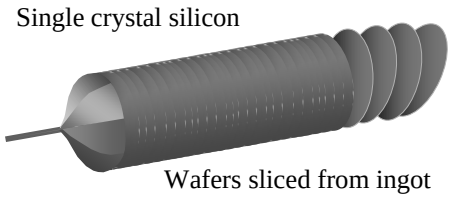
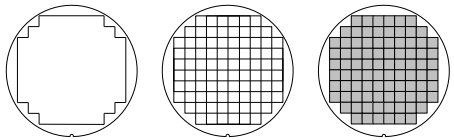
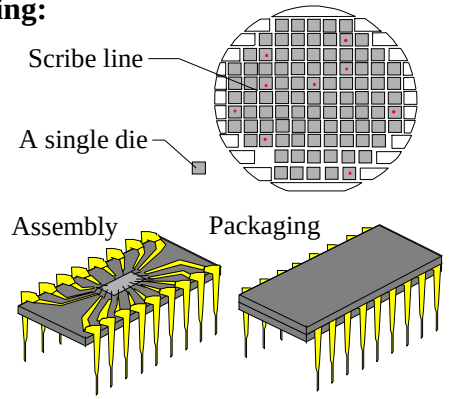
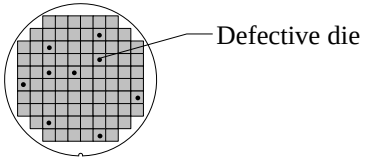
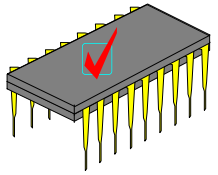
# **Devices** and **Layers** from a Silicon Chip




**- Only first few microns of the silicon is used**
**- The bulk of the silicon is for rigidity during processing**

Figure 1.5

# 5 Stages of IC Fabrication

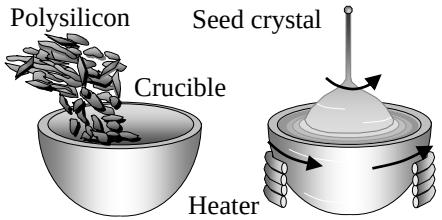
| | | | | |
|---|---|---|---|---|
| 1. | **Wafer Preparation** includes crystal growing, rounding, slicing and polishing. |  | 4. | **Assembly and Packaging:**<br>The wafer is cut along scribe lines to separate each die.<br>Metal connections are made and the chip is encapsulated. |
| 2. | **Wafer Fabrication** includes cleaning, layering, patterning, etching and doping. |  | |  |
| 3. | **Test/Sort** includes probing, testing and sorting of each die on the wafer. |  | 5. | **Final Test** ensures IC passes electrical and environmental testing.  |

These five stages are interdependent

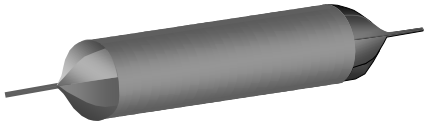
Figure 1.6

# Preparation of Silicon Wafers

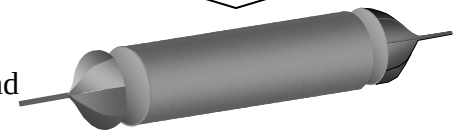
1. Crystal Growth



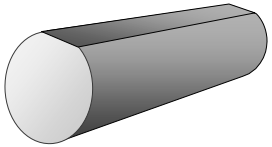

2. Single Crystal Ingot



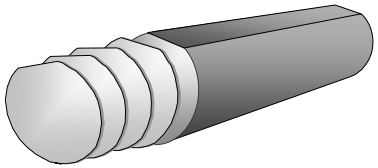
3. Crystal Trimming and Diameter Grind



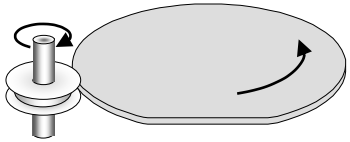
4. Flat Grinding



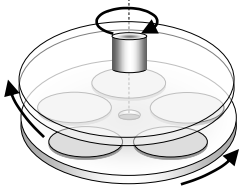
5. Wafer Slicing



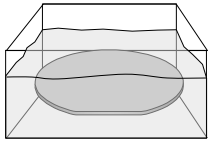
6. Edge Rounding



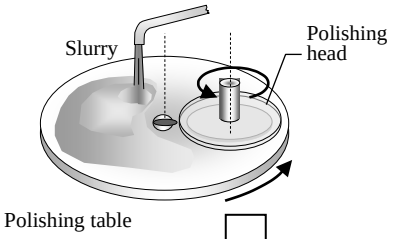
7. Lapping



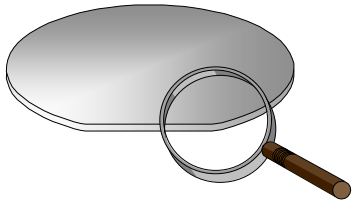
8. Wafer Etching



9. Polishong




10. Wafer Inspection



(*Note:* Terms in Figure 1.7 are explained in Chapter 4.)

Figure 1.7

# IC Chip Manufacturing Involves:

- Materials: ultra-high pure gases, liquids, which are poisonous, flammable, explosive, or corrosive…
- Processing equipment: specialized tools, such as CVD, etch, PVD, implanter, furnace…, which are sophisticated and expensive. Hence, reduce downtime and high throughput are important
- Batch or single-wafer, multi-chamber cluster tools are popular

# Wafer Fab

**Fabless company**: design house
**Foundry**: produce chips only for other company


Photo courtesy of Advanced Micro Devices-Dresden, © S. Doering

Photo 1.6

# Sample of Microchip Packaging

Wafer Test/Sort first before package

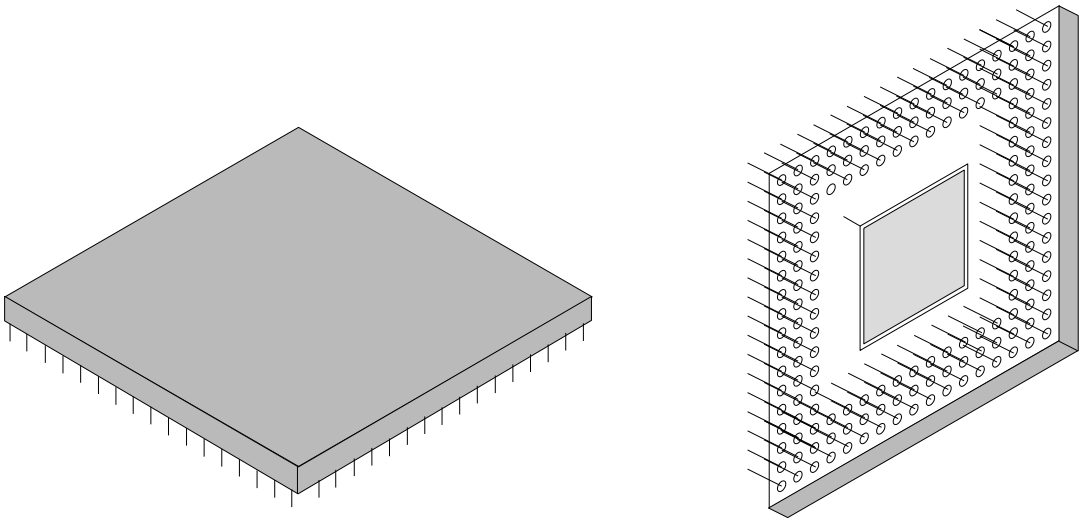
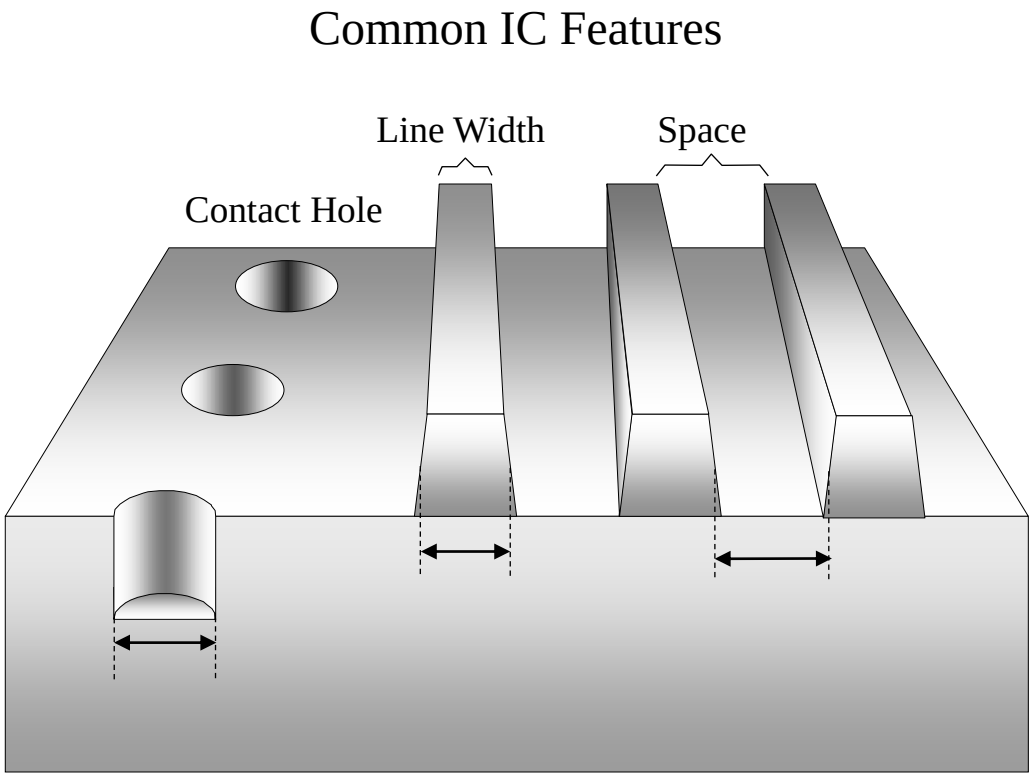


Figure 1.8

# Semiconductor Three Trends

- Increase in Chip Performance
  - Critical Dimension (CD)
  - Components per Chip
  - Moore's Law
  - Power Consumption
- Increase in Chip Reliability
- Reduction in Chip Price

# Critical Dimension




The physical dimension: feature size
Minimum feature size called critical dimension, CD

Figure 1.9

# Past and Future Technology Nodes for Device Critical Dimension (CD)

| | **1988** | **1992** | **1995** | **1997** | **1999** | **2001** | **2002** | **2005** |
|---|---|---|---|---|---|---|---|---|
| **CD (μm)** | 1.0 | 0.5 | 0.35 | 0.25 | 0.18 | 0.15 | 0.13 | 0.10 |

1. Shrinking of device dimension on the chip : **scaling**.
2. Reducing CD permits more components on the wafer.
3. 1950: 125 μm.

Table 1.2

# Introduction

*Table PIDS2a High-performance (HP) Logic Technology Requirements - TCAD*

| *Year of Production* | *2013* | *2014* | *2015* | *2016* | *2017* | *2018* | *2019* | *2020* |
|---|---|---|---|---|---|---|---|---|
| *Logic Industry "Node Range" Labeling (nm) [based on 0.71x reduction per "Node Range" ("Node" = ~2x Mx)* | **"16/14"** | | **"11/10"** | | **"8/7"** | | **"6/5"** | |
| *MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (contacted)* | **40** | **32** | **32** | **28.3** | **25.3** | **22.5** | **20.0** | **17.9** |
| *$L_g$: Physical Gate Length for HP Logic (nm)* | **20** | **18** | **16.7** | **15.2** | **13.9** | **12.7** | **11.6** | **10.6** |
| *$L_{ch}$: Effective Channel Length (nm) [3]* | **16.0** | **14.4** | **13.4** | **12.2** | **11.1** | **10.2** | **9.3** | **8.5** |
| *$V_{dd}$: Power Supply Voltage (V)* | | | | | | | | |
| Bulk/SOI/MG | **0.86** | **0.85** | **0.83** | **0.81** | **0.80** | **0.78** | **0.77** | **0.75** |
| *EOT: Equivalent Oxide Thickness* | | | | | | | | |
| Bulk/SOI/MG (nm) | **0.80** | **0.77** | **0.73** | **0.70** | **0.67** | **0.64** | **0.61** | **0.59** |
| Dielectric constant (K) of gate dielectrics | **12.5** | **13.0** | **13.5** | **14.0** | **14.5** | **15.0** | **15.5** | **16.0** |
| Physical gate oxide thickness (nm) | **2.56** | **2.57** | **2.53** | **2.51** | **2.49** | **2.46** | **2.42** | **2.42** |
| *Channel Doping ($10^{18}/cm^3$) [4]* | | | | | | | | |
| Bulk | **6.0** | **7.0** | **7.7** | **8.4** | **9.0** | | | |
| SOI/MG | **0.1** | **0.1** | **0.1** | **0.1** | **0.1** | **0.1** | **0.1** | **0.1** |
| *Body Thickness (nm) [5]* | | | | | | | | |
| SOI | | | | | | | | |
| MG | **6.4** | **5.8** | **5.3** | **4.9** | **4.4** | **4.1** | **3.7** | **3.4** |

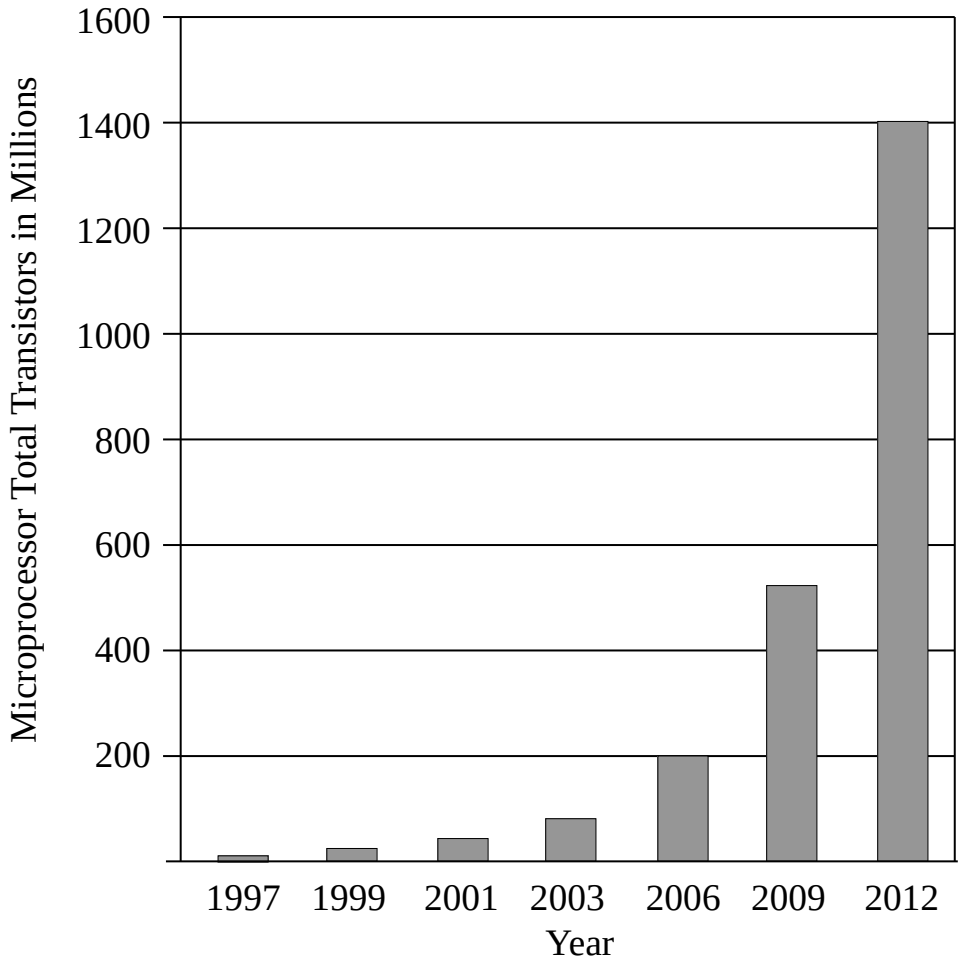
Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known | Manufacturable solutions are NOT known

*ITRS Reports .2013 edition*

Challenge for planar CMOS scaling → Short channel effect (SCE), Leakage currents, Gate Controllability…….

# Increase in Total Transistors/Chip




Redrawn from Semiconductor Industry Association, *The National Technology Roadmap for Semiconductors*, 1997.

Figure 1.10

# Moore's Law for Microprocessors

The number of transistors on a chip double every 18 months.

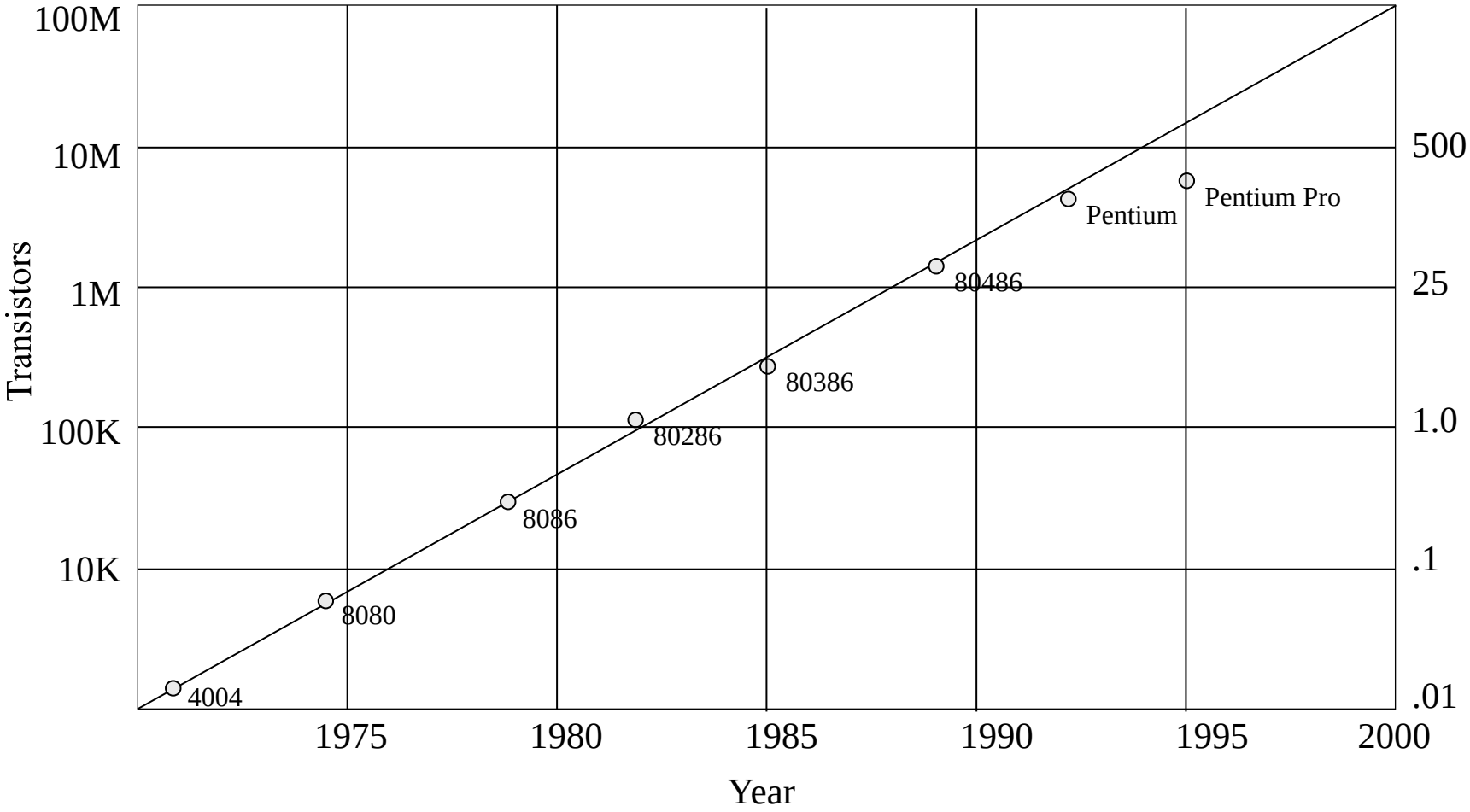


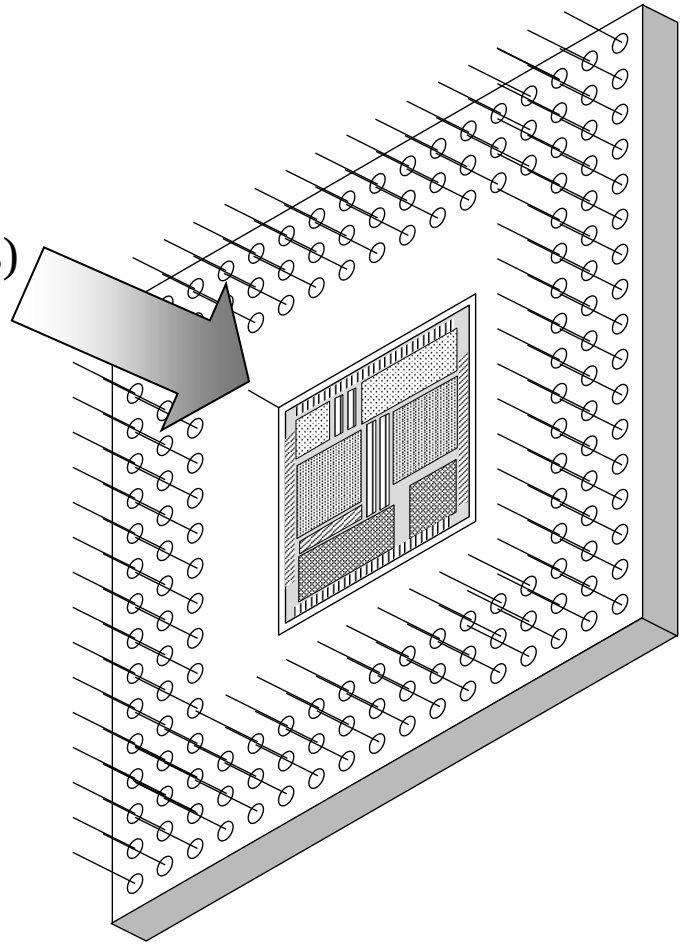



Figure 1.11

# Size Comparison of Early and Modern Semiconductors

1990s Microchip
(5~25 million transistors)

U.S. coin, 10 cents



1960s Transistor

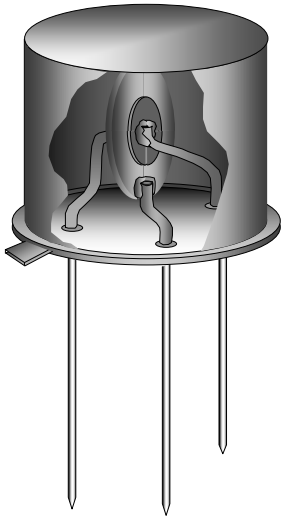
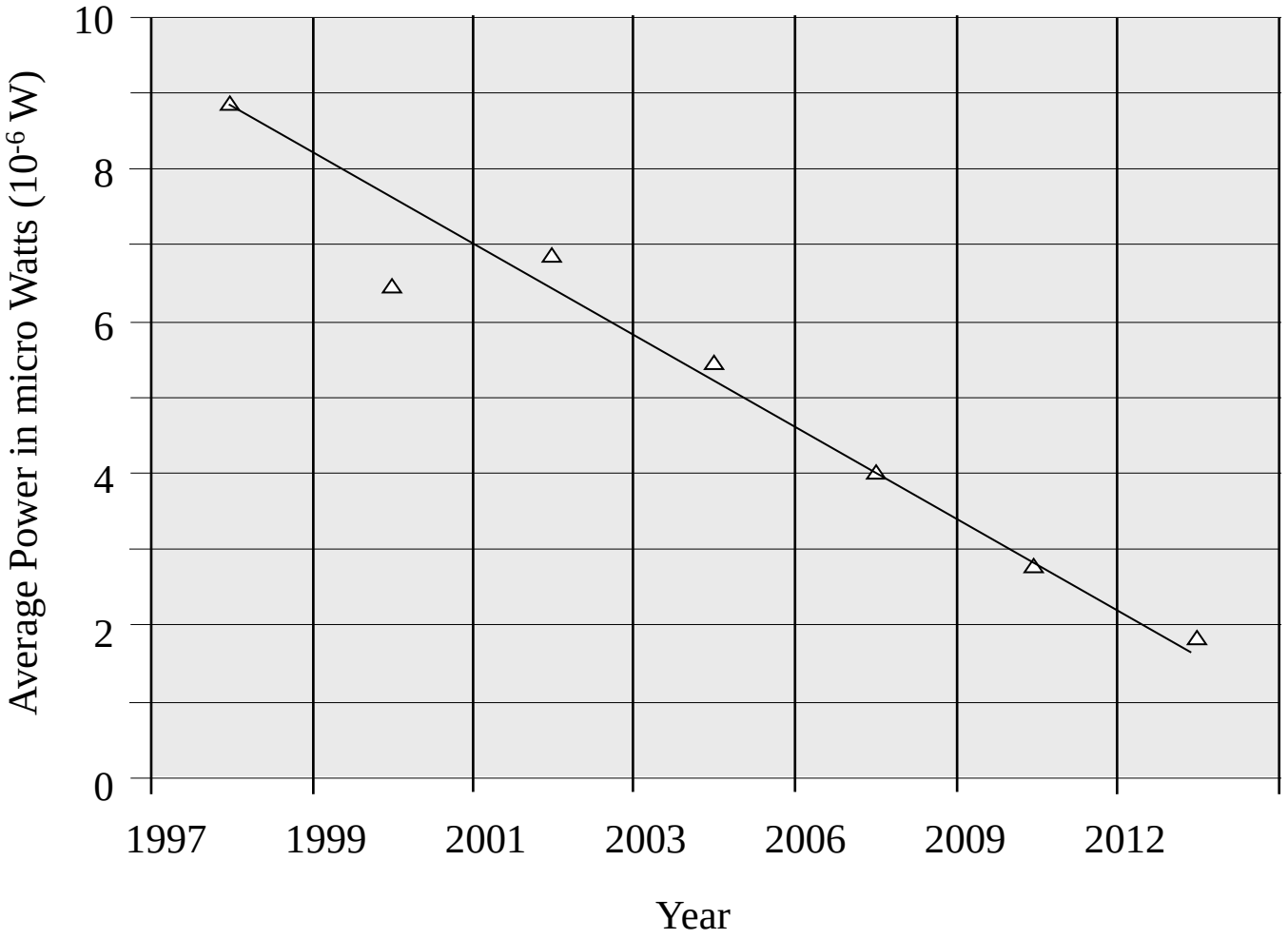


Figure 1.12

# Reduction in Chip Power Consumption per IC




Redrawn from Semiconductor Industry Association,
*National Technology Roadmap, 1997*

Figure 1.13

# Reliability Improvement of Chips

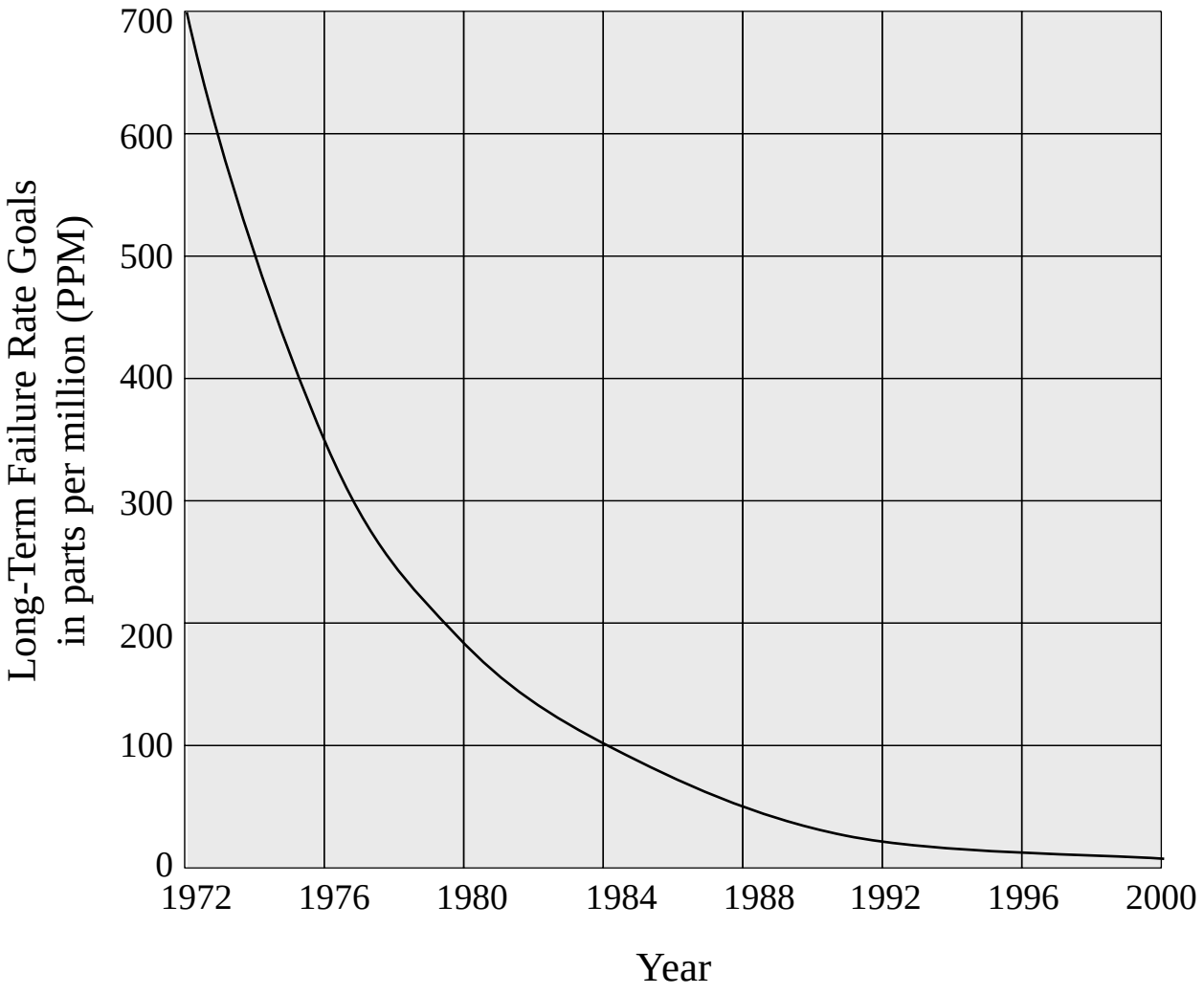
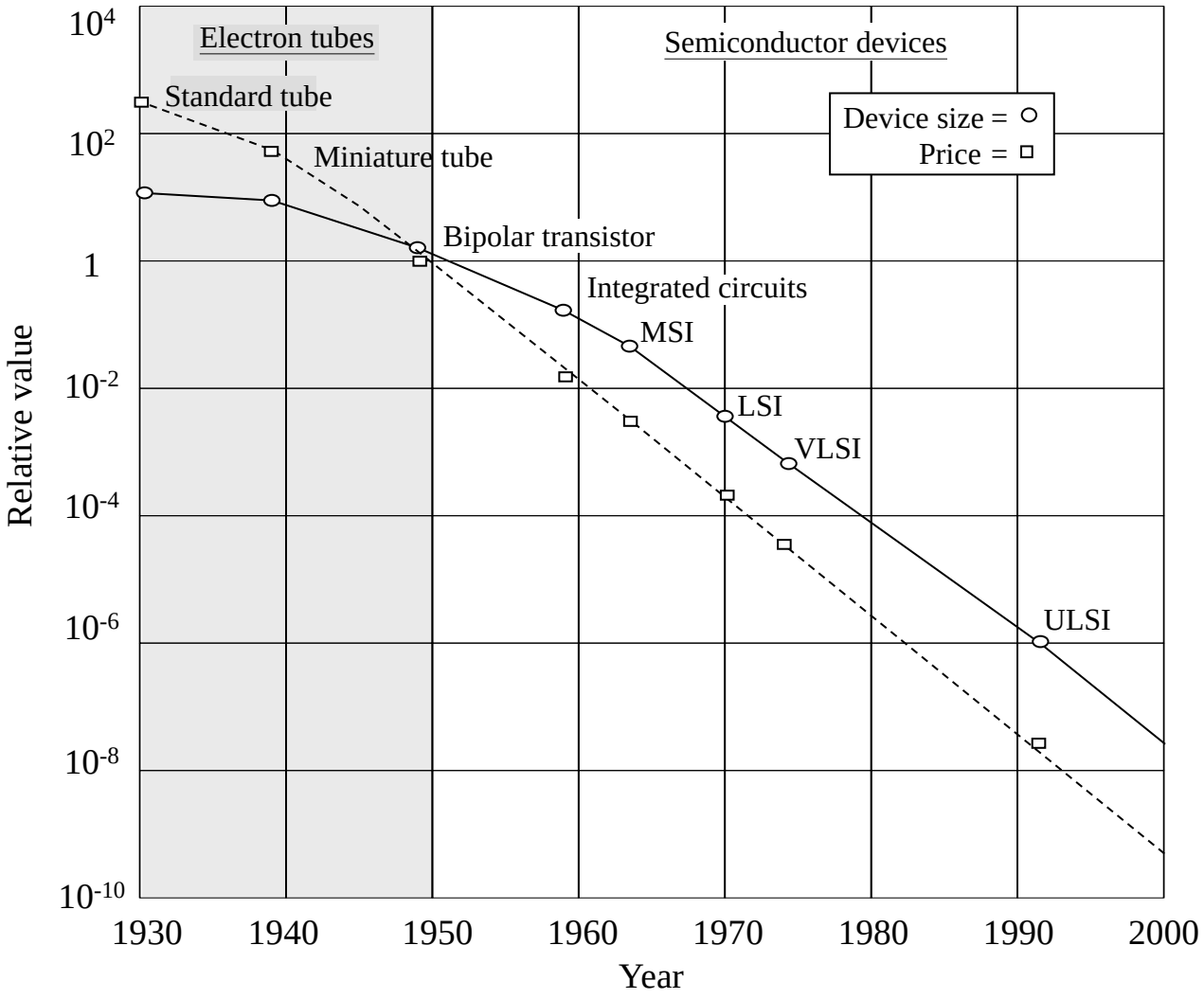



Figure 1.14

# Price Decrease of Semiconductor Chips




- In 1958, $10 to buy a single transistor
- Today, $10 might buy a memory chip over 20 million
- CD: from 0.35-> 0.25 μm, dies increase from 150-> 275.

Redrawn from C. Chang & S. Sze, McGraw-Hill, *ULSI Technology*, (New York: McGraw-Hill, 1996), xxiii.
Figure 1.15

# The Electronic Era

- 1950s: Transistor Technology
- 1960s: Process Technology
- 1970s: Competition
- 1980s: Automation
- 1990s: Volume Production
- 2007 : Smart Phone

# Start-Up Cost of Wafer Fabs

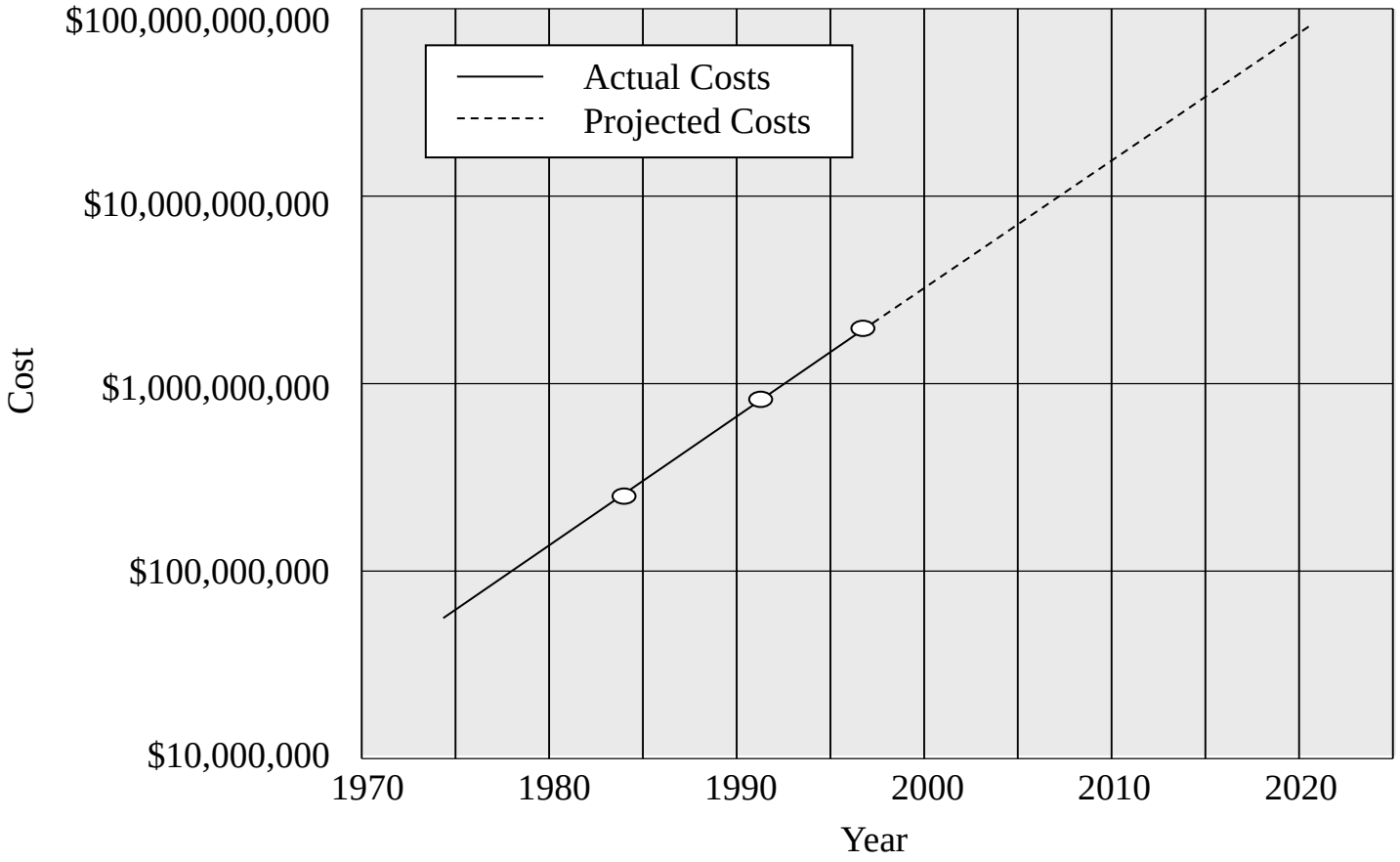





Figure 1.16

# Career Paths in the Semiconductor Industry

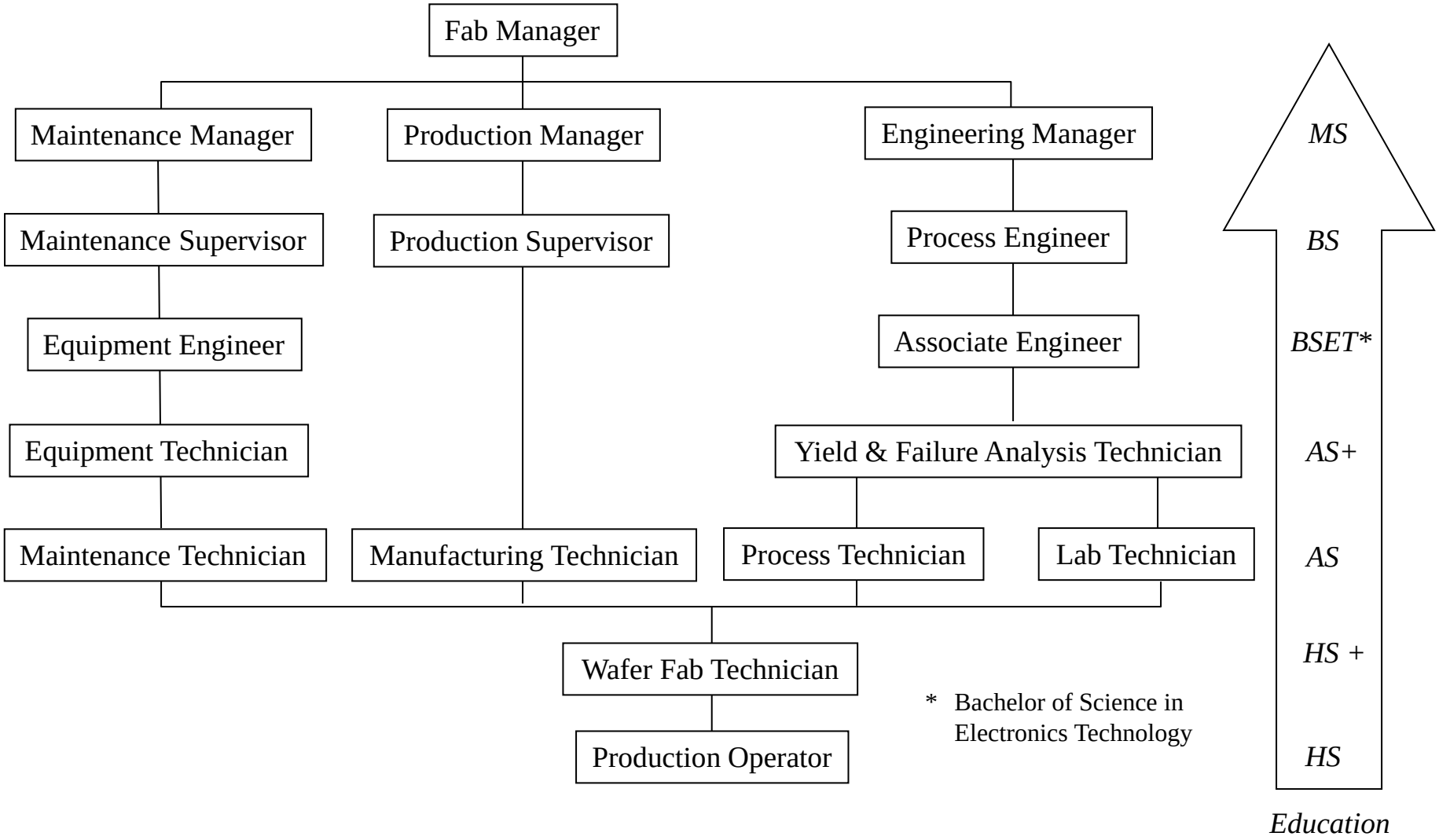
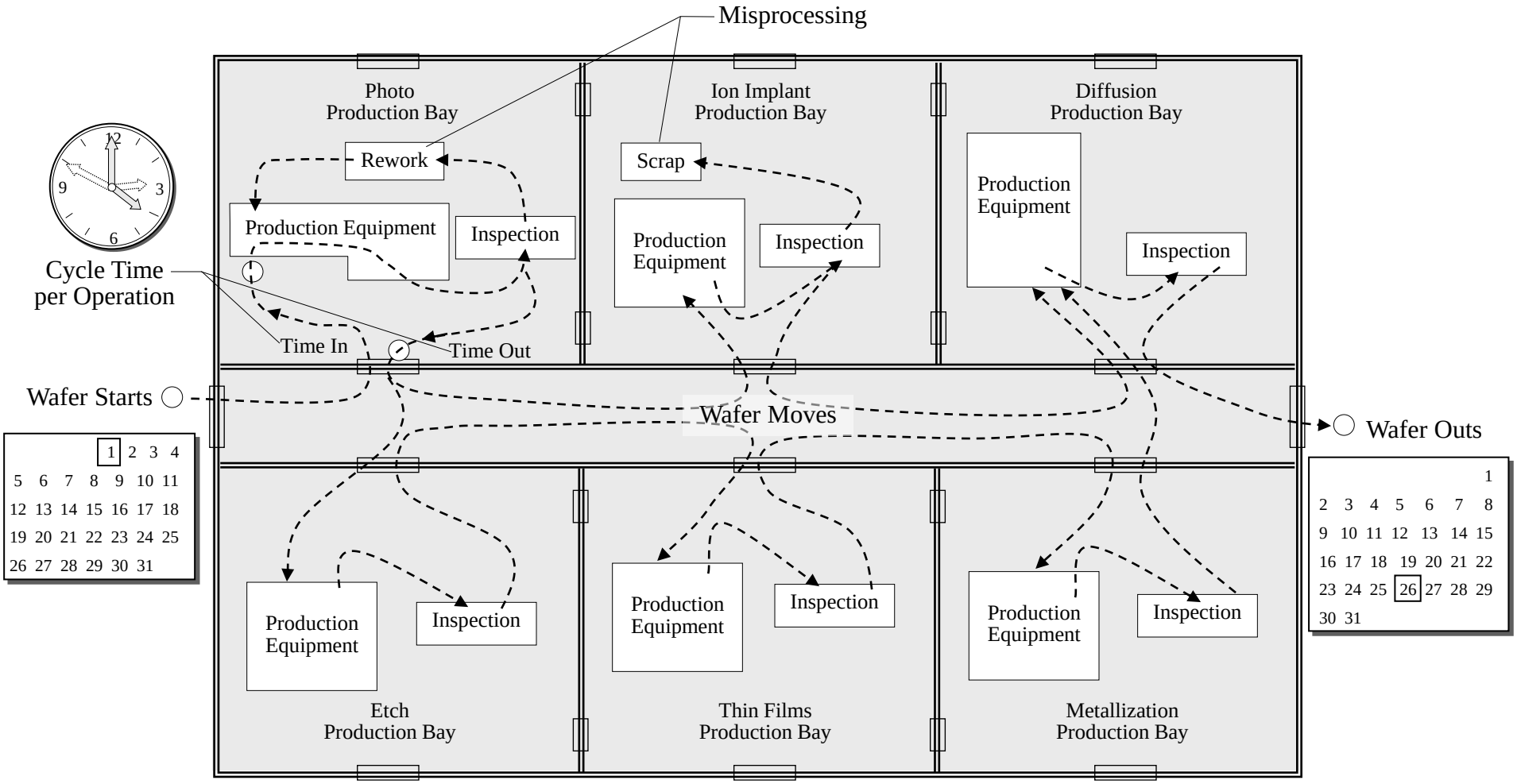



Figure 1.17

# Productivity Measurements in a Wafer Fab




| | | | | | | |
|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | | |
| 5 | 6 | 7 | 8 | 9 | 10 | 11 |
| 12 | 13 | 14 | 15 | 16 | 17 | 18 |
| 19 | 20 | 21 | 22 | 23 | 24 | 25 |
| 26 | 27 | 28 | 29 | 30 | 31 | |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | | | | | 1 |
| 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 16 | 17 | 18 | 19 | 20 | 21 | 22 |
| 23 | 24 | 25 | 26 | 27 | 28 | 29 |
| 30 | 31 | | | | | |

Production Cycle Time = (Date and Time of Wafer Start) - (Date and Time of Wafer Out)

Wafer Outs = Wafer Starts - Wafers Scrapped

Operator Efficiency = Theoretical Cycle Time / Actual Cycle Time

Figure 1.18

# Equipment Technician in a Wafer Fab

Photograph courtesy of Advanced Micro Devices

Photo 1.7

# Technician in Wafer Fab

Photo courtesy of Advanced Micro Devices

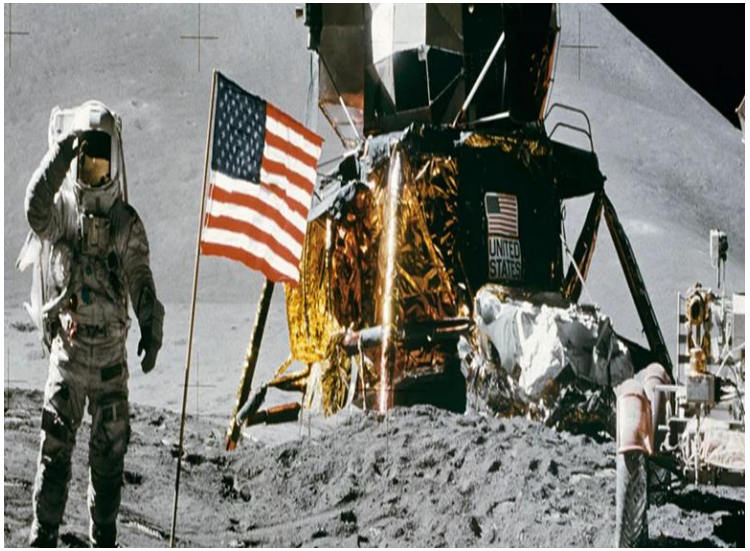
Photo 1.8

# 施敏-數位時代的故事

「台灣沒有豐富的地下資源,只有靠著腦力資源才有未來。」

- 1976年身為經濟部長的孫運璿必須決定台灣是否積極發展積體電路? 該引進哪一家公司的技術? 該選擇哪一種技術? 忍受多大的投資風險?
- 七人小組: 建議台灣應該發展IC產業
- 施敏教授建議: 選擇RCA之CMOS
- 當時名單有: Hughes Electronics, GE, RCA, Fairchild.
- 投資: 400萬美元
- RCA: NMOS, Bipolar, **CMOS**
- CMOS: 省電

# Apollo 11 vs. iPhone 11




RAM : 1: $10^6$

ROM: 1: $7x10^6$

CPU : 1: $10^5$

- Face ID
- 氣壓感測器
- 三軸陀螺儀
- 加速度計
- 接近感測器
- 環境光度感測器