

# **Semiconductor Manufacturing Technology**

**Michael Quirk & Julian Serda**  
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## **Chapter 18**

### **Chemical Mechanical Planarization**

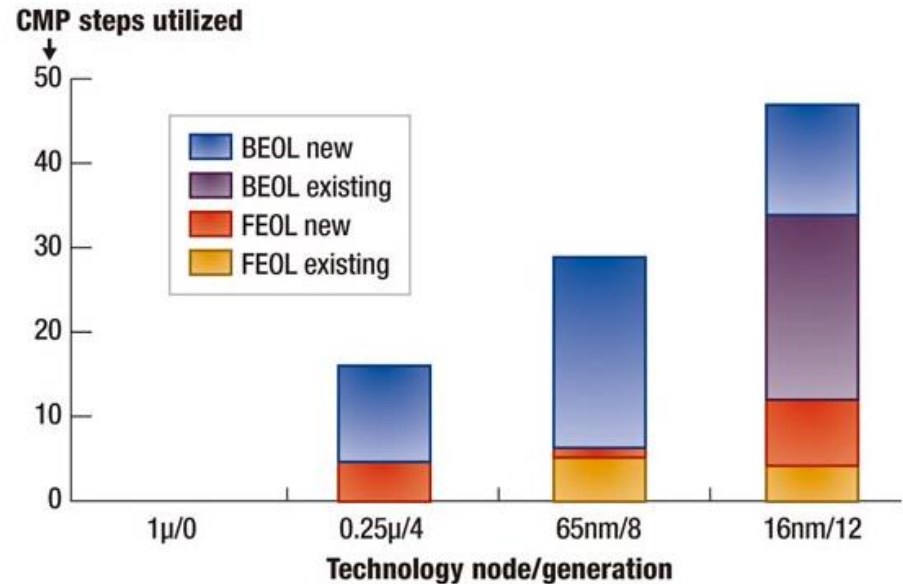
# Objectives

After studying the material in this chapter, you will be able to:

1. Describe the **terminology** for planarization.
2. List and discuss **three** traditional types of planarization.
3. Discuss chemical mechanical planarization (CMP), the issues of **wafer planarity** and the advantage of CMP.
4. Describe the **slurry** and **pad** for both oxide and metal CMP.
5. Discuss CMP equipment, including **endpoint** detection and wafer carriers.
6. Explain the **post-CMP clean** procedure.
7. List and describe seven different CMP **applications**.

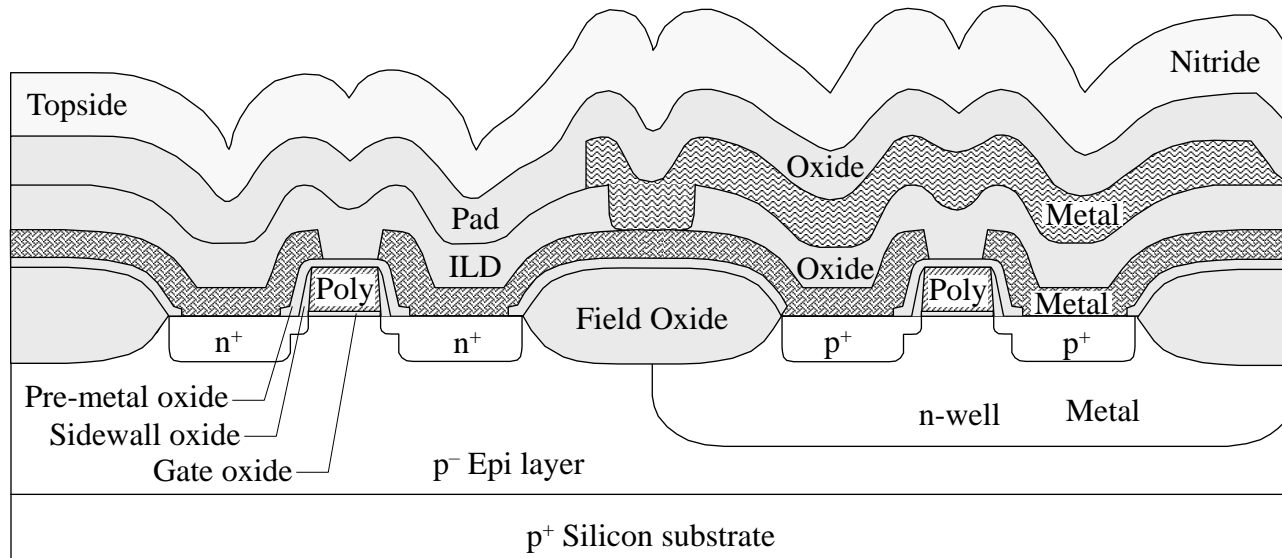
# Introduction

- **Multilayer** metal promotes higher device density because of its efficient use of vertical space on the chip surface
- But the wafer surface became **nonplanar**, which is undesirable for pattern because of the limiting **depth of focus**
- **IBM** developed in the late 1980s, and became the standard during 1990s



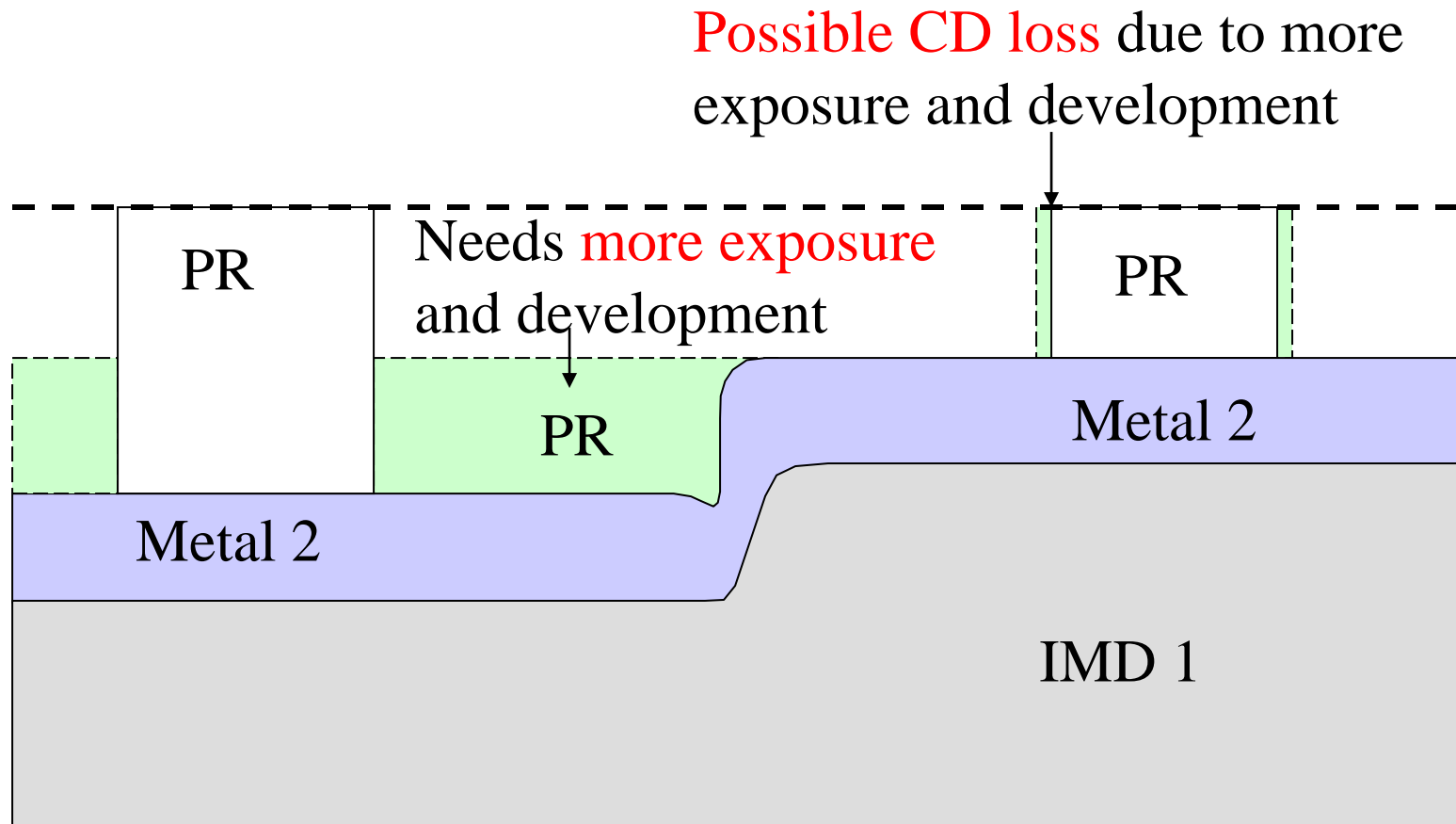
圖一：從0.25μm節點開始，每一個新的CMOS技術世代約增加四道新的CMP步驟

# Single Metal Layer IC with Topography



- A major negative consequence of topography is loss of line width control during photolithography.
- The PR thickness variations due to **topography** are a major factor inhibiting subquarter micron lithography due to the **depth-of-focus** limitations of optical steppers
- A planarized wafer has a flat surface with minimal layer thickness variations on each layer
- **Filling** in low features or **removing** high features are two ways to planarized a wafer surface

- Over Exposure and Over Development

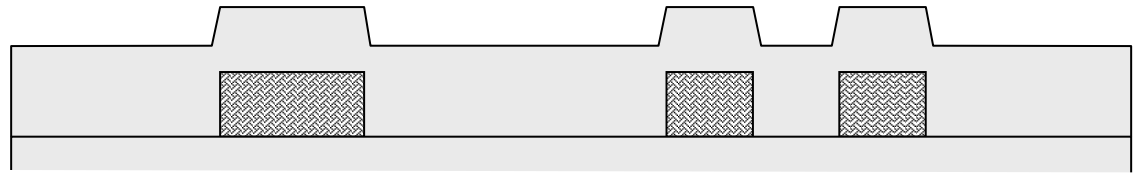


# Terminology for Wafer Planarization

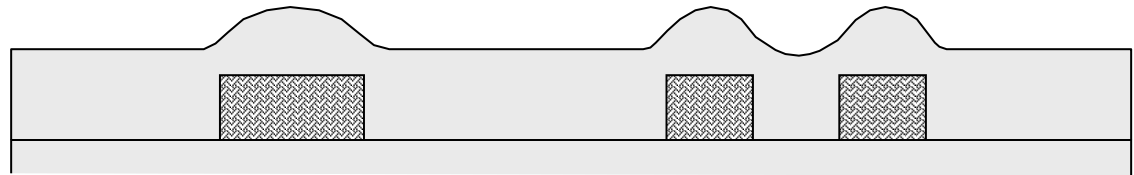
Type of Planarization	Description
<b>Smoothing</b>	Step height corners rounded and sidewalls sloped, but the height is not significantly reduced.
<b>Partial Planarization</b>	Smoothing plus a reduction in step height locally.
<b>Local Planarization</b>	Complete filling of smaller gaps (1 – 10 $\mu\text{m}$ ) or local areas within a die. The total step height to flat areas across the wafer is not significantly reduced.
<b>Global Planarization</b>	Achieves local planarization plus a significant reduction in the total step height across the entire wafer surface. This is also referred to as uniformity.

# Qualitative Definitions of Planarization

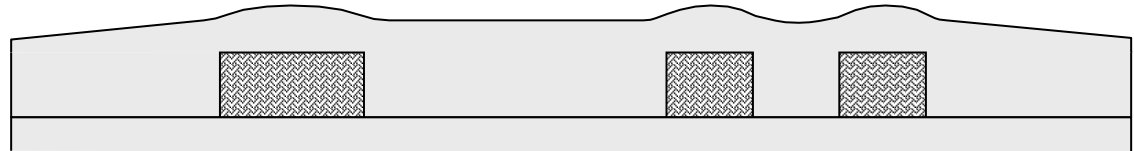
a) No planarization



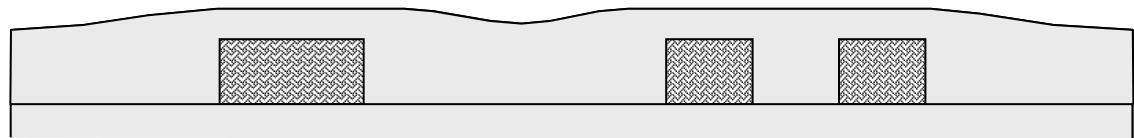
b) Smoothing



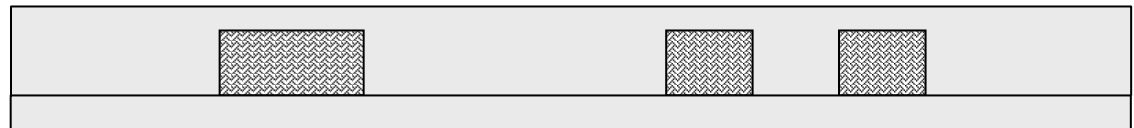
c) Partial planarization



d) Local planarization

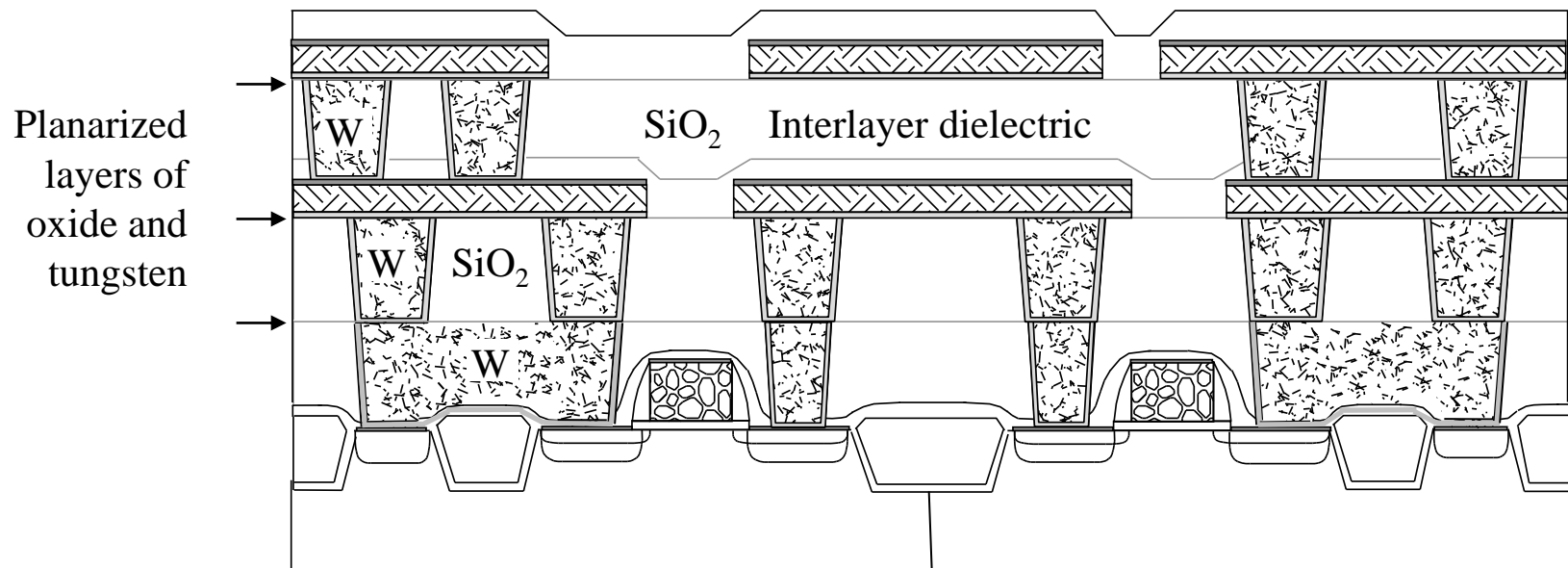


e) Global planarization



# Multilayer Metallization with Chemical Mechanical Planarization (CMP)

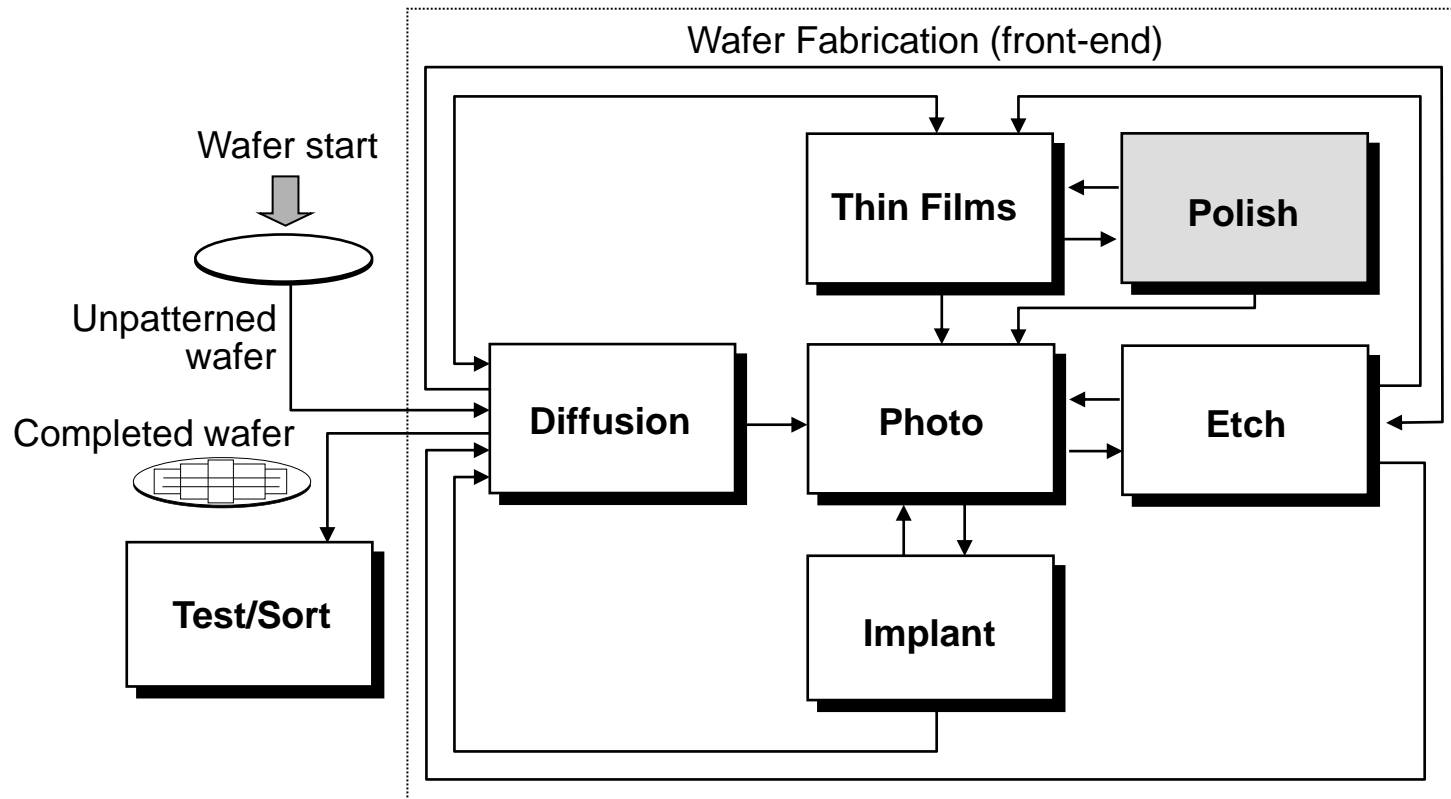
- CMP, commonly referred to as **chemical mechanical polish**, has been used for many years for optical glass polishing and wafer polishing during silicon wafer production



Subquarter micron CMOS cross section

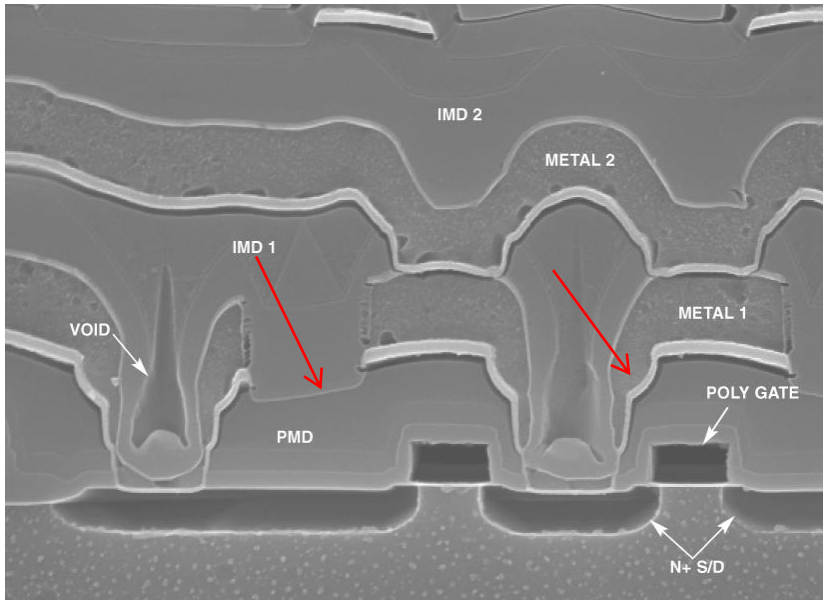


# Wafer Process Flow with CMP

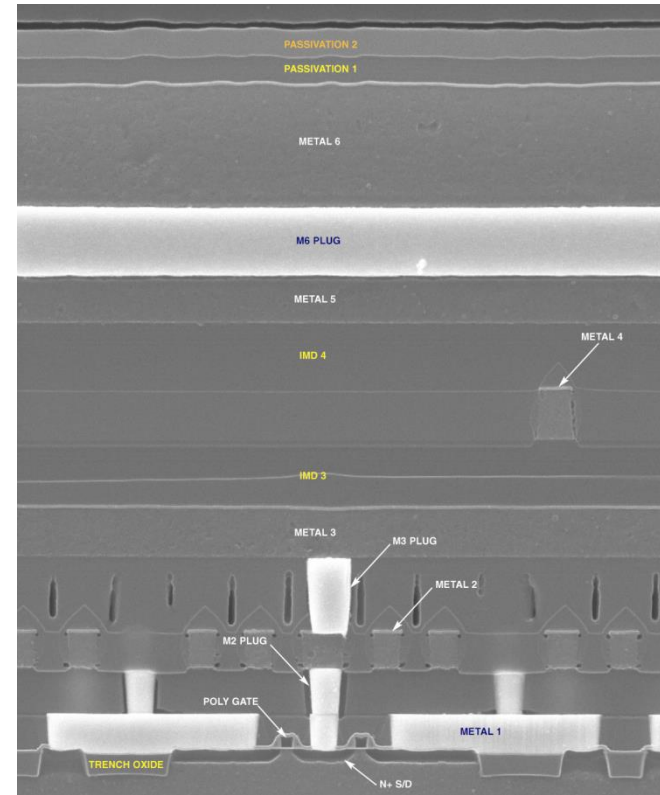


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# Multilayer Metallization with Non-planarized and Planarized Surfaces



Non-planarized IC product

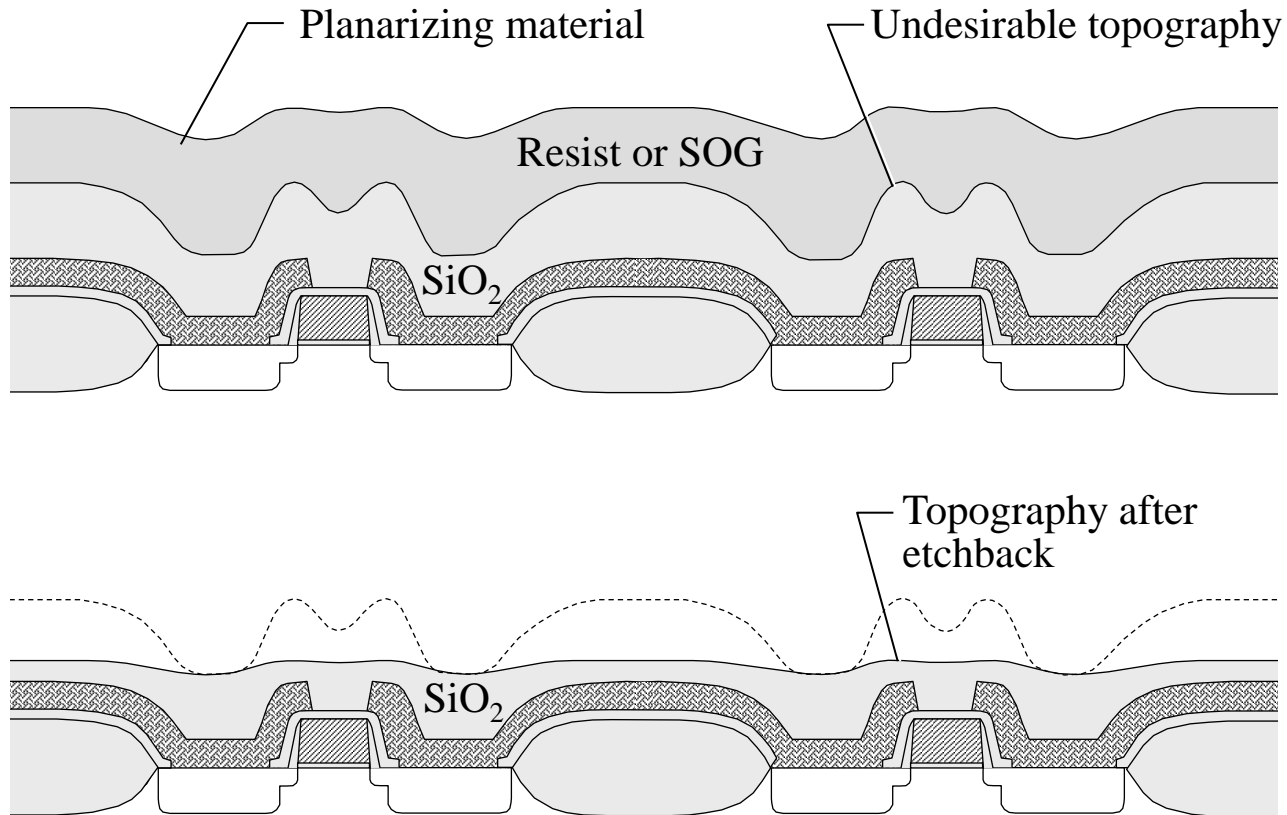


Planarized IC product

# Traditional Planarization

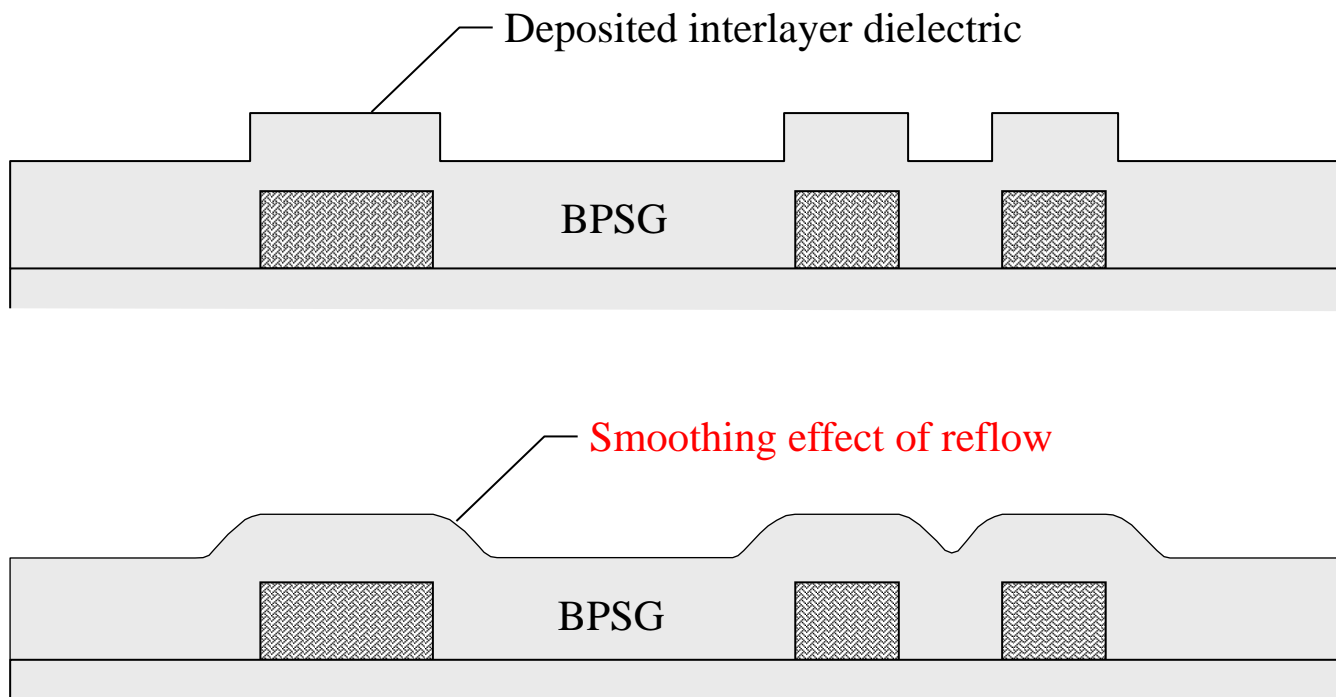
- Etchback
- Glass Reflow
- Spin-on-films

# Etchback Planarization



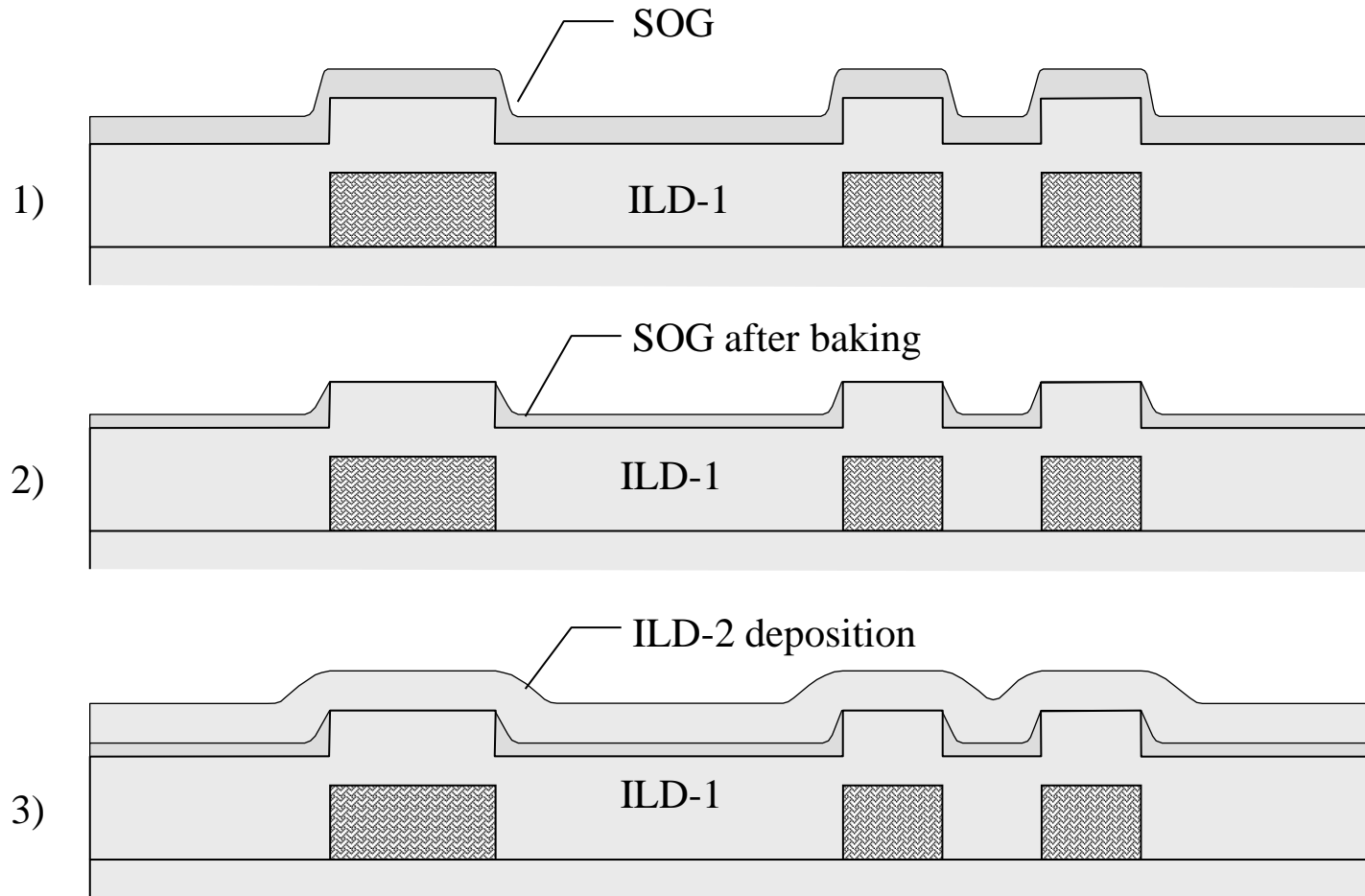
- The sacrificial material fills voids and the low spots on the surface.
- Etching of the sacrificial layer is then done using a **dry etch** to smooth the surface features by removing high feature at a faster rate than low features
- It is a **local planarization**.

# BPSG Reflow Planarization



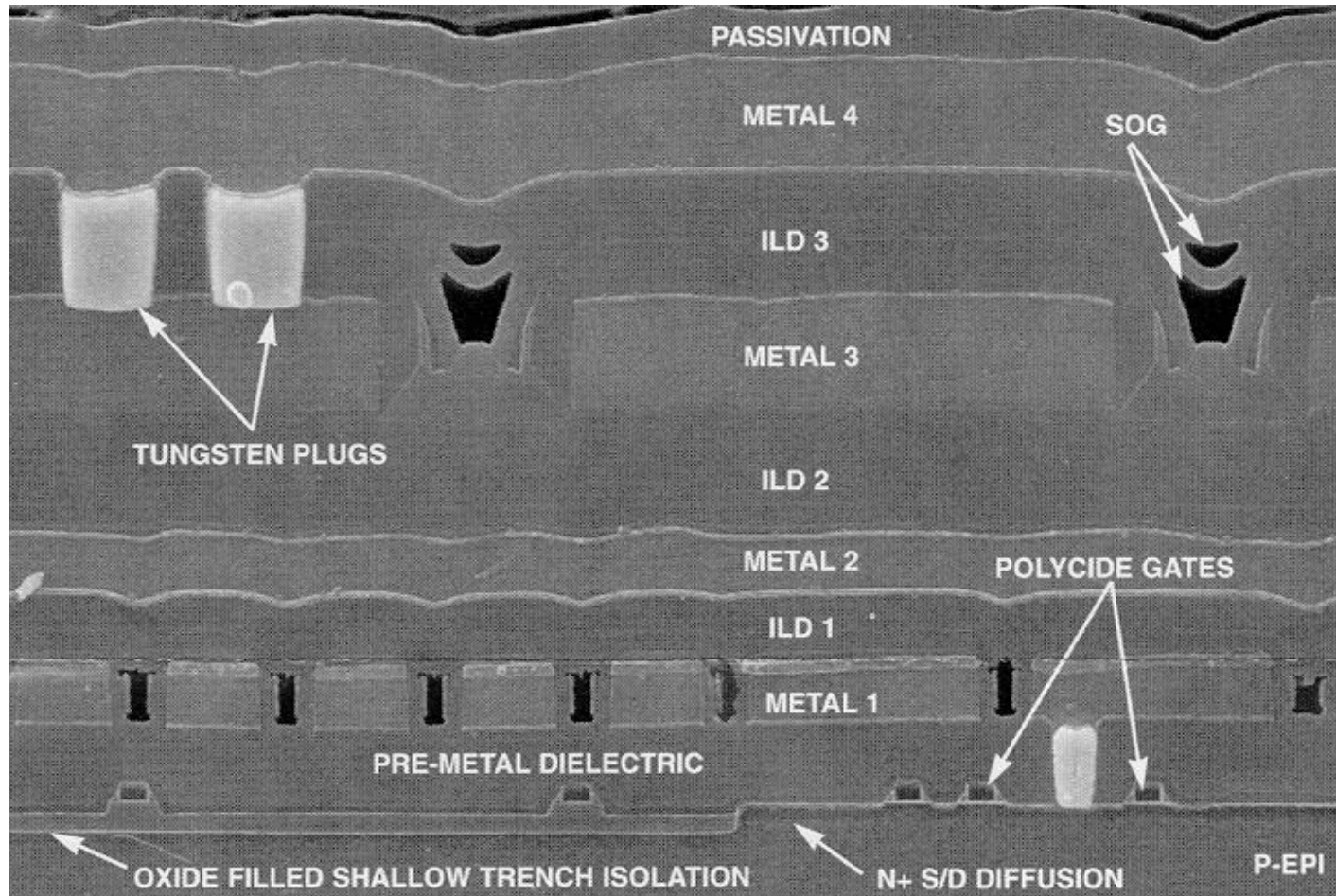
1. 850°C 30-min causes BPSG flow, resulting flow angle  $< 20^\circ$
2. It is not adequate for deep submicron ICs with multiple metals (**high-temp**)

# Spin On film with Etchback



- The most common method for planarization and **gap-fill** at 0.35  $\mu\text{m}$  and larger
- Possible formulation: 80% solvent and 20%  $\text{SiO}_2$
- It is important for low-k deposition

- SOG Etchback



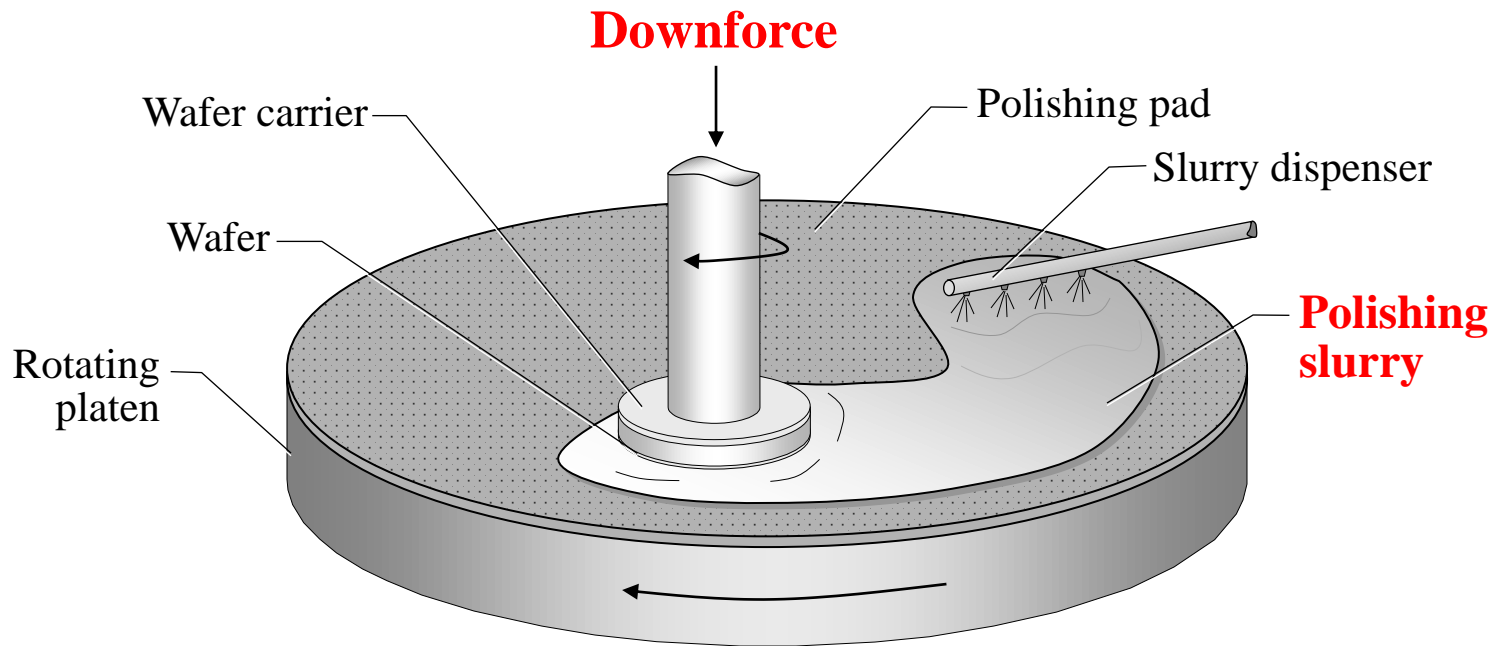
# Chemical Mechanical Planarization

- CMP Planarity
- Advantages of CMP
- CMP Mechanisms
- CMP Slurry and Pad
- CMP Equipment
- CMP Clean
- CMP Equipment Manufacturers



# Schematic of Chemical Mechanical Planarization (CMP)

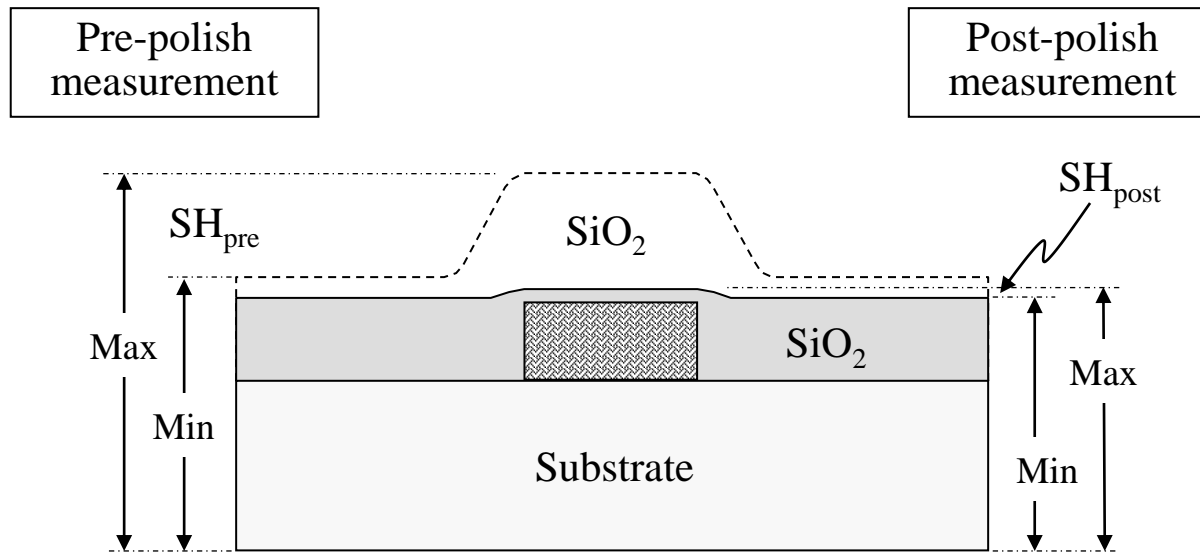
Step height: etchback  $\sim 7000\text{\AA}$  vs. CMP  $\sim 50\text{\AA}$



- CMP achieves wafer planarity by removing high features on the surface more quickly relative to the low feature (high pressure by Preston's eq.)
- Both metal and dielectric layers can be removed

# Wafer Measurements for Degree of Planarization

$$DP(\%) = \left( 1 - \frac{SH_{post}}{SH_{pre}} \right) \times 100$$



- Planarity: surface topography variation
- Uniformity: film thickness variation
- Perfect flat: DP is 100%. If SH post=1 μm, pre is 20 μm, then DP(%) is 95%.

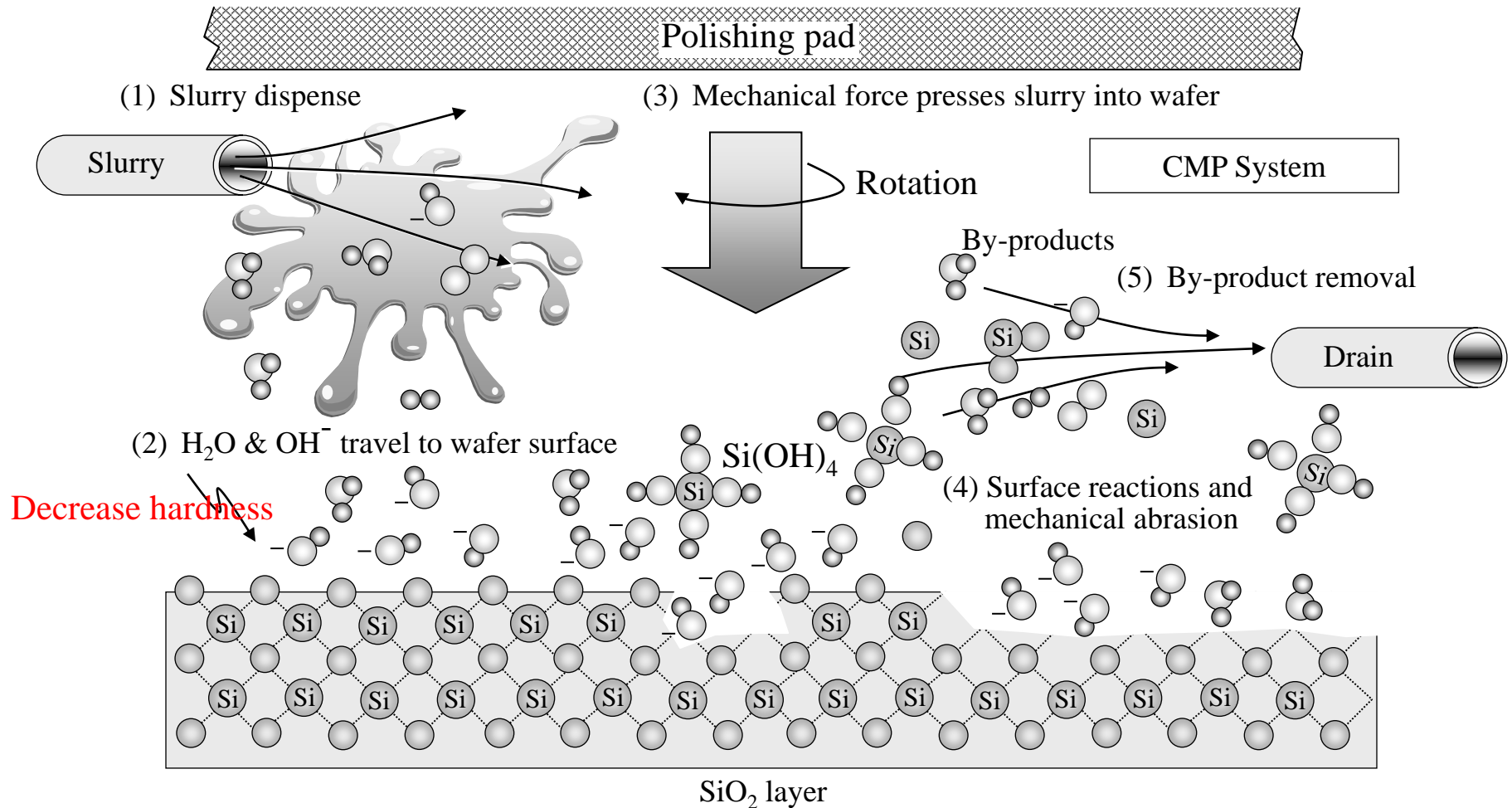
# Advantages of CMP

Benefits	Remarks
1. Planarization	Achieves global planarization.
2. Planarize different materials	Wide range of wafer surfaces can be planarized.
3. Planarize multi-material surfaces	Useful for planarizing multiple materials during the same polish step.
4. Reduce severe topography	Reduces topography to allow for fabrication with tighter design rules and additional interconnection levels.
5. Alternative method of metal patterning	Provides an alternate means of patterning metal (e.g., <b>Damascene</b> process), eliminating the need of the plasma etching for difficult-to-etch metals and alloys.
6. Improved metal step coverage	Improves metal step coverage due to reduction in topography.
7. Increased IC reliability	Contributes to increasing IC reliability, speed and yield (lower defect density) of sub-0.5 $\mu$ m devices and circuits.
8. Reduce defects	CMP is a subtractive process and can remove surface defects.
9. No hazardous gases	Does not use hazardous gases common in dry etch process.

# Disadvantages of CMP

Disadvantages	Remarks
1. New technology	CMP is a new technology for wafer planarization. There is relatively poor control over the process variables with <b>a narrow process latitude</b> .
2. New defects	New types of defects from CMP can affect die yield. These defects become more critical for sub-0.25 $\mu\text{m}$ feature sizes.
3. Need for additional process development	CMP requires additional process development for process control and metrology. An example is the <b>endpoint of CMP</b> is difficult to control for a desired thickness.
4. Cost of ownership is high	CMP is expensive to operate because of <b>costly equipment</b> and consumables. CMP process materials require high maintenance and frequent replacement of chemicals and parts.

# CMP Oxide Mechanism (surface hydration by Cook's theory)

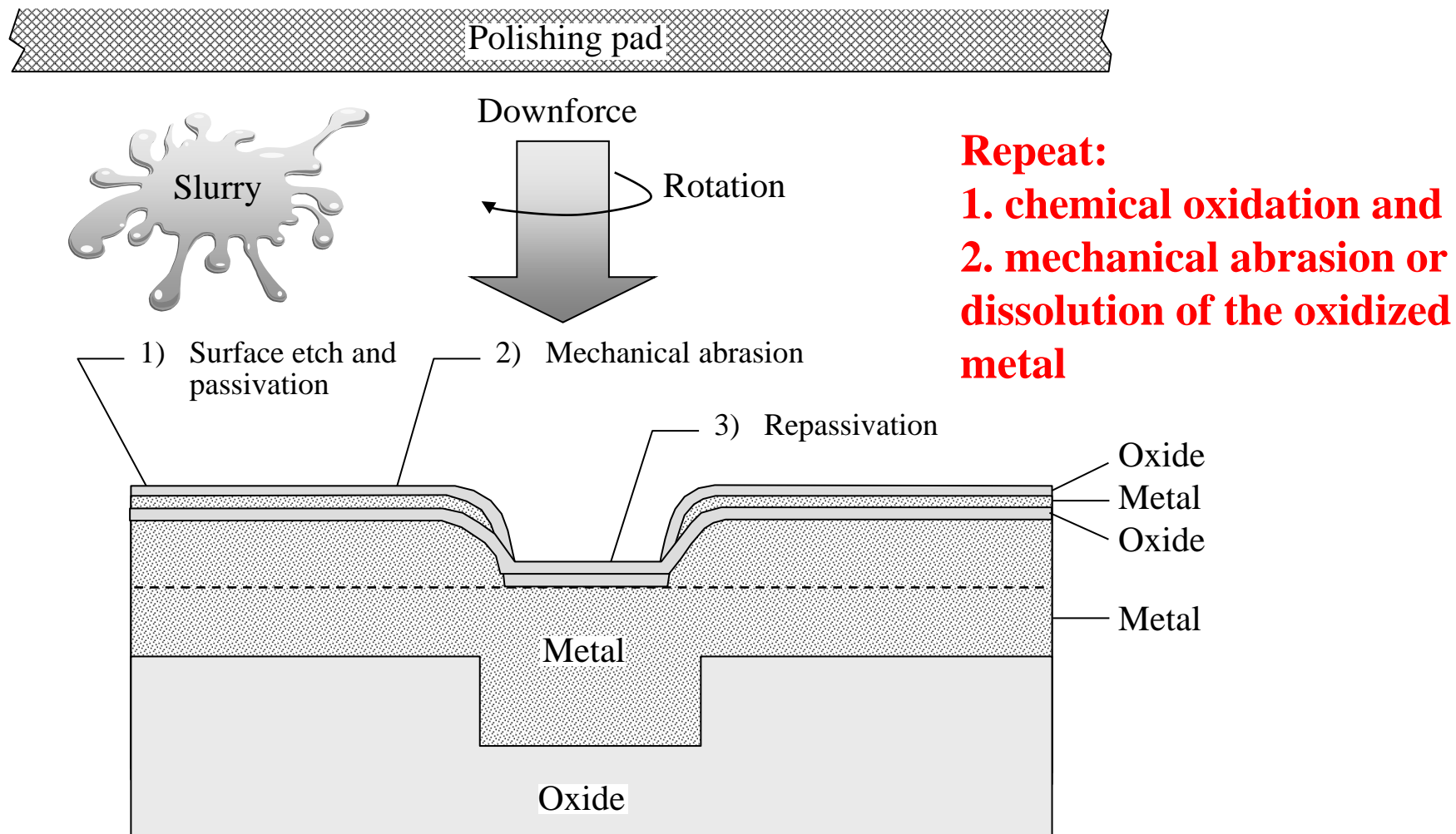


- Chemical: slurry chemistry forms a wafer surface that is easy to remove.
- Mechanical: slurry abrasive component and applied pressure and relative velocity

# Oxide Polish

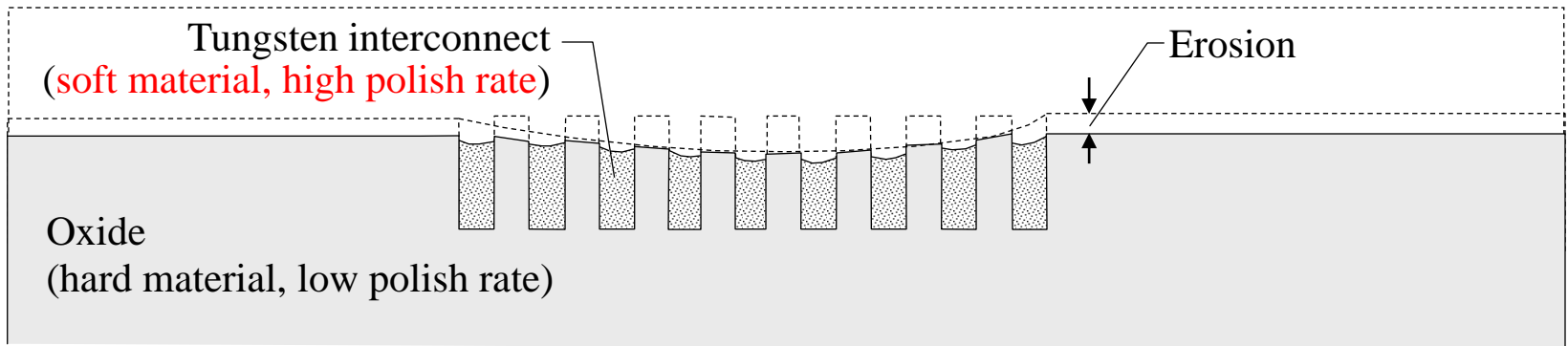
- To planarize the ILD
- Speed of removal is given by Preston's eq.
  - $R = kPv$
  - Where  $P$  is applied pressure
  - $v$  is relative velocity between wafer and pad
  - $k$ : constant depends on oxide hardness, slurry, and pad

# Mechanism for Metal CMP



**For example: Cu CMP, CuO or Cu<sub>2</sub>O or Cu(OH)<sub>2</sub> are formed**

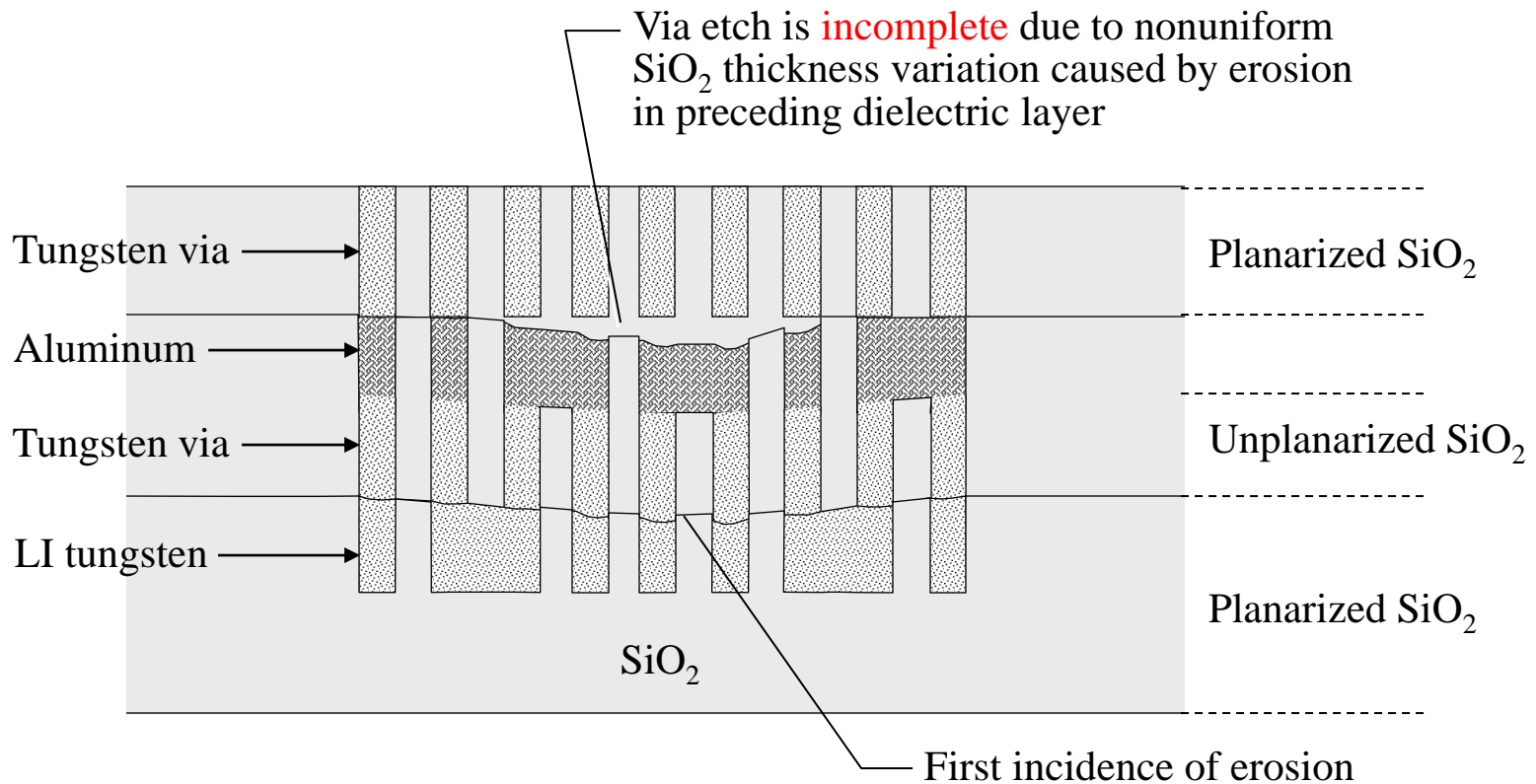
# CMP Erosion in High Wiring Density



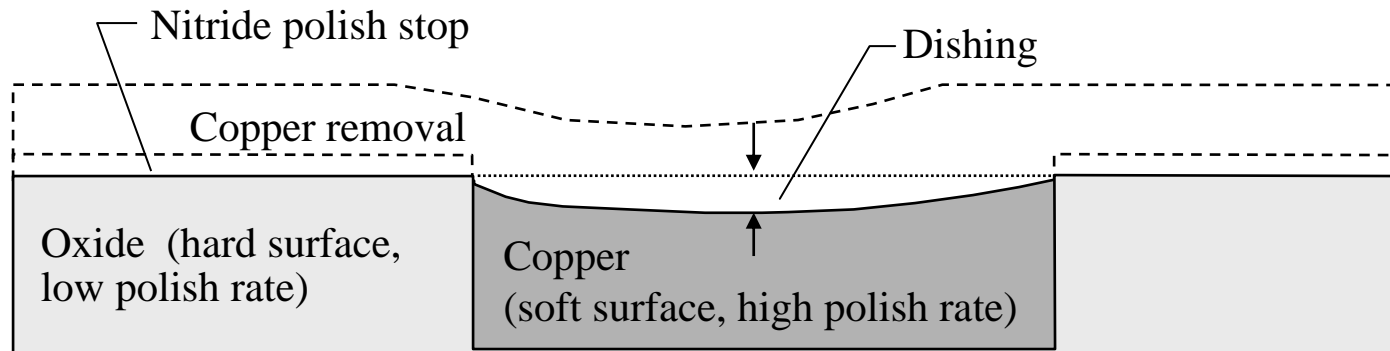
- Narrowly spaced feature often polish at a greater rate than widely spaced feature.
- Small isolated raised feature encounter greater pressure during planarization and polish at a high rate.
- To solve: shorten the overpolish time, and another oxide polish at elevated region.



# Incomplete Via Etch due to Erosion



# CMP Dishing in a Large Feature

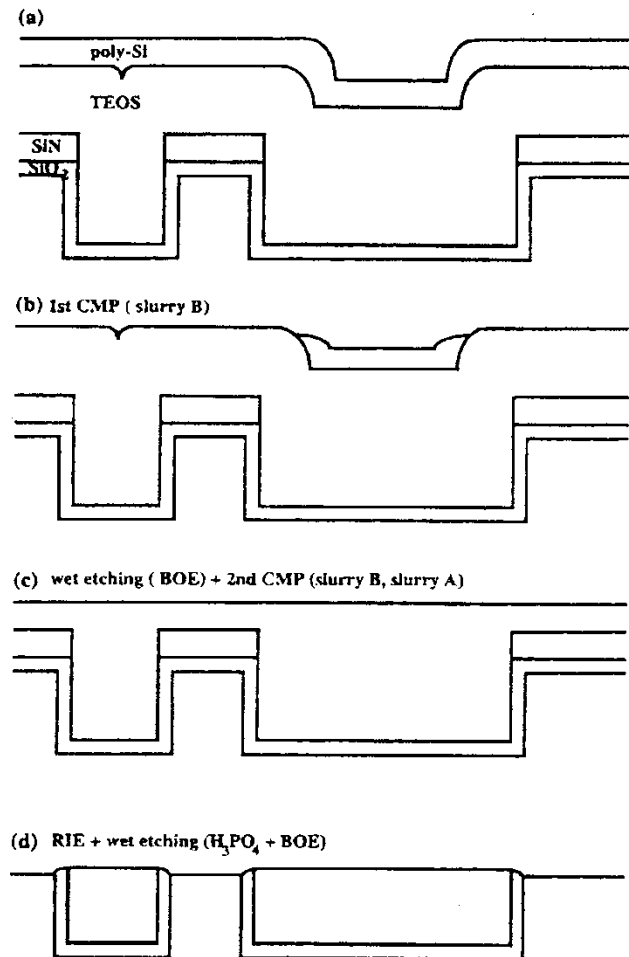
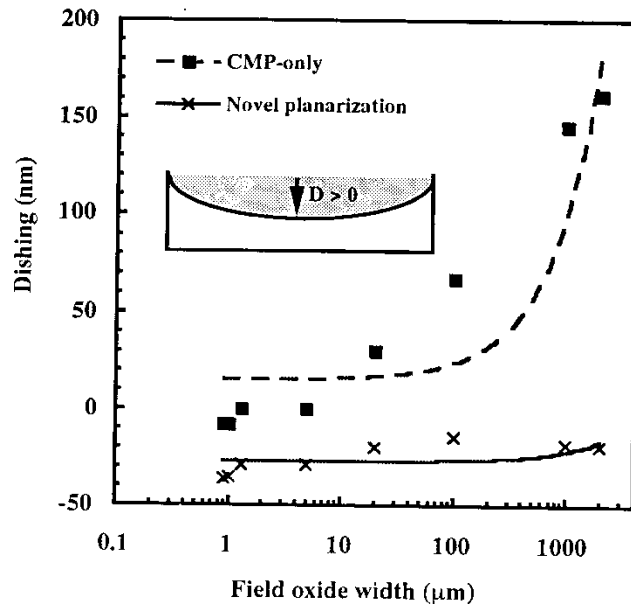


- **Wider** lines having more tendency to dish
- Softer polishing pads bend into the soft metal line and exert pressure to causes dishing

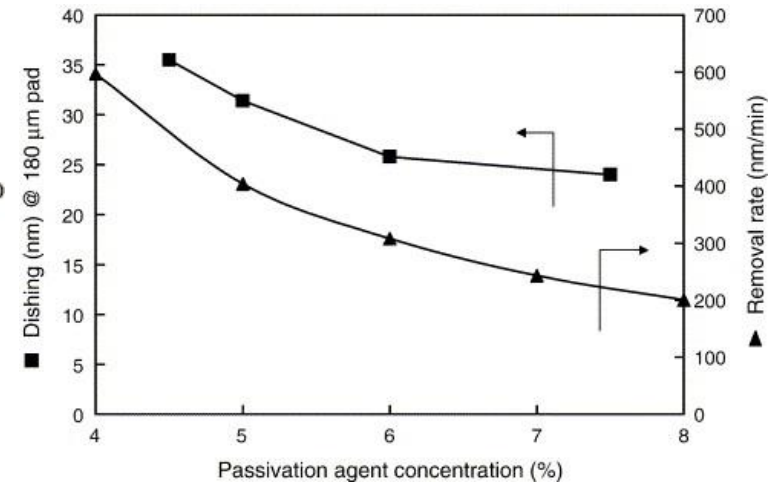
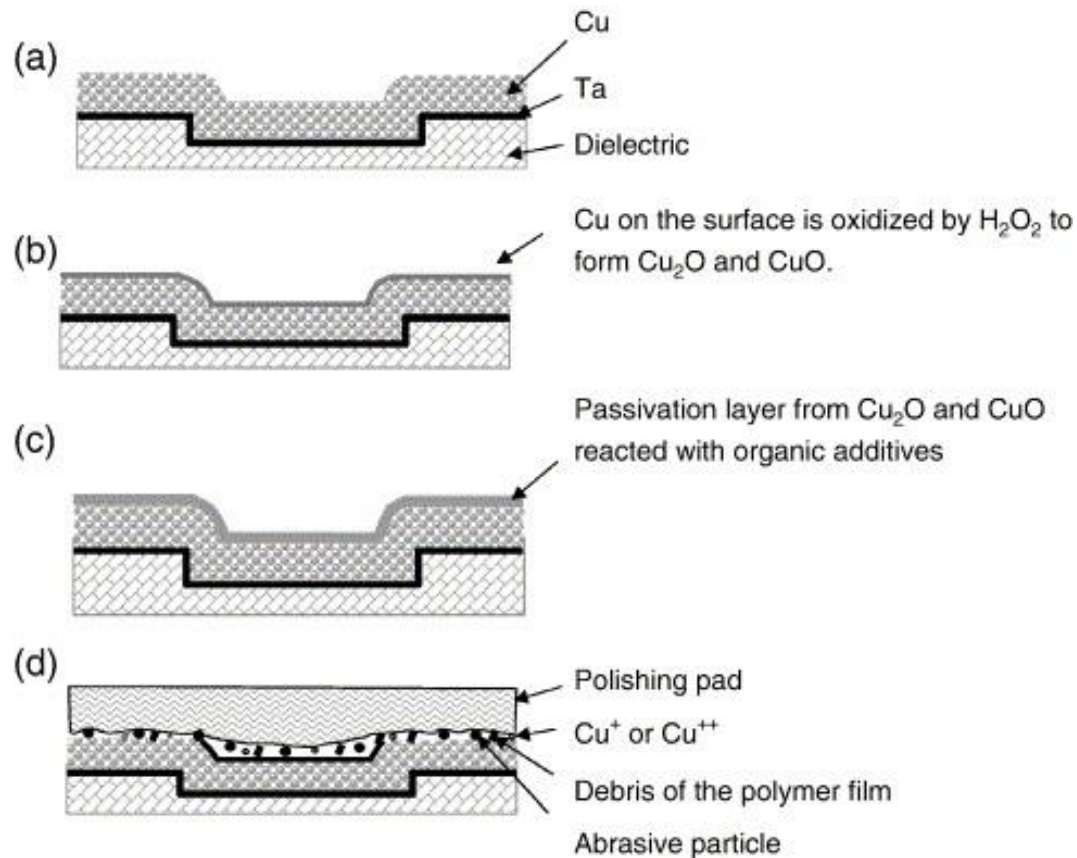
# A Novel Planarization of Oxide-filled STI

(J. Electrochem. Soc., 1997, p.315)

- Using high selectivity CMP on poly-Si/oxide
- Dishing effect in wide field regions is improved



# Novel slurry solution for dishing elimination in copper process beyond 0.1- $\mu\text{m}$ technology (Thin Solid Films, 498, p.50, 2006)

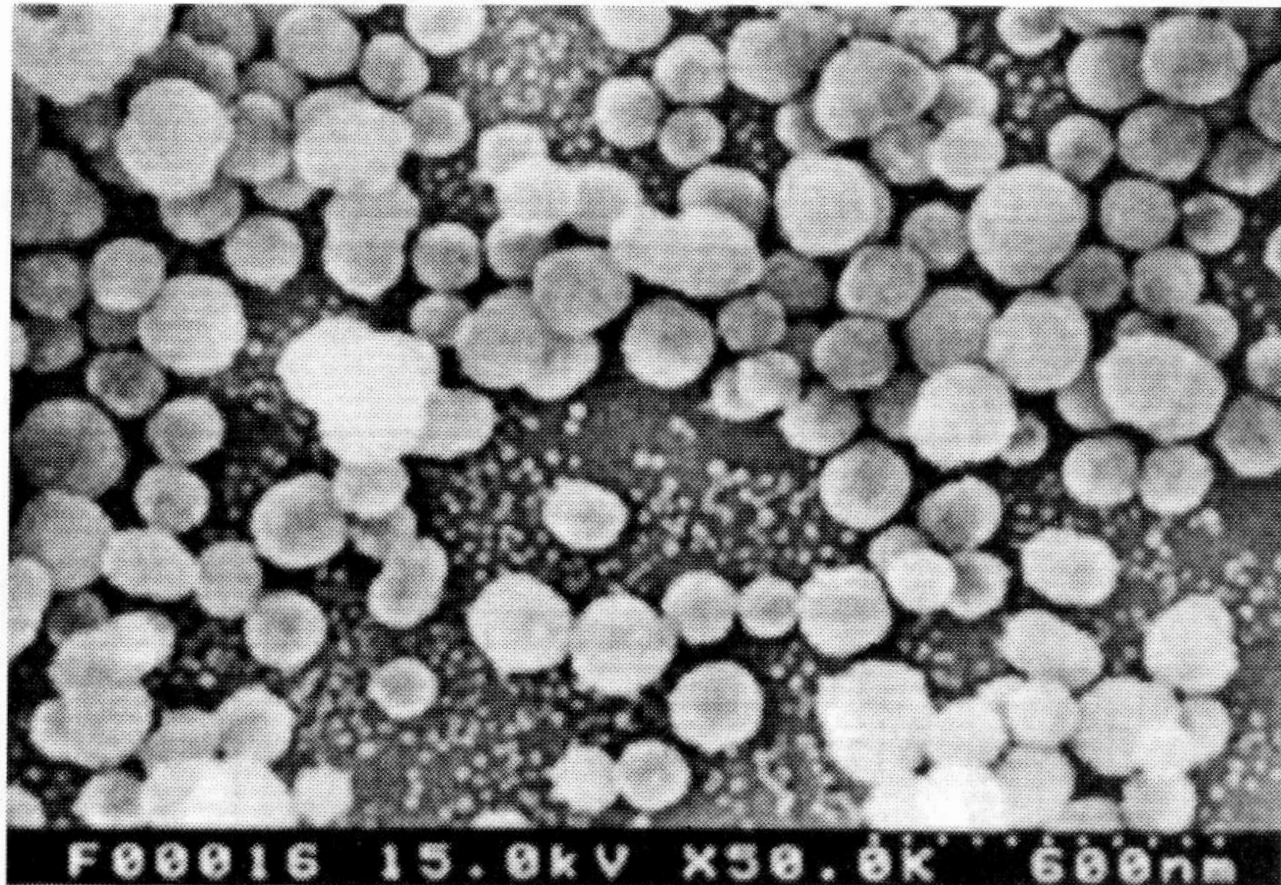


- inhibitor of copper corrosion due to its active adsorption ability on the copper surface to prevent the copper oxidation

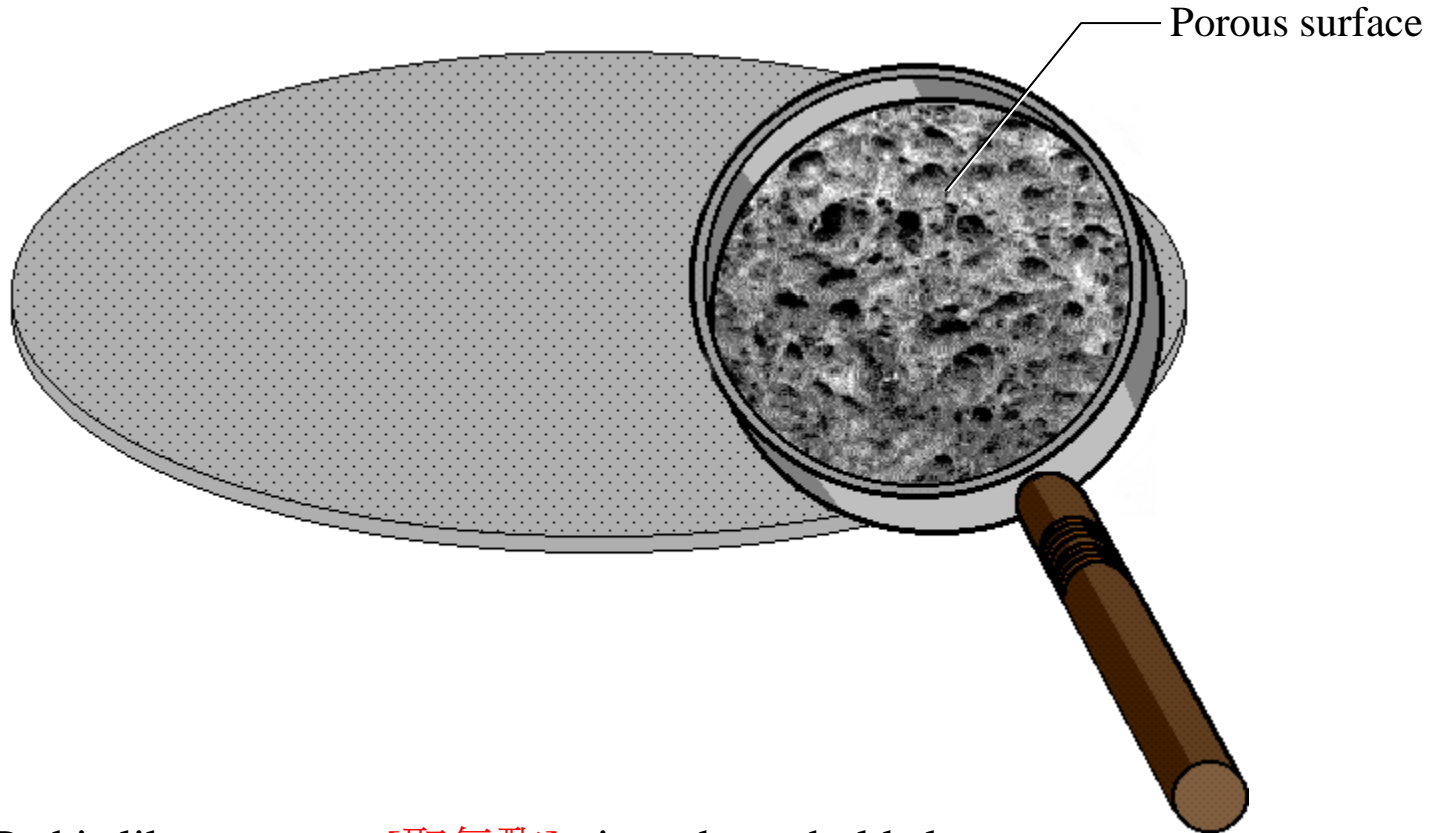
# Slurry

- Slurry is a mixture of fine abrasive particles and chemicals
- Precise slurry mixing, uniform **suspended** and uniformly distribution are important
- Oxide slurry: **silica colloidal + KOH or NH<sub>4</sub>OH** (pH ~ 10-11). KOH is preferred for its stable **colloidal suspension**, but K is mobile ion. **BPSG** as the **gettering layer**.
- W-slurry: fine **Al<sub>2</sub>O<sub>3</sub> or silica** (more soft, less scratch) + **H<sub>2</sub>O<sub>2</sub>**. Oxidizes the W as WO<sub>3</sub> (soft and remove)
- Cu-slurry: **NH<sub>4</sub>OH+alumina powder**

# Silica Particulates

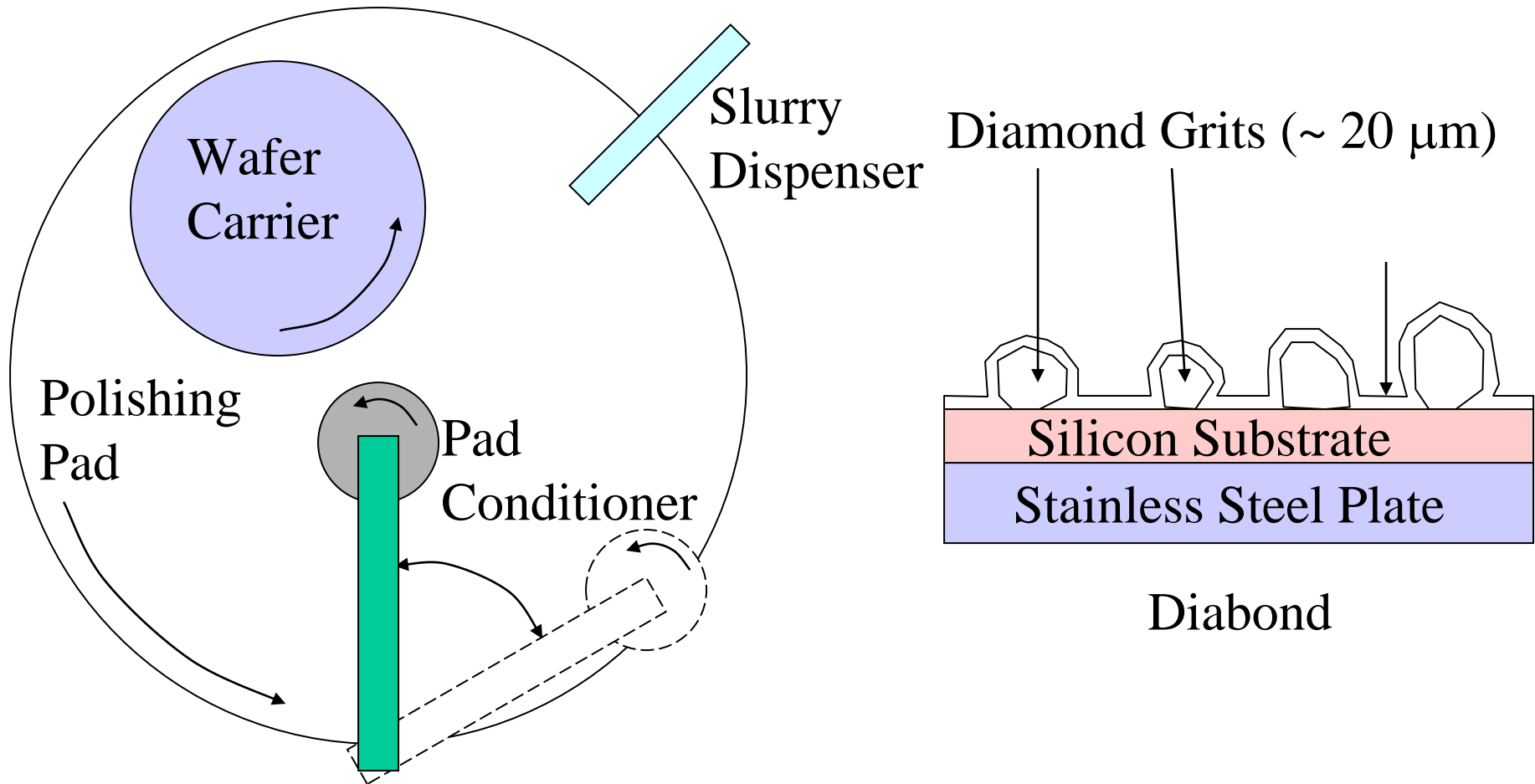


# CMP Polishing Pad



- Pad is like a **sponge** [聚氨酯] , in order to hold slurry.
- After polishing for a long time, the pad surface becomes flatted and smooth → **glazing**
- Needs conditioning to slow down the glazing: **abrasion or DI water jet spray**

- Polishing Pad and Pad Conditioner



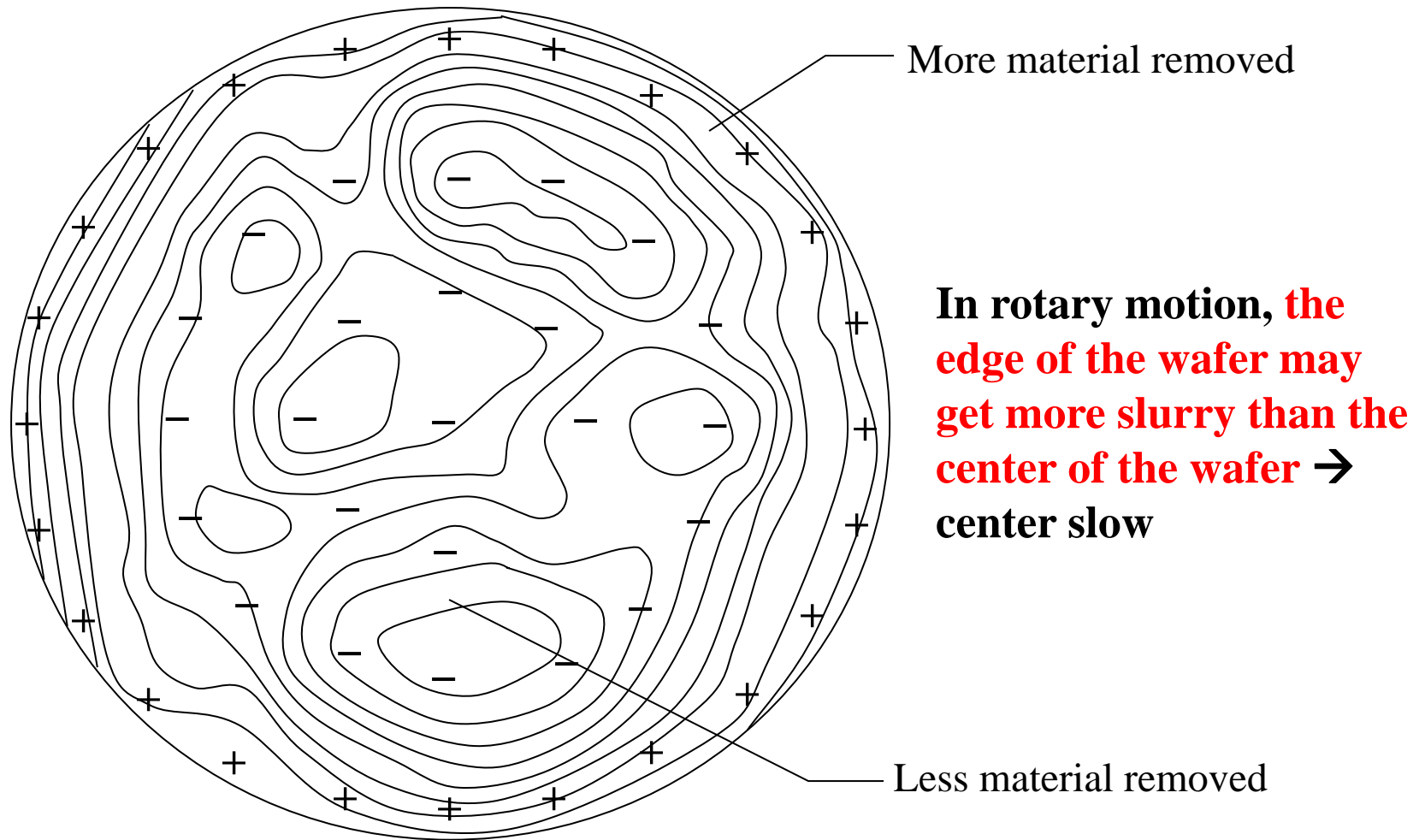


# CMP Polishing Pad



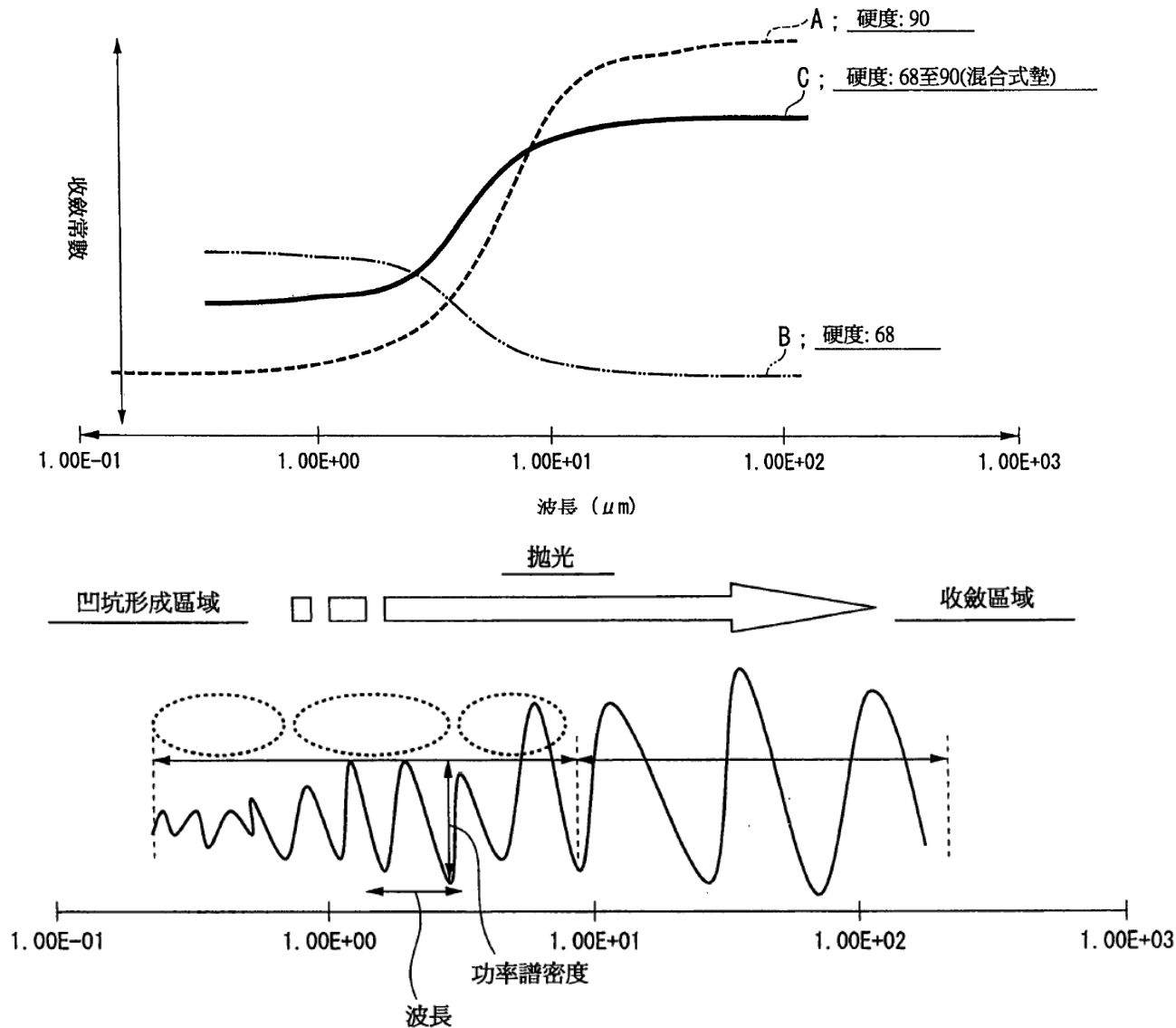
Photo courtesy of Speedfam-IPEC

# CMP Contour Plot for Center Slowness



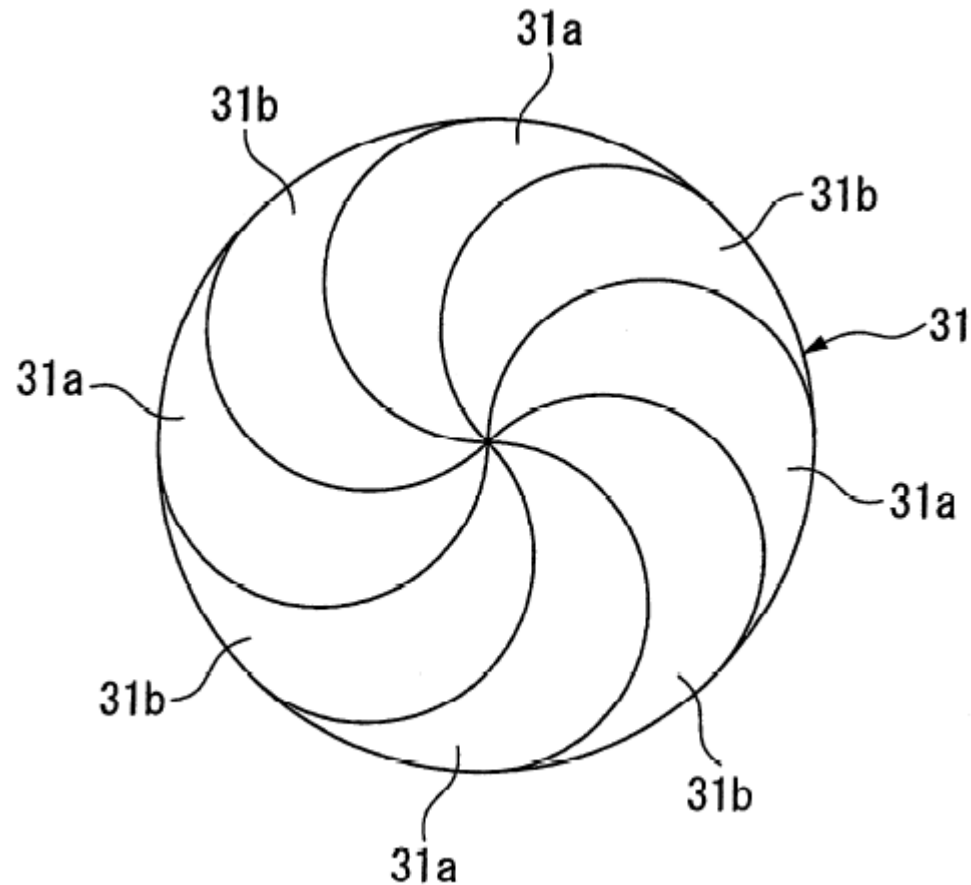
# Polish Rate and Uniformity

- A **hard** polishing generally promotes local wafer planarization
- A **soft** polishing pad will reduce the **scratches**
- Higher down force and rotational speed will increase the removal rates, at the expense of uniformity and scratches
- In many cases, the best planarity : a **hard polishing pad and low pressure**
- Selectivity: **one** for simultaneous polishing of multiple materials; but **high** for metal/ILD to minimize erosion
- To reduce polishing time, it needs to minimizing the **overburden** thickness. For example, ILD polish on metal.



由硬度90之發泡胺甲酸乙酯製成習用硬拋光墊來進行晶圓表面拋光時，如第2A圖中曲線A所示，具有大波長的部份可在短時間內移除(亦即收斂常數較大)，而具有短波長的部份的收斂常數就較小。再者，其發現，在使用由硬度68之麂皮製成的習用軟拋光墊來進行晶圓表面拋光時，如第2A圖中曲線B所示，具有小波長的部份可以在短時間內移除(亦即收斂常數較大)，而具有大波長的部份的收斂常數就較小

習知的拋光製程中，其係使用一設有硬拋光墊的晶圓拋光裝置來進行第一拋光製程，以移除晶圓表面上的粗糙不均勻度，使該表面平坦，再使用一設有軟拋光墊的晶圓拋光裝置來進行第二拋光製程，以消除晶圓表面上的小凹坑，而將該晶圓表面加工成平直而無應變的表面

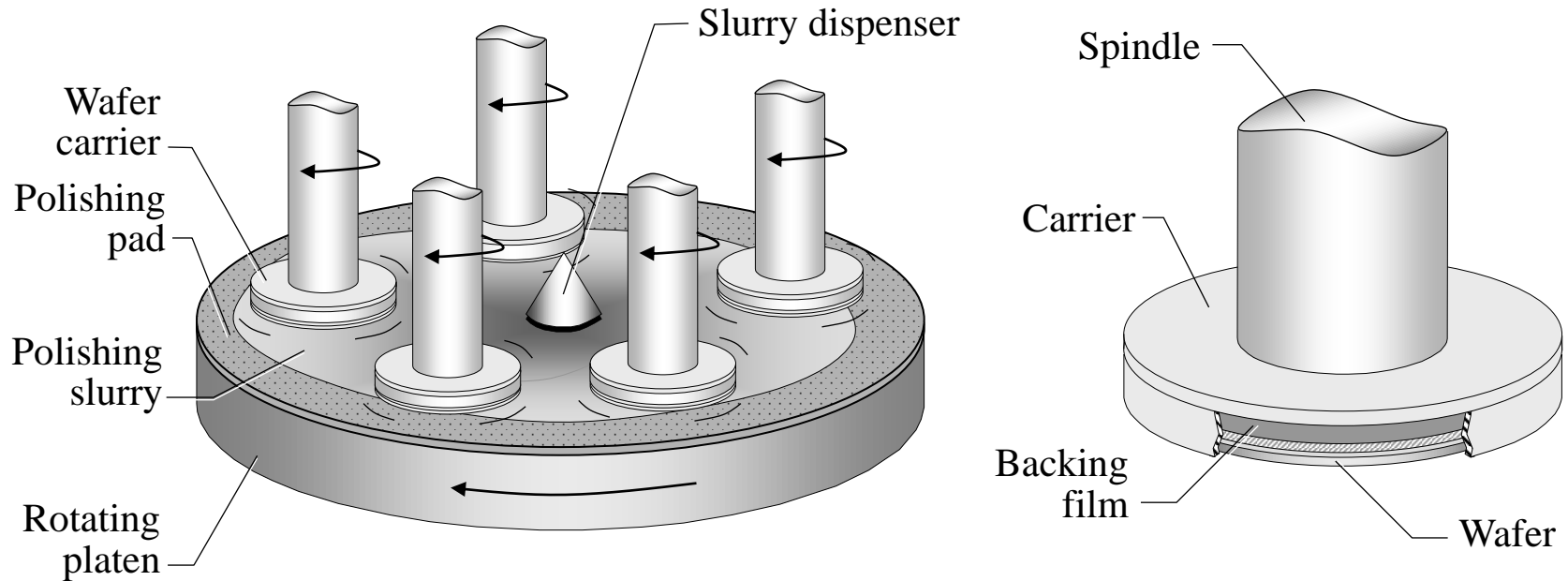


包括**硬度不同之第一區域及第二區域等多個區域**的拋光墊係被加以轉動，而一轉動中的矽晶圓則被壓貼並磨擦該拋光墊，以透過該拋光墊將晶圓表面上的粗糙不均勻度及小凹坑加以移除，因此不再需要如同習用般針對要移除粗糙不均勻度的情形或是要消除小凹坑的情形來更換晶圓拋光裝置及拋光墊，且可以減少拋光晶圓所需的設備及拋光材料，因之可以簡化拋光製程及縮短晶圓的拋光週期，因此之故可以更有效率地拋光晶圓

# CMP Parameters

Parameter	Planarization Results on Wafer
Polish time	<ul style="list-style-type: none"><li>• Amount of material removed</li><li>• Planarity</li></ul>
Pressure on wafer carrier (downforce)	<ul style="list-style-type: none"><li>• Removal rate</li><li>• Planarization and non-uniformity</li></ul>
Platen speed	<ul style="list-style-type: none"><li>• Removal rate</li><li>• Non-uniformity</li></ul>
Carrier speed	<ul style="list-style-type: none"><li>• Non-uniformity</li></ul>
Slurry chemistry	<ul style="list-style-type: none"><li>• Material selectivity</li><li>• Removal rate</li></ul>
Slurry flow rate	<ul style="list-style-type: none"><li>• Affects how much slurry is on the pad and the lubrication properties of the system</li></ul>
Pad conditioning	<ul style="list-style-type: none"><li>• Removal rate</li><li>• Non-uniformity</li><li>• Stability of CMP process</li></ul>
Wafer/slurry temperature	<ul style="list-style-type: none"><li>• Removal rate</li></ul>
Wafer back pressure	<ul style="list-style-type: none"><li>• Center slowness/non-uniformity</li><li>• Wafer breakage</li></ul>

# CMP Tool with Multiple Wafer Carriers



- Most difficult: **endpoint detection** which is the ability of the CMP tool to detect when the planarization process has polished the materials to the correct thickness

# CMP Tool

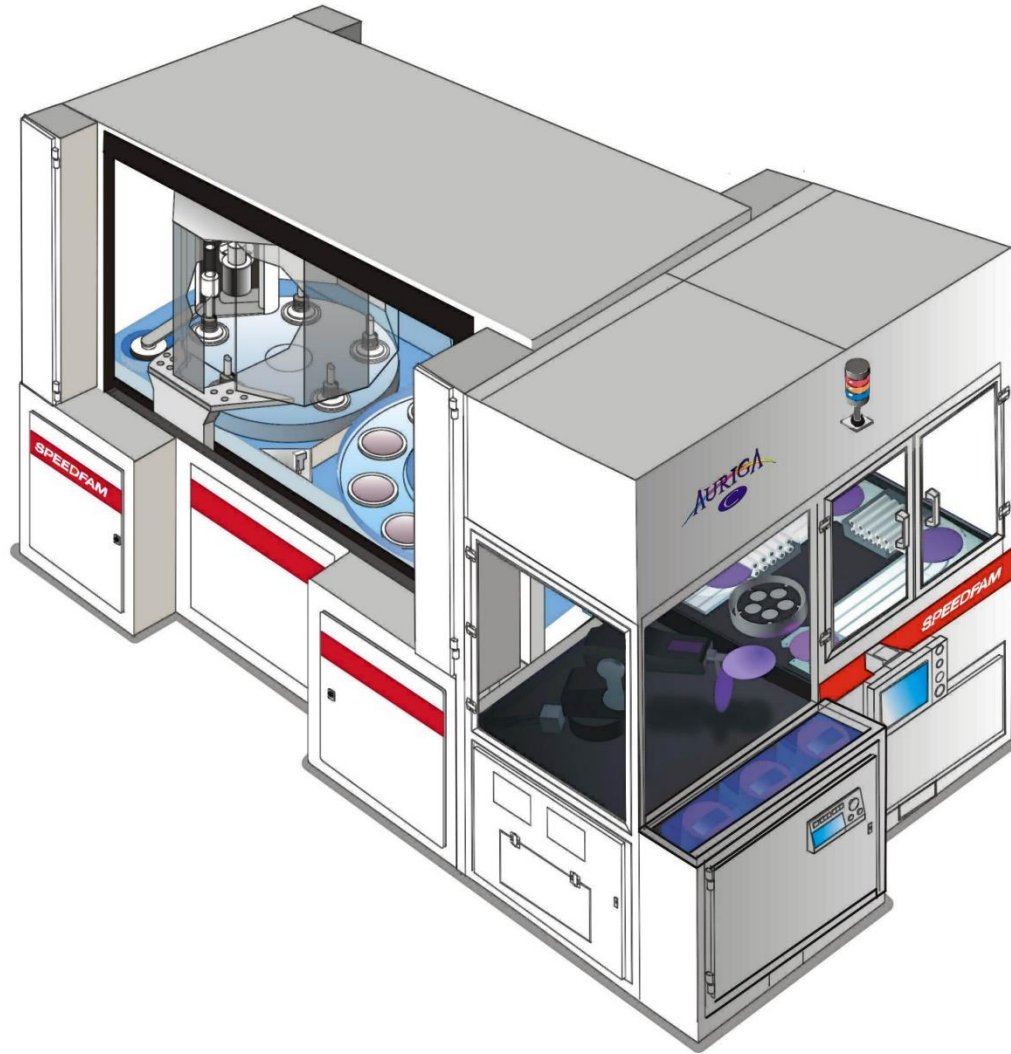
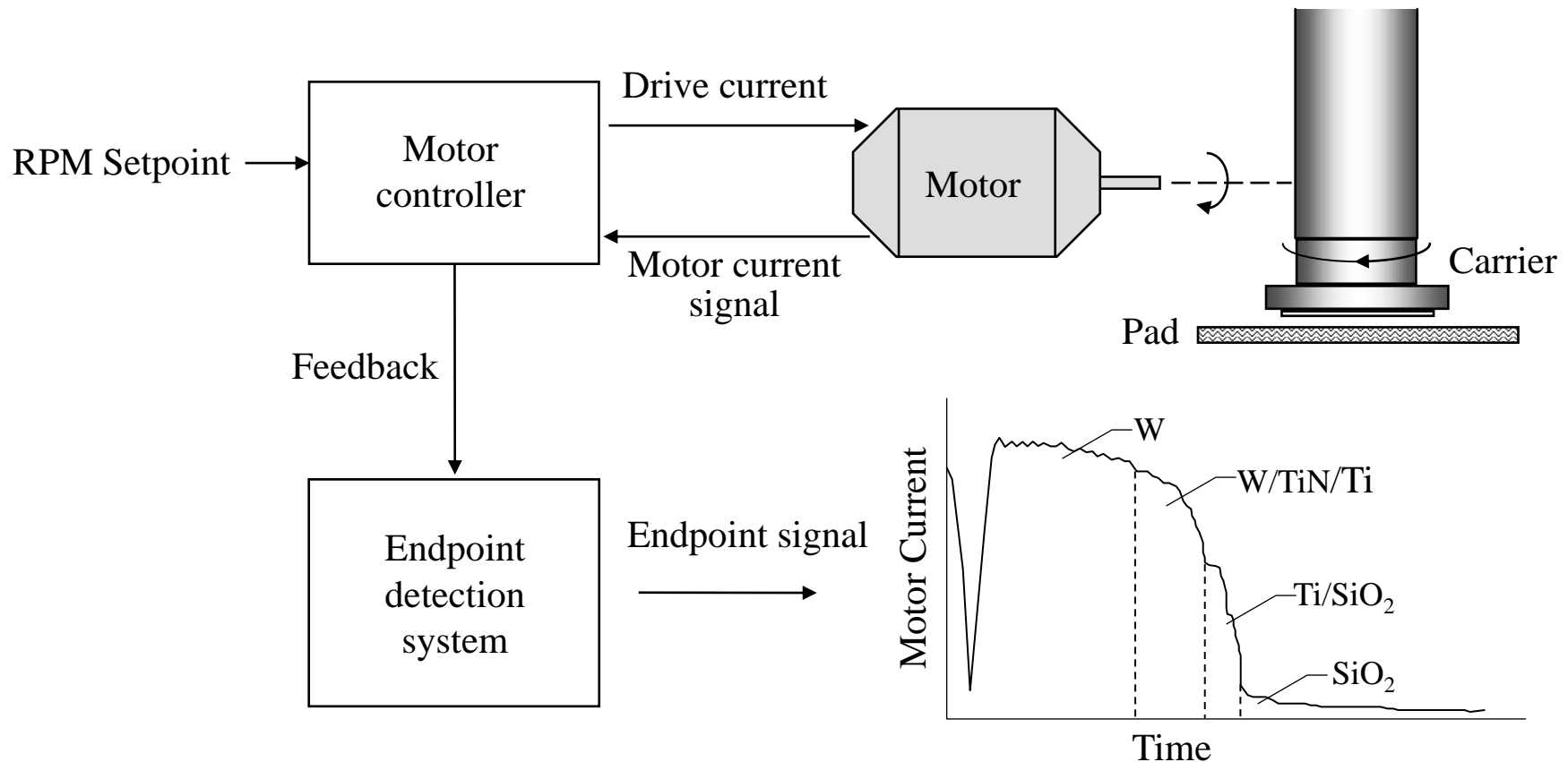


Photo courtesy of Speedfam-IPEC

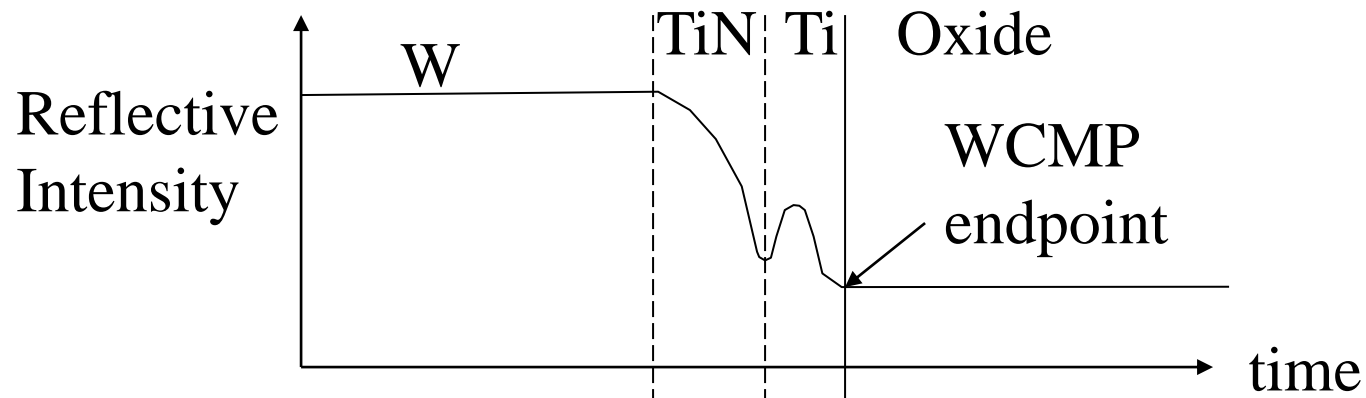
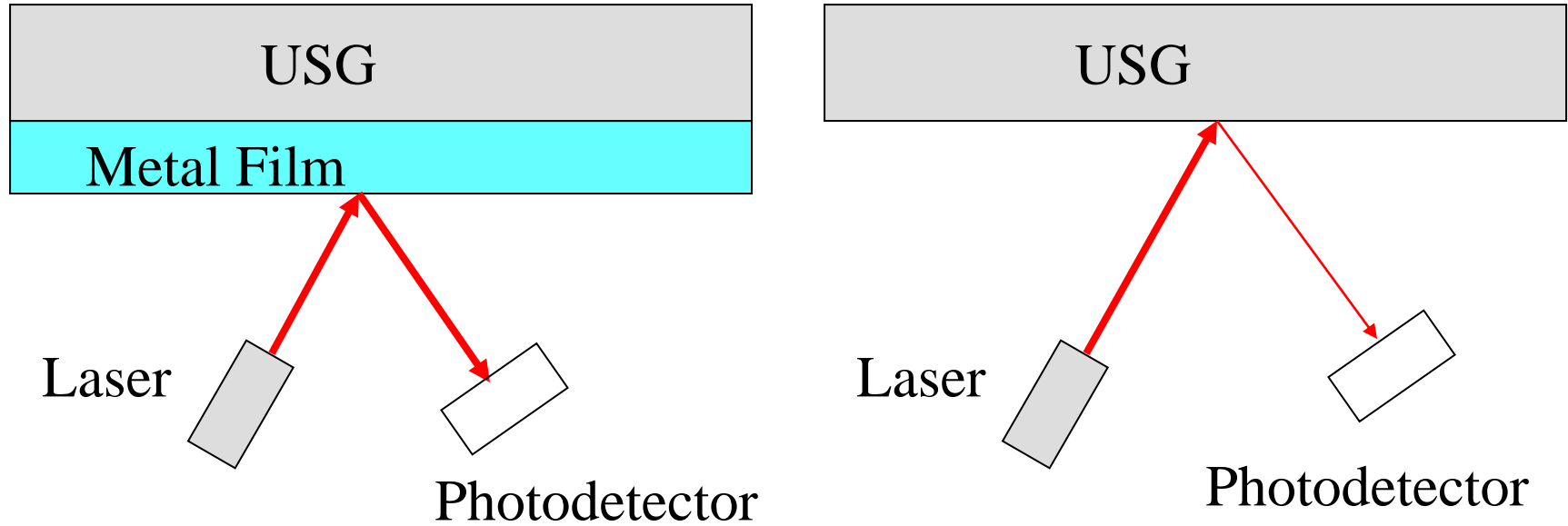


# Motor Current Endpoint Detection



- Wafer carrier rotates at a constant speed, so the drive current is sensitive to changes at the wafer surface due to **friction** or surface **roughness**
- This is not the case for CMP ILD, a predetermined oxide thickness needs to leave

- Endpoint of Metal CMP



# LI Metal Formation

Ti/TiN is used: Ti for adhesion and TiN for diffusion barrier

Tungsten (W) is preferred over Aluminum (Al) for LI metal due to its ability to fill holes without leaving voids

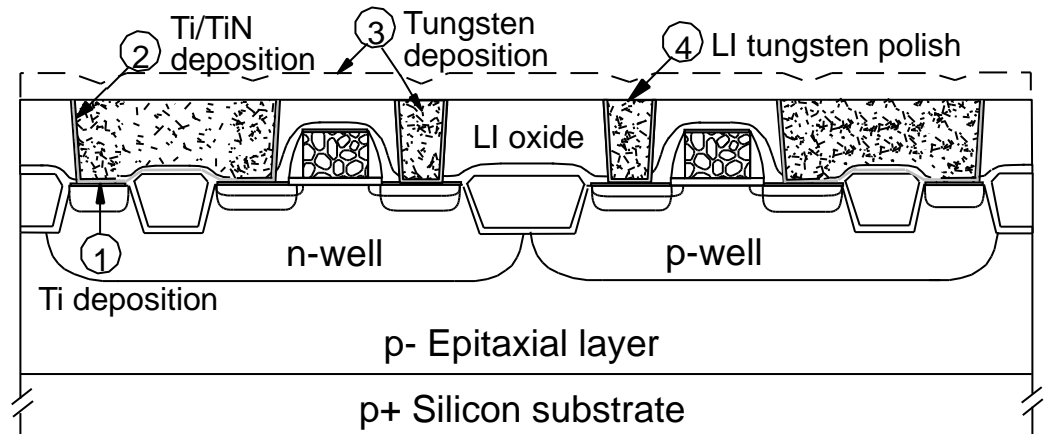
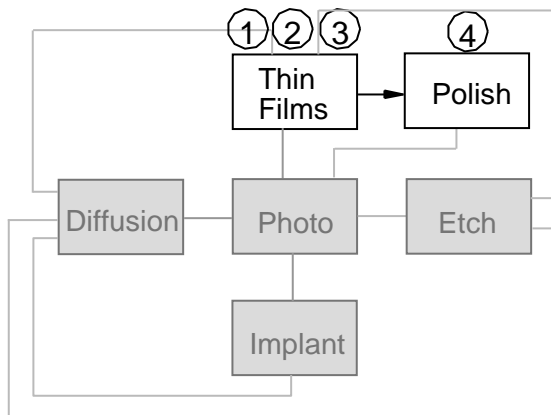


Figure 9.22

# LI Oxide Dielectric Formation

1. **Nitride: protect active region**
2. **Doped oxide**
3. **Oxide polish**
4. **9<sup>th</sup> mask**

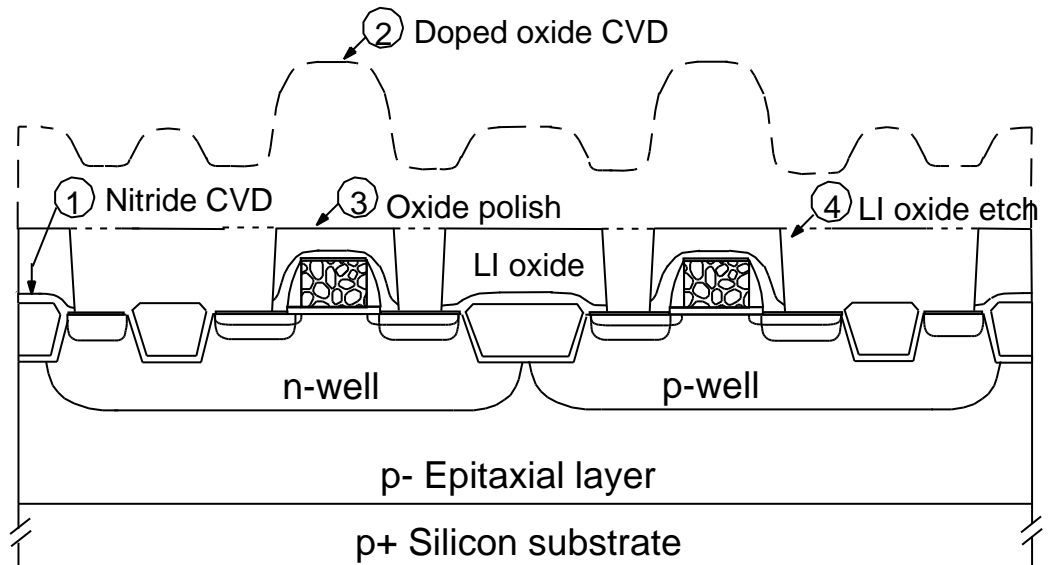
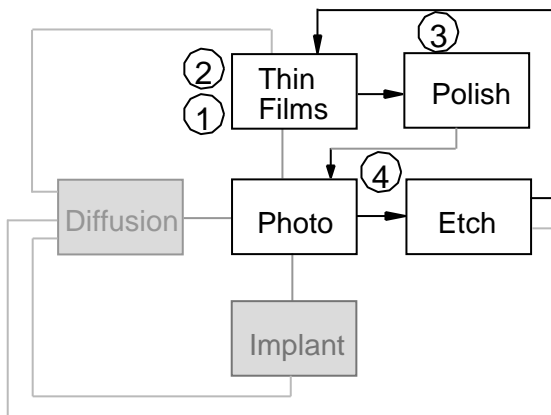
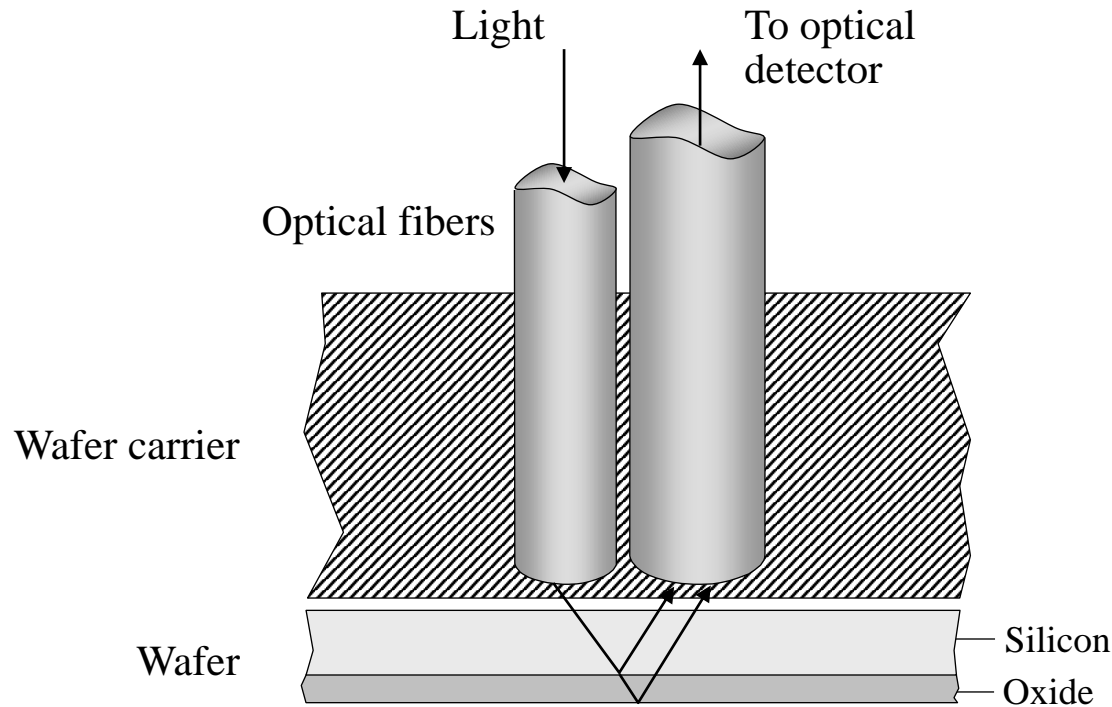


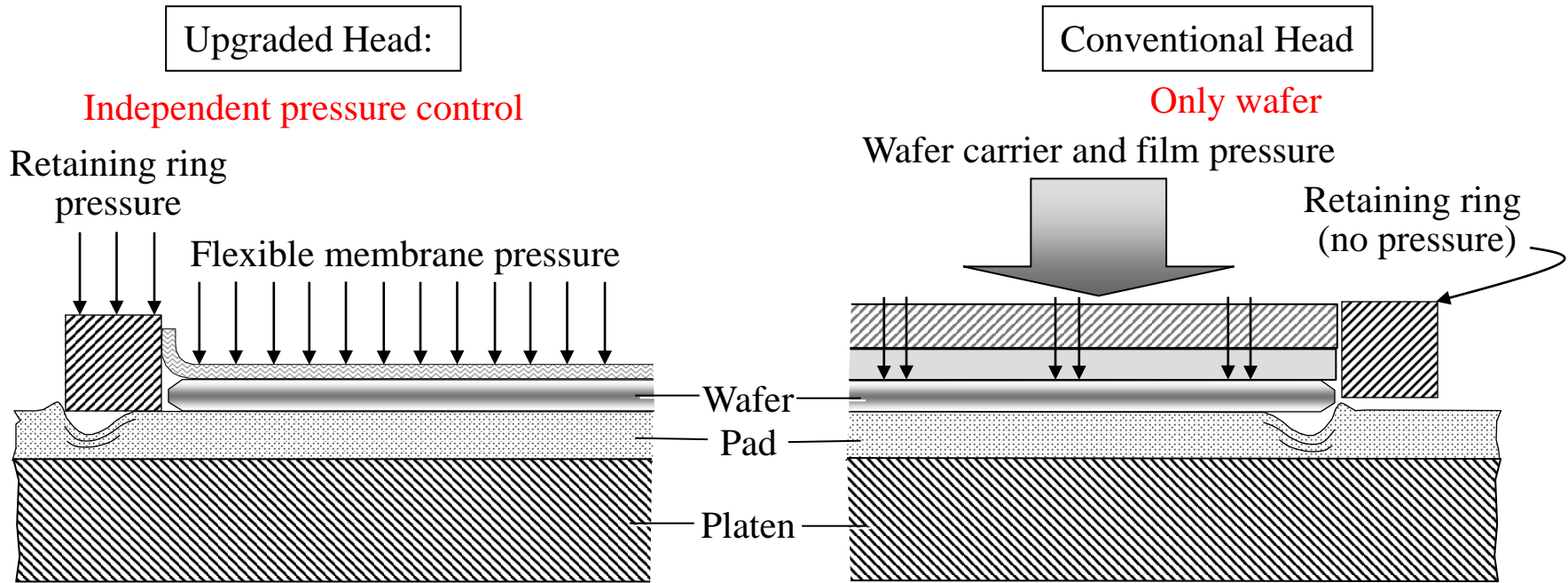
Figure 9.21

# Optical Interferometry for Endpoint Detection



- Based on light reflectance
- For example, endpoint detection of STI, oxide over nitride is within  $\pm 100 \text{ \AA}$

# CMP Head Carrier Design and Wafer Edge Nonuniformity

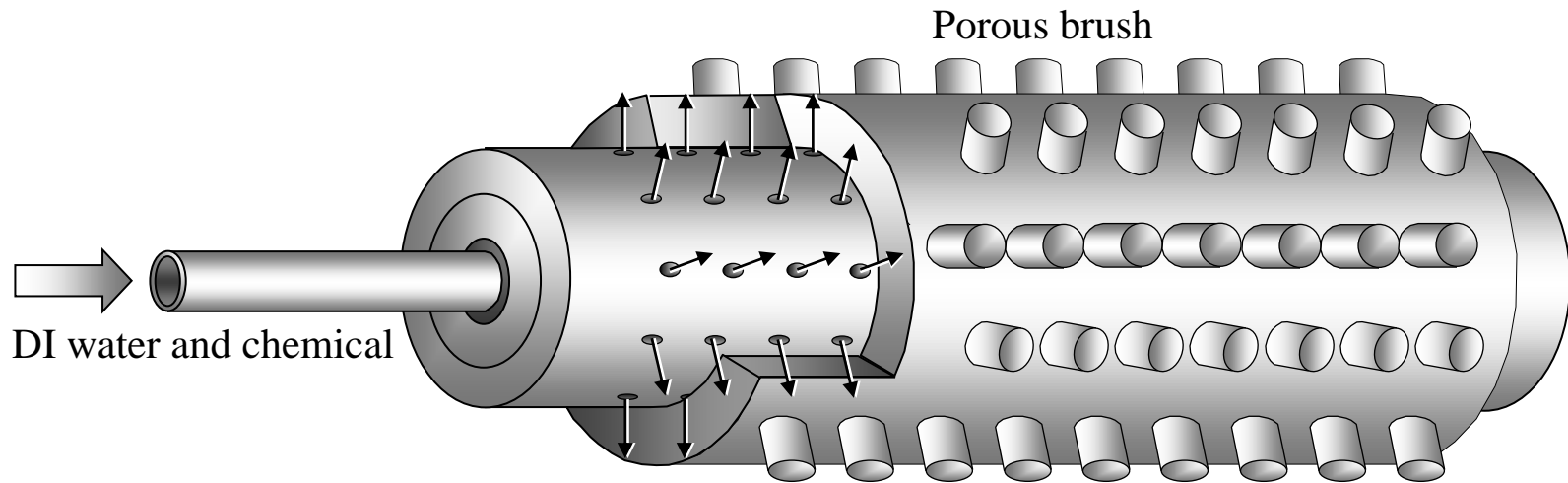


**Edge exclusion: 3 mm for high density ICs**

# Evolution of Post-CMP Cleaning

	Wet bench with megasonics	Doublesided scrubber + DI water	DSS + NH <sub>4</sub> OH	DSS + NH <sub>4</sub> OH and HF	DSS + Additional Chemistries
Oxide CMP	√	√	√	√	
Tungsten CMP			√	√	
Copper CMP					√

# Through-the-Brush Chemical Delivery for Post-CMP Cleaning



Redrawn from D. Hynes, et al, "Brush Scrubbing Emerges as Future Wafer-Cleaning Technology, *Solid State Technology*, (July 1997): p. 210.



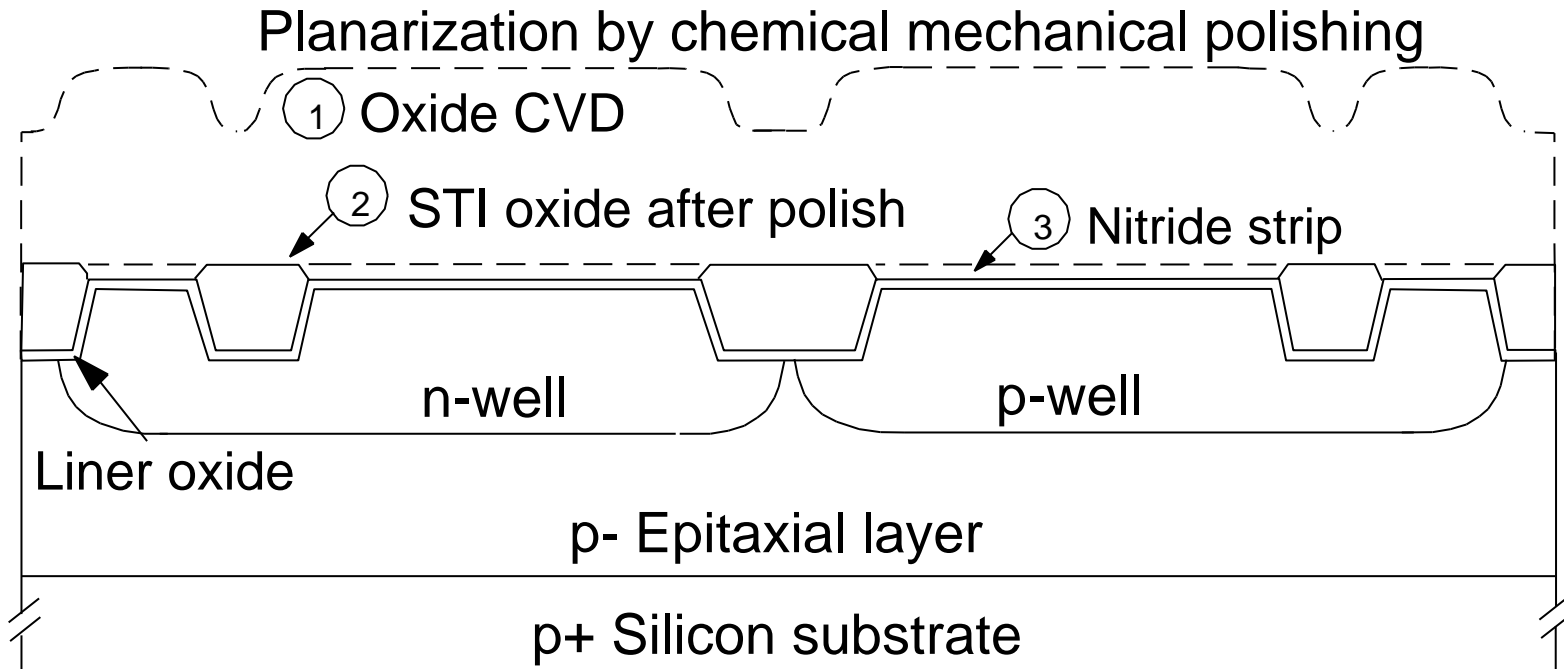
# Examples of Some Commercial CMP Equipment Systems

Supplier / Model	Type of Motion	No. of Platens/Dia. (in.)	# of Wafer Carriers (or heads)	Dry-In/ Dry-Out	Endpoint Detection
<b>Applied Materials</b> Mirra 3400	Rotary	3 / 20"	4	Yes	Yes
<b>Ebara</b> EPO-222	Rotary	2 / 23.6"	1	Yes	Yes
<b>Speedfam-IPEC</b> Avanti 472 Avanti 672 IPEC 676/776 Auriga-C	Orbital Orbital Orbital Rotary	2 / 22.5" 3 or 6 / 32" 4 / 16"	1 3 or 6 4	Yes Yes Yes	Yes Yes Yes
<b>Lam</b> Teres	Linear	2 belts	4	Yes	Yes
<b>SpeedFam</b> Auriga	Orbital	2 / 32"	5	Yes	Yes
<b>Strasbaugh</b> Symphony	Rotary	3 / 32"	4	Yes	Yes

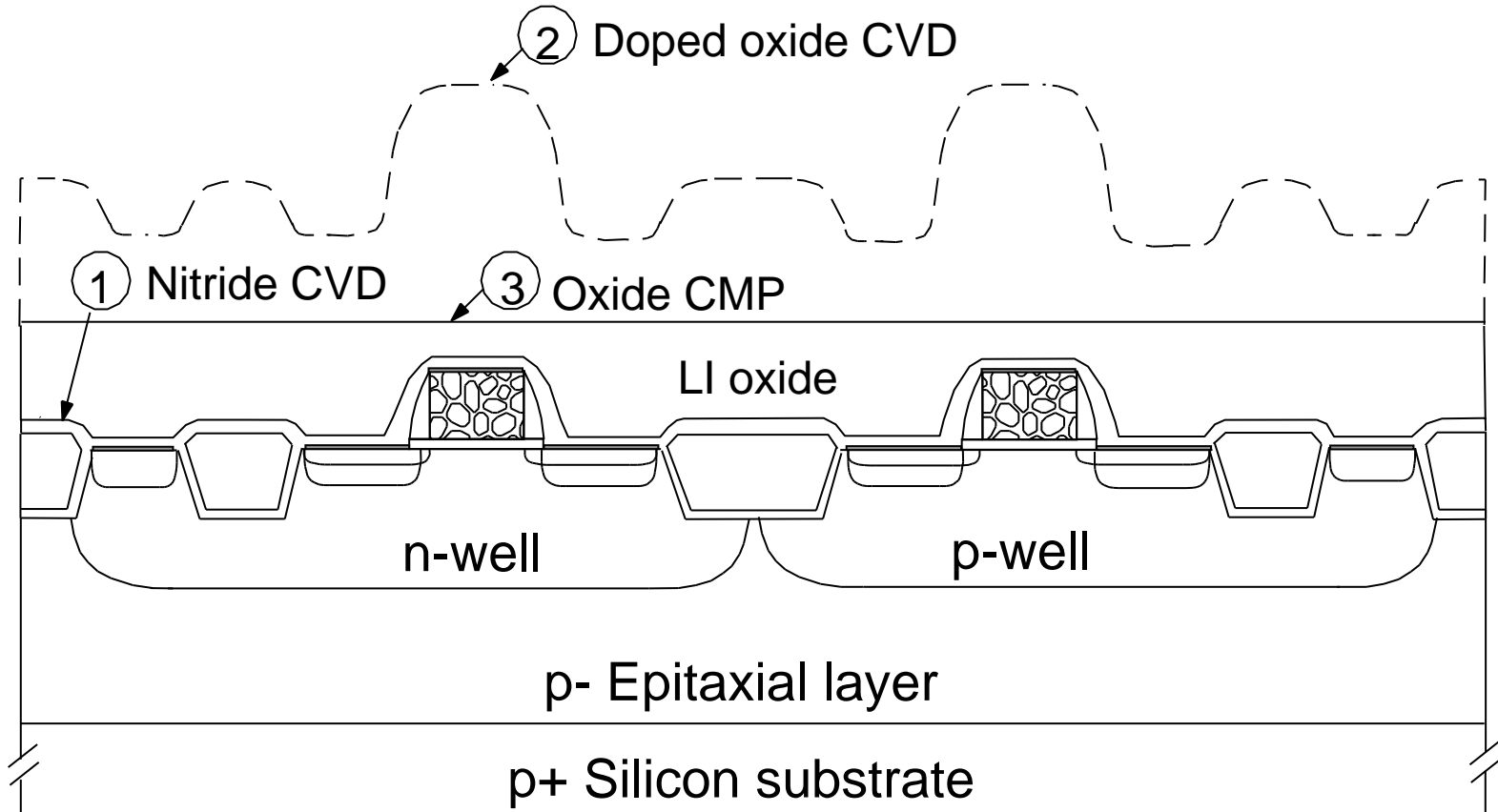
# CMP Applications

- STI oxide polish
- ILD-1 oxide polish
- LI tungsten polish
- ILD oxide polish
- Tungsten plug polish
- Dual Damascene copper polish

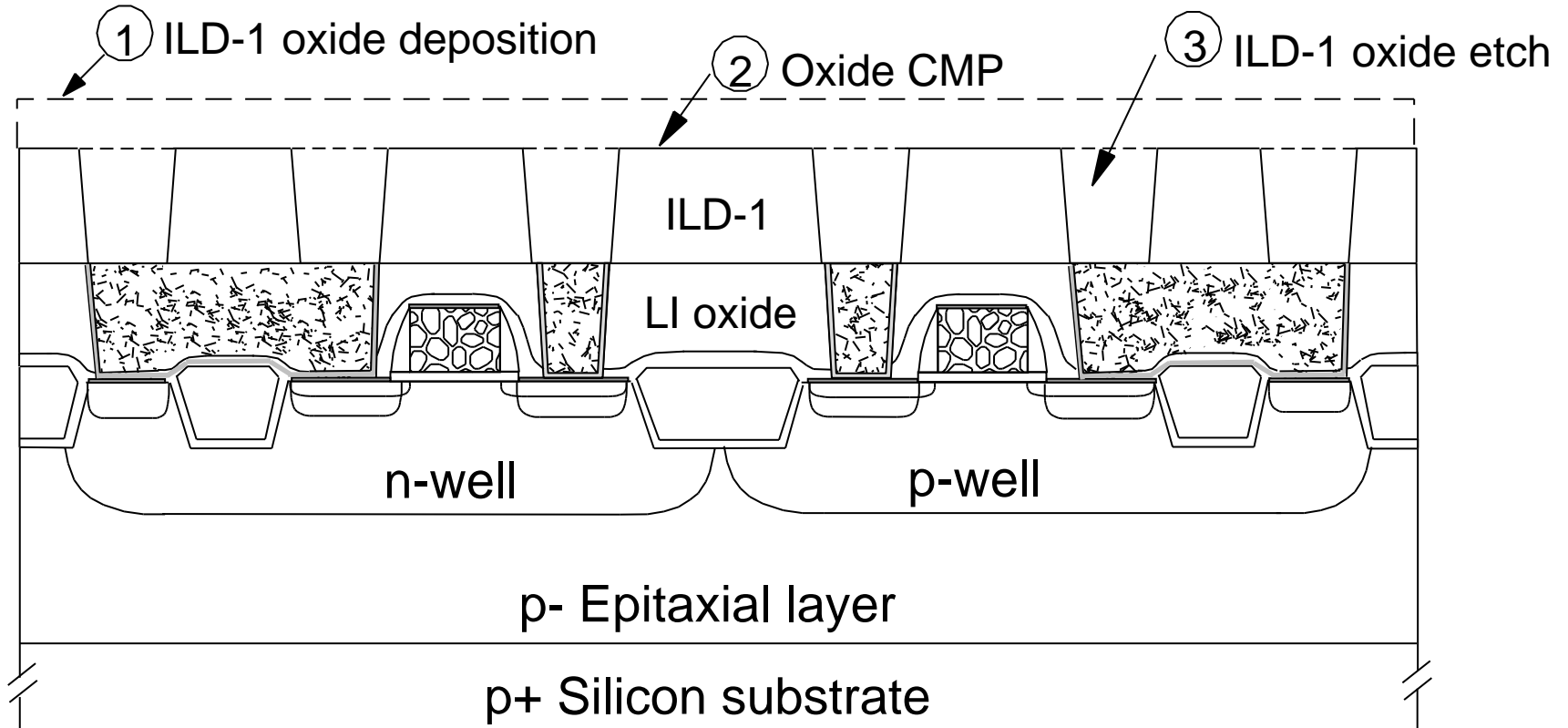
# CMP for Oxide Fill of STI



# LI Oxide before and after CMP Planarization

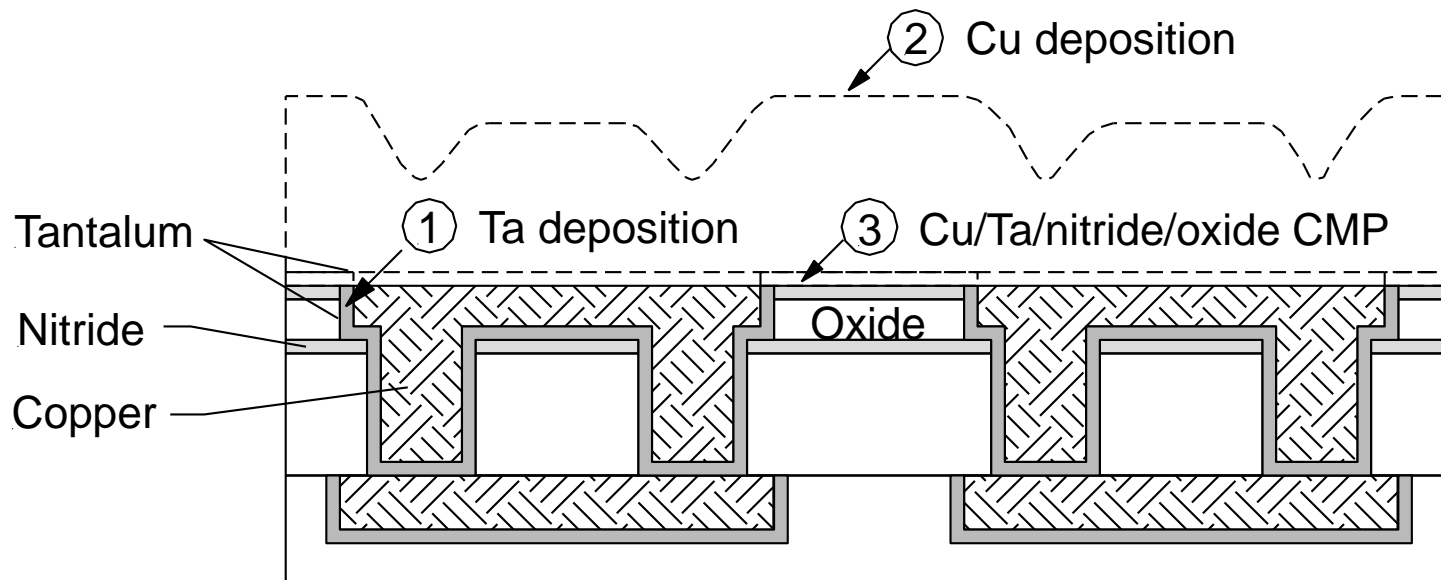


# ILD Oxide Polish

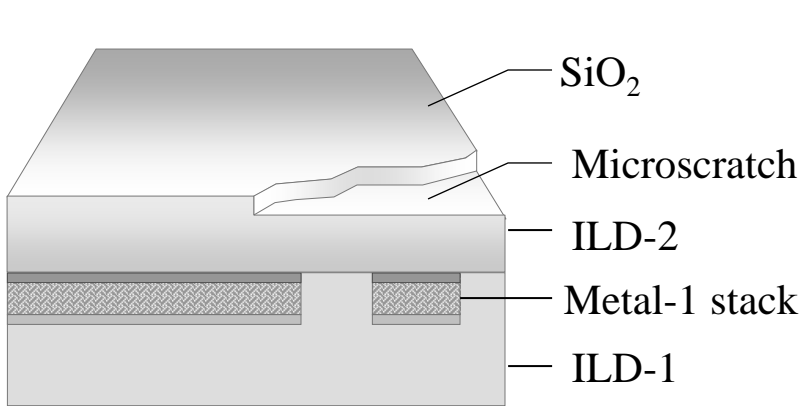


# CMP for Dual Damascene Copper Metallurgy

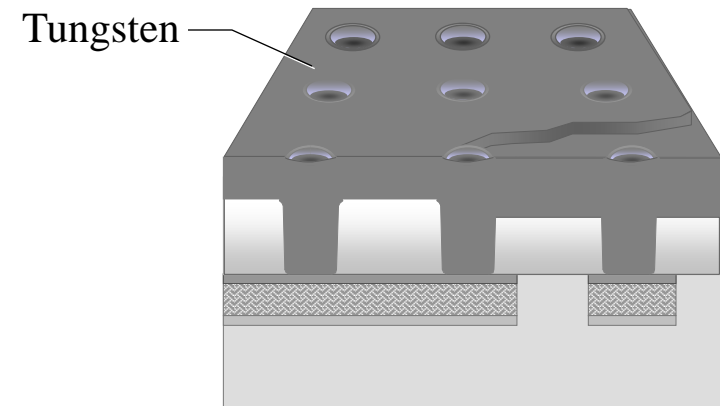
- Via and trench patterns are first formed in the ILD material by lithography and dry etching
- A barrier metal ( $\sim 75\text{\AA}$ ), followed by a thin copper seed layer ( $\sim 500\text{\AA}$ )
- The selectivity of Cu and Ta affects how well planarity quality
- A two-step process, one for Cu and another for Ta



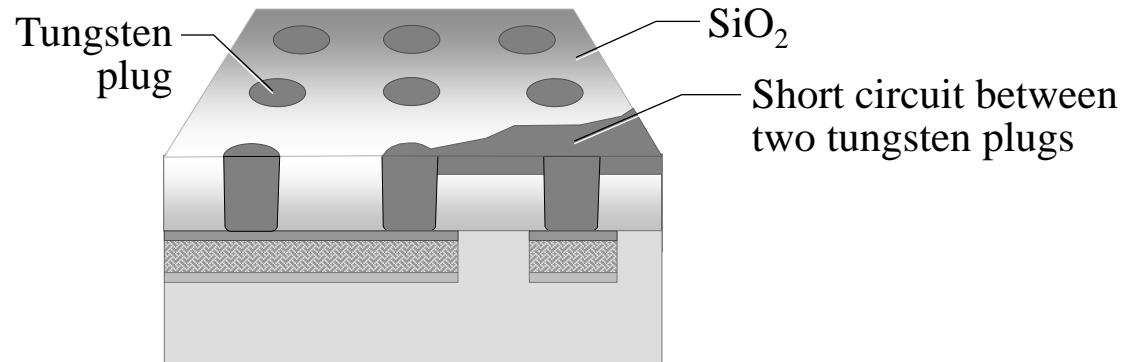
# Results of CMP Micro-Scratch



1) SiO<sub>2</sub> deposition followed by CMP



2) Via etch followed by tungsten via fill



3) Tungsten CMP