Chapter 10

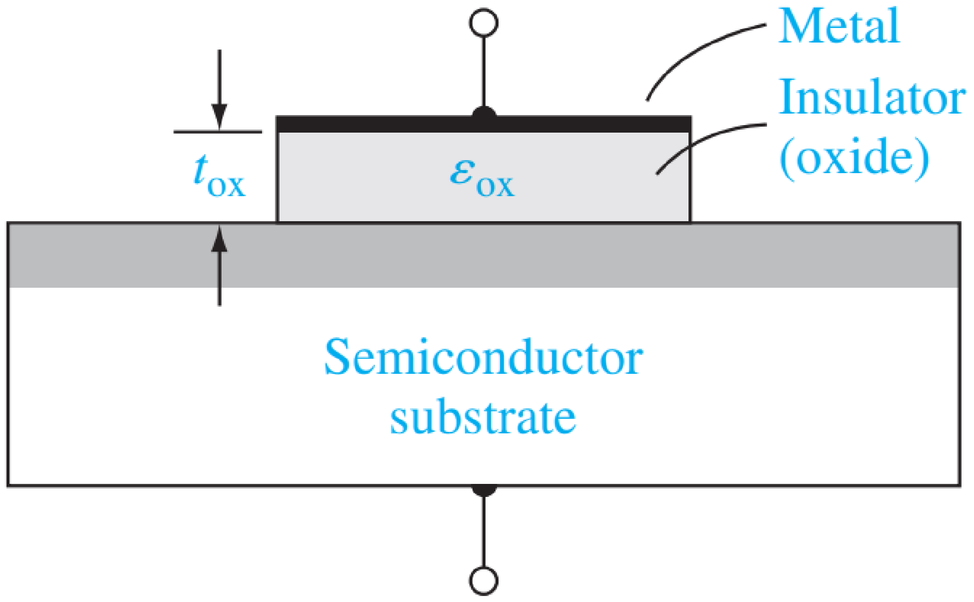
Fundamentals of the Metal-Oxide-Semiconductor Field-Effect Transistor

The Two-Terminal MOS Structure

- The heart of MOSFET is the MOS capacitor
- The metal may be aluminum (Al) or high-conductivity poly-Si.

t_{ox} Thickness

ε_{ox} Permittivity



The Two-Terminal MOS Structure

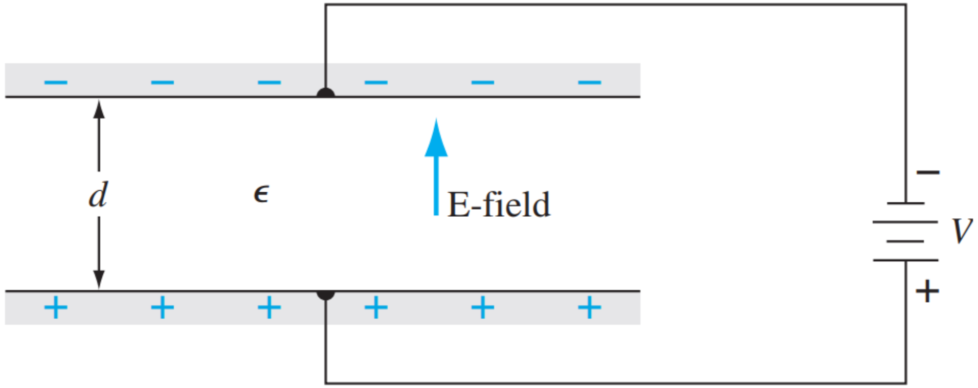
- 電容每單位面積

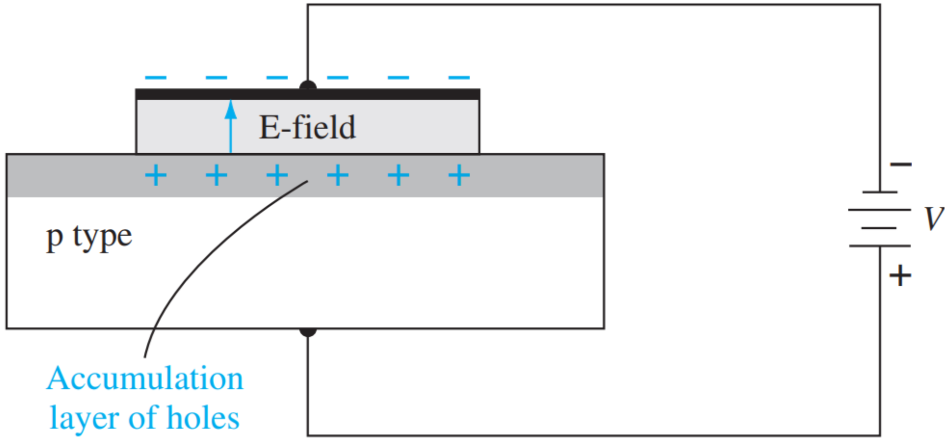
$$C' = \frac{\varepsilon_{ox}}{d}$$

- 電場大小

$$E = \frac{V}{d}$$

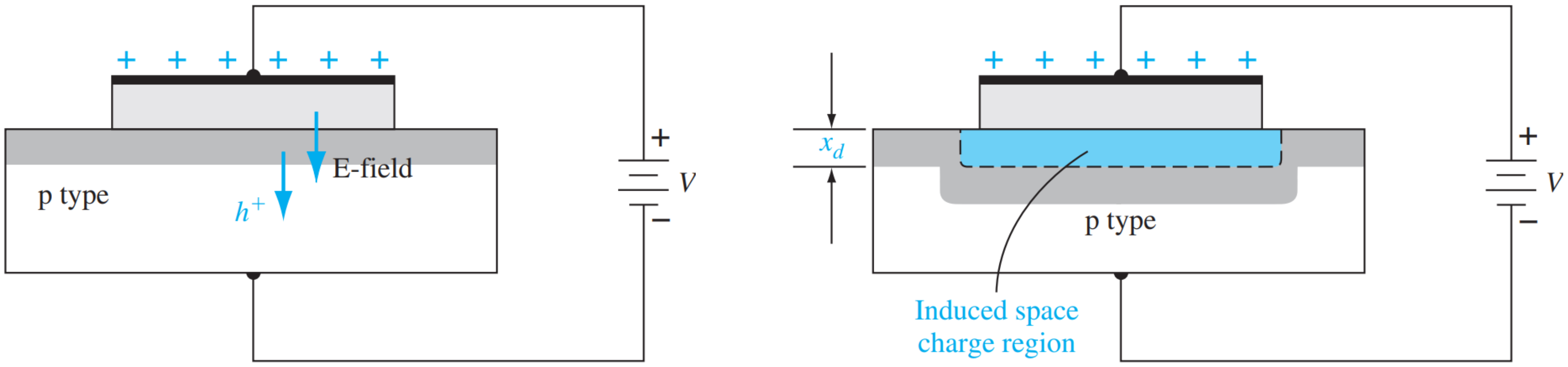
- $V_{gs} < 0$，因施加的外部電場將p型基板內的電洞推向氧化物-半導體介面，而產生一層電洞的累積。(accumulation layer)





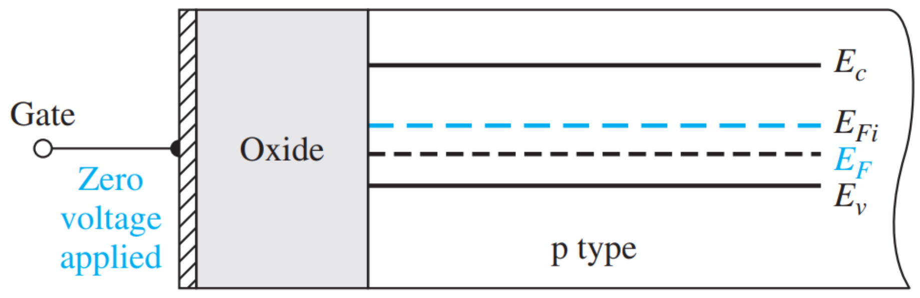
The Two-Terminal MOS Structure

- $V_{gs} > 0$，改變外部電場方向
- 導致氧化物-半導體介面下方產生帶負電的空乏區

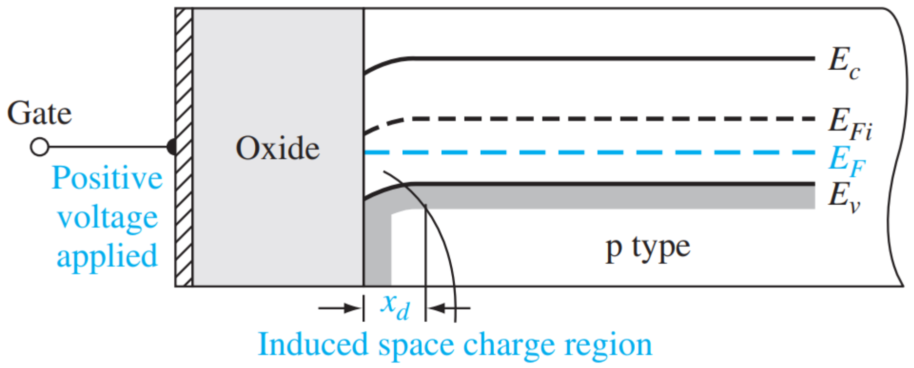


MOS (p-substrate)

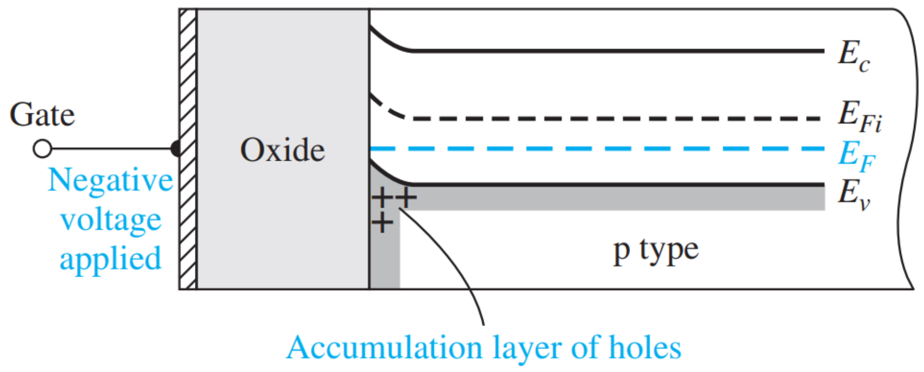
$V_{gs} = 0$



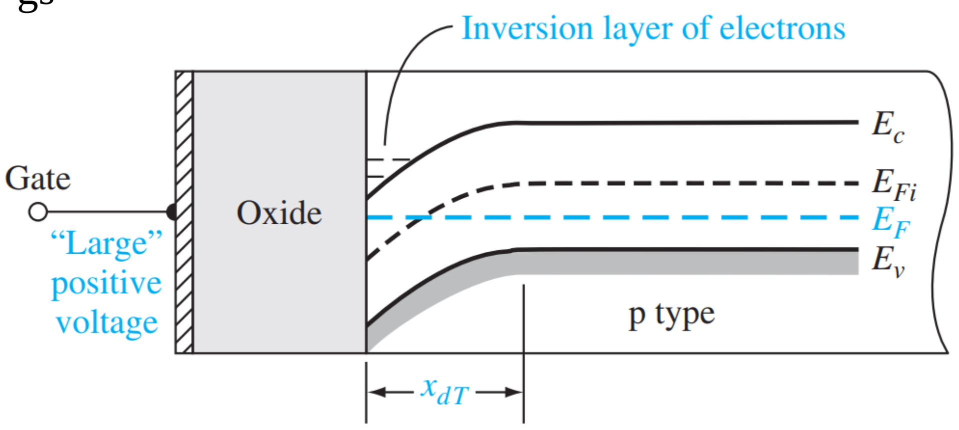
$V_{gs} > 0$



$V_{gs} < 0$

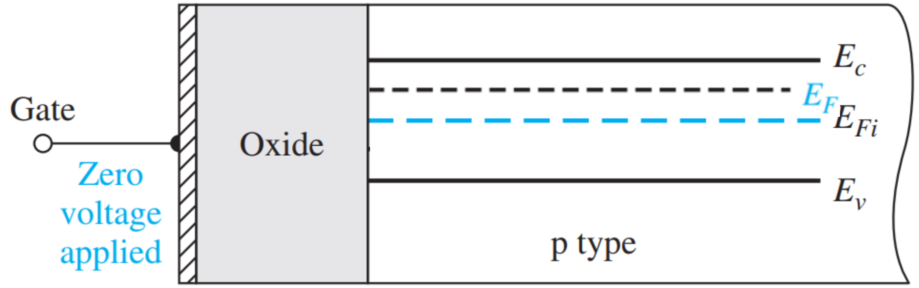


$V_{gs} > 0$

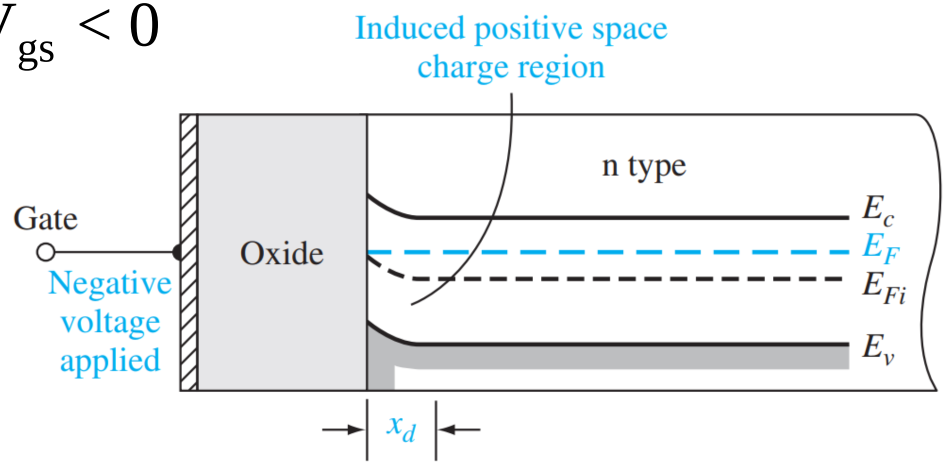


MOS (n-substrate)

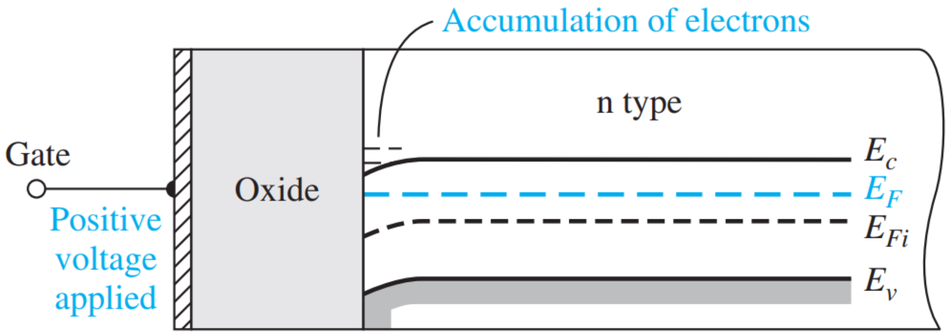
$V_{gs} = 0$



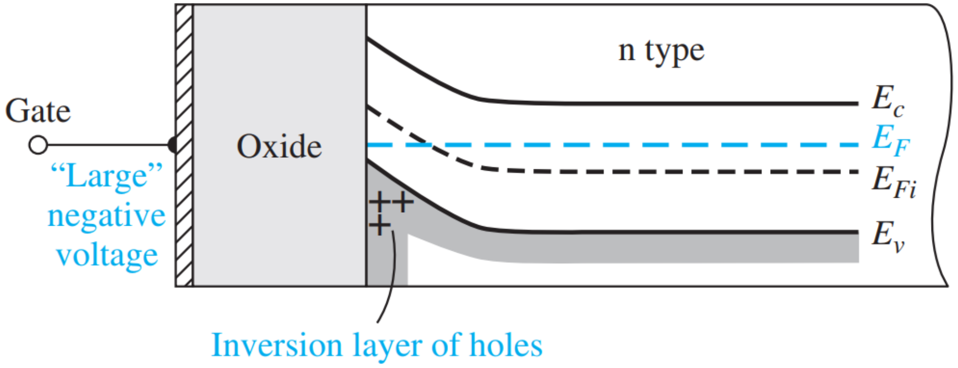
$V_{gs} < 0$



$V_{gs} > 0$



$V_{gs} < 0$

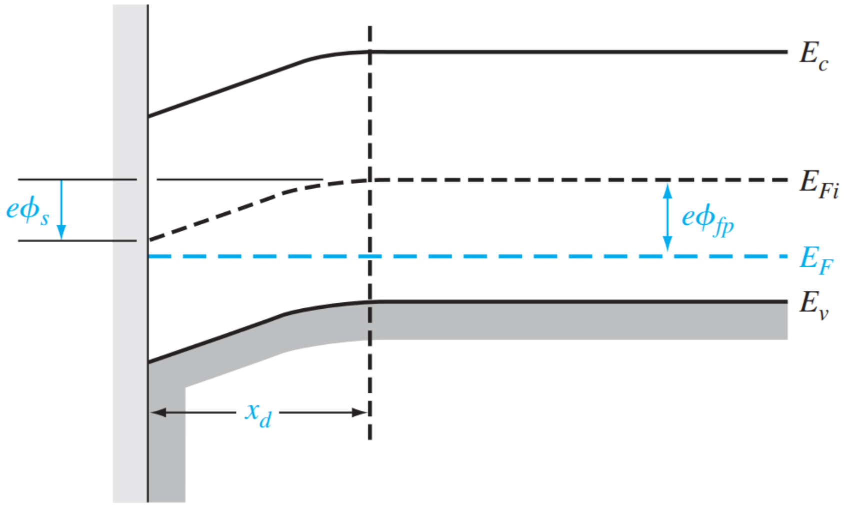


MOS (p-substrate)

$V_{gs} > 0$

$$\phi_{fp} = kT \ln\left(\frac{N_a}{n_i}\right)$$ Ch. 07

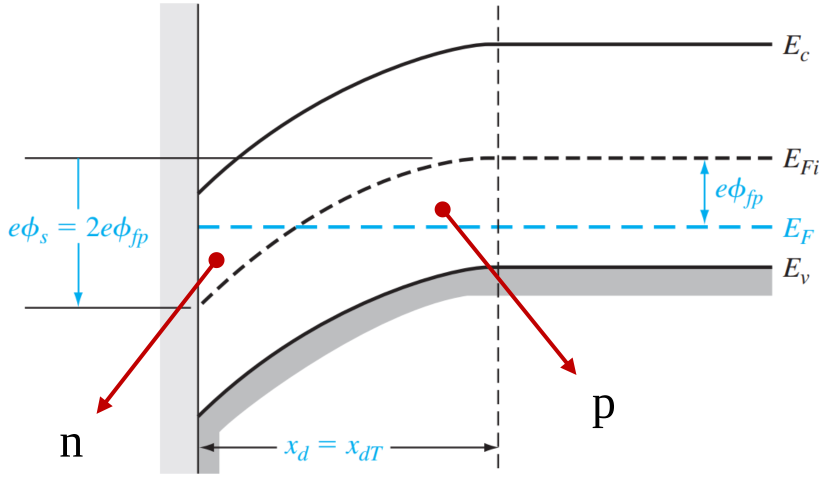
$$x_d = \sqrt{\frac{2\varepsilon_s \phi_s}{eN_a}}$$ one-sided junction



Threshold inversion point $\phi_s = 2\phi_{fp}$

Threshold voltage V_{th}

$$x_{dT} = \sqrt{\frac{4\varepsilon_s \phi_{fp}}{eN_a}}$$



MOS (n-substrate)

$V_{gs} < 0$

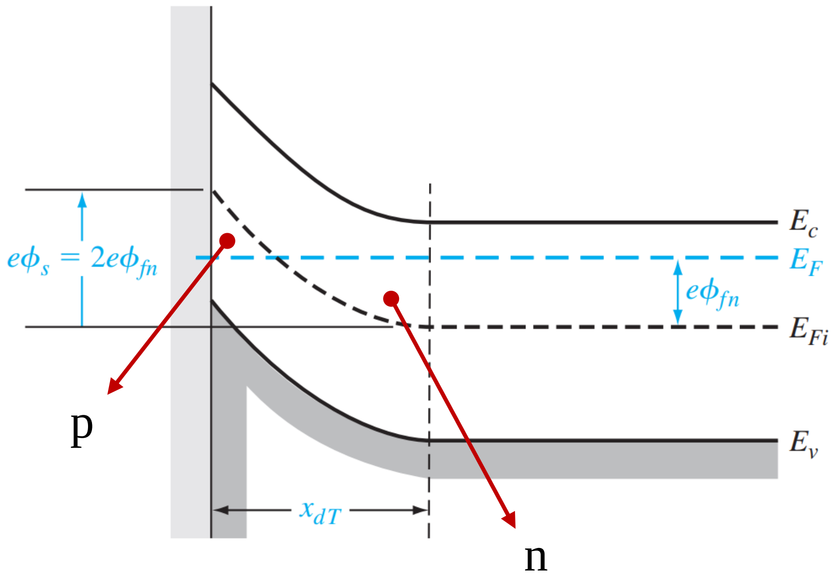
$$\phi_{fn} = kT \ln\left(\frac{N_d}{n_i}\right)$$ From Ch. 7

$$x_d = \sqrt{\frac{2\varepsilon_s \phi_s}{eN_d}}$$ one-sided junction

Threshold inversion point $\phi_s = 2\phi_{fn}$

Threshold voltage V_{th}

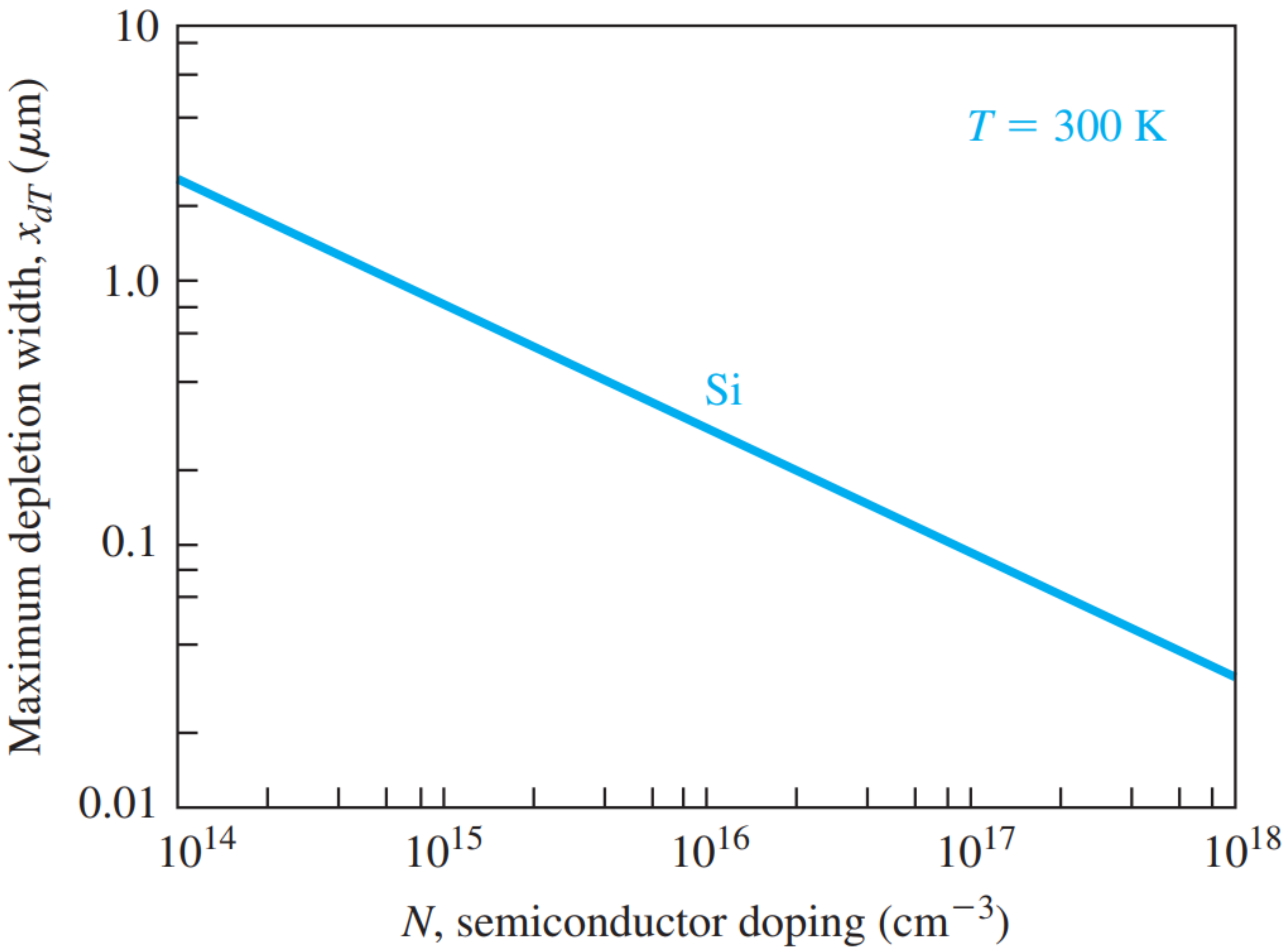
$$x_{dT} = \sqrt{\frac{4\varepsilon_s \phi_{fn}}{eN_d}}$$



空乏區寬度

$$x_{dT} = \sqrt{\frac{4\varepsilon_s \phi_{fp}}{eN_a}}$$

$$x_{dT} = \sqrt{\frac{4\varepsilon_s \phi_{fn}}{eN_d}}$$



Example 10.1

Objective: Calculate the maximum space charge width for a given semiconductor doping concentration.

Consider silicon at $T = 300$ K doped to $N_a = 10^{16}$ cm^{-3}. The intrinsic carrier concentration is $n_i = 1.5 \times 10^{10}$ cm^{-3}.

Example 10.1

Objective: Calculate the maximum space charge width for a given semiconductor doping concentration.

Consider silicon at $T = 300$ K doped to $N_a = 10^{16}$ cm^{-3}. The intrinsic carrier concentration is $n_i = 1.5 \times 10^{10}$ cm^{-3}.

$$\phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right) = (0.0259)\ln\left(\frac{10^{16}}{1.5 \times 10^{10}}\right) = 0.3473 \text{ V}$$

$$x_{dT} = \left[\frac{4\epsilon_s \phi_{fp}}{eN_a}\right]^{1/2} = \left[\frac{4(11.7)(8.85 \times 10^{-14})(0.3473)}{(1.6 \times 10^{-19})(10^{16})}\right]^{1/2}$$

$$x_{dT} \cong 0.30 \times 10^{-4} \text{ cm} = 0.30 \ \mu\text{m}$$

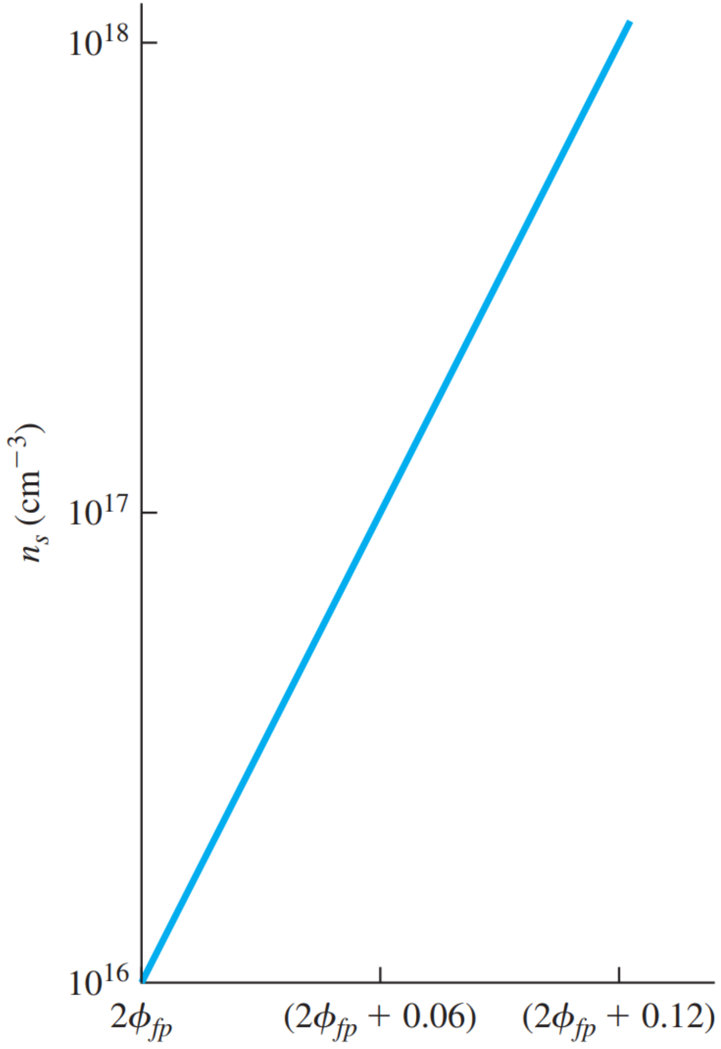
空乏區表面電荷密度

From Ch. 4

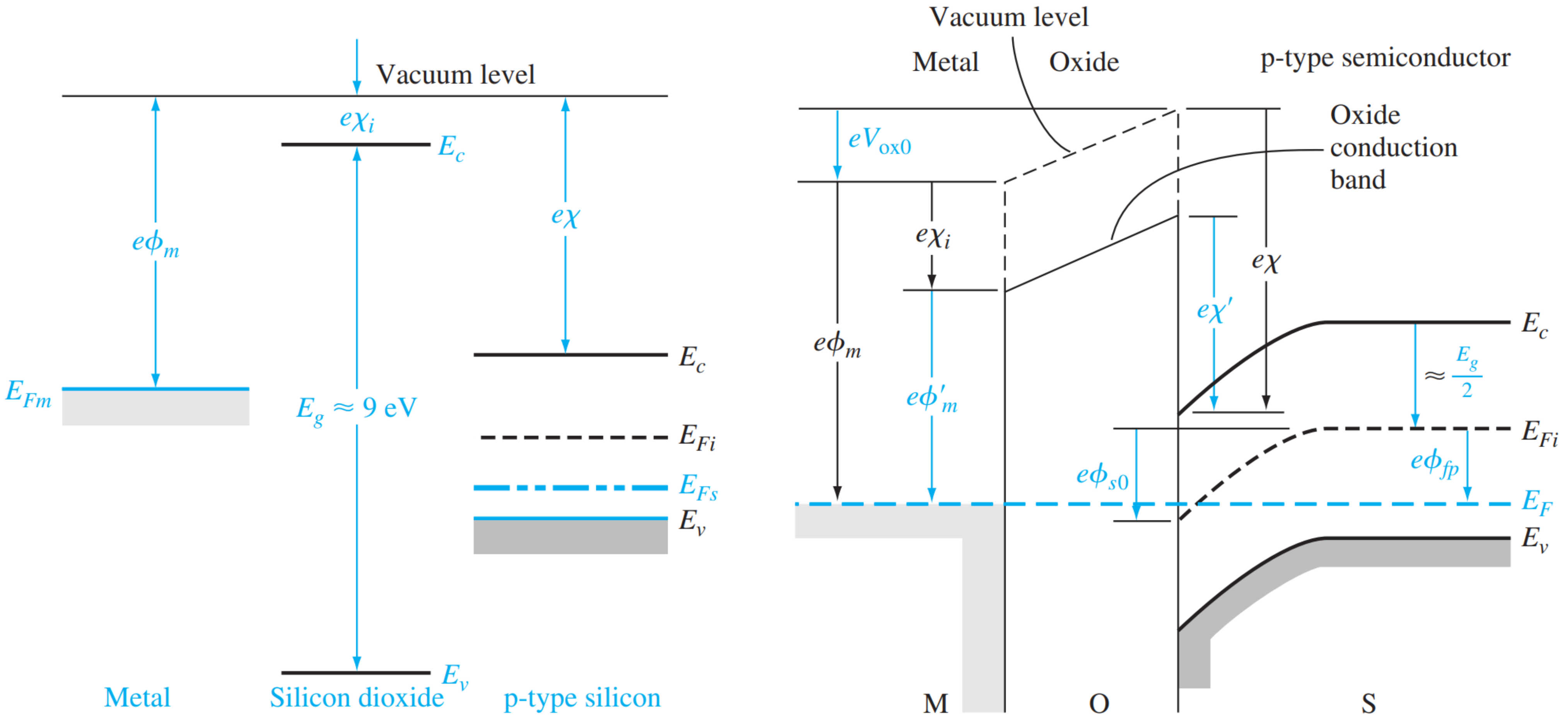
$$n = n_i \exp\left(\frac{E_F - E_{Fi}}{kT}\right) = n_i \exp\left[\frac{e\left(\phi_{fp} + \Delta\phi_s\right)}{kT}\right]$$

$$n_s = n_i \exp\left(\frac{e\phi_{fp}}{kT}\right)\exp\left(\frac{e\Delta\phi_s}{kT}\right) = n_{st} \exp\left(\frac{e\Delta\phi_s}{kT}\right)$$

- n_{st}: threshold inversion charge density
- The inversion charge density increases by a factor of 10 with a 60-mV increase in surface potential
- The charge density increases rapidly, means the space charge width essentially reaches a maximum value.



Work Function Difference



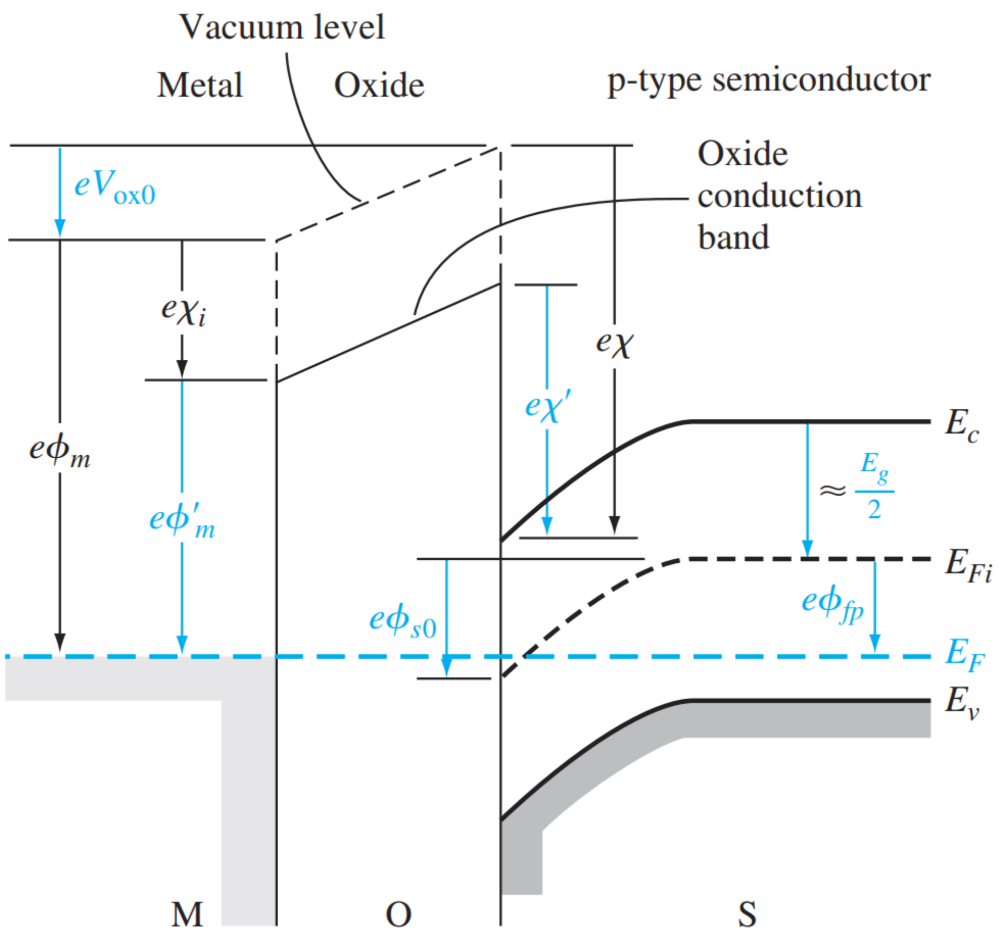
Work Function Difference

$$e\phi'_m + eV_{ox0} = e\chi' + \frac{E_g}{2} - \left(e\phi_{s0} - e\phi_{fp}\right)$$

$$V_{ox0} + \phi_{s0} = -\left[\phi'_m - \left(\chi' + \frac{E_g}{2e} + \phi_{fp}\right)\right]$$

Metal-semiconductor work function difference

$$\phi_{ms} = \phi'_m - \left(\chi' + \frac{E_g}{2e} + \phi_{fp}\right)$$ p-substrate



Example 10.2

Objective: Determine the metal–semiconductor work function difference, ϕ_{ms}, for a given MOS system and semiconductor doping.

For an aluminum–silicon dioxide junction, $\phi'_m = 3.20$ V and, for a silicon–silicon dioxide junction, $\chi' = 3.25$ V. We may assume that $E_g = 1.12$ V. Let the p-type doping be $N_a = 10^{15}$ cm^{-3}.

Example 10.2

Objective: Determine the metal–semiconductor work function difference, ϕ_{ms}, for a given MOS system and semiconductor doping.

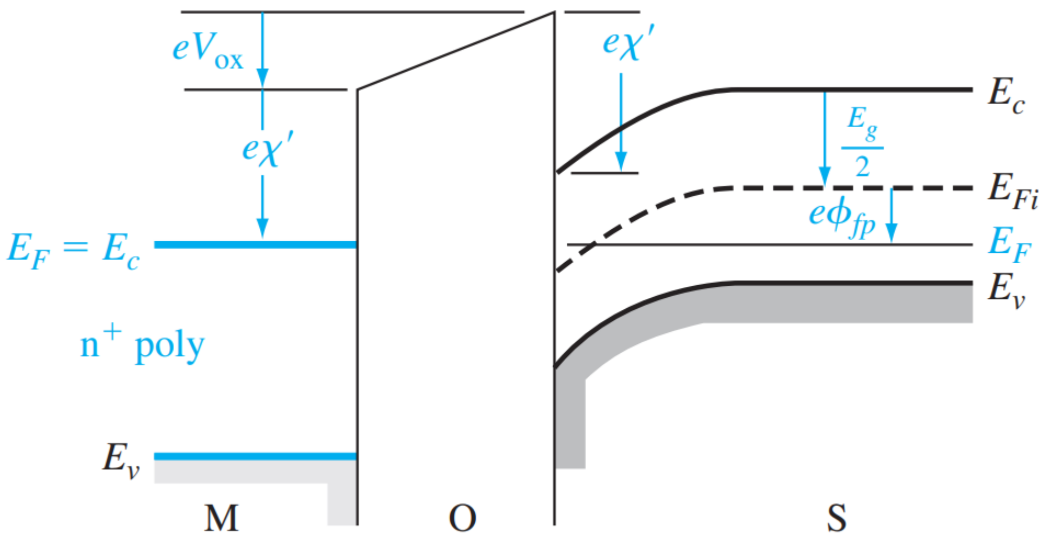
For an aluminum–silicon dioxide junction, $\phi'_m = 3.20$ V and, for a silicon–silicon dioxide junction, $\chi' = 3.25$ V. We may assume that $E_g = 1.12$ V. Let the p-type doping be $N_a = 10^{15}\ \text{cm}^{-3}$.

$$\phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right) = (0.0259)\ln\left(\frac{10^{15}}{1.5 \times 10^{10}}\right) = 0.288\ \text{V}$$

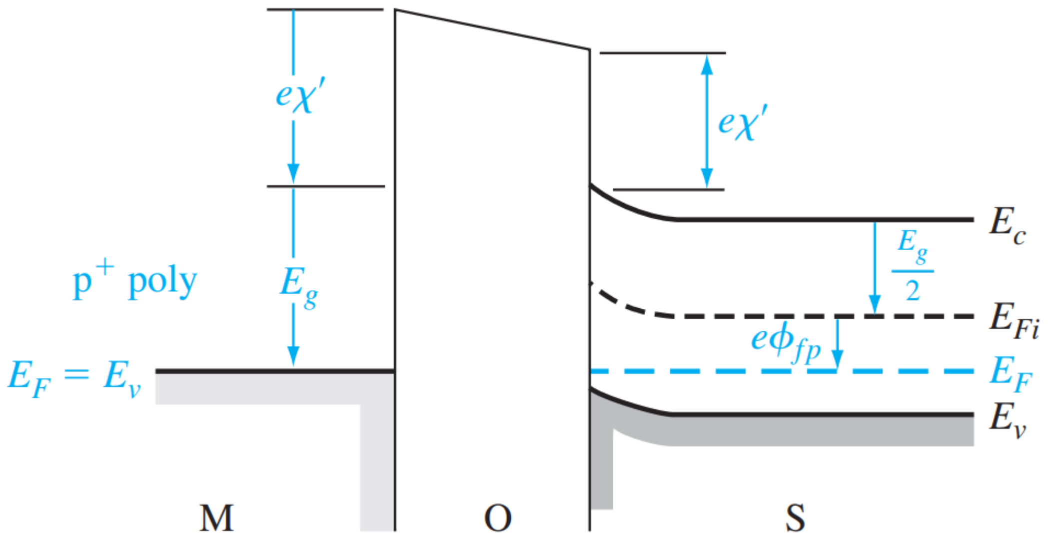
$$\phi_{ms} = \phi'_m - \left(\chi' + \frac{E_g}{2e} + \phi_{fp}\right) = 3.20 - (3.25 + 0.560 + 0.288)$$

$$\phi_{ms} = -0.898\ \text{V}$$

Polysilicon – Oxide – Semiconductor



$n^+ - O - p$



$p^+ - O - p$

$$\phi'_m = \chi'$$

$$\phi_{ms} = \phi'_m - \left(\chi' + \frac{E_g}{2e} + \phi_{fp}\right) = -\left(\frac{E_g}{2e} + \phi_{fp}\right)$$

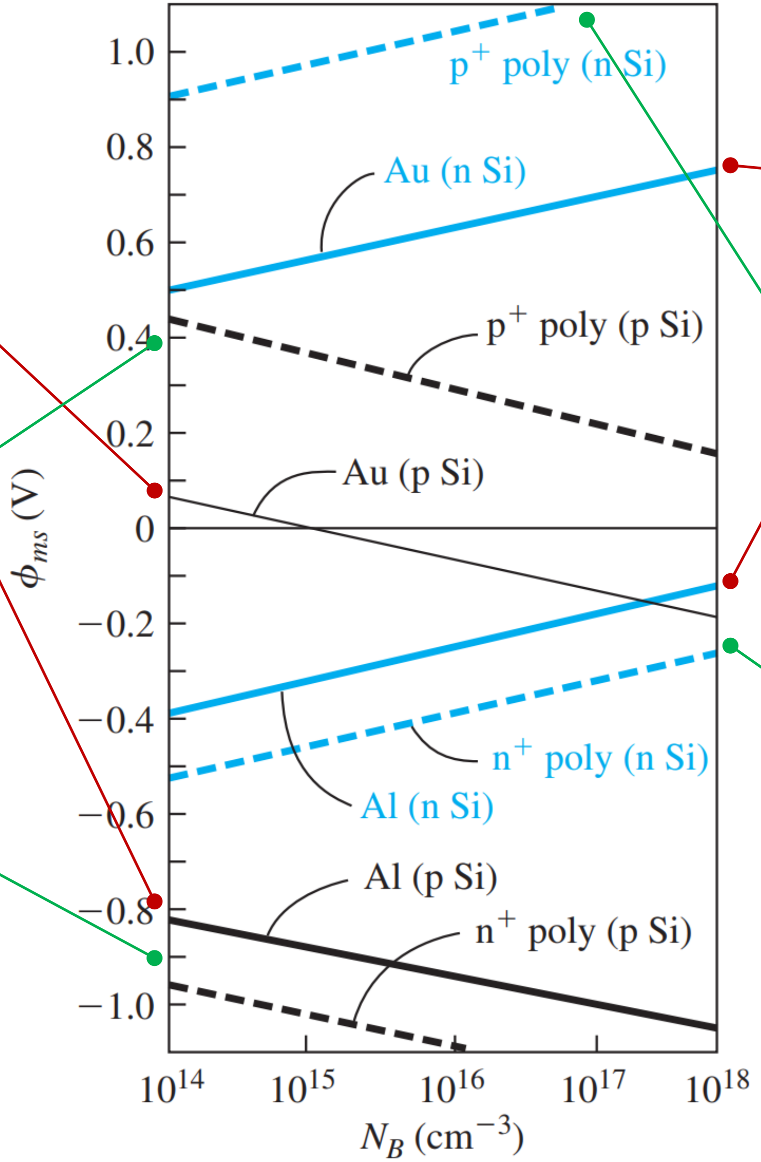
$$\phi'_m = \chi' + E_g / e$$

$$\phi_{ms} = \phi'_m - \left(\chi' + \frac{E_g}{2e} + \phi_{fp}\right) = \frac{E_g}{2e} - \phi_{fp}$$

Work Function Difference vs Doping

$$\phi'_m - \left(\chi' + \frac{E_g}{2e} + \phi_{fp} \right)$$

$$\phi'_m - \left(\chi' + \frac{E_g}{2e} - \phi_{fn} \right)$$



$p^+ - O - p$ $\qquad \dfrac{E_g}{2e} - \phi_{fp}$

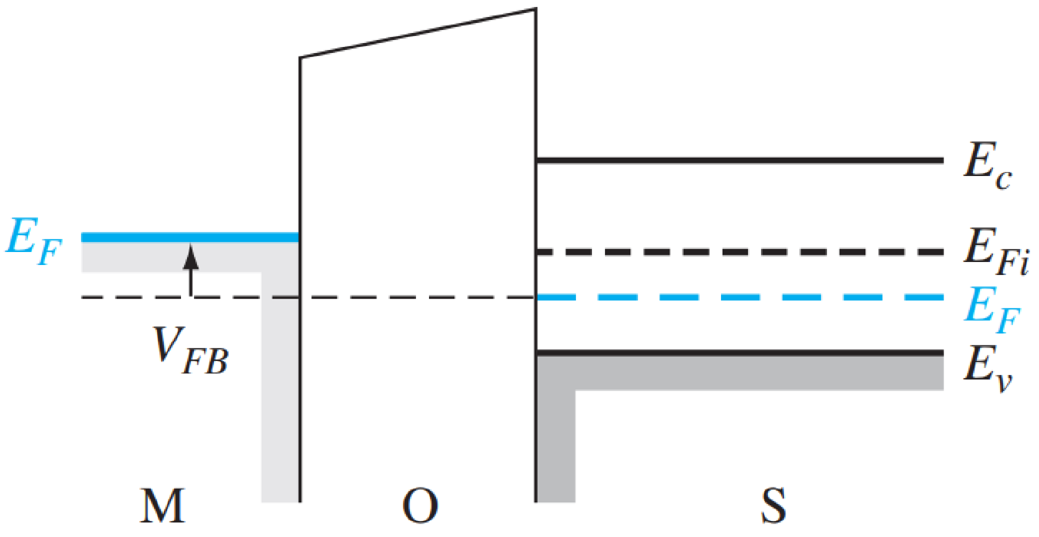
$\dfrac{E_g}{2e} + \phi_{fn}$ $\qquad p^+ - O - n$

$n^+ - O - p$ $\qquad -\dfrac{E_g}{2e} - \phi_{fp}$

$-\dfrac{E_g}{2e} + \phi_{fn}$ $\qquad n^+ - O - n$

Flat-Band Voltage

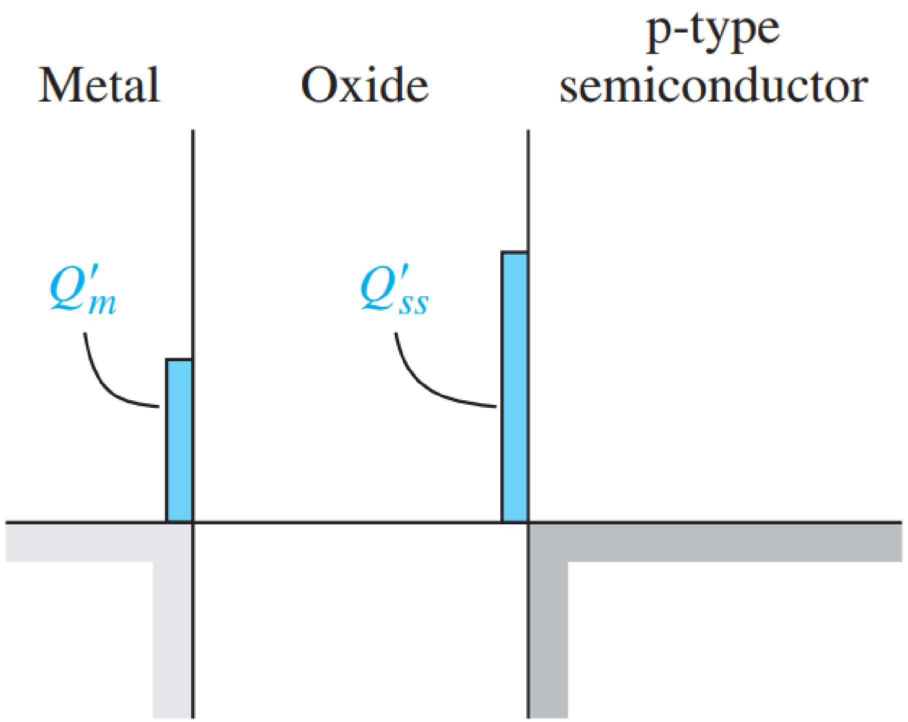
平帶電壓：施加的電壓剛好可以讓半導體區域能帶不彎曲，或者說無空乏區。
The *flat-band voltage* is defined as the applied gate voltage such that there is no band bending in the semiconductor and, as a result, zero net space charge in this region.



Fixed Charges

在氧化物和半導體的邊界處，因為懸鍵導致氧化物表面帶正電。

Some positive charge, Q'_{ss}, has been identified with broken or dangling covalent bonds near oxide-semiconductor interface due to excessive silicon.



$$V_{ox0} + \phi_{s0} = -\phi_{ms}$$

$$V_G = \Delta V_{ox} + \Delta\phi_s = (V_{ox} - V_{ox0}) + (\phi_s - \phi_{s0}) = V_{ox} + \phi_s + \phi_{ms}$$

$$Q'_m + Q'_{ss} = 0 \Rightarrow V_{ox} = -\frac{Q'_{ss}}{C_{ox}}$$

$$V_{FB} = -\frac{Q'_{ss}}{C_{ox}} + \phi_{ms}$$ flat-band for this MOS device.

Example 10.3

Objective: Calculate the flat-band voltage for a MOS capacitor with a p-type semiconductor substrate.

Consider a MOS capacitor with a p-type silicon substrate doped to $N_a = 10^{16}$ cm^{-3}, a silicon dioxide insulator with a thickness of $t_{ox} = 20$ nm $= 200$ Å, and an n^+ polysilicon gate. Assume that $Q'_{ss} = 5 \times 10^{10}$ electronic charges per cm^2.

Example 10.3

Objective: Calculate the flat-band voltage for a MOS capacitor with a p-type semiconductor substrate.

Consider a MOS capacitor with a p-type silicon substrate doped to $N_a = 10^{16}\ \text{cm}^{-3}$, a silicon dioxide insulator with a thickness of $t_{ox} = 20$ nm $= 200$ Å, and an n^+ polysilicon gate. Assume that $Q'_{ss} = 5 \times 10^{10}$ electronic charges per cm^2.

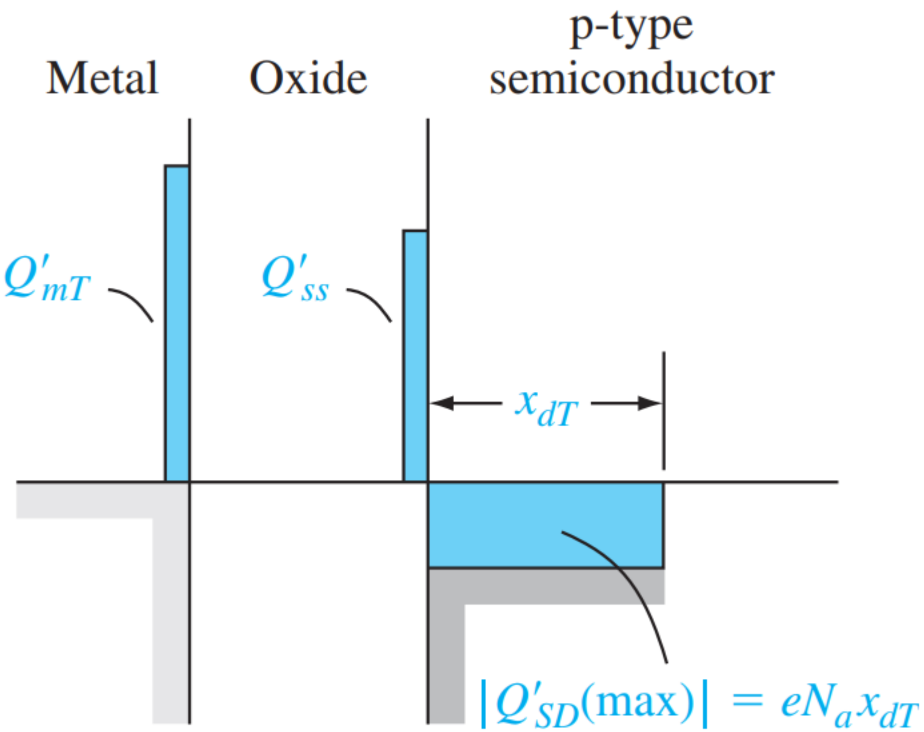
$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{(3.9)(8.85 \times 10^{-14})}{200 \times 10^{-8}} = 1.726 \times 10^{-7}\ \text{F/cm}^2$$

$$Q'_{ss} = (5 \times 10^{10})(1.6 \times 10^{-19}) = 8 \times 10^{-9}\ \text{C/cm}^2$$

$$V_{FB} = \phi_{ms} - \frac{Q'_{ss}}{C_{ox}} = -1.1\ \frac{-8 \times 10^{-9}}{1.726 \times 10^{-7}} = -1.15\ \text{V}$$

Threshold Voltage

The threshold voltage is defined as the applied gate voltage required to achieve the threshold inversion point. $\phi_s = 2\phi_{fp}$



$$Q'_{mT} + Q'_{ss} = \left|Q'_{SD}(\max)\right| = eN_a x_{dT}$$

$$V_G = V_{ox} + \phi_s + \phi_{ms}$$

$$V_{TN} = V_{oxT} + 2\phi_{fp} + \phi_{ms} = \frac{Q'_{mT}}{C_{ox}} + 2\phi_{fp} + \phi_{ms}$$

$$= \frac{\left|Q'_{SD}(\max)\right| - Q'_{ss}}{C_{ox}} + 2\phi_{fp} + \phi_{ms}$$

$$= \frac{\left|Q'_{SD}(\max)\right|}{C_{ox}} + V_{FB} + 2\phi_{fp}$$

Example 10.4

Objective: Calculate the threshold voltage of a MOS system using an aluminum gate.

Consider a p-type silicon substrate at $T = 300$ K doped to $N_a = 10^{15}$ cm^{-3}. Let $Q'_{ss} = 10^{10}$ cm^{-2}, $t_{ox} = 12$ nm $= 120$ Å, and assume the oxide is silicon dioxide.

Example 10.4

Objective: Calculate the threshold voltage of a MOS system using an aluminum gate.

Consider a p-type silicon substrate at $T = 300$ K doped to $N_a = 10^{15}$ cm^{-3}. Let $Q'_{ss} = 10^{10}$ cm^{-2}, $t_{ox} = 12$ nm $= 120$ Å, and assume the oxide is silicon dioxide.

$$\phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right) = (0.0259)\ln\left(\frac{10^{15}}{1.5 \times 10^{10}}\right) = 0.2877 \text{ V}$$

$$x_{dT} = \left\{\frac{4\epsilon_s \phi_{fp}}{eN_a}\right\}^{1/2} = \left\{\frac{4(11.7)(8.85 \times 10^{-14})(0.2877)}{(1.6 \times 10^{-19})(10^{15})}\right\}^{1/2} = 8.63 \times 10^{-5} \text{ cm}$$

$$|Q'_{SD}(\max)| = eN_a x_{dT} = (1.6 \times 10^{-19})(10^{15})(8.63 \times 10^{-5}) = 1.381 \times 10^{-8} \text{ C/cm}^2$$

$$V_{TN} = (|Q'_{SD}(\max)| - Q'_{ss})\left(\frac{t_{ox}}{\epsilon_{ox}}\right) + \phi_{ms} + 2\phi_{fp}$$

$$= [(1.381 \times 10^{-8}) - (10^{10})(1.6 \times 10^{-19})] \cdot \left[\frac{120 \times 10^{-8}}{(3.9)(8.85 \times 10^{-14})}\right]$$

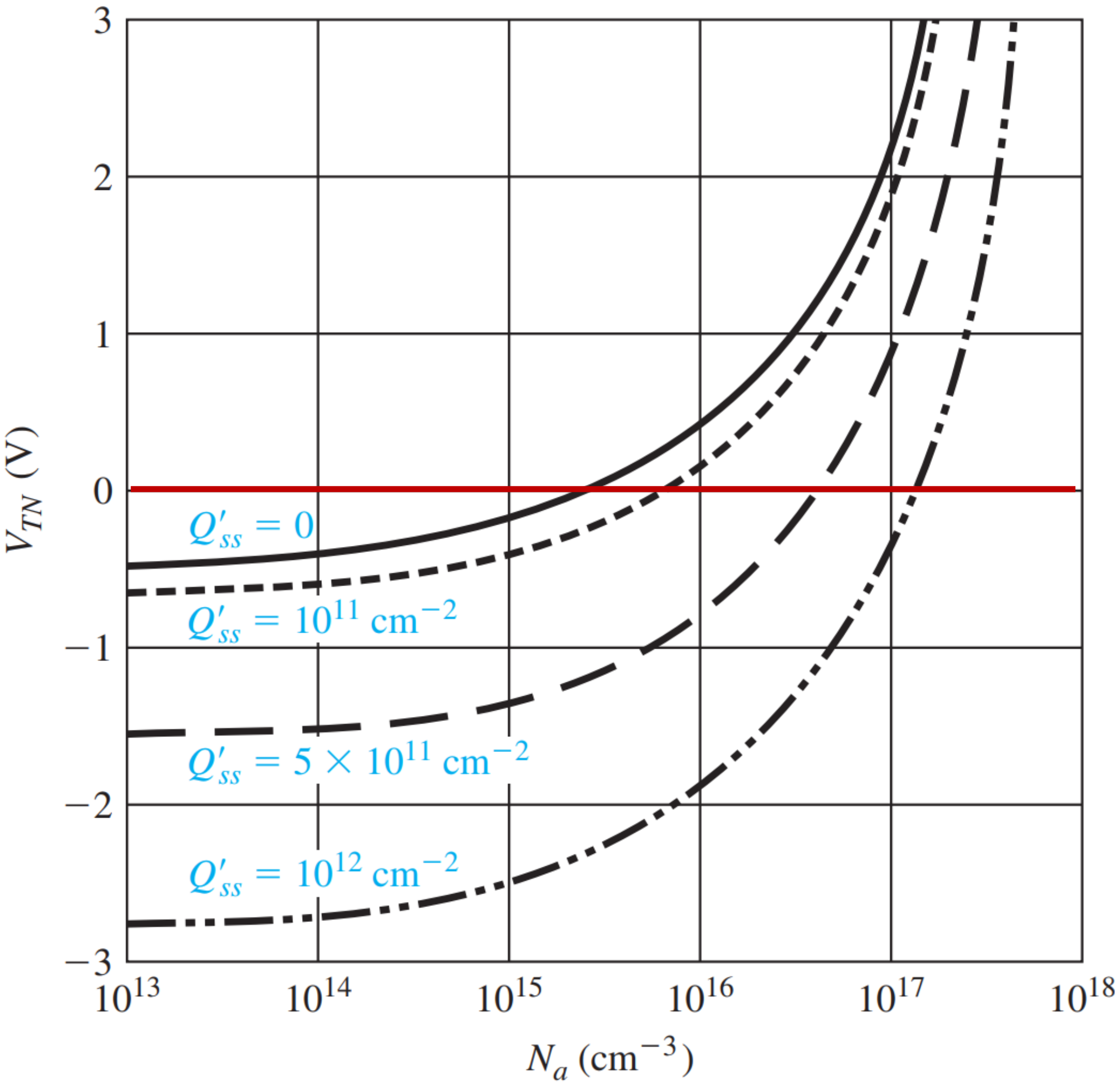
$$+ (-0.88) + 2(0.2877) = -0.262 \text{ V}$$

Threshold Voltage

$$V_{TN} = \frac{|Q'_{SD}(\max)| - Q'_{ss}}{C_{ox}} + 2\phi_{fp} + \phi_{ms}$$

$$= \frac{|Q'_{SD}(\max)|}{C_{ox}} + V_{FB} + 2\phi_{fp}$$

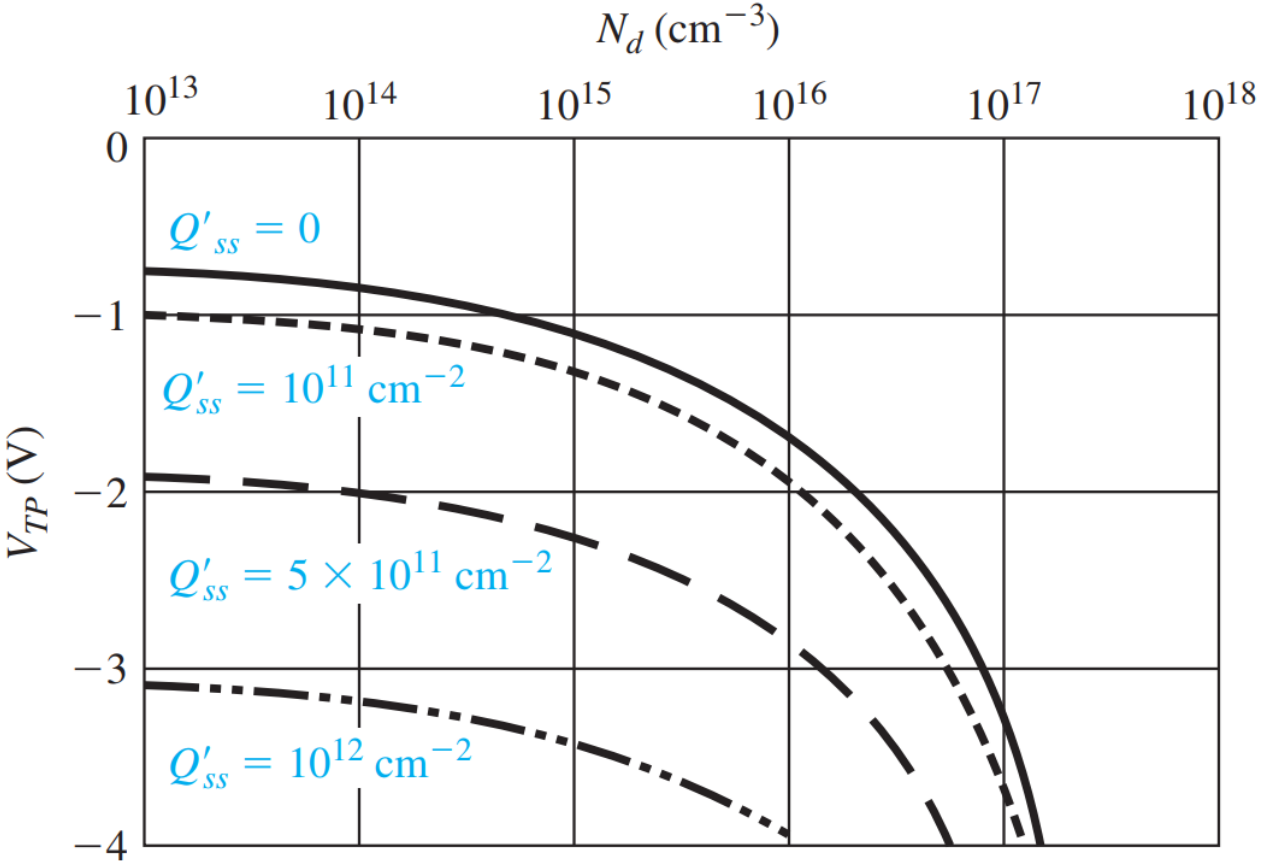
還沒給電壓就已經達到反轉，所以必須做高濃度摻雜才能維持在 enhancement mode。



Threshold Voltage

$$V_{TP} = \frac{-\left|Q'_{SD}(\max)\right| - Q'_{ss}}{C_{ox}} - 2\phi_{fn} + \phi_{n}$$

$$= \frac{-\left|Q'_{SD}(\max)\right|}{C_{ox}} + V_{FB} - 2\phi_{fn}$$



Example 10.5

Objective: Determine the gate material and design the semiconductor doping concentration to yield a specified threshold voltage.

Consider a MOS device with silicon dioxide and an n-type silicon substrate. The oxide thickness is $t_{ox} = 12$ nm $= 120$ Å and the oxide charge is $Q'_{ss} = 2 \times 10^{10}$ cm^{-2} . The threshold voltage is to be approximately $V_{TP} = -0.3$ V.

Example 10.5

Objective: Determine the gate material and design the semiconductor doping concentration to yield a specified threshold voltage.

Consider a MOS device with silicon dioxide and an n-type silicon substrate. The oxide thickness is $t_{ox} = 12$ nm $= 120$ Å and the oxide charge is $Q'_{ss} = 2 \times 10^{10}$ cm^{-2}. The threshold voltage is to be approximately $V_{TP} = -0.3$ V.

$$\phi_{fn} = V_t \ln\left(\frac{N_d}{n_i}\right) = (0.0259)\ln\left(\frac{10^{17}}{1.5 \times 10^{10}}\right) = 0.407 \text{ V}$$

$$x_{dT} = \left(\frac{4\epsilon_s \phi_{fn}}{eN_d}\right)^{1/2} = \left\{\frac{4(11.7)(8.85 \times 10^{-14})(0.407)}{(1.6 \times 10^{-19})(10^{17})}\right\}^{1/2}$$

$$= 1.026 \times 10^{-5} \text{ cm}$$

$$|Q'_{SD}(\max)| = eN_d x_{dT} = (1.6 \times 10^{-19})(10^{17})(1.026 \times 10^{-5})$$

$$= 1.642 \times 10^{-7} \text{ C/cm}^2$$

$$V_{TP} = [-|Q'_{SD}(\max)| - Q'_{ss}] \cdot \left(\frac{t_{ox}}{\epsilon_{ox}}\right) + \phi_{ms} - 2\phi_{fn}$$

$$V_{TP} = \frac{[-(1.642 \times 10^{-7}) - (2 \times 10^{10})(1.6 \times 10^{-19})] \cdot (120 \times 10^{-8})}{(3.9)(8.85 \times 10^{-14})} + 1.1 - 2(0.407)$$

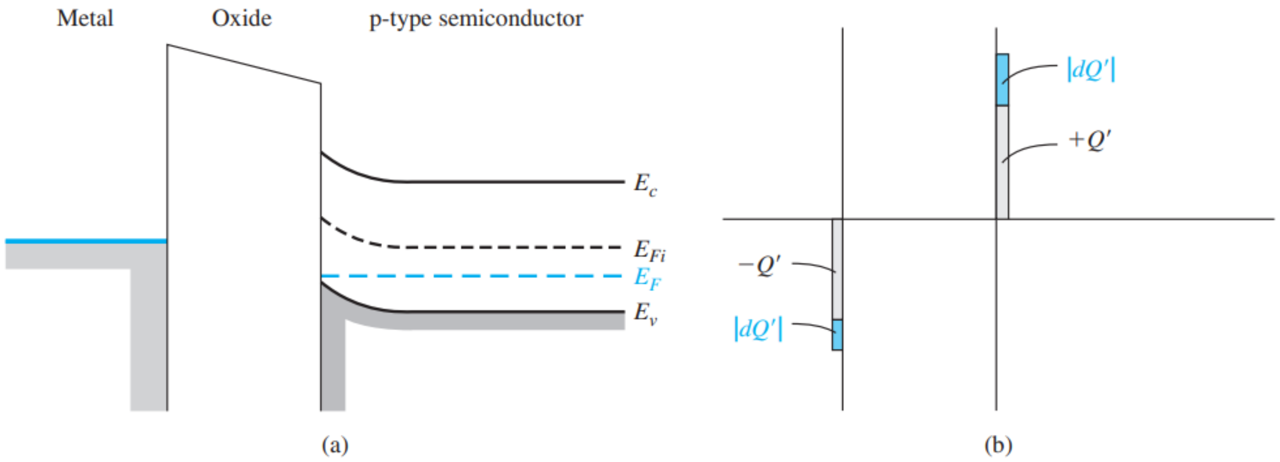
$$V_{TP} = -0.296 \text{ V} \cong -0.3 \text{ V}$$

Ideal C–V Characteristics

- Initially considered there is zero charge trapped in the oxide and also that there is no charge trapped at the oxide–semiconductor interface

negative voltage is applied to the gate

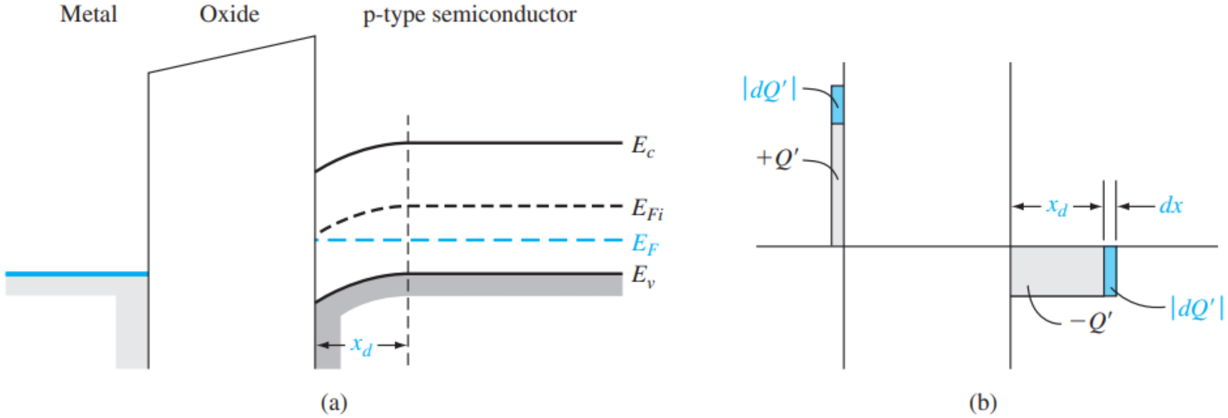
$$C'(acc) = C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$



positive voltage is applied to the gate

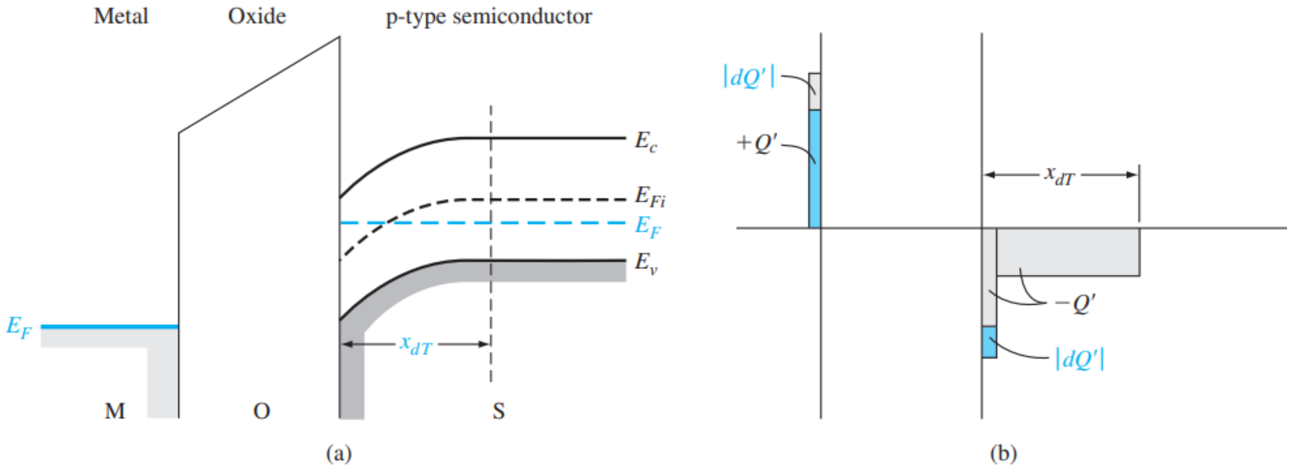
$$\frac{1}{C'(depl)} = \frac{1}{C_{ox}} + \frac{1}{C'_{SD}} = \frac{1}{\frac{\varepsilon_{ox}}{t_{ox}}} + \frac{1}{\frac{\varepsilon_s}{x_d}}$$

$$C'_{\min} = \frac{C_{ox}}{1+\frac{C_{ox}}{C'_{SD,\min}}} = \frac{\varepsilon_{ox}}{t_{ox} + \left(\frac{\varepsilon_{ox}}{\varepsilon_s}\right)x_{dT}}$$



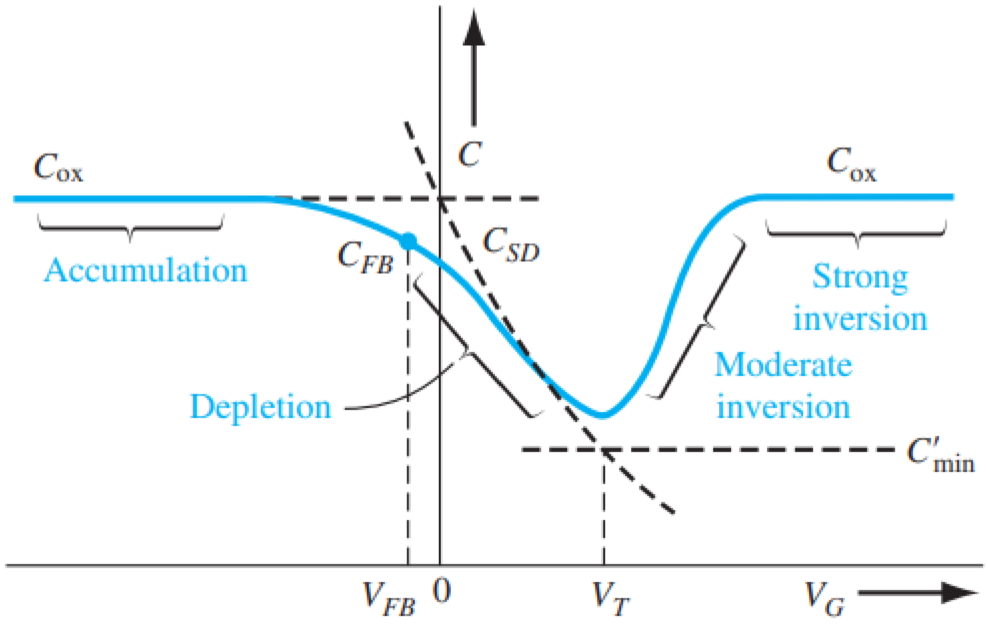
Ideal C–V Characteristics

large positive voltage is applied to the gate



$$C'(inv) = C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

- Ideal low-frequency capacitance versus gate voltage of a MOS capacitor with a p-type substrate.



$$C'_{FB} = \frac{\varepsilon_{ox}}{t_{ox} + \left(\frac{\varepsilon_{ox}}{\varepsilon_s}\right)\sqrt{\frac{kT}{e}\left(\frac{\varepsilon_s}{eN_a}\right)}}$$

EXAMPLE 10.6

Objective: Calculate C_{ox}, $C'_{\min}$, and C'_{FB} for a MOS capacitor.

Consider a p-type silicon substrate at $T = 300$ K doped to $N_a = 10^{16}$ cm^{-3}.

The oxide is silicon dioxide with a thickness of $t_{ox} = 18$ nm $= 180$ Å, and the gate is aluminum.

EXAMPLE 10.6

Objective: Calculate C_{ox}, $C'_{\min}$, and C'_{FB} for a MOS capacitor.

Consider a p-type silicon substrate at $T = 300$ K doped to $N_a = 10^{16}$ cm^{-3}.

The oxide is silicon dioxide with a thickness of $t_{ox} = 18$ nm $= 180$ Å, and the gate is aluminum.

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{(3.9)(8.85 \times 10^{-14})}{180 \times 10^{-8}} = 1.9175 \times 10^{-7} \text{ F/cm}^2$$

$$\phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right) = (0.0259) \ln\left(\frac{10^{16}}{1.5 \times 10^{10}}\right) = 0.3473 \text{ V}$$

$$x_{dT} = \left\{\frac{4\epsilon_s \phi_{fp}}{eN_a}\right\}^{1/2} = \left\{\frac{4(11.7)(8.85 \times 10^{-14})(0.3473)}{(1.6 \times 10^{-19})(10^{16})}\right\}^{1/2}$$

$$\cong 0.30 \times 10^{-4} \text{ cm}$$

$$C'_{\min} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right) x_{dT}} = \frac{(3.9)(8.85 \times 10^{-14})}{180 \times 10^{-8} + \left(\frac{3.9}{11.7}\right)(0.30 \times 10^{-4})}$$

$$= 2.925 \times 10^{-8} \text{ F/cm}^2$$

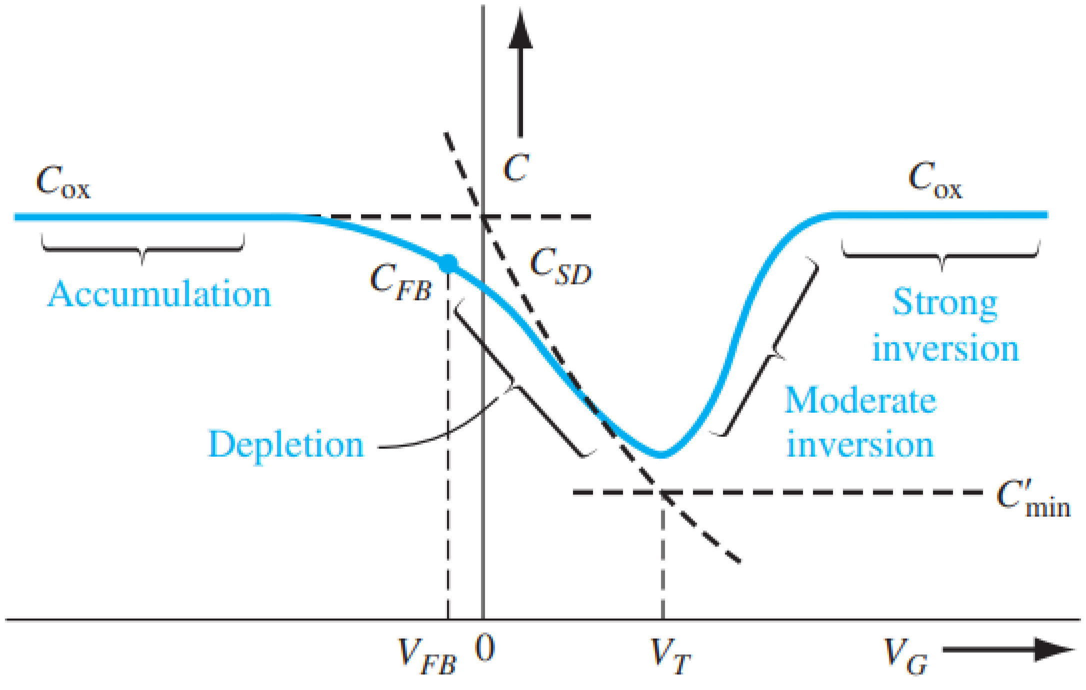
$$C'_{FB} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right)\sqrt{\frac{V_t \epsilon_s}{eN_a}}}$$

$$= \frac{(3.9)(8.85 \times 10^{-14})}{180 \times 10^{-8} + \left(\frac{3.9}{11.7}\right)\sqrt{\frac{(0.0259)(11.7)(8.85 \times 10^{-14})}{(1.6 \times 10^{-19})(10^{16})}}}$$

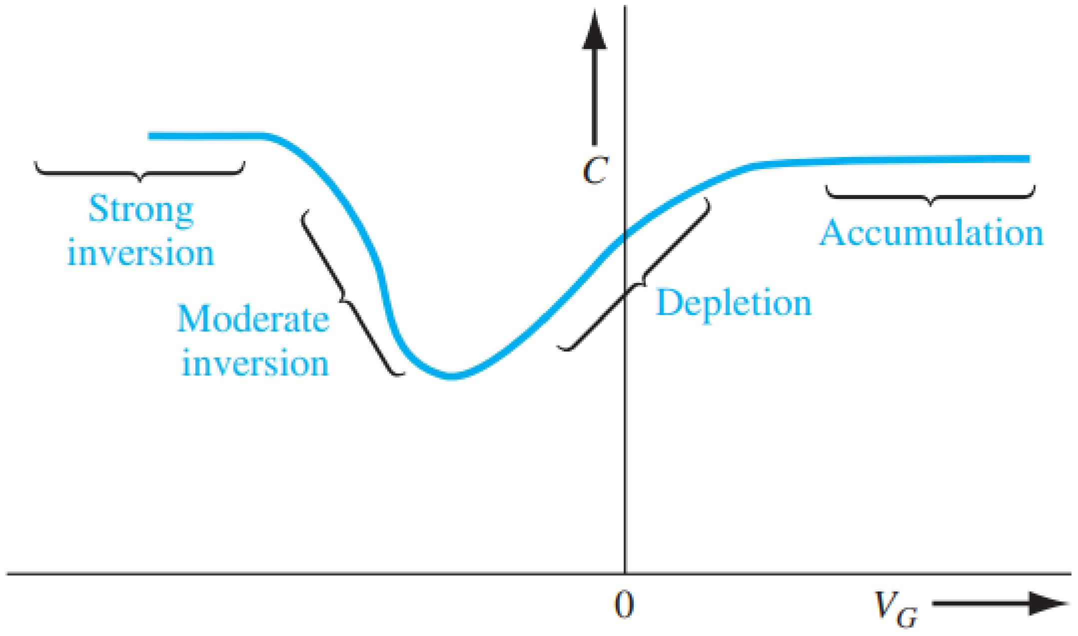
$$= 1.091 \times 10^{-7} \text{ F/cm}^2$$

p-type substrate v.s. n-type substrate

p-type substrate

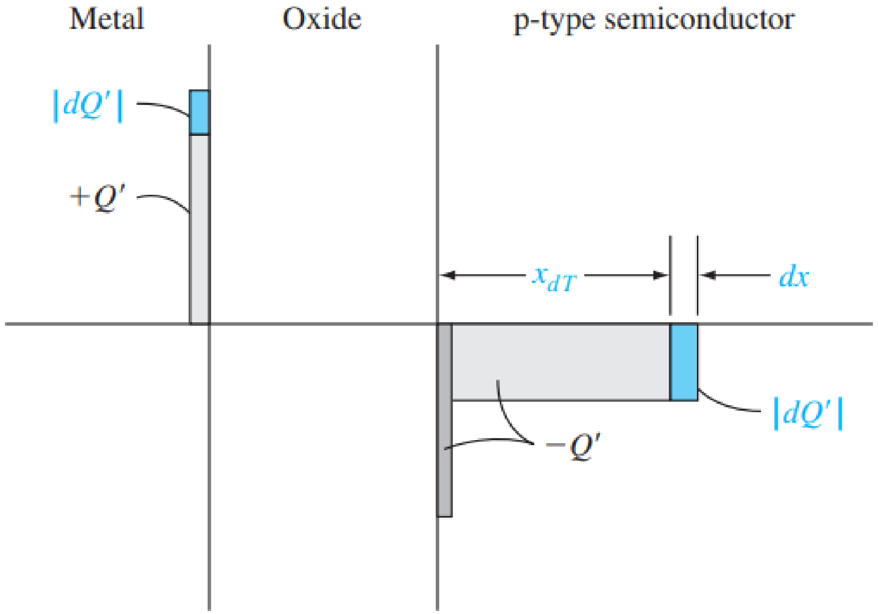


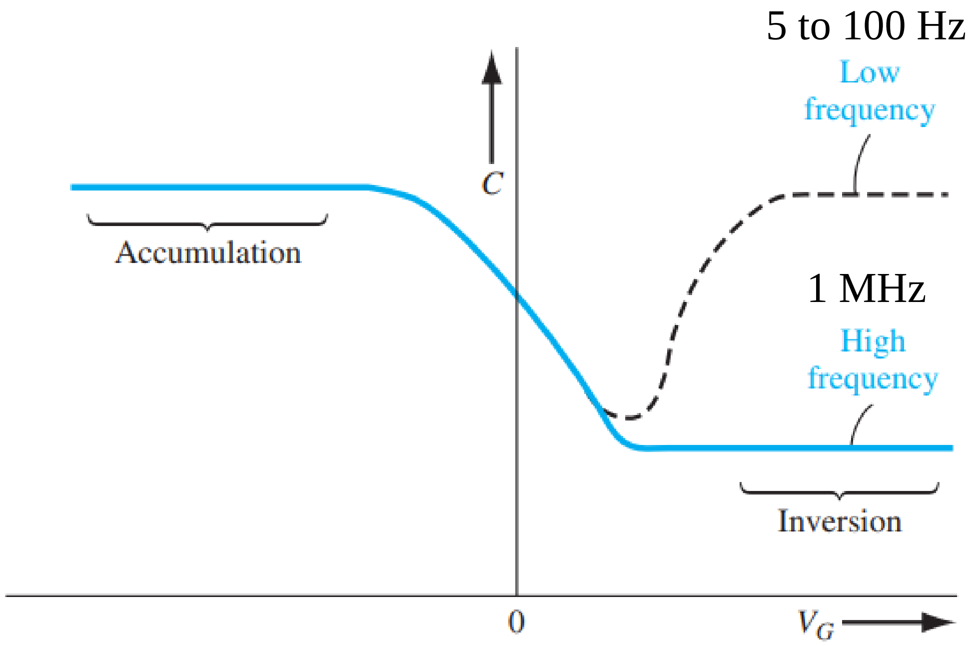
n-type substrate



Frequency Effects

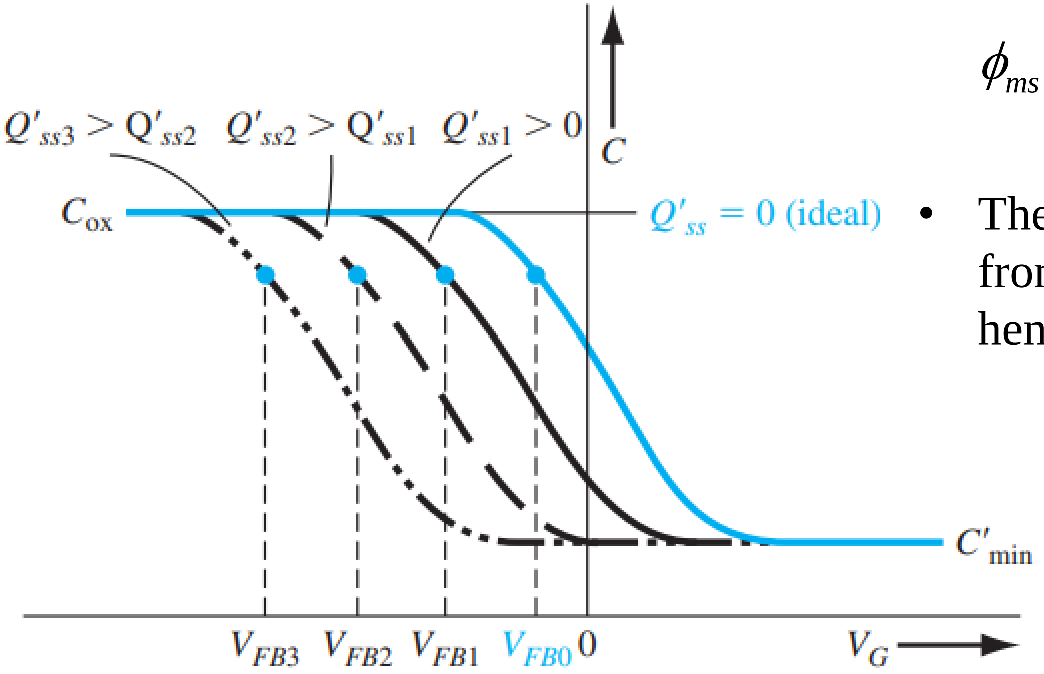
- We must consider the source of electrons that produces a change in the inversion charge density
- First source: y diffusion of minority carrier electrons from the p-type substrate across the space charge region
- Second source: thermal generation of electron–hole pairs within the space charge region
- The electron concentration in the inversion layer, then, cannot change instantaneously





Fixed Oxide

$$V_{FB} = \phi_{ms} - \frac{Q'_{ss}}{C_{ox}}$$



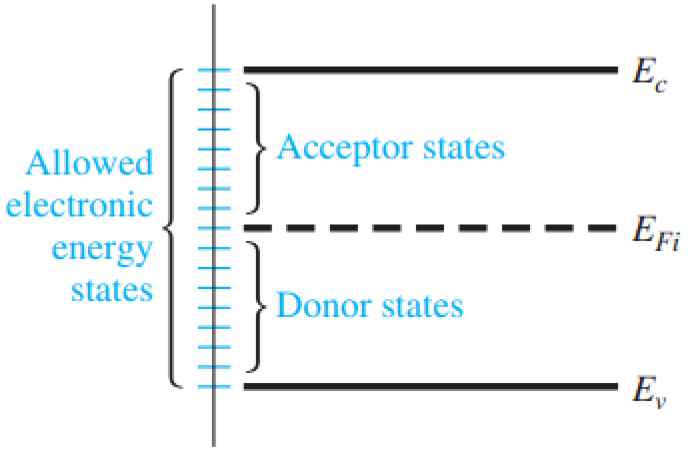
Q'_{ss} : equivalent fixed oxide charge

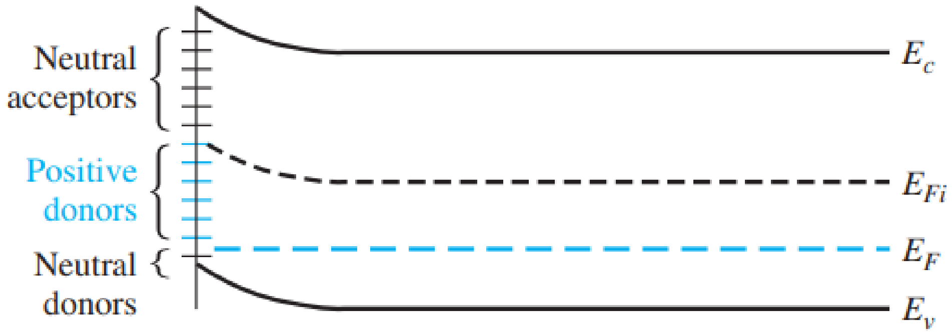
ϕ_{ms} : metal ? semiconductor work function difference

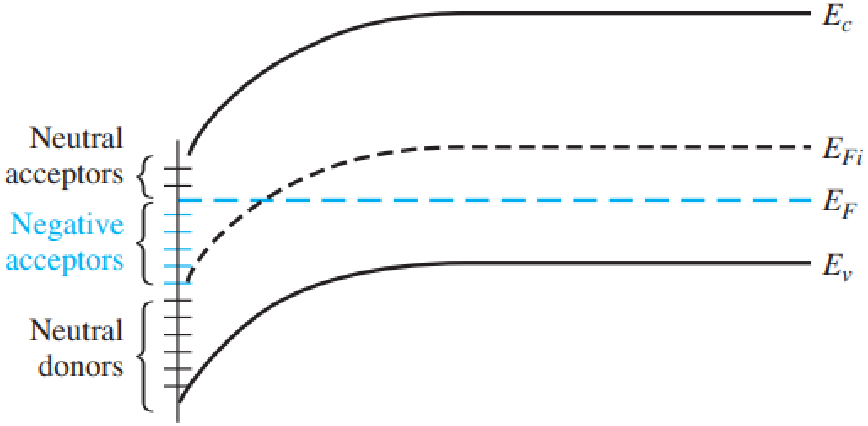
- The experimental value of flat-band voltage can be measured from the C–V curve, and the value of fixed oxide charge can hen be determined(早期用在太空輻射)

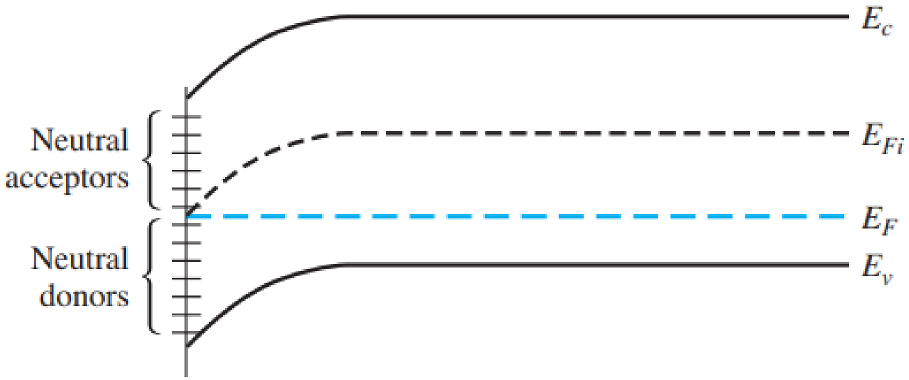
Interface Charge Effects

- The periodic nature of the semiconductor is abruptly terminated at the interface so that allowed electronic energy levels will exist within the forbidden bandgap (interface states)
- Charge can fl ow between the semiconductor and interface states, in contrast to the fi xed oxide charge



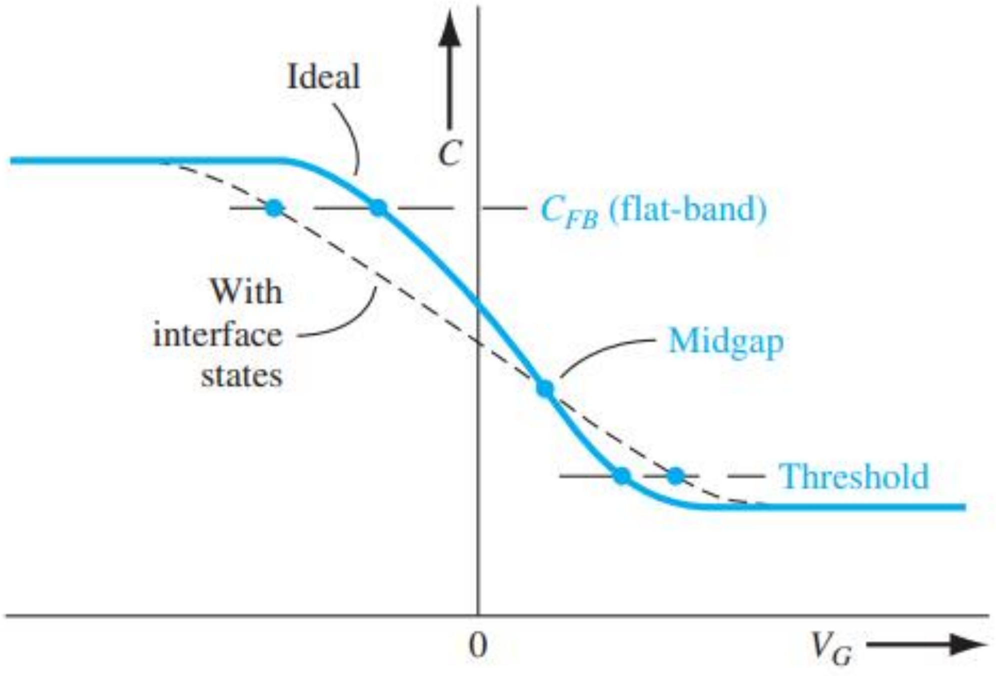




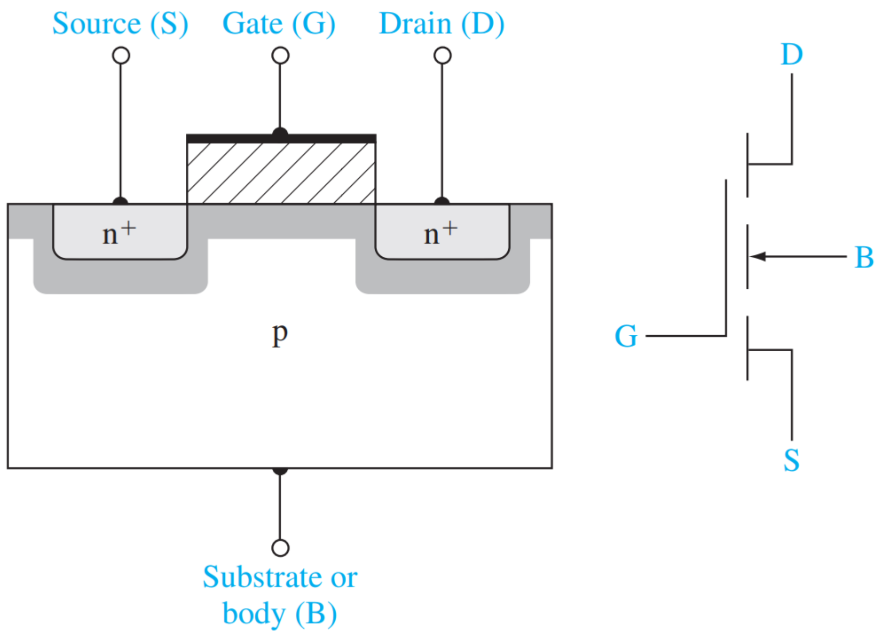


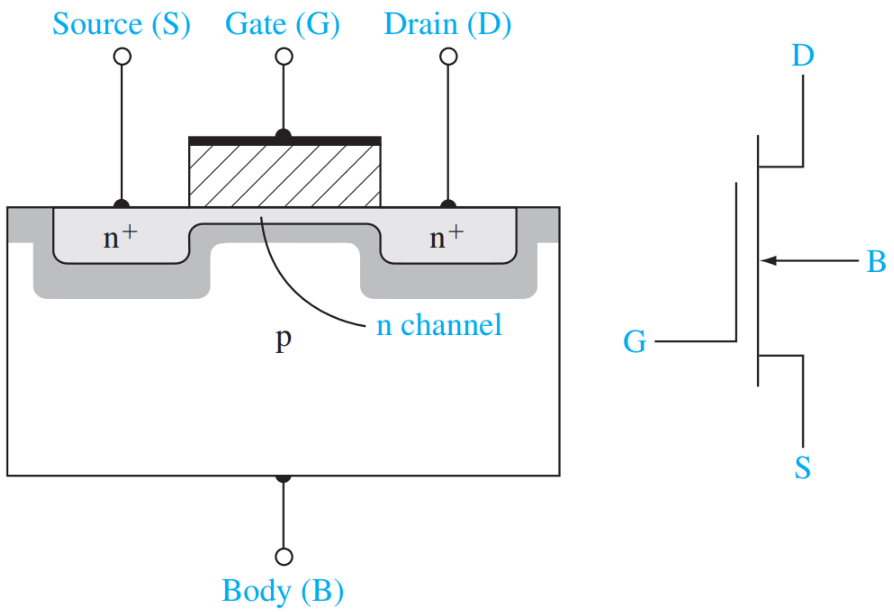
Smearing out of the curve

- Smearing out in the experimental curve indicates the presence of interface states and any parallel shift indicates the presence of fixed oxide charge



The Basic MOSFET Operation

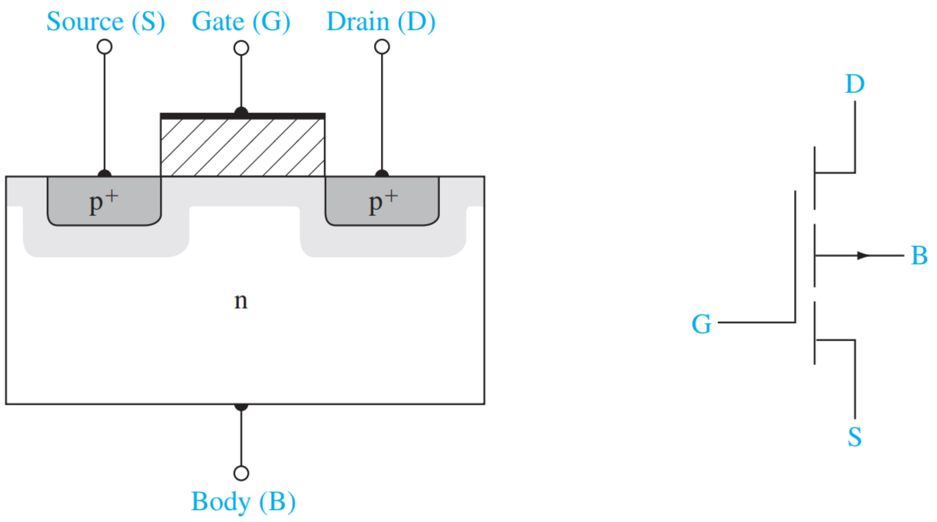


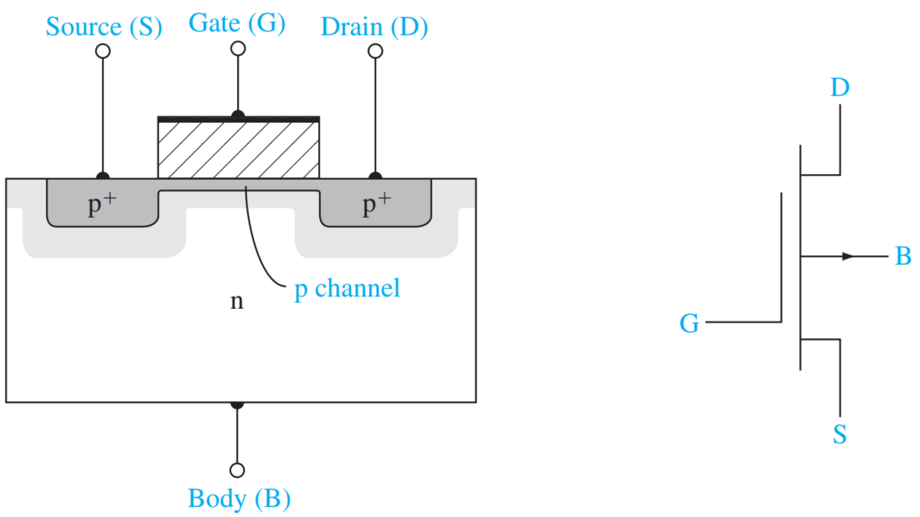


n-channel enhancement mode: the substrate is not inverted directly under $\mathbf{V_G=0}$.

n-channel depletion mode: an n-channel region exists under the oxide at $\mathbf{V_G=0}$.

The Basic MOSFET Operation

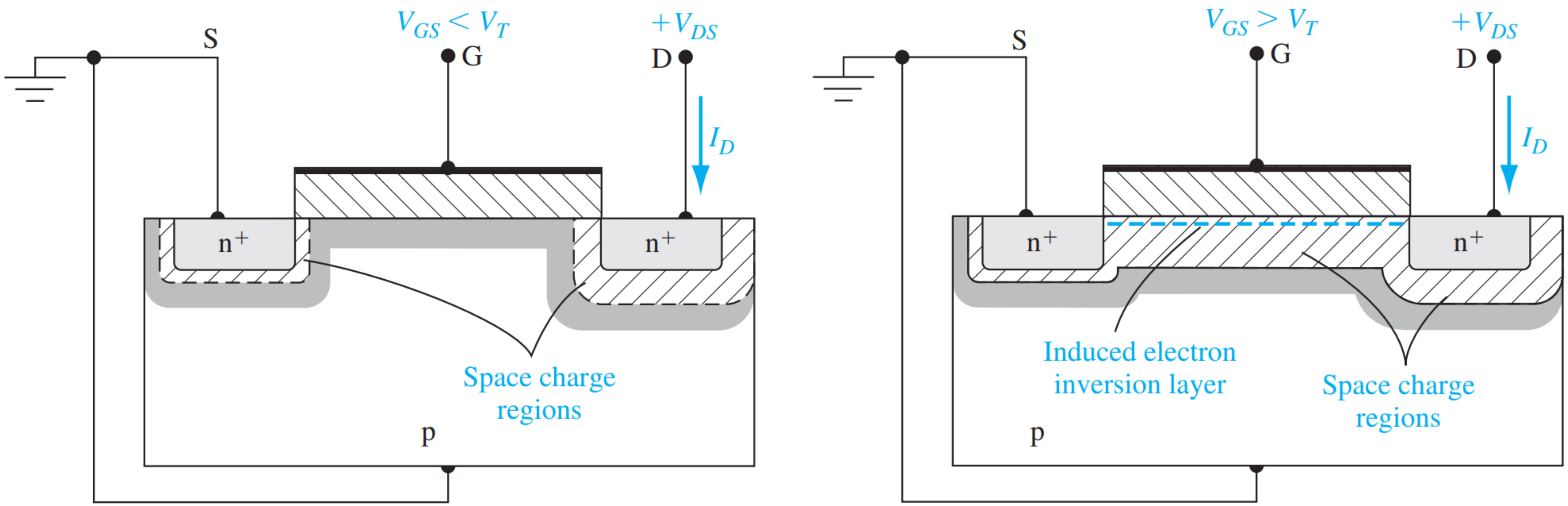




p-channel enhancement mode: the substrate is not inverted directly under $\mathbf{V_G=0}$.

p-channel depletion mode: an n-channel region exists under the oxide at $\mathbf{V_G=0}$.

Current-Voltage Relationship Concepts



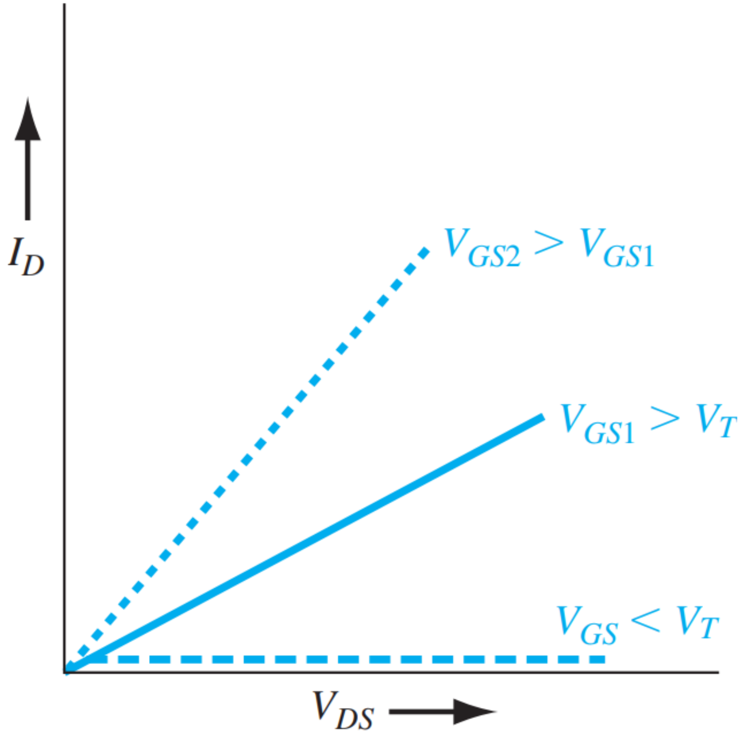
- $V_G < V_T$，no inversion layer，無法導通，無電流
- $V_G > V_T$，an inversion layer has been created，可導通

Current-Voltage Relationship Concepts

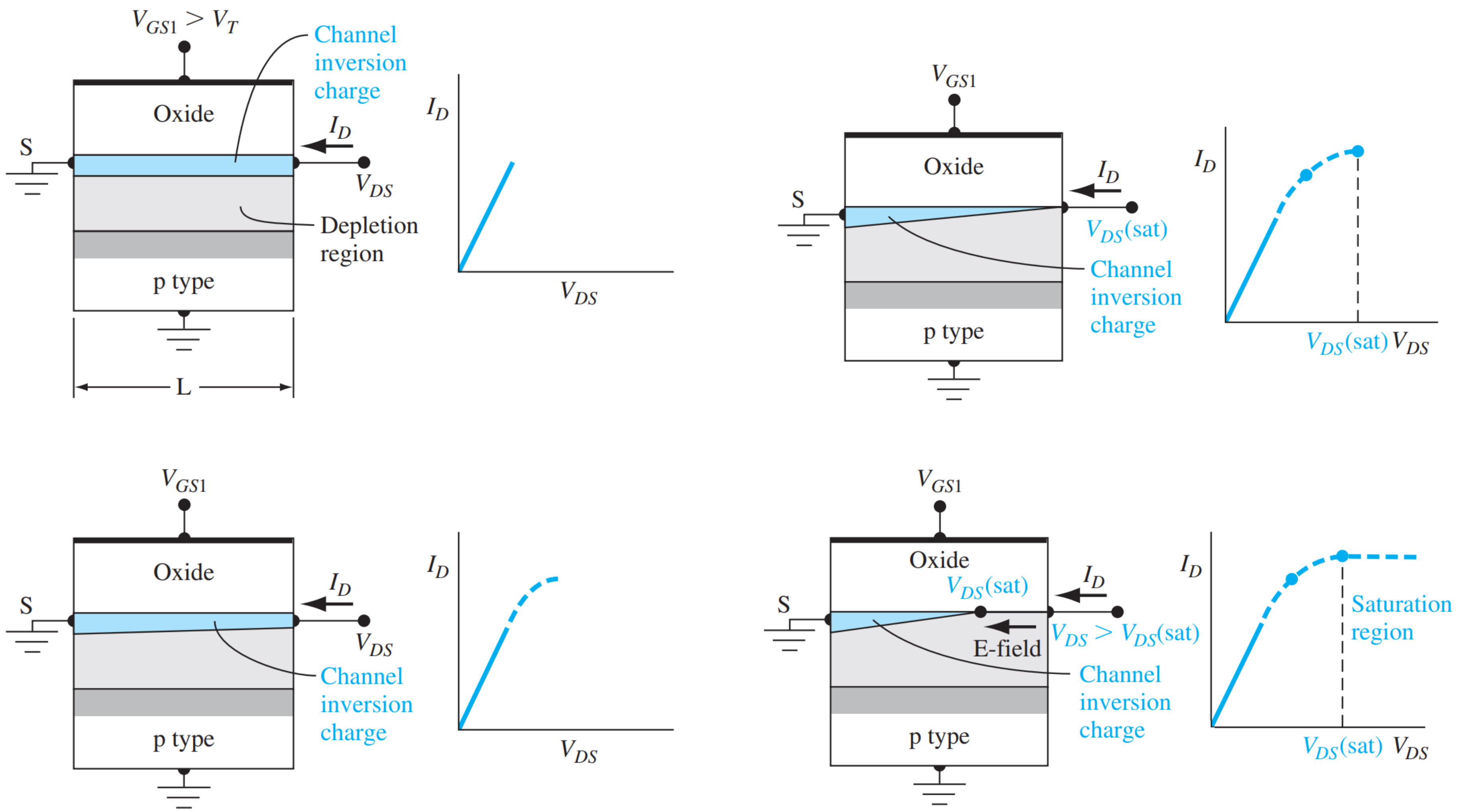
For small V_{DS}, the channel region has the characteristic of a resistor

$$I_D = g_v V_{DS}$$

channel conductance

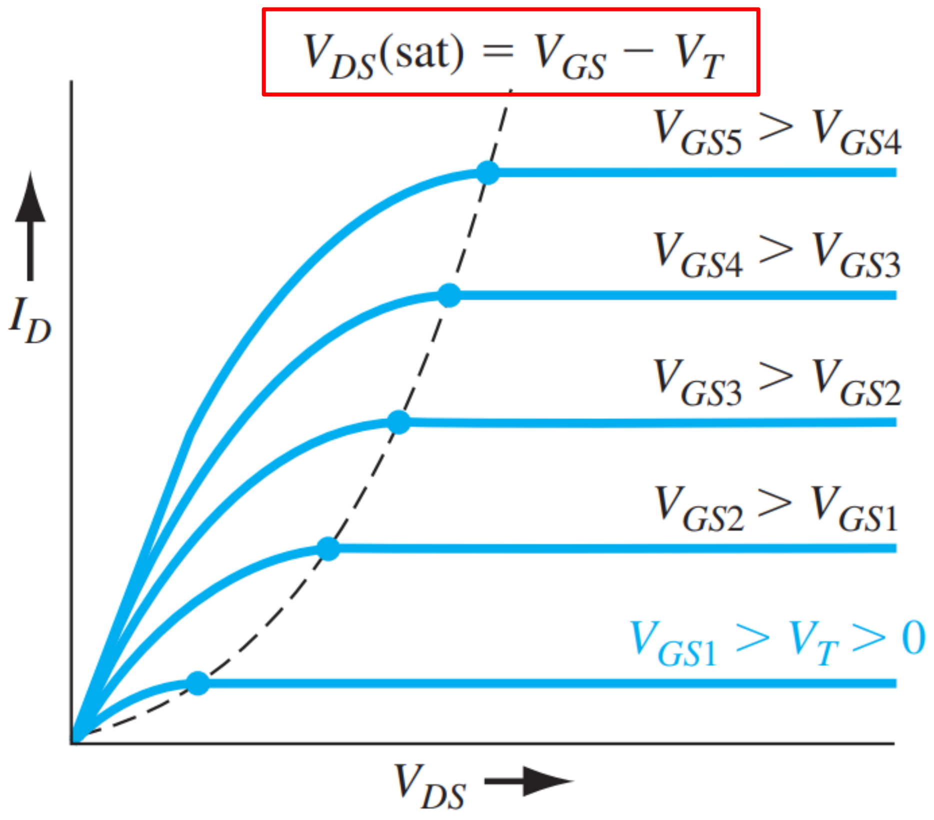


Current-Voltage Relationship Concepts

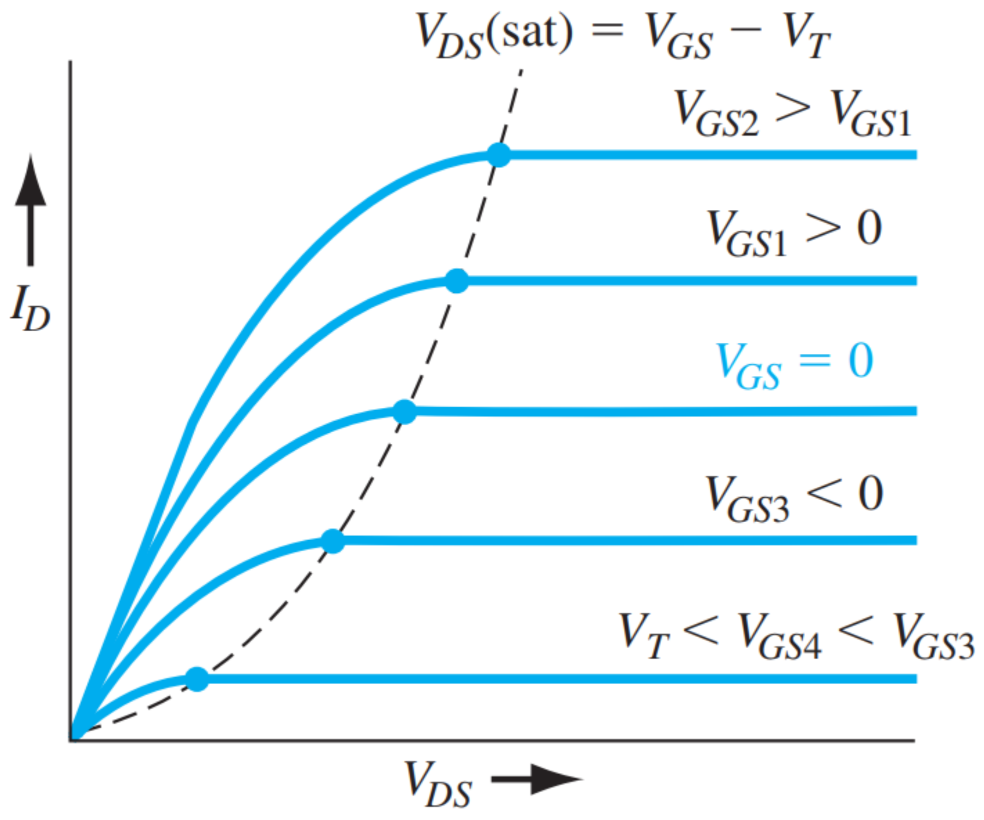


Current-Voltage Relationship Concepts

n-channel enhancement mode



n-channel depletion mode



The Ideal I-V Relation for n-channel MOSFET:

$$I_D = \frac{W}{2L}\mu_n C_{ox}\left[2\left(V_{GS}-V_T\right)V_{DS}-V_{DS}^2\right]$$

conductance parameter (A/V²).

$$I_D = \frac{W_n}{2L}k'\left[2\left(V_{GS}-V_T\right)V_{DS}-V_{DS}^2\right]$$

process conductance parameter (A/V²).

$$I_D = K_n\left[2\left(V_{GS}-V_T\right)V_{DS}-V_{DS}^2\right]$$

$$V_{DS}=V_{GS}-V_T \Rightarrow I_D = K_n\left(V_{GS}-V_T\right)^2$$

Example 10.7

Objective: Design the width of a MOSFET such that a specified current is induced for a given applied bias.

Consider an ideal n-channel MOSFET with parameters $L = 1.25\ \mu\text{m}$, $\mu_n = 650\ \text{cm}^2/\text{V-s}$, $C_{\text{ox}} = 6.9 \times 10^{-8}\ \text{F/cm}^2$, and $V_T = 0.65$ V. Design the channel width W such that $I_D(\text{sat}) = 4$ mA for $V_{GS} = 5$ V.

$$I_D(\text{sat}) = \frac{W\mu_n C_{\text{ox}}}{2L}(V_{GS} - V_T)^2$$

$$4 \times 10^{-3} = \frac{W(650)(6.9 \times 10^{-8})}{2(1.25 \times 10^{-4})} \cdot (5 - 0.65)^2 = 3.39\ W$$

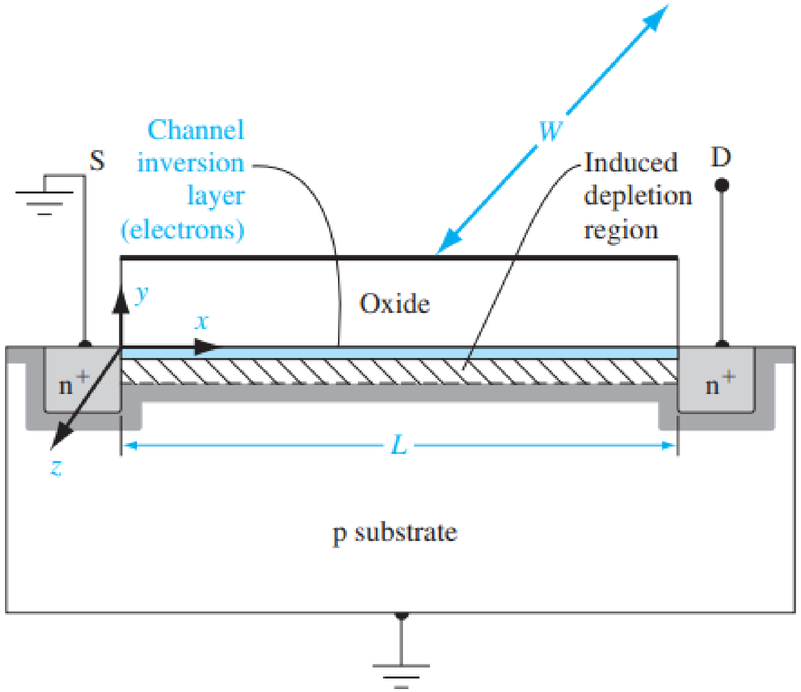
$$W = 11.8\ \mu\text{m}$$

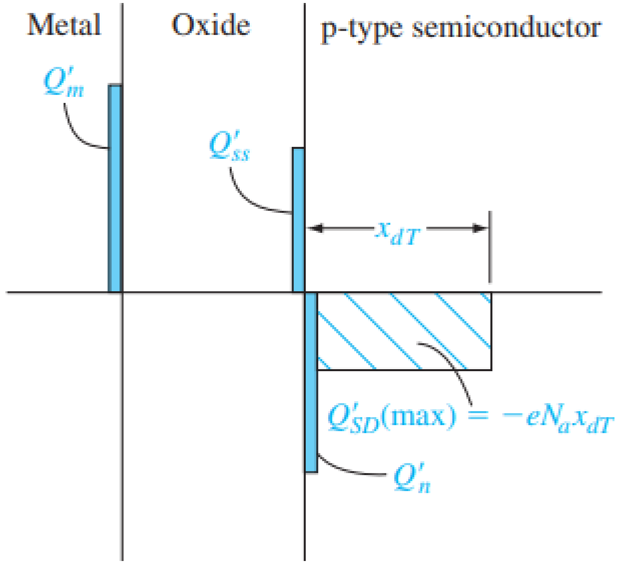
Current–Voltage Relationship—Mathematical*

Assumptions

- The current in the channel is due to drift rather than diffusion
- There is no current through the gate oxide
- A gradual channel approximation is used in which ${\partial E_x}/{\partial y} >> {\partial E_x}/{\partial x}$ (E_x is constant)
- Any fixed oxide charge is an equivalent charge density at the oxide
- The carrier mobility in the channel is constant

Current–Voltage Relationship—Mathematical*





$$J_x = \sigma E_x \text{(ohm's law)}$$

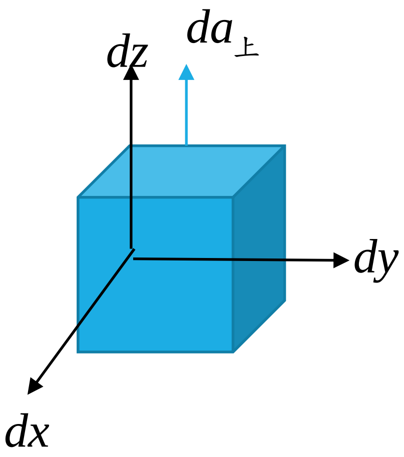
$$I_x = \int_y \int_z J_x dydz$$

$$Q'_n = -\int en(y)dy$$

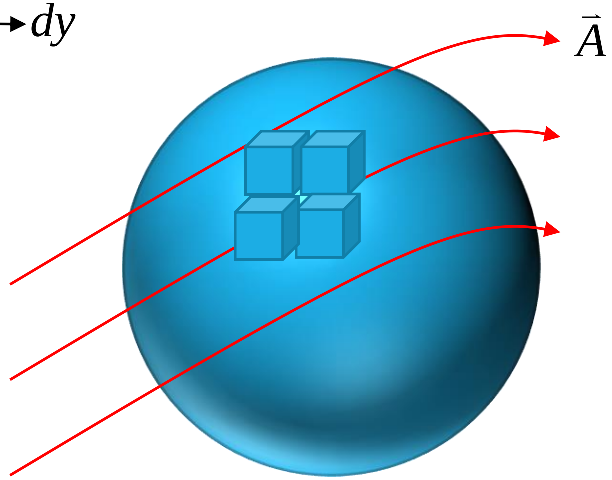
$$I_x = -W\mu_n Q'_n E_x$$

$$Q'_m + Q'_{ss} + Q'_n + Q'_{SD}(\max) = 0 \quad \text{電中性}$$

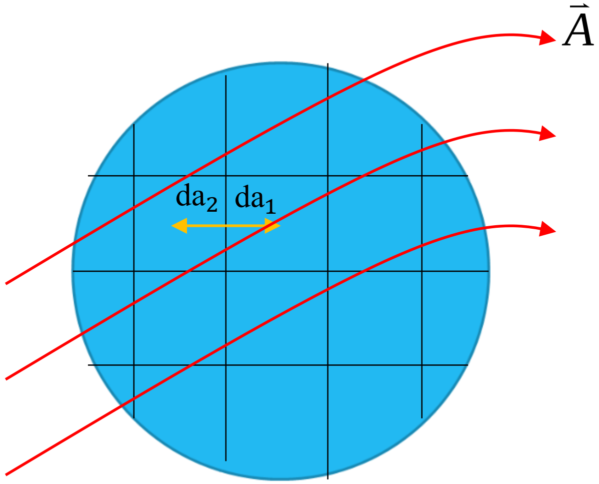
Divergence theorem



Volume



Corss section

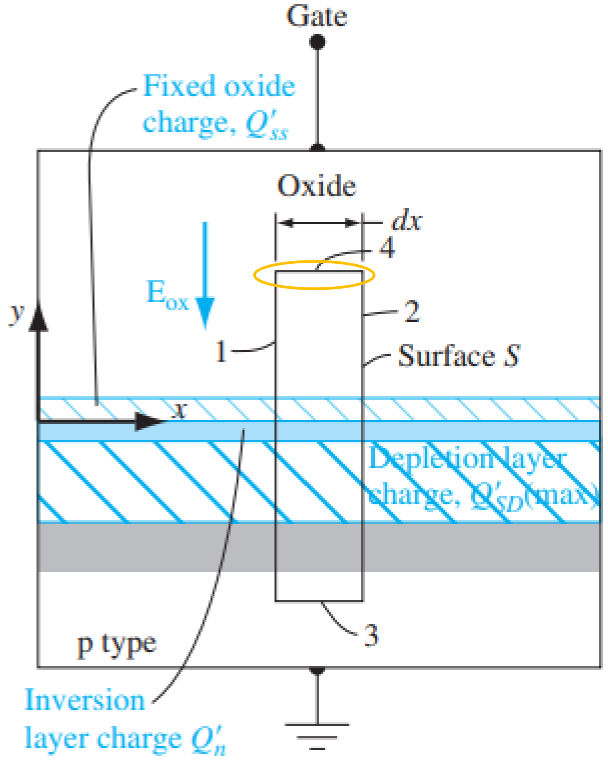


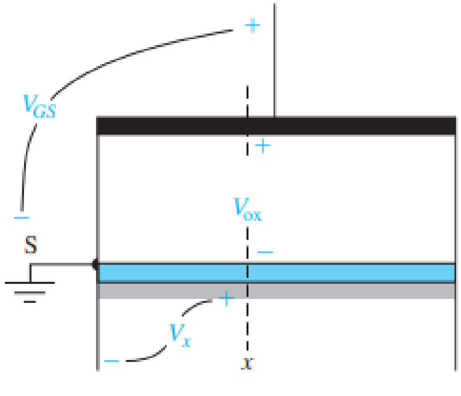
Current–Voltage Relationship—Mathematical*

$$\oint_S \varepsilon E_n dS = -\varepsilon_{ox} E_{ox} W dx = Q_T$$

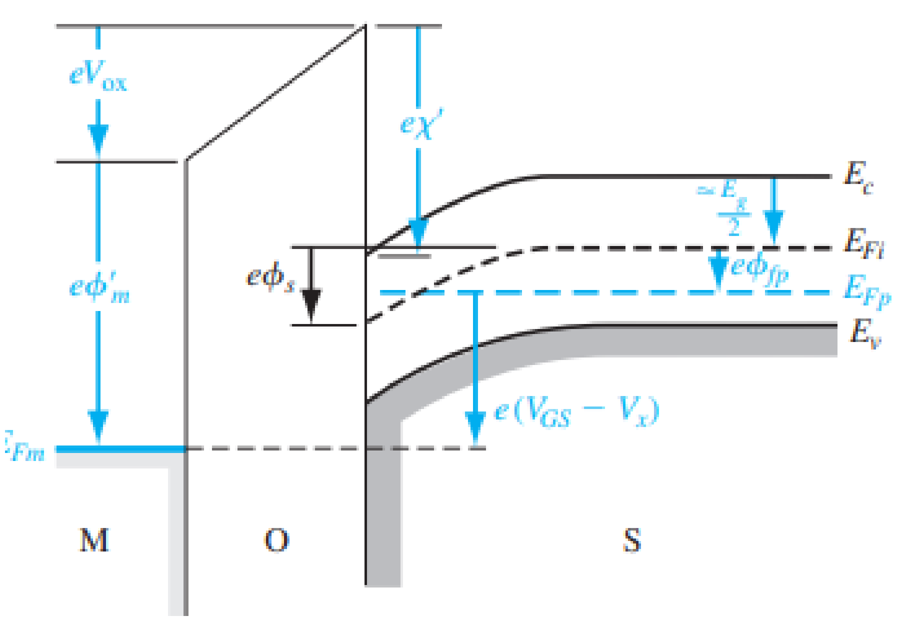
$$Q_T = \left[Q'_{ss} + Q'_n + Q'_{SD}(\max) \right] W dx$$

$$-\varepsilon_{ox} E_{ox} = Q'_{ss} + Q'_n + Q'_{SD}(\max)$$





(a)



$$E_{Fp} - E_{Fm} = e(V_{GS} - V_x) e(\phi'_m + V_{ox}) - \left(\chi' + \frac{E_g}{2e} - \phi_s + \phi_{fp} \right) = V_{ox} + 2\phi_{fp} + \phi_{ms}$$

Inversion condition

$$-\varepsilon_{ox} E_{ox} = -\varepsilon_{ox} \frac{V_{ox}}{t_{ox}} = -\varepsilon_{ox} \frac{\left[(V_{GS} - V_x) - (\phi_{ms} + 2\phi_{fp}) \right]}{t_{ox}} = Q'_{ss} + Q'_n + Q'_{SD}(\max)$$

$$I_x = -W \mu_n Q'_n E = -W \mu_n C_{ox} \frac{dV_x}{dx} \left[(V_{GS} - V_x) - V_T \right]$$

Current–Voltage Relationship—Mathematical*

Integrate over the length of channel

$$\int_0^L I_x dx = -W\mu_n C_{ox} \int_{V_x(0)}^{V_x(L)} \left[\left(V_{GS} - V_T\right) - V_x\right] dV_x$$

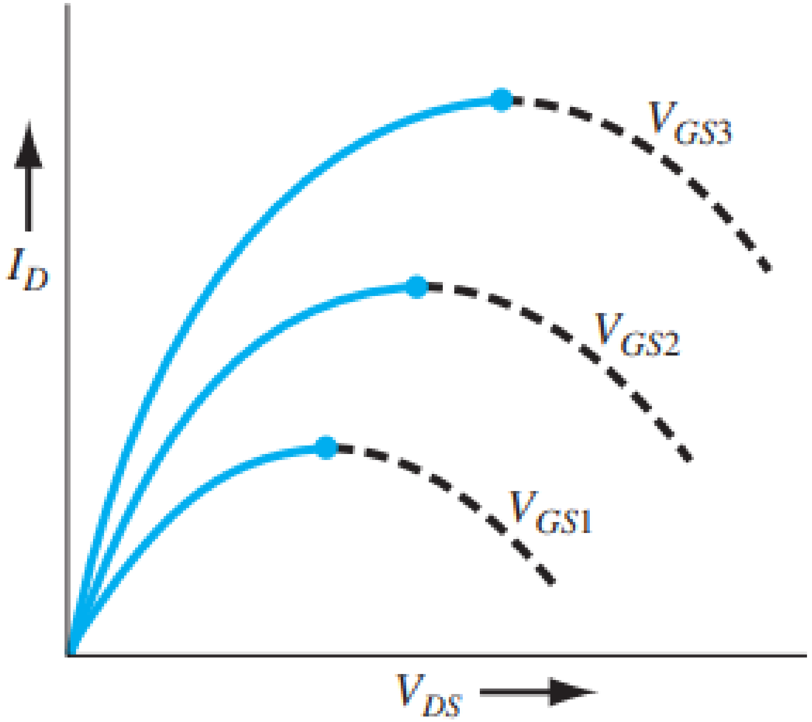
$$I_D = \frac{W\mu_n C_{ox}}{2\mathrm{L}}\left[2\left(V_{GS} - V_T\right)V_{DS} - V_{DS}^{\ 2}\right](\text{適用非飽和區})$$

$$k_n' = \mu_n C_{ox}\left(process\_parameter\right)$$

$$K_n = \frac{W\mu_n C_{ox}}{2\mathrm{L}}\left(conduction\_parameter\right)$$

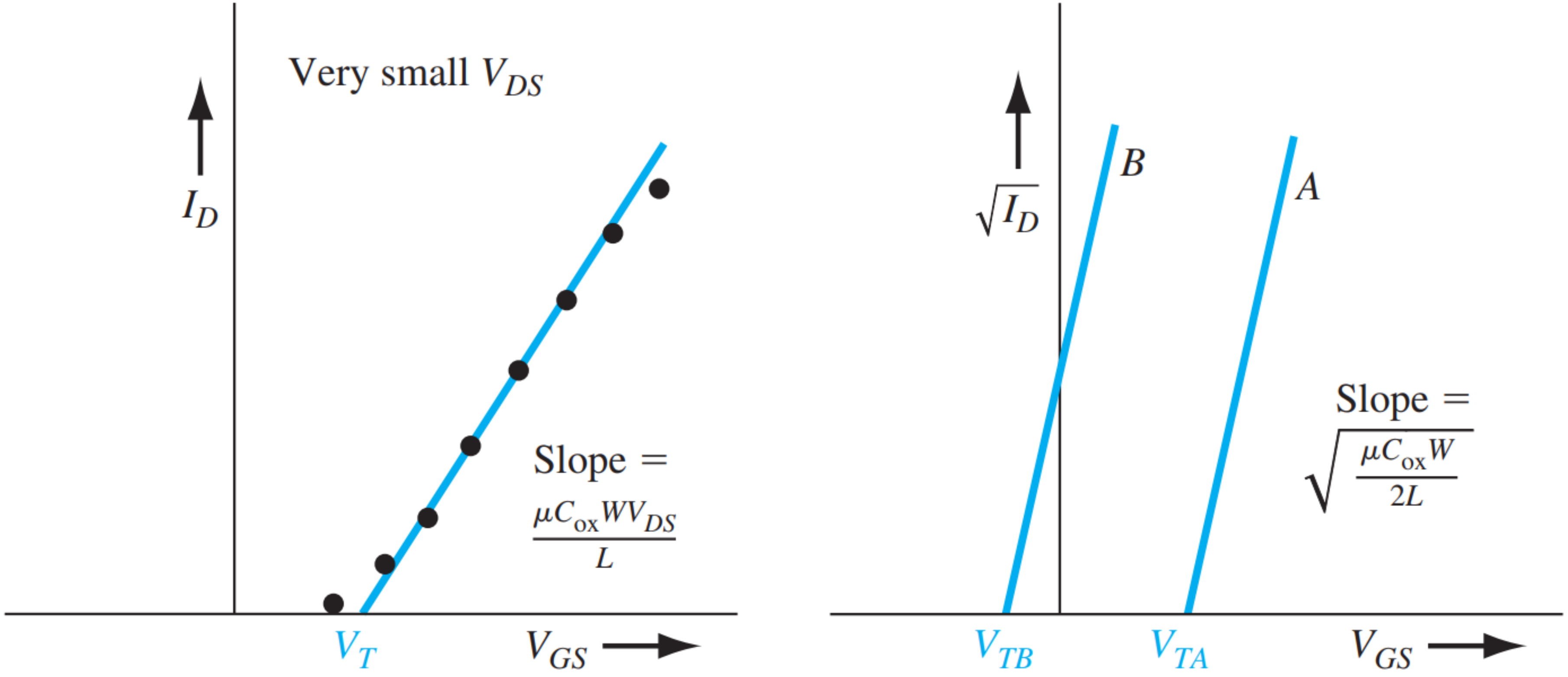
$$\partial I_D \big/ \partial V_{DS} = 0 \Rightarrow V_{DS} = V_{GS} - V_T \text{帶回} \mathrm{I}_D$$

$$I_D\left(sat\right) = \frac{W\mu_n C_{ox}}{2L}\left(V_{GS} - V_T\right)^2$$



The Ideal I-V Relation for n-channel MOSFET:

$$I_D = K_n\left[2\left(V_{GS}-V_T\right)V_{DS}-V_{DS}^2\right] \Rightarrow 2K_n\left(V_{GS}-V_T\right)V_{DS}$$



Example 10.8

Objective: Determine the inversion carrier mobility from experimental results.

Consider an n-channel MOSFET with $W = 15\ \mu m$, $L = 2\ \mu m$, and $C_{ox} = 6.9 \times 10^{-8}\ F/cm^2$. Assume that the drain current in the nonsaturation region for $V_{DS} = 0.10$ V is $I_D = 35\ \mu A$ at $V_{GS} = 1.5$ V and $I_D = 75\ \mu A$ at $V_{GS} = 2.5$ V.

$$I_{D2} - I_{D1} = \frac{W\mu_n C_{ox}}{L}(V_{GS2} - V_{GS1})V_{DS}$$

$$75 \times 10^{-6} - 35 \times 10^{-6} = \left(\frac{15}{2}\right)\mu_n(6.9 \times 10^{-8})(2.5 - 1.5)(0.10)$$

$$\mu_n = 773\ \text{cm}^2/\text{V-s}$$

$$V_T = 0.625\ \text{V}$$

The Ideal I-V Relation for p-channel MOSFET:

$$I_D = \frac{W}{2L}\mu_p C_{ox}\left[2\left(V_{SG}+V_T\right)V_{SD}-V_{SD}^2\right]$$

$$I_D = \frac{W}{2L}k_n'\left[2\left(V_{SG}+V_T\right)V_{SD}-V_{SD}^2\right]$$

$$I_D = K_n\left[2\left(V_{SG}+V_T\right)V_{SD}-V_{SD}^2\right]$$

$$V_{SD}=V_{SG}+V_T \Rightarrow I_D = K_n\left(V_{SG}+V_T\right)^2$$