Semiconductor Manufacturing Technology

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Chapter 9

IC Fabrication Process Overview

Objectives

After studying the material in this chapter, you will be able to:

1. Draw a diagram showing how a typical wafer flows in a sub-micron CMOS IC fab.
2. Give an overview of the six major process areas and the sort/test area in the wafer fab.
3. For each of the 14 CMOS manufacturing steps, describe its primary purpose.
4. Discuss the key process and equipment used in each CMOS manufacturing step.

Major Fabrication Steps in MOS Process Flow

Operations fall into four basic categories: layering, patterning, etching, and doping

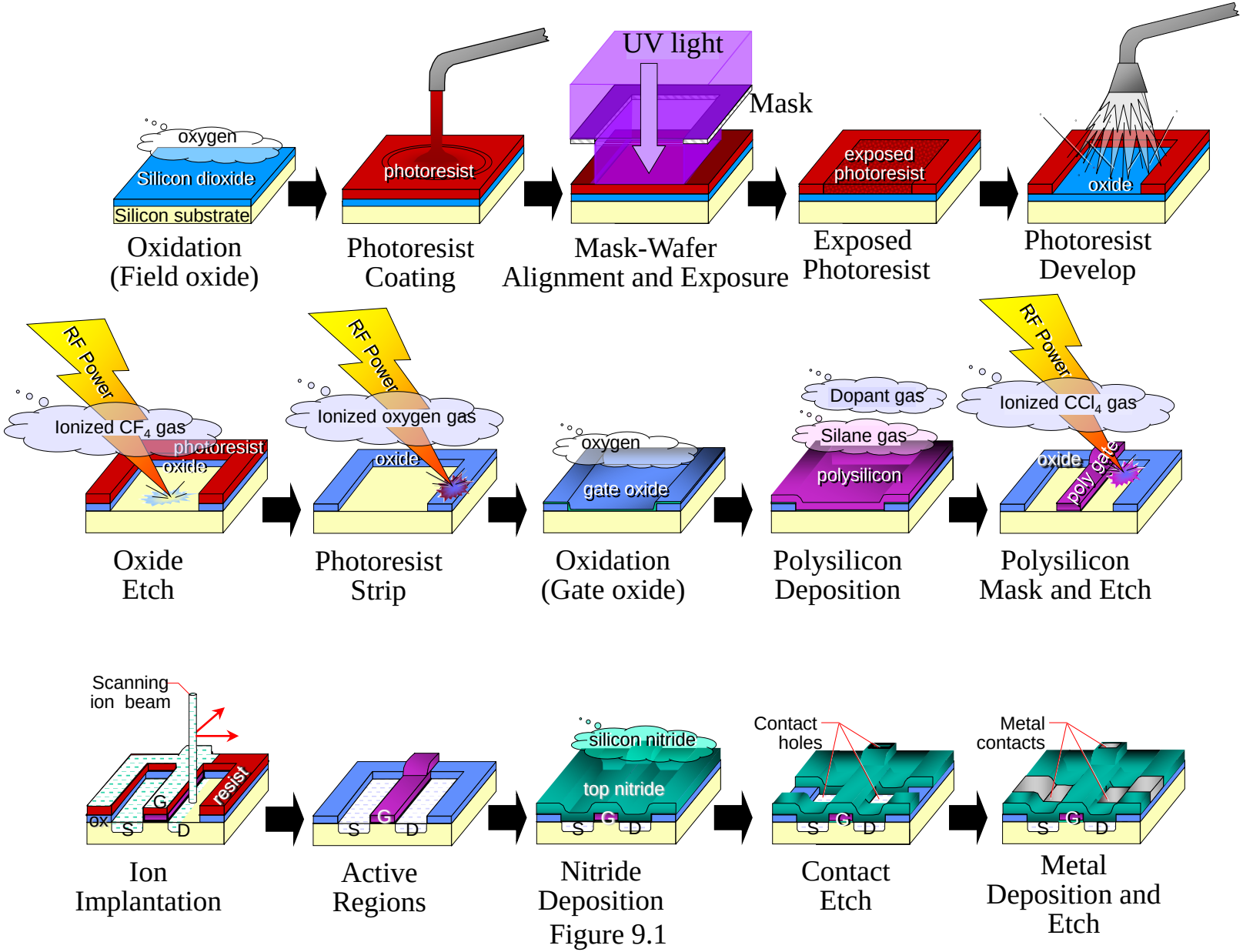
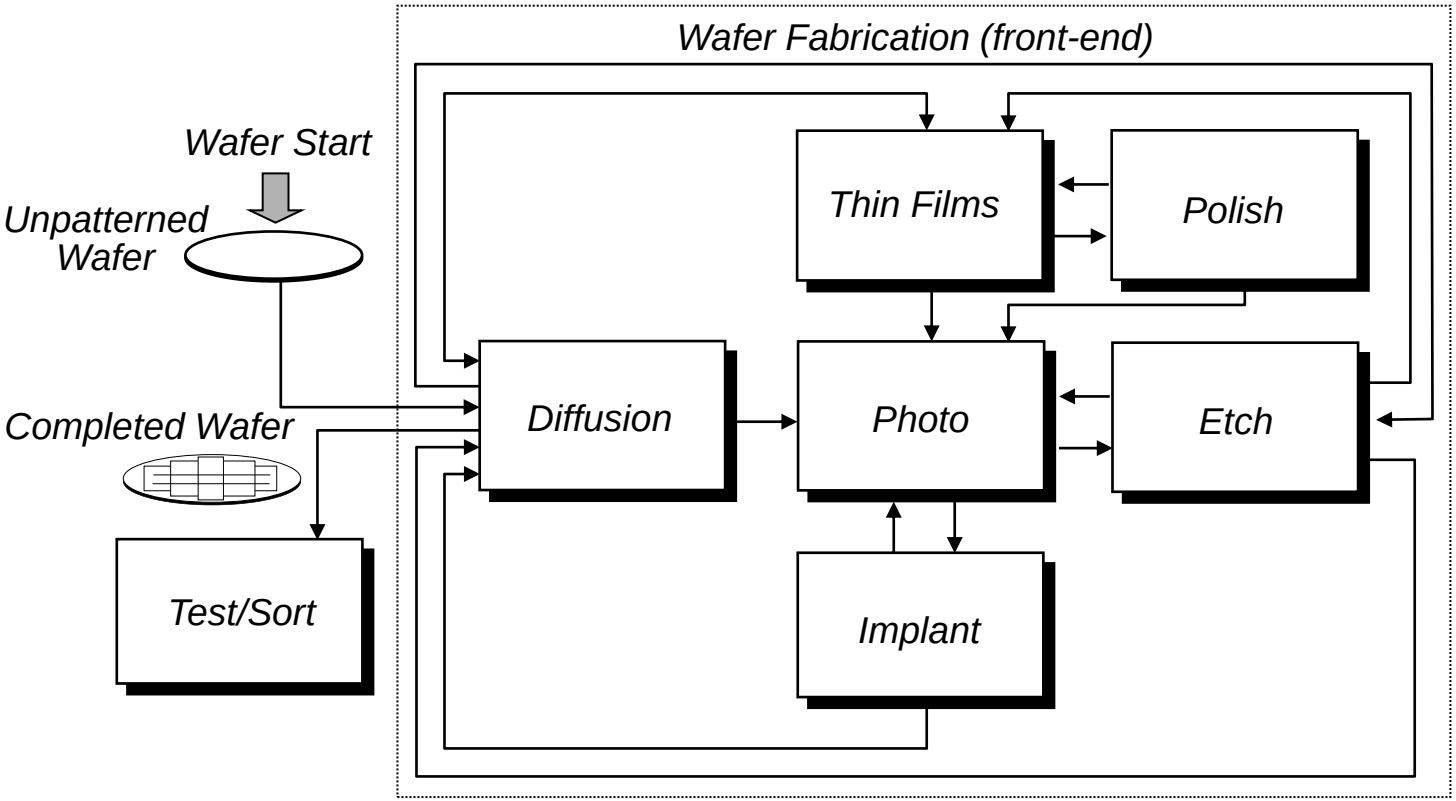


Figure 9.1

CMOS Process Flow

- Overview of Areas in a Wafer Fab
  - Diffusion (oxidation, deposition and doping)
  - Photolithography
  - Etch
  - Ion Implant
  - Thin Films
  - Polish
- CMOS Manufacturing Steps
- Parametric Testing
- 6~8 weeks involve 350-step

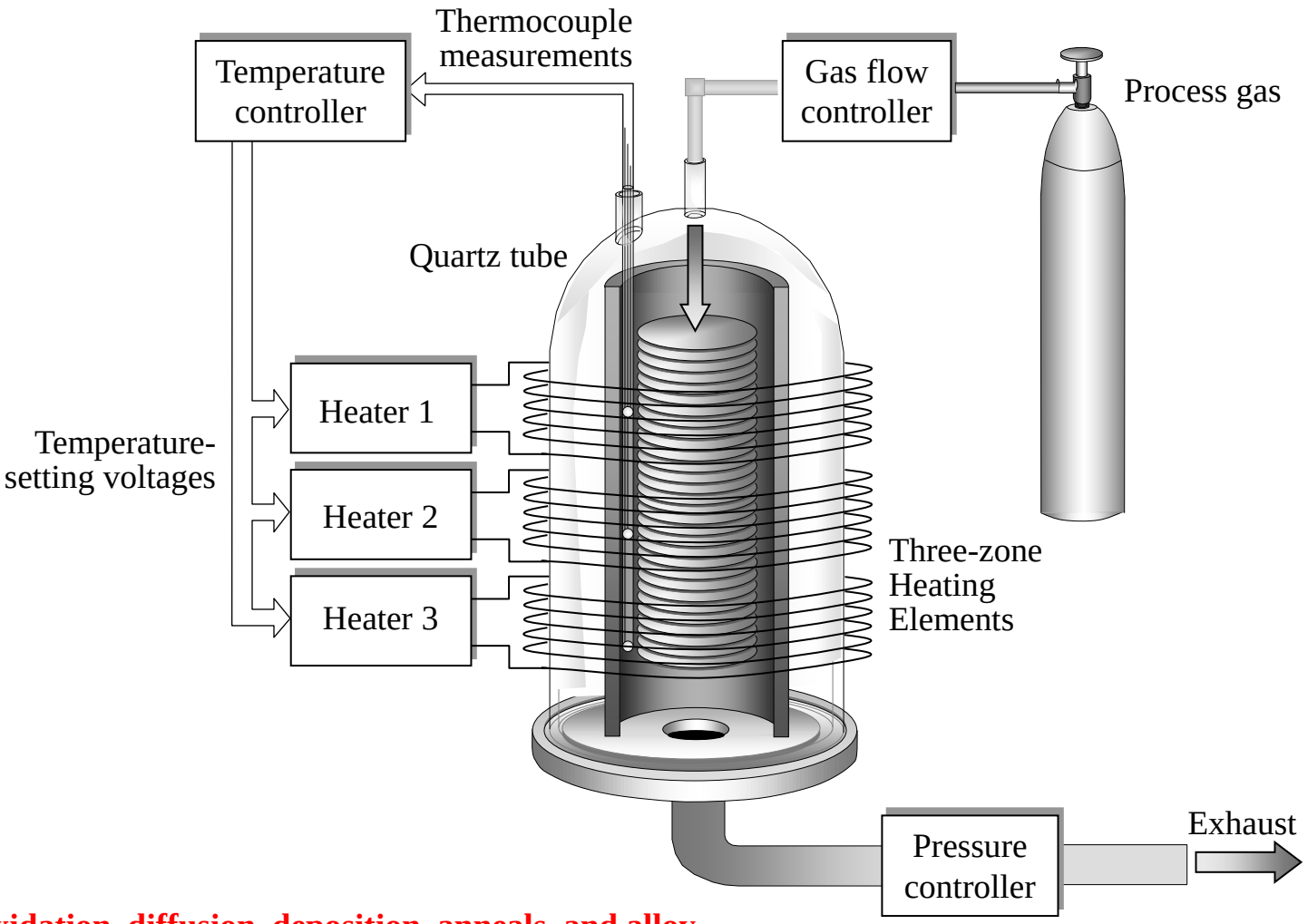
Model of Typical Wafer Flow in a Sub-Micron CMOS IC Fab



6 major production areas

Figure 9.2

Diffusion: Simplified Schematic of High-Temperature Furnace



Can do : oxidation, diffusion, deposition, anneals, and alloy

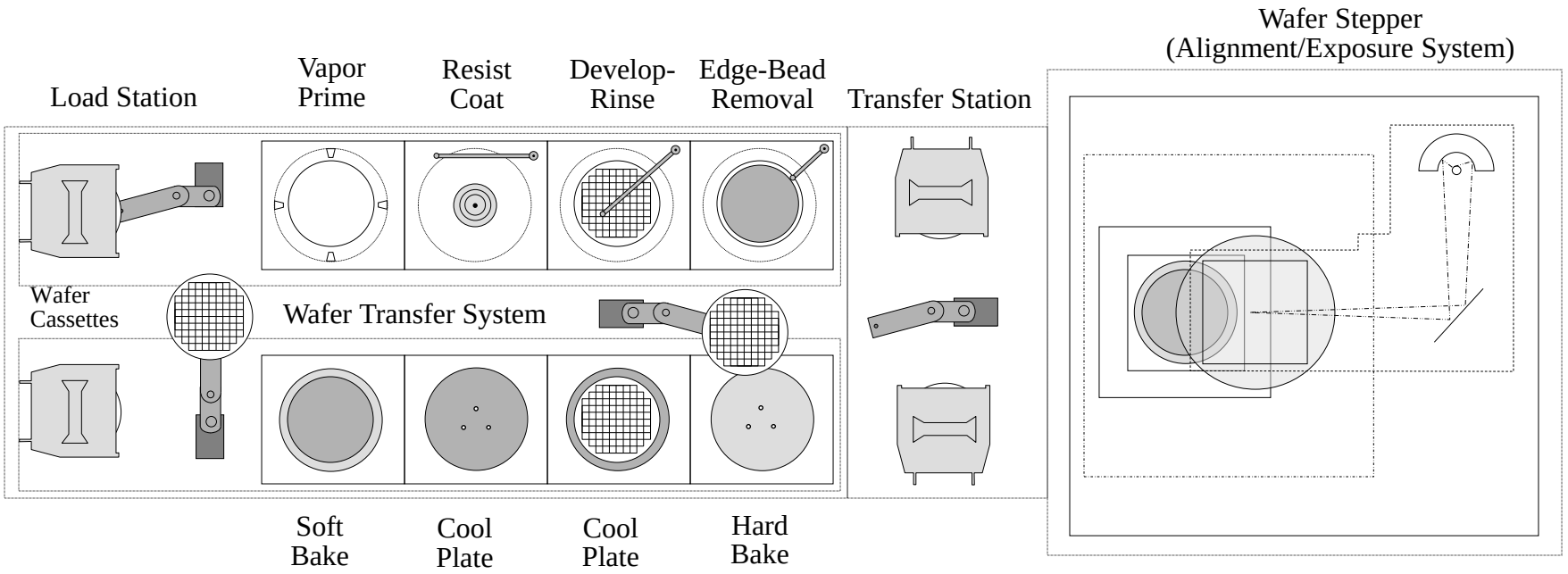
Figure 9.3

Photolithography Bay in a Sub-micron Wafer Fab

- It is to photograph the image of a circuit pattern onto the photoresist that coats the wafer surface.
- Yellow fluorescent does not affect photoresist, but sensitive to UV

Photo 9.1

Simplified Schematic of a Photolithography Processing Module



Note: **wafers flow from photolithography into only two other areas: <u>etch</u> and <u>ion</u> <u>implant</u>**

Figure 9.4

Simplified Schematic of Dry Plasma Etcher

- The etch process creates a permanent pattern on the wafer in areas not protected by the photoresist pattern
- Including: dry etching, wet etching and photoresist stripper
- After dry etching: photoresist stripper + wet cleaning

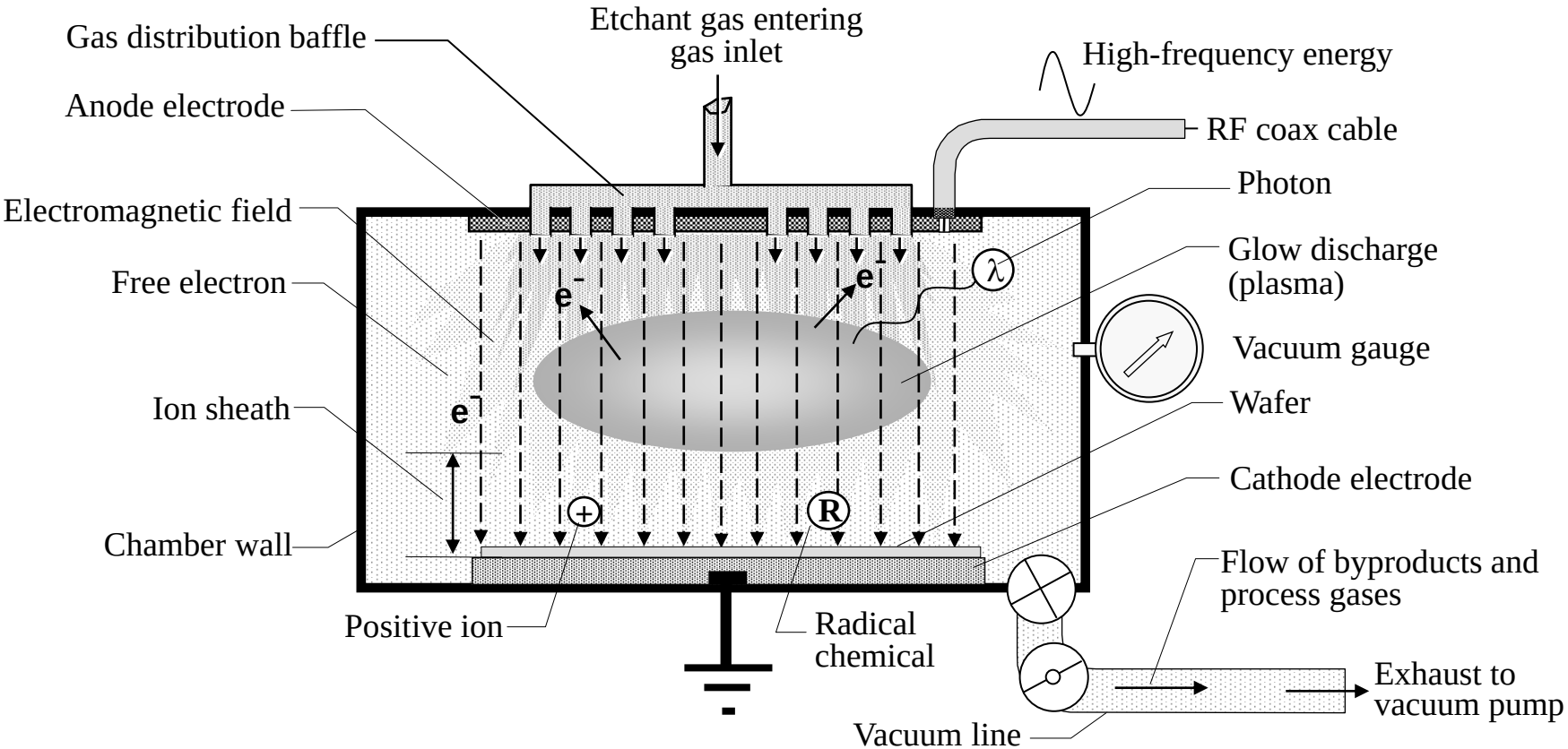


Figure 9.5

Simplified Schematic of Ion Implanter

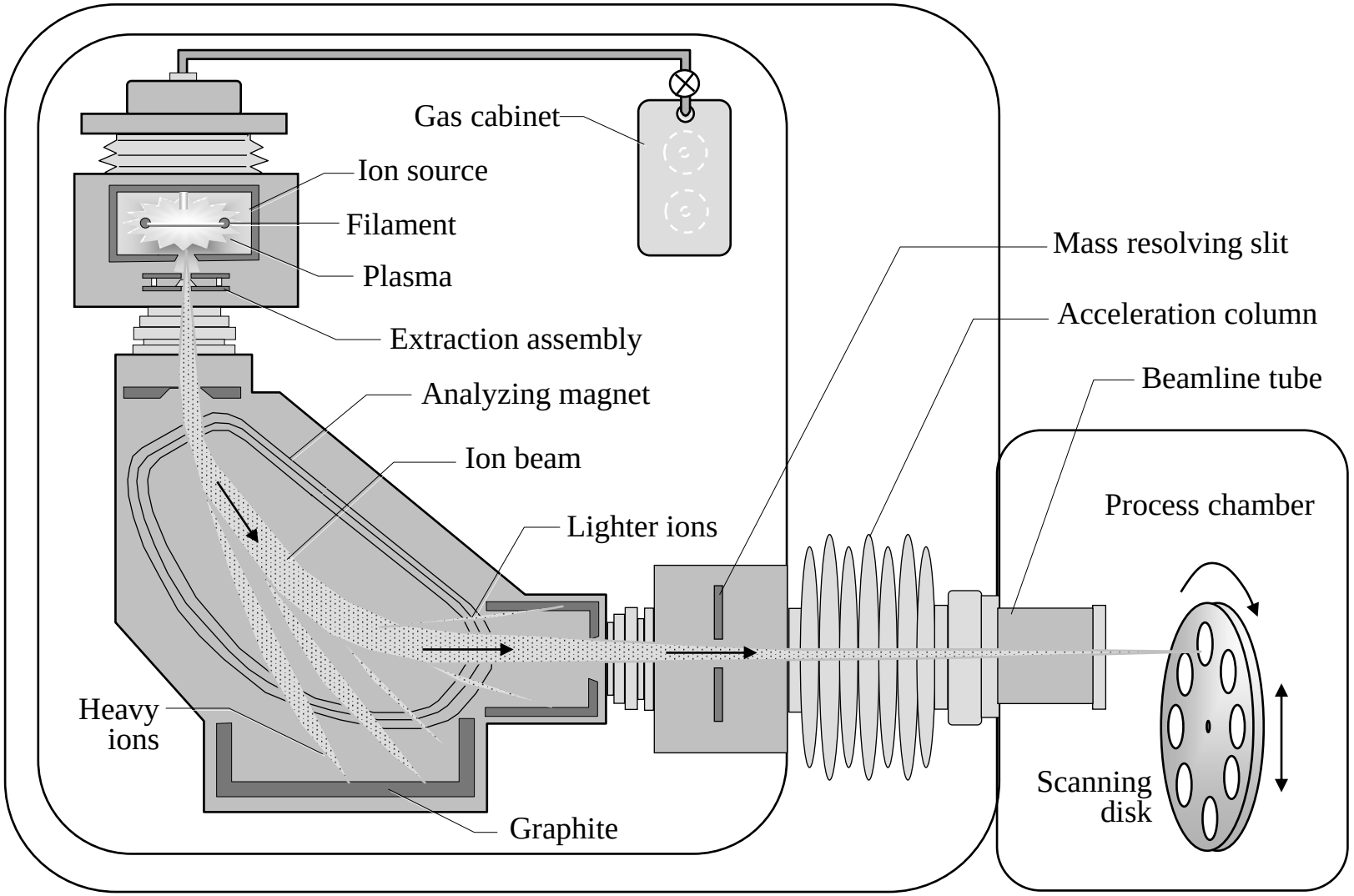


Figure 9.6

Thin Film Metallization Bay

Photo 9.2

Simplified Schematics of CVD Processing System

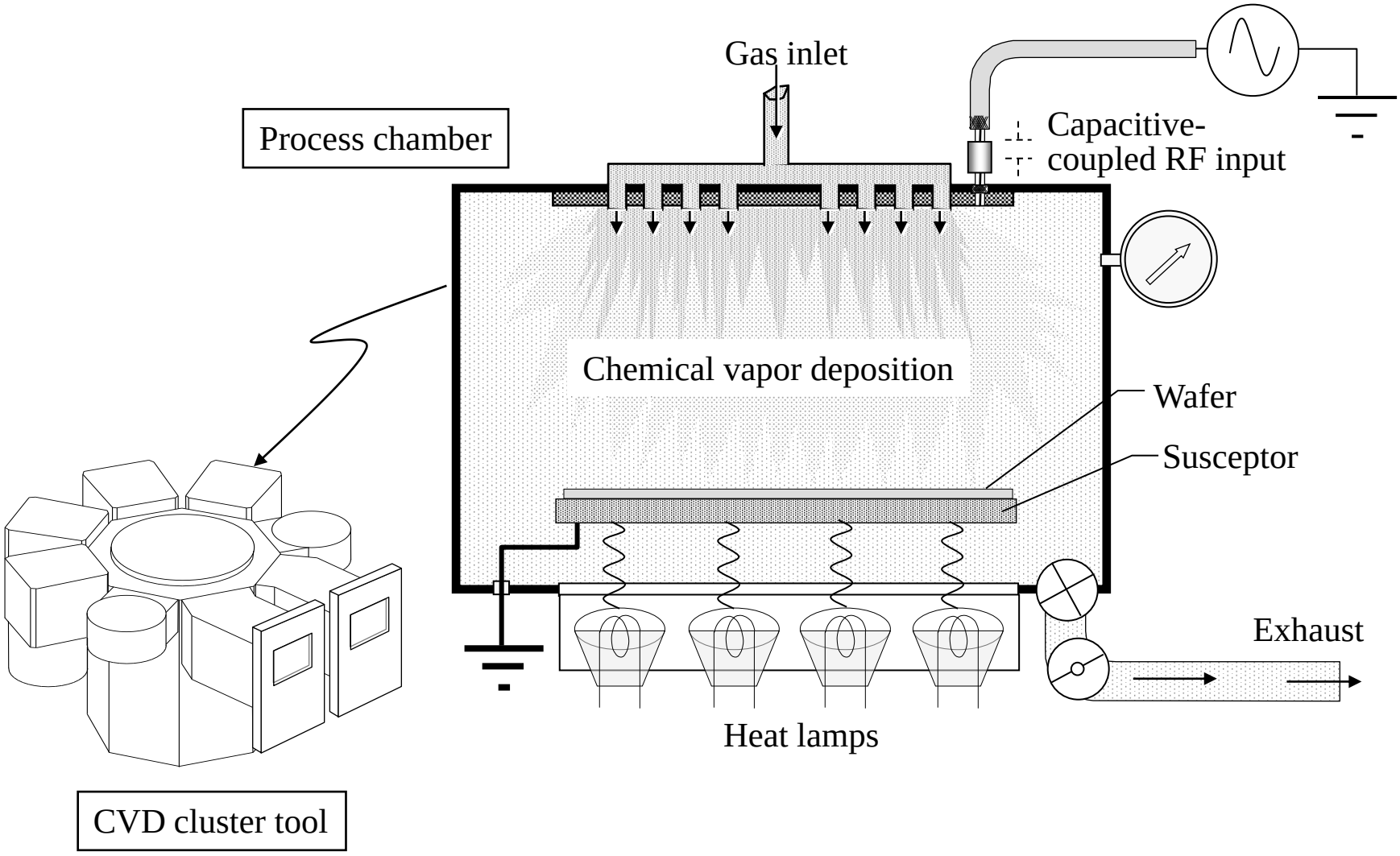


Figure 9.7

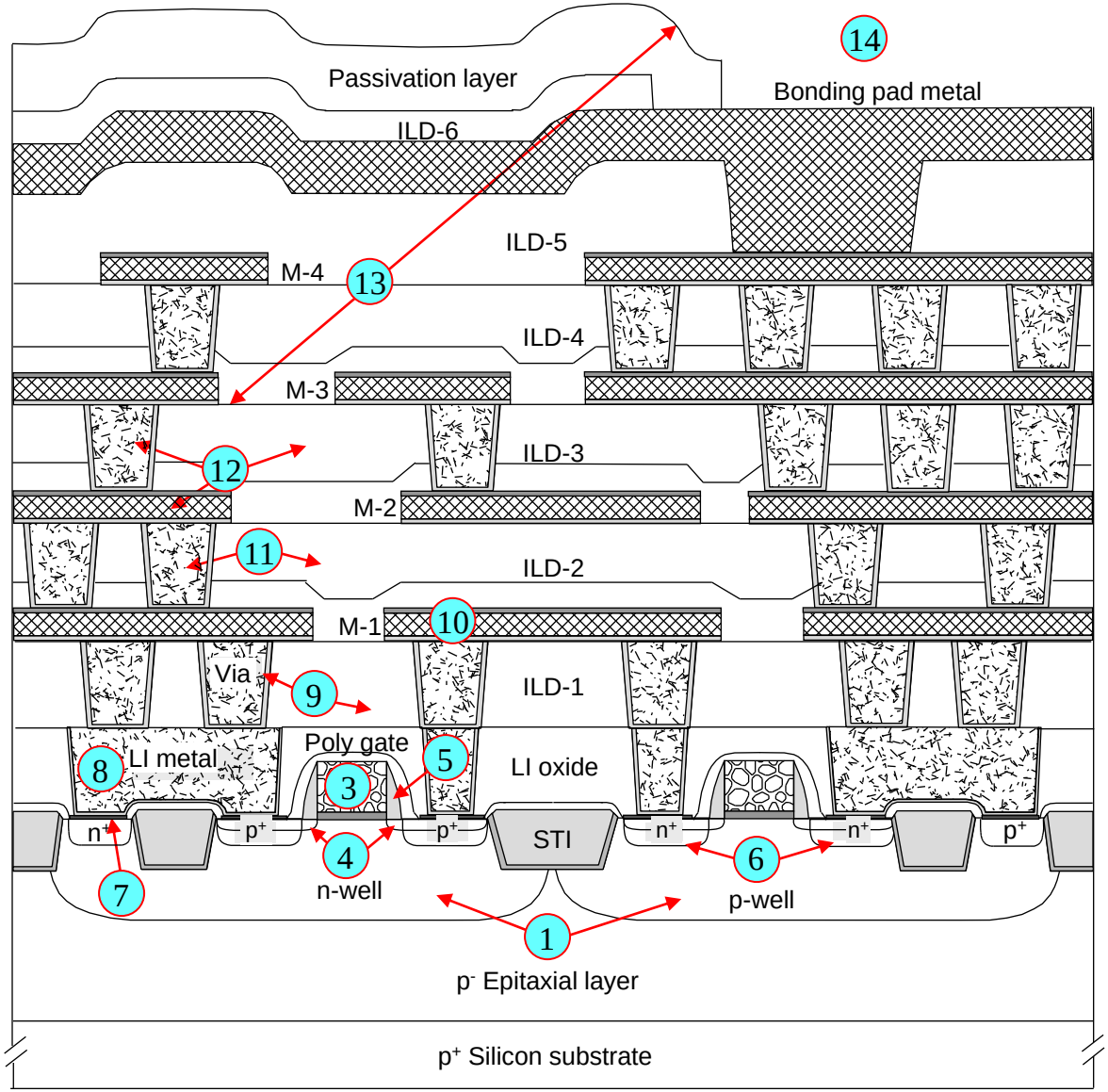
Polish Bay in a Sub-micron Wafer Fab

- Chemical mechanical planarization (CMP) process is to planarize the top surface of the wafer by lowering the high topography to be level with the lower surface area of the wafer
- It combines chemical etching and mechanical abrading to remove layer

Photo 9.3

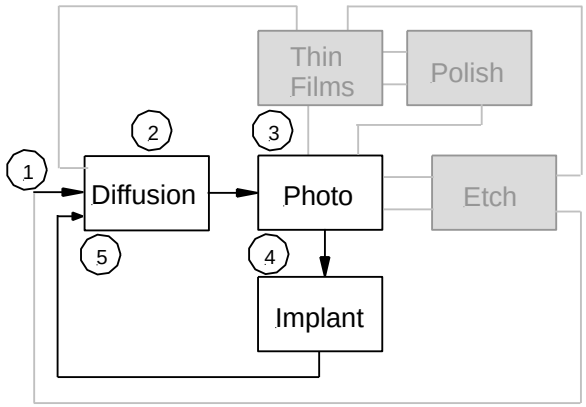
CMOS Manufacturing Steps

1. Twin-well Implants
2. Shallow Trench Isolation
3. Gate Structure
4. Lightly Doped Drain Implants
5. Sidewall Spacer
6. Source/Drain Implants
7. Contact Formation
8. Local Interconnect
9. Interlayer Dielectric to Via-1
10. First Metal Layer
11. Second ILD to Via-2
12. Second Metal Layer to Via-3
13. Metal-3 to Pad Etch
14. Parametric Testing



n-well Formation

- Epitaxial layer : improved quality and fewer defect
- In step 2, initial oxide (15 nm) : (1) protects epi layer from contamination, (2) prevents excessive damage to ion/implantation, (3) control the depth of the dopant during implantation
- In step 5, anneal: (1) drive-in, (2) repair damage, (3) activation



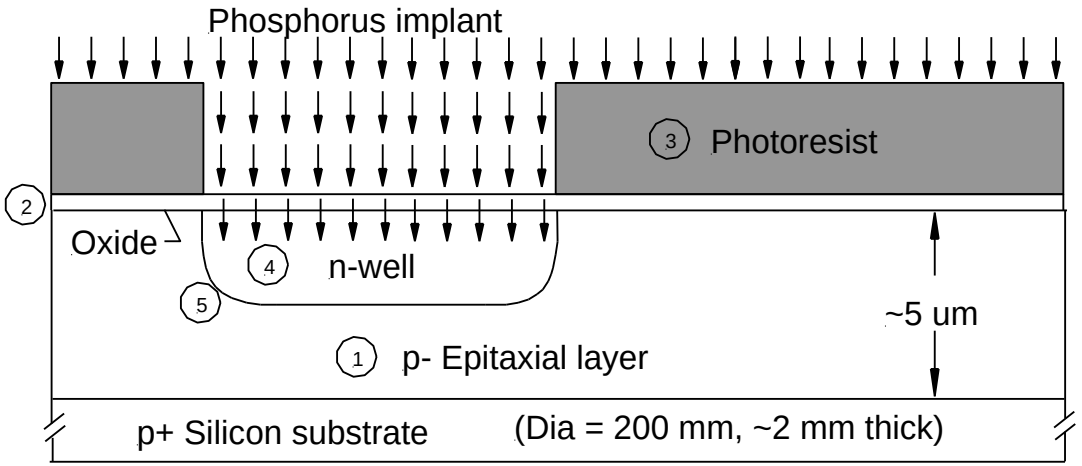
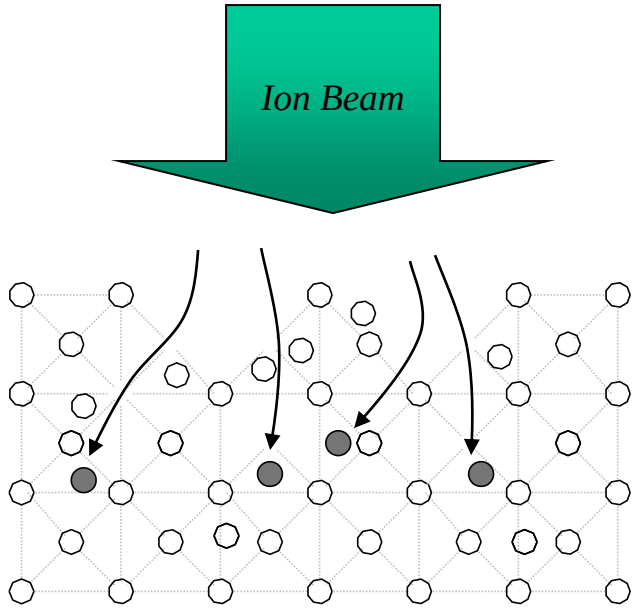


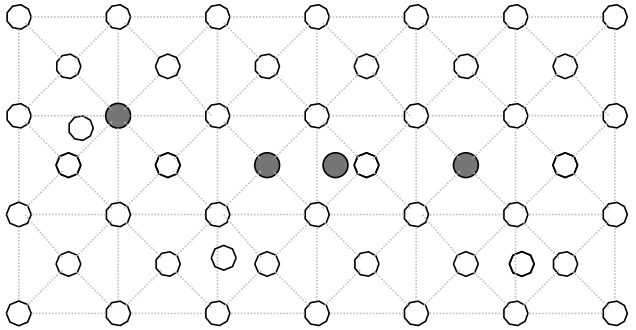
Figure 9.8

Annealing of Silicon Crystal



a) Damaged Si lattice during implant

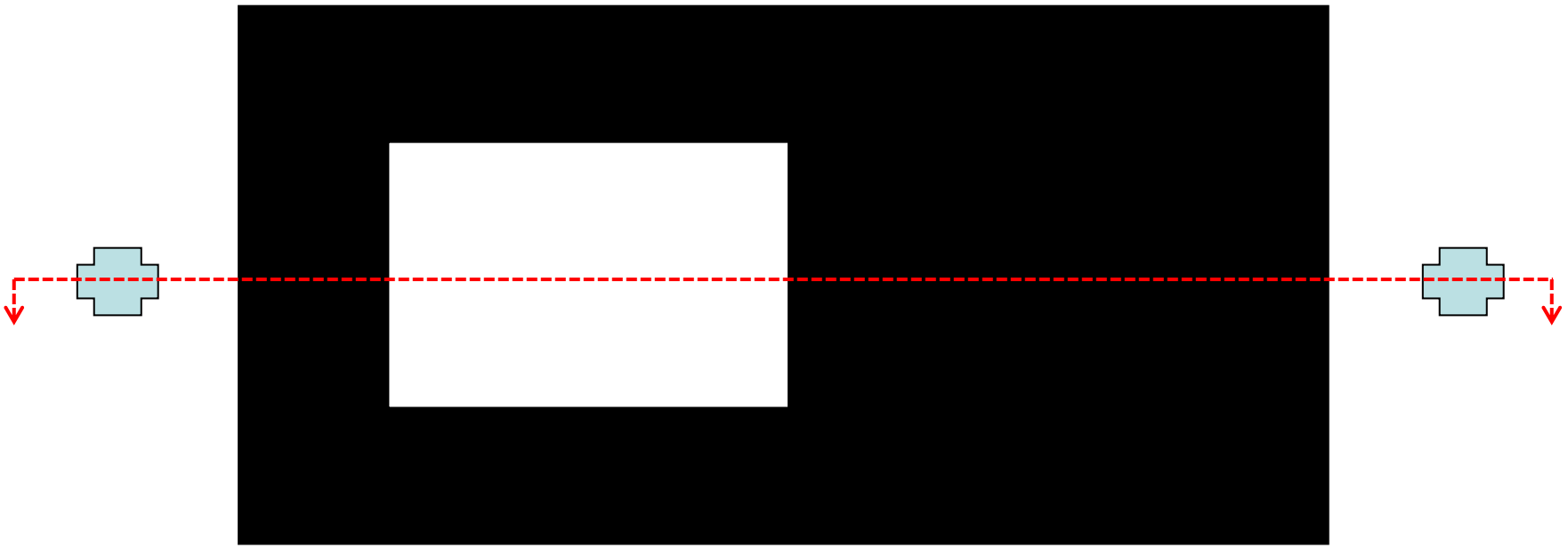
Repaired Si lattice structure and activated dopant-silicon bonds



b) Si lattice after annealing

- *Using Furnace or RTA, hot-wall furnace using high temperature causes extensive dopant diffusion and is undesirable*
- *RTA minimizes a phenomenon known as transient enhanced diffusion, to achieve acceptable junction depth control in shallow implants (~150 ℃/sec)*

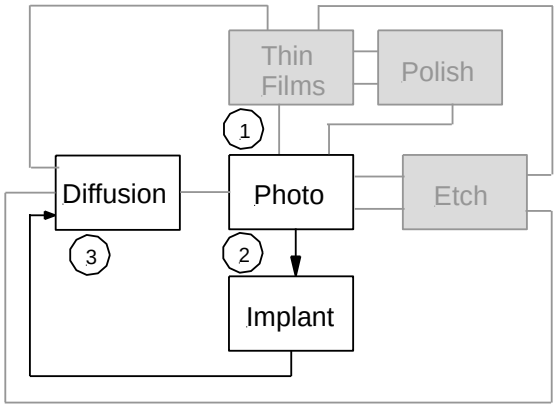
Figure 17.27



Mask # 1 : N-well formation

p-well Formation

- 2nd mask, this mask is the direct opposite of the n-well implant mask
- Boron is 1/3 the mass of P, so 1/3 energy is used.



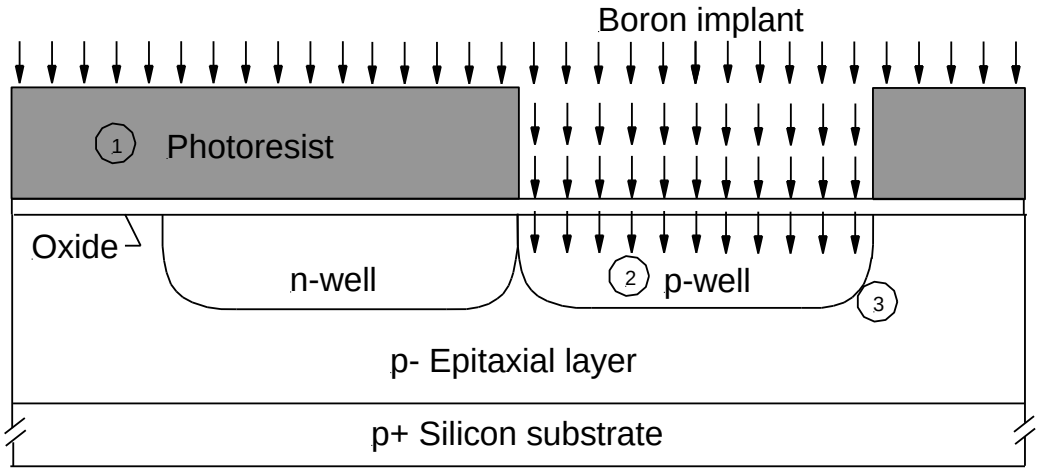
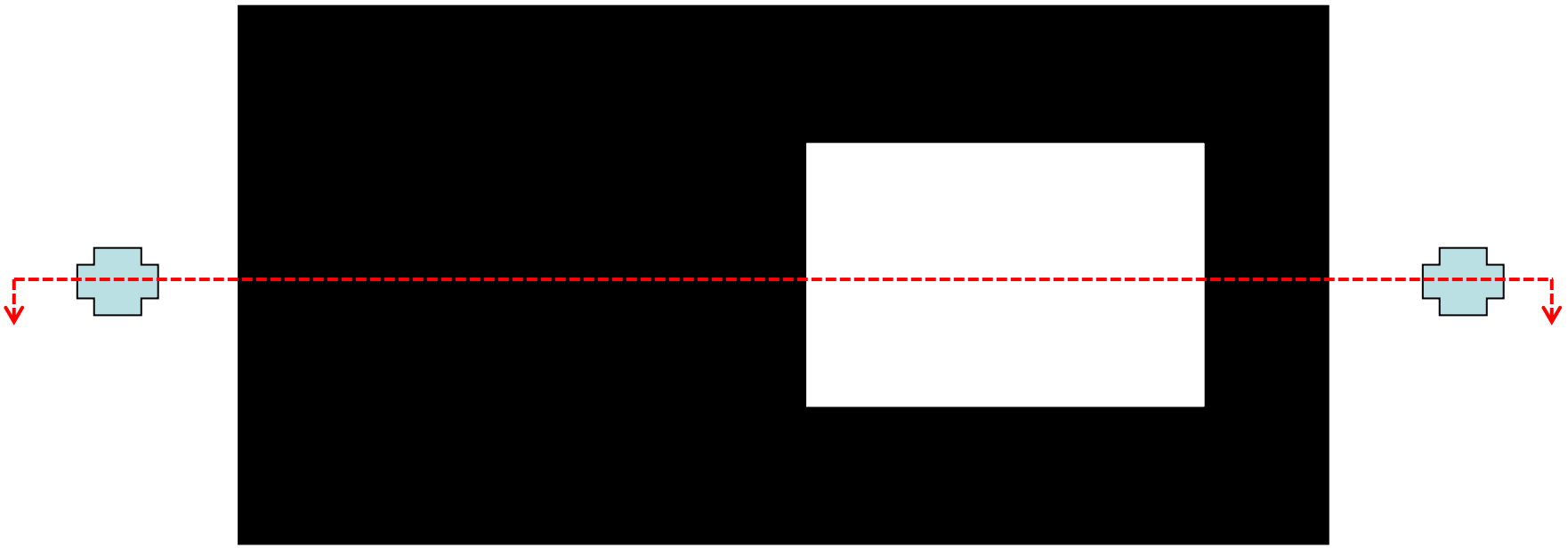


Figure 9.9

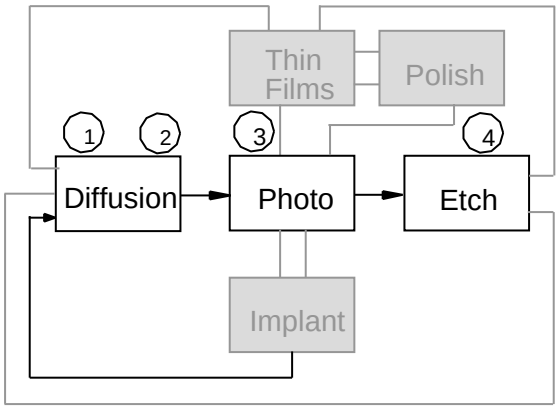


Mask # 2 : P-well formation

STI Trench Etch

STI: shallow trench isolation

- Barrier oxide: a new oxide
- Nitride: (1) protect active region, (2) stop layer during CMP
- 3rd mask
- STI etching



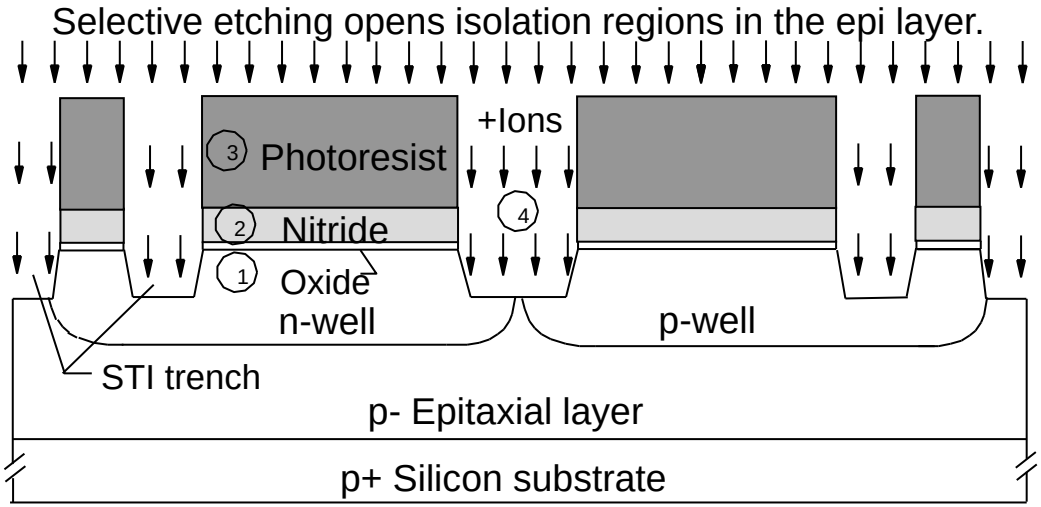
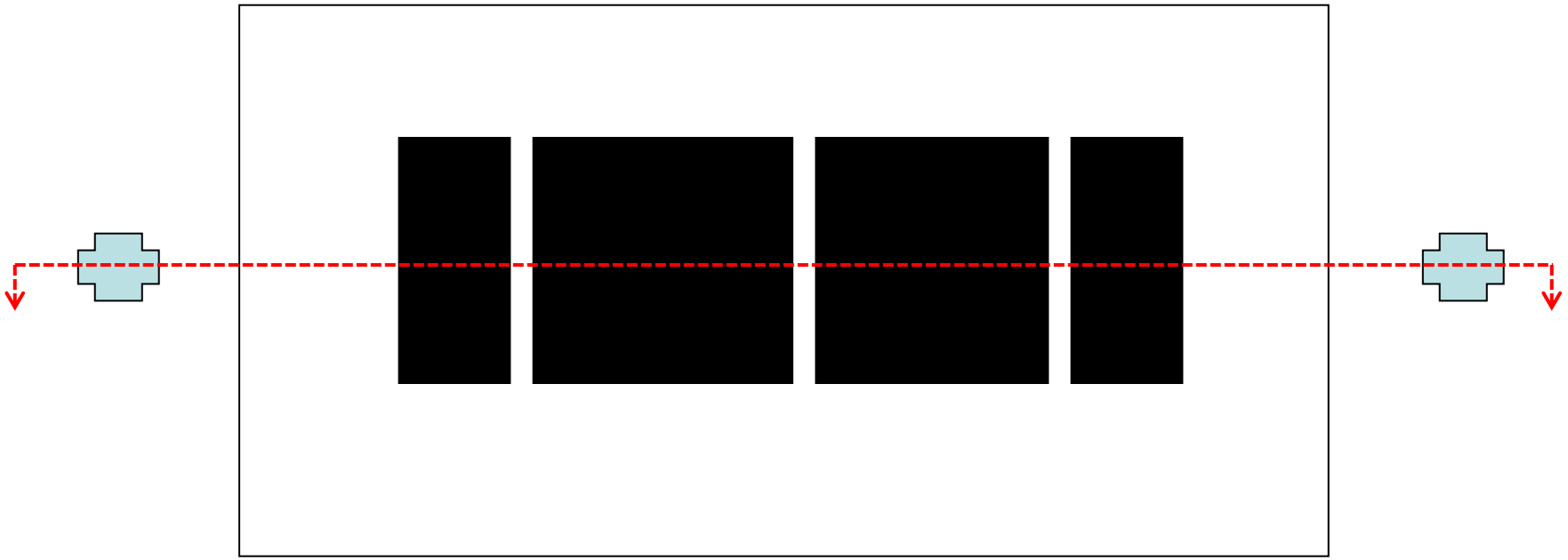


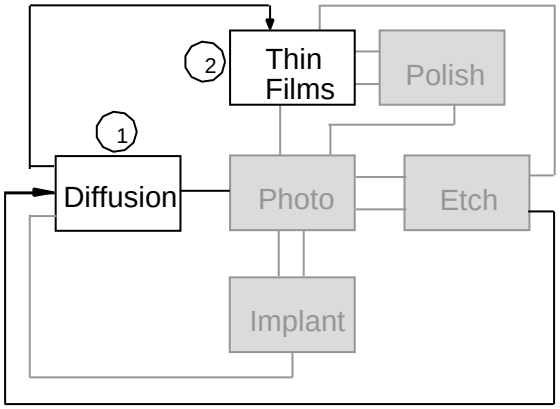
Figure 9.10



Mask # 3: Shallow Trench Isolation formation

STI Oxide Fill

- Liner oxide to improve the interface between the silicon and trench CVD oxide
- CVD oxide deposition or spin-on-glass (SOG)



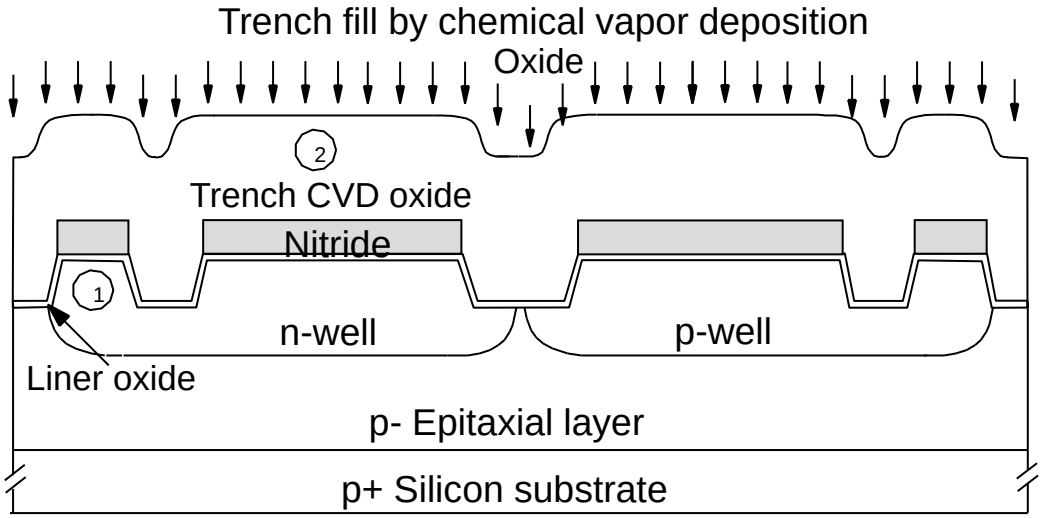
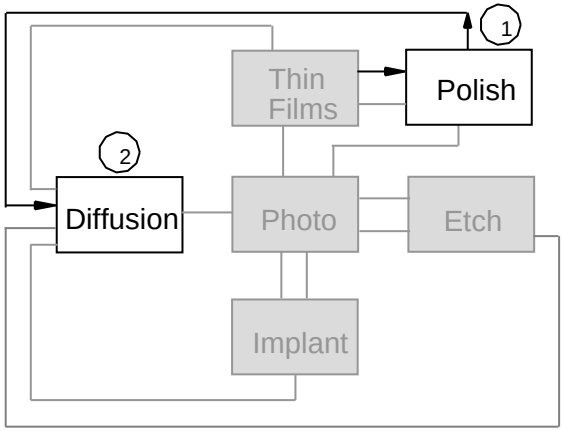


Figure 9.11

STI Formation

1. Trench oxide polish (CMP): nitride as the CMP stop layer since nitride is harder than oxide
2. Nitride strip: hot phosphoric acid
3. Anti-punch-through and Vth adjustment ion implantation



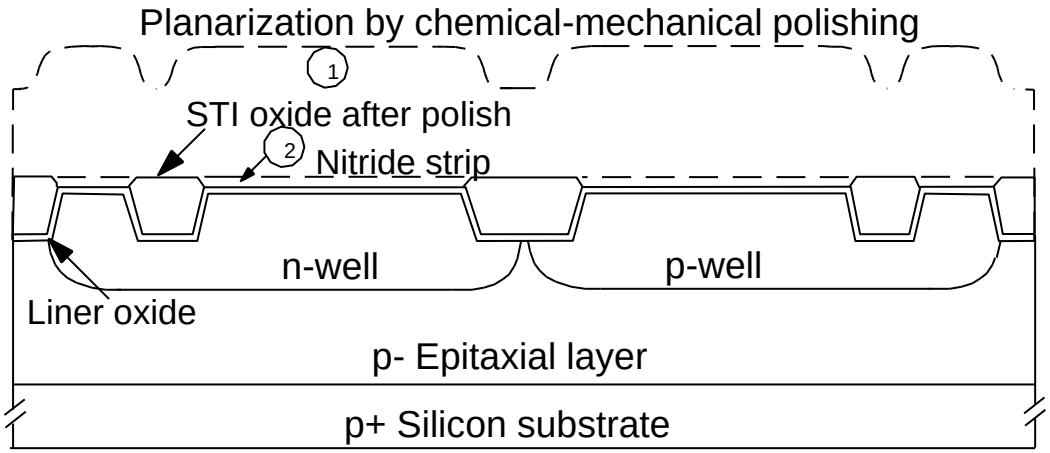
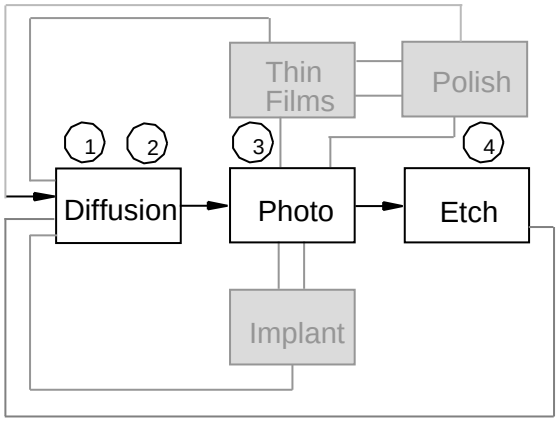


Figure 9.12

Poly Gate Structure Process

- Oxide thickness 1.5 ~ 5.0 nm is thermal grown
- Poly-Si ~ 300 nm is doped and deposited in LPCVD using SiH_4
- Need Antireflective coating (ARC), very critical
- The most critical etching step in dry etching



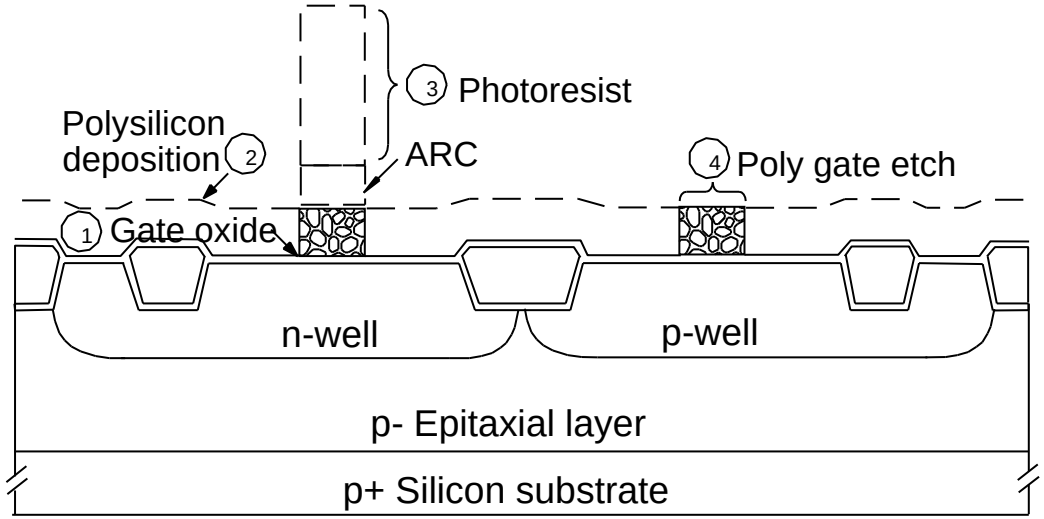
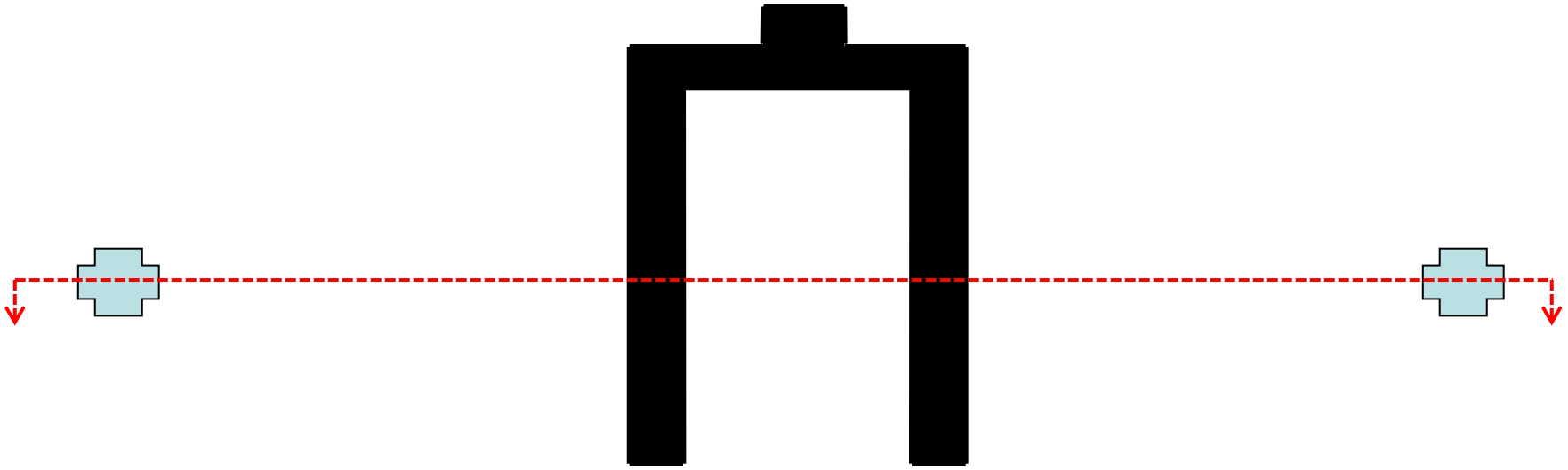


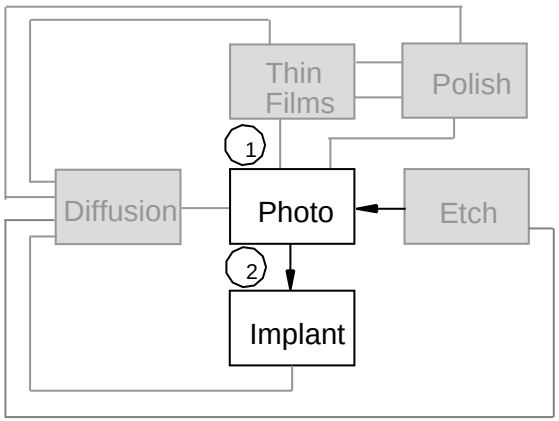
Figure 9.13



Mask # 4 :Poly-Si gate formation

n^- LDD Implant

- LDD: lightly doped drain to reduce S/D leakage
- Large mass implant (BF_2, instead of B, As instead of P) and amorphous surface helps maintain a shallow junction
- 5^{th} mask



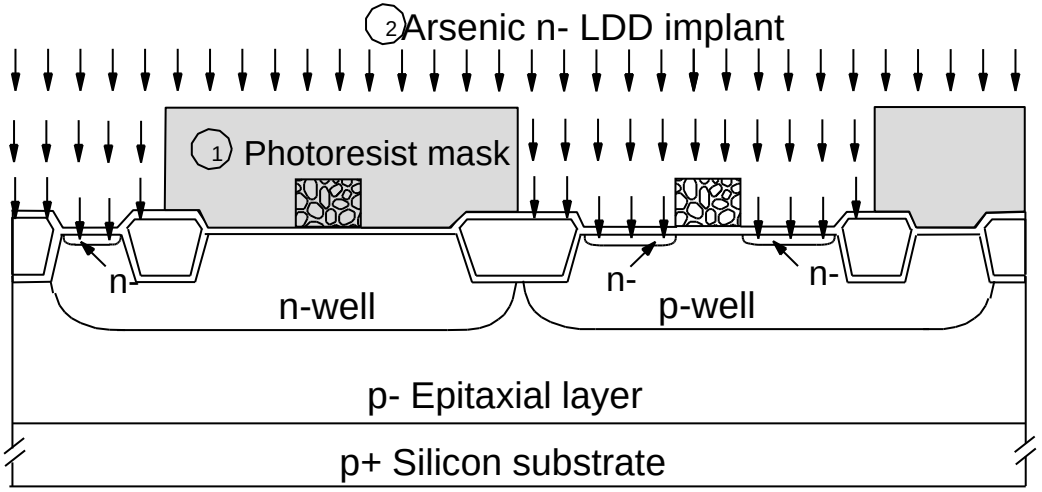
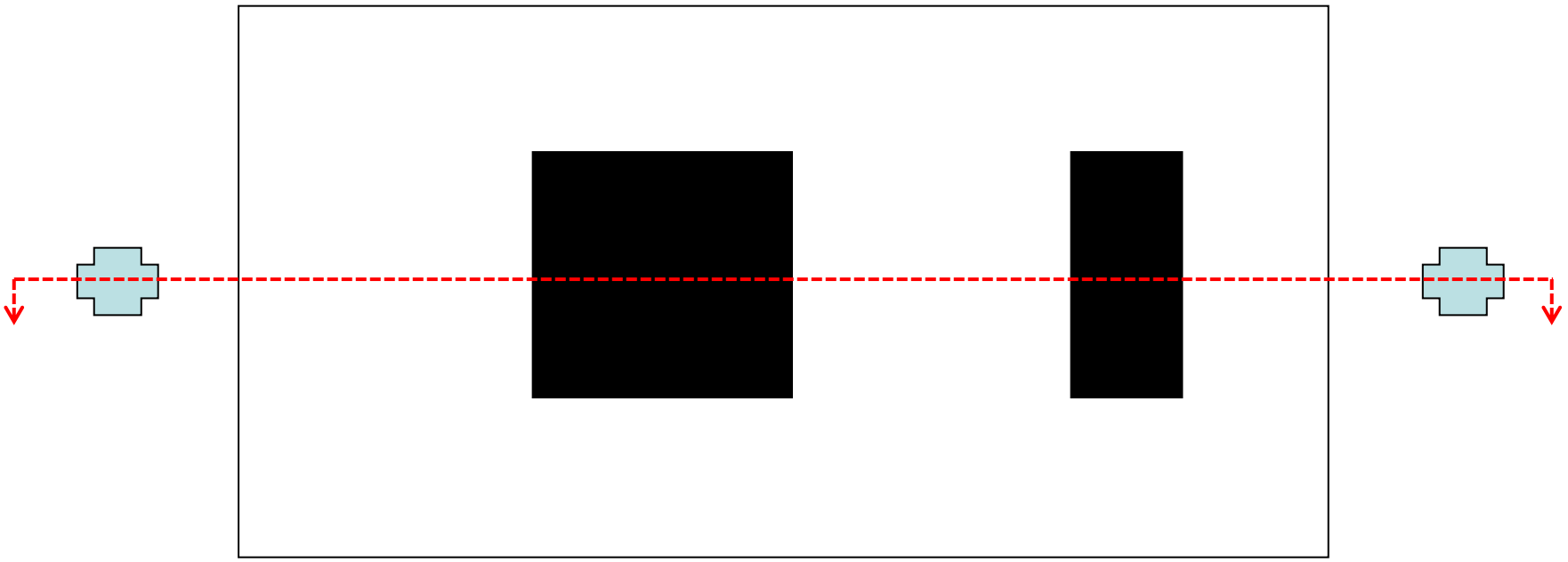


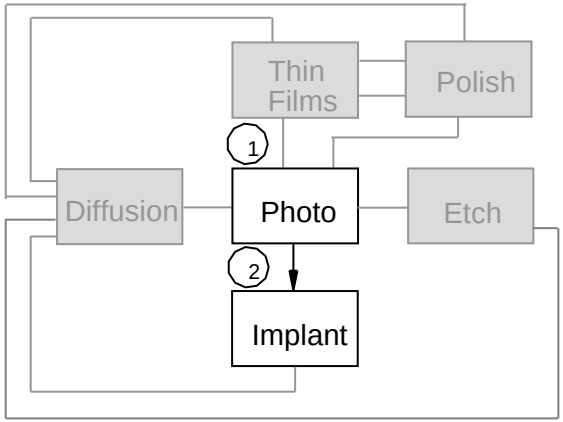
Figure 9.14



Mask # 5: N^- LDD formation

p^- LDD Implant

- 6th mask
- In modern device, high doped drain is used to reduce series resistance. It called S/D extension



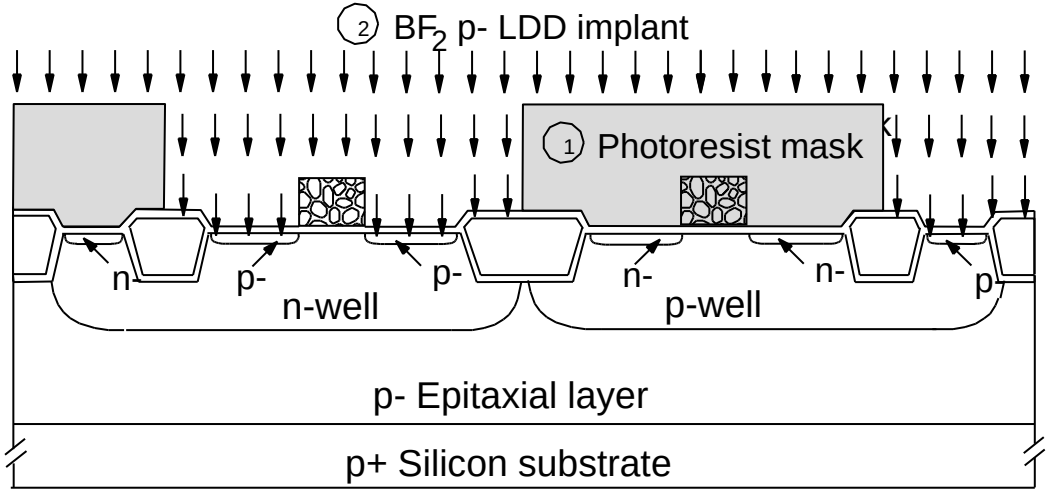
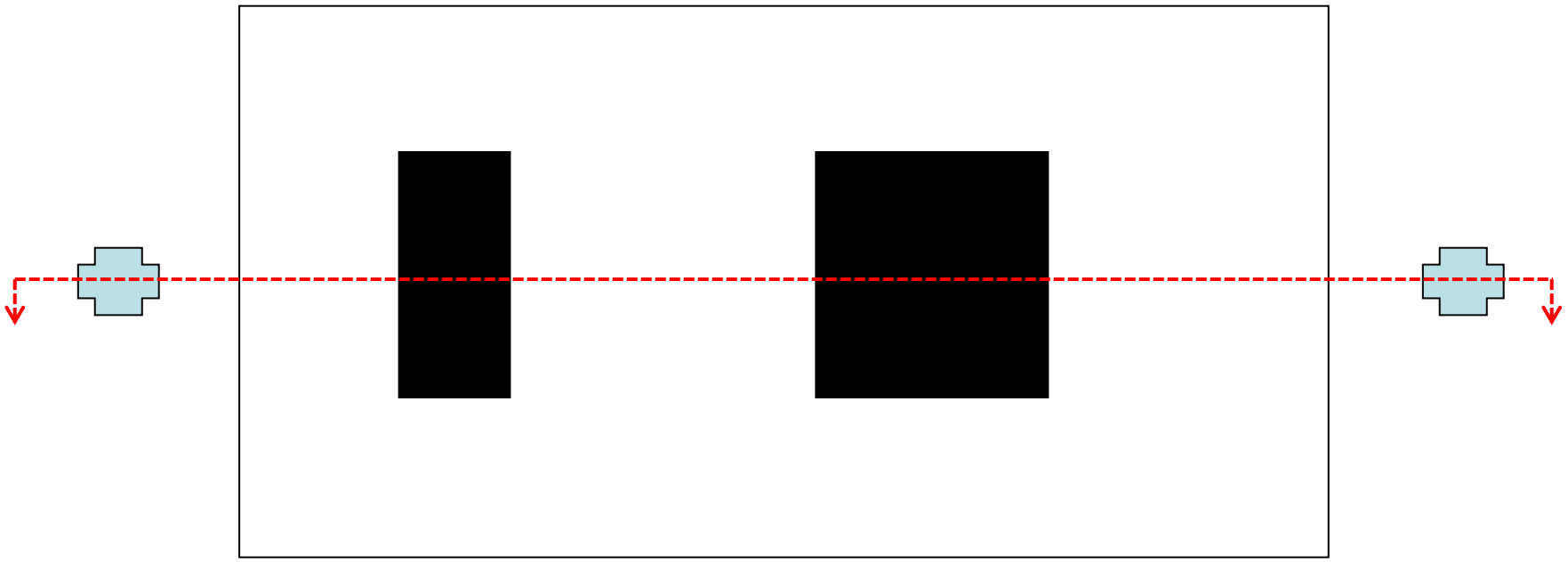


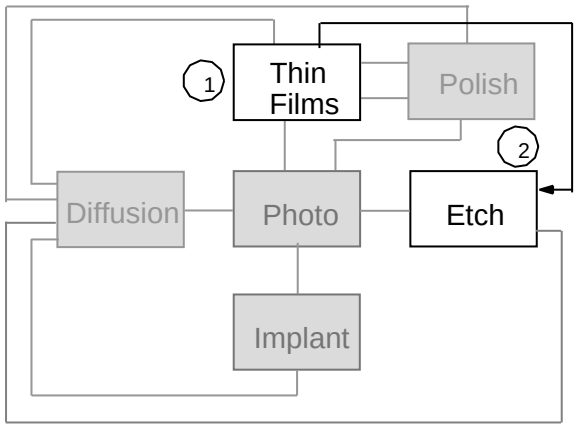
Figure 9.15



Mask # 6: P^- LDD formation

Side Wall Spacer Formation

- Spacer is used to prevent higher S/D implant from penetrating too close to the channel, cover LDD.
- CVD oxide + etch back by anisotropic plasma etching



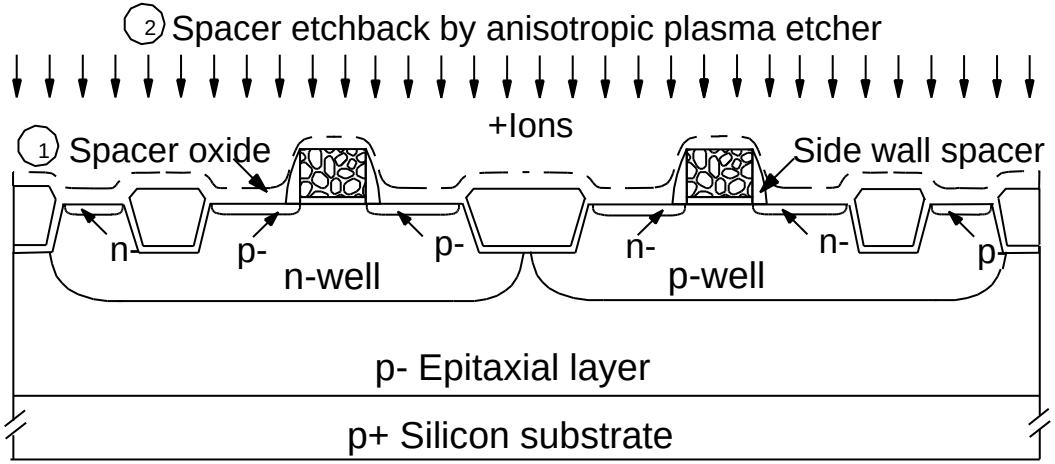
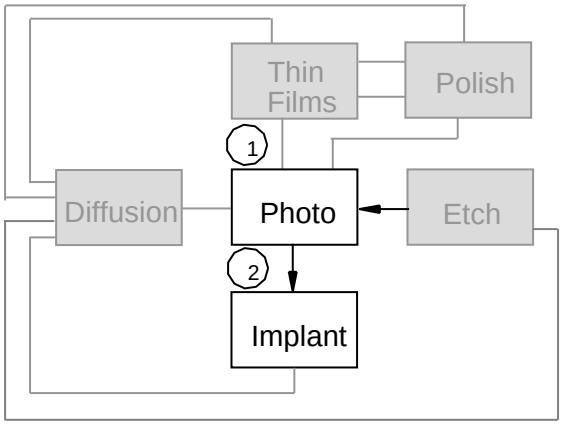


Figure 9.16

n^+ Source/Drain Implant

- Energy is high than LDD I/I, the junction is deep
- 7^{th} mask



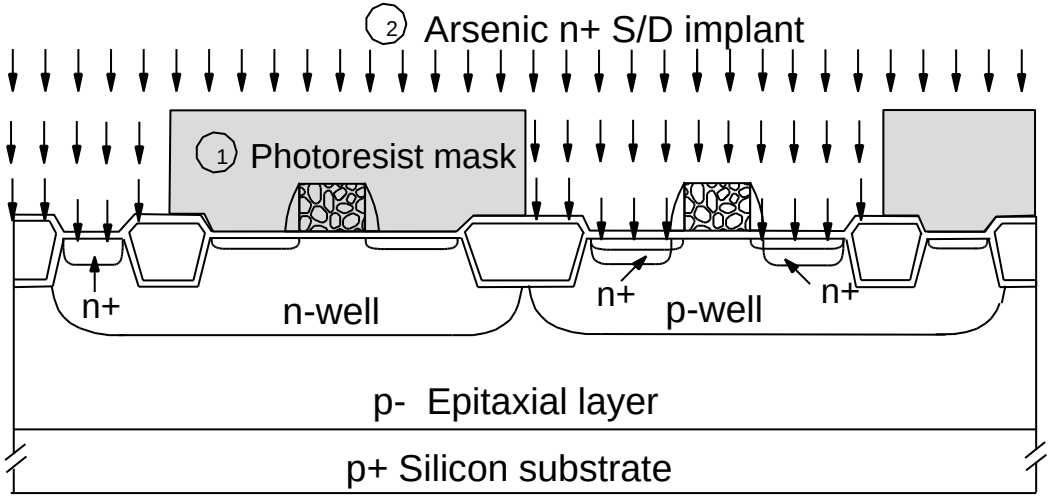
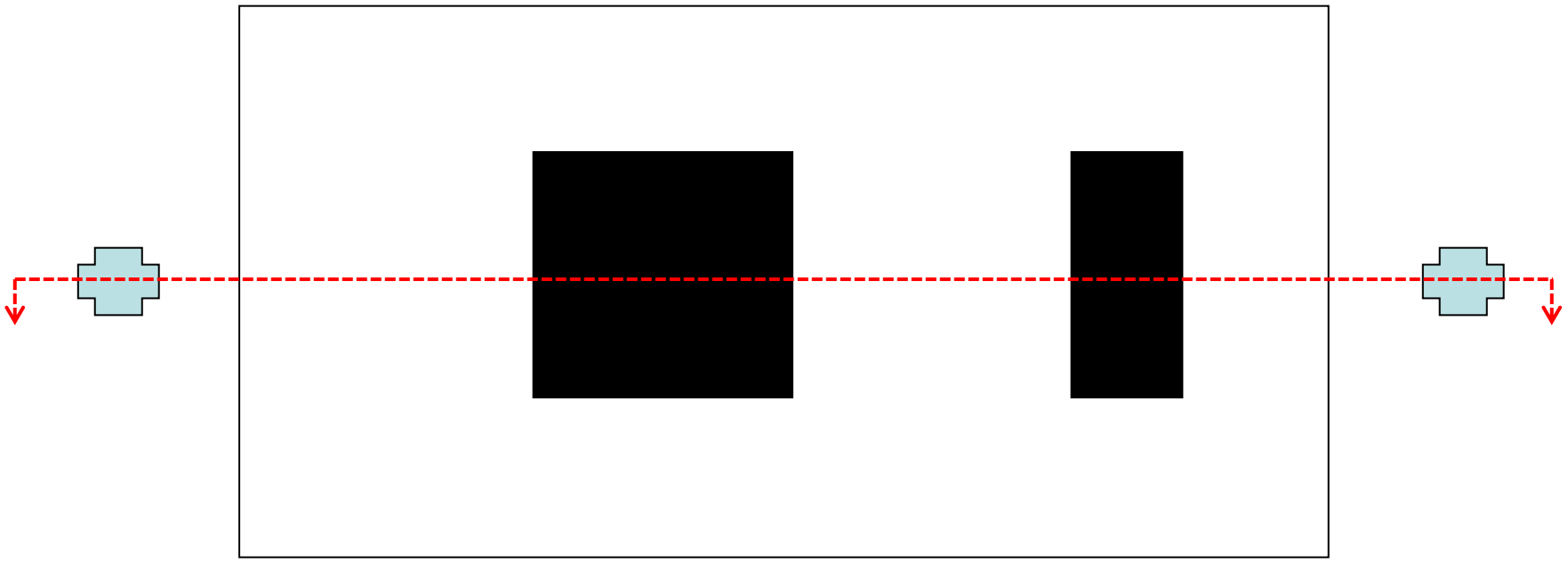


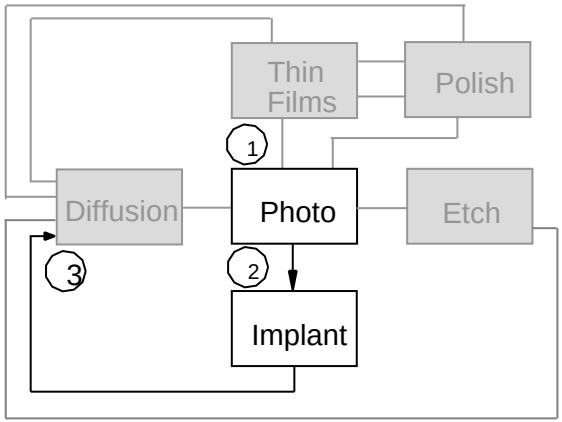
Figure 9.17



Mask # 7: N^+ Source/Drain formation

p^+ Source/Drain Implant

- 8th mask
- Using rapid thermal anneal (RTA) to prevent dopant spreading and to control diffusion of dopant



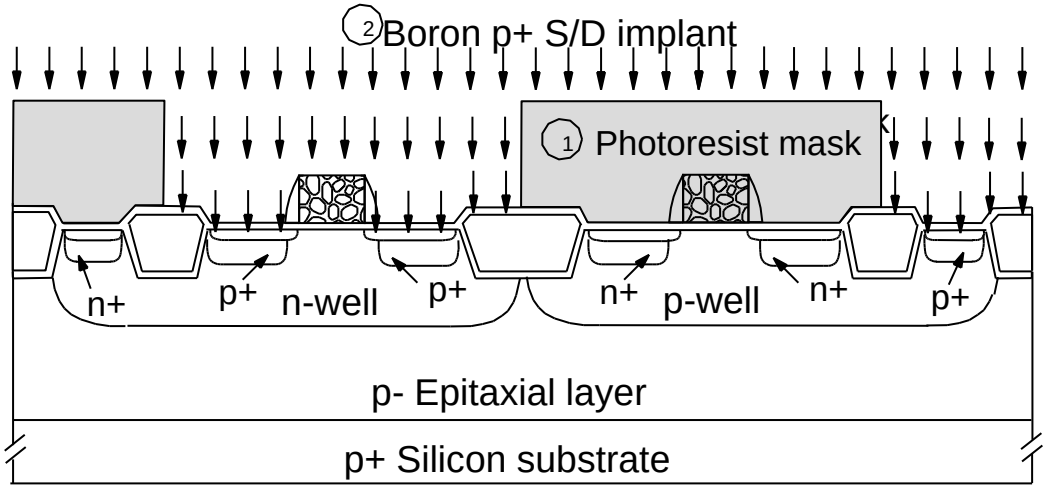
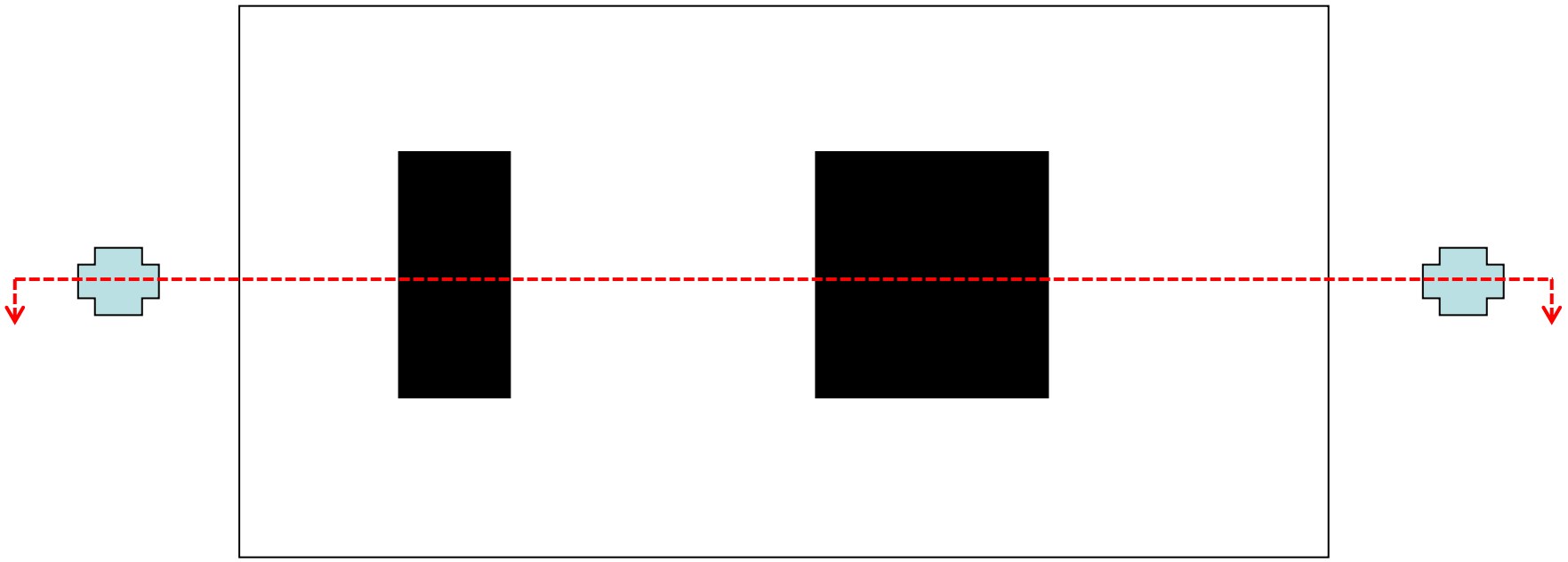


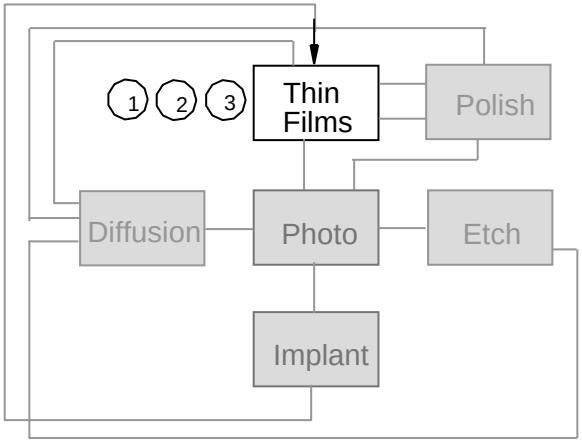
Figure 9.18



Mask # 8 : P^+ Source/Drain formation

Contact Formation

- Titanium (Ti) is a good choice for metal contact due to low resistivity and good adhesion
- No mask needed, called self-align
- Using Ar to sputtering metal
- Anneal to form $TiSi_2$, tisilicide
- Chemical etching to remove unreact Ti, leaving $TiSi_2$, called selective etching



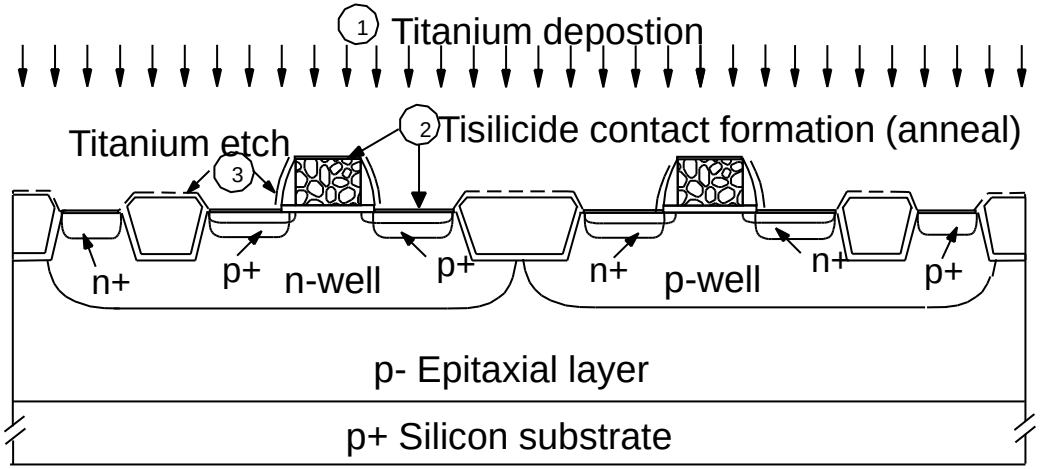
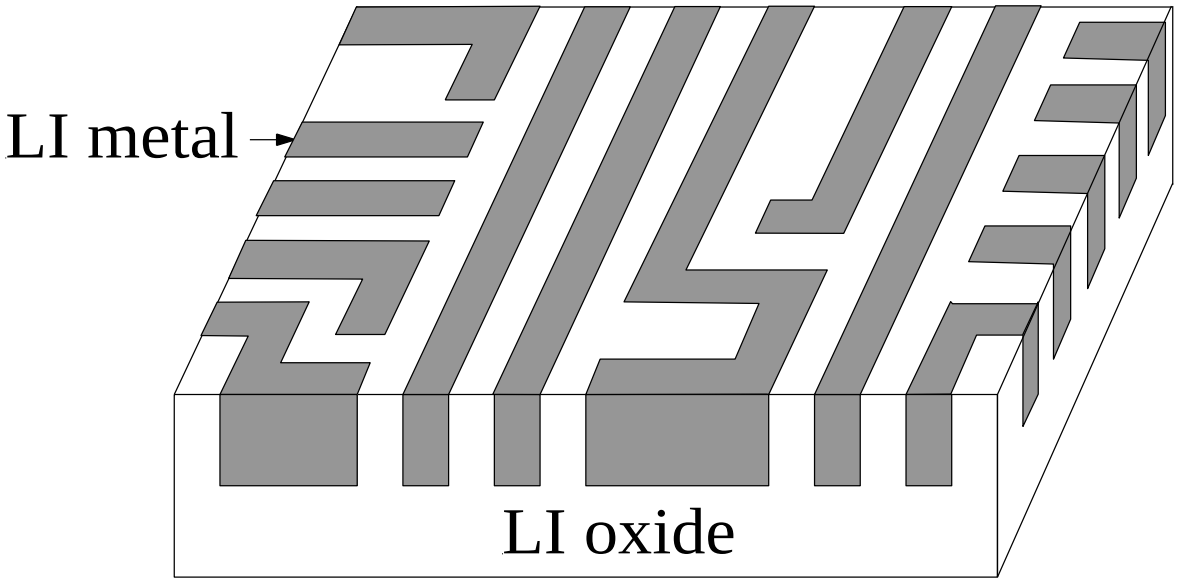


Figure 9.19

LI Oxide as a Dielectric for Inlaid LI Metal (Damascene)

- Damascene: a name doped of year ago from a practice that began thousands ago by artist in Damascus, Syria



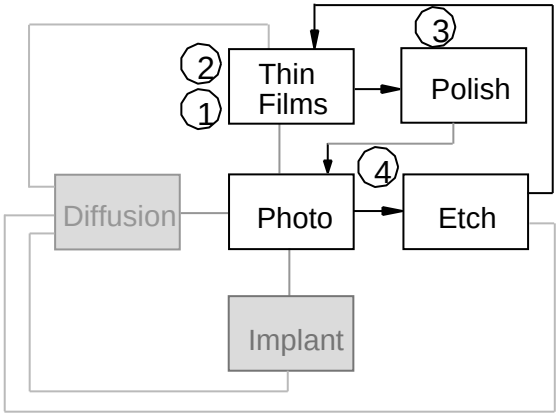
LI: local interconnection

Figure 9.20

景泰藍，學名銅胎掐絲琺瑯，又稱燒青，是金屬胎嵌搪瓷工藝在中國衍生出來的一個獨立品種。世傳此物大行於景泰年間[1]，晚清古董行沿用此說，命名為「景泰琺瑯」或「景泰瑯」。後來又因其所用搪瓷釉料多為月藍色，且「瑯」「藍」音近，訛變為「景泰藍」[wiki]。

LI Oxide Dielectric Formation

- Nitride: protect active region
- Doped oxide
- Oxide polish
- 9th mask



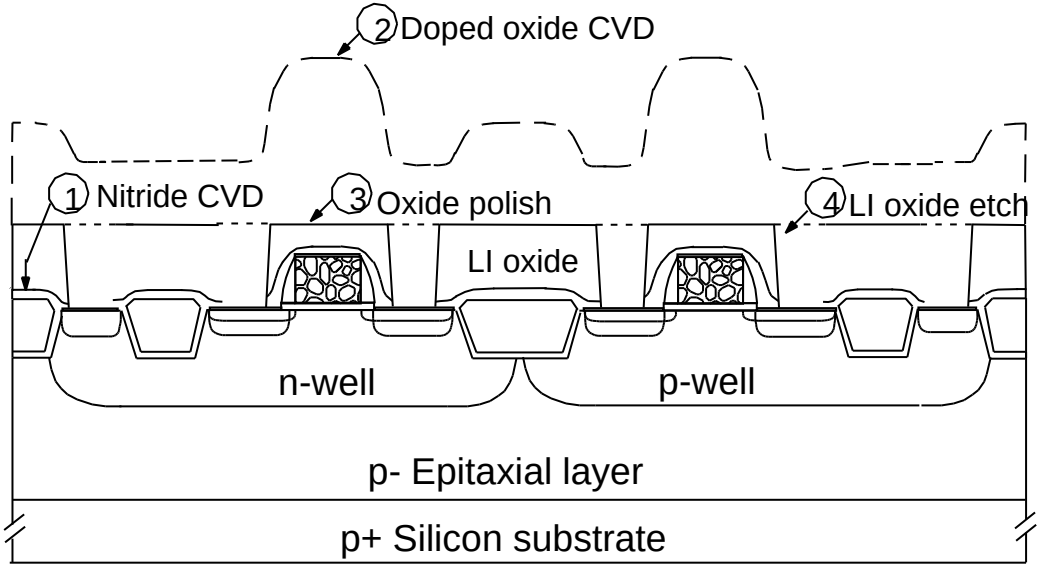
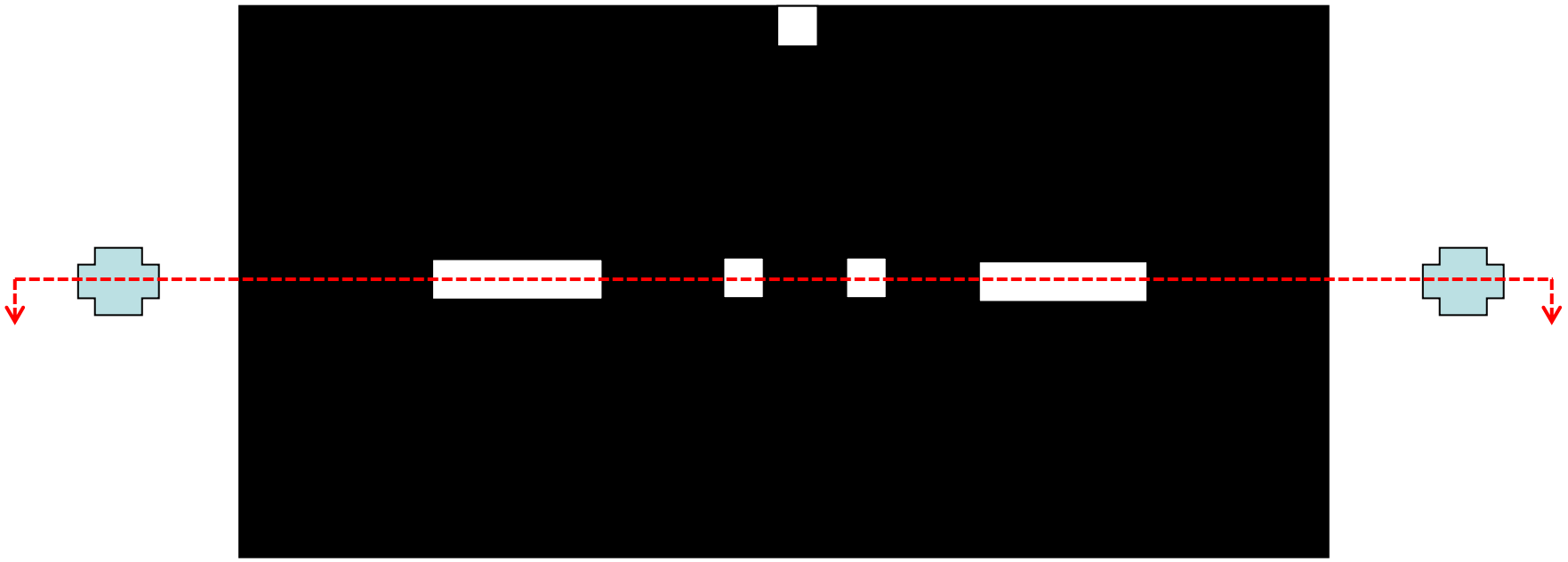


Figure 9.21



Mask # 9: Local Interconnection formation

LI Metal Formation

- Ti/TiN is used: Ti for adhesion and TiN for diffusion barrier
- Tungsten (W) is preferred over Aluminum (Al) for LI metal due to its ability to fill holes without leaving voids

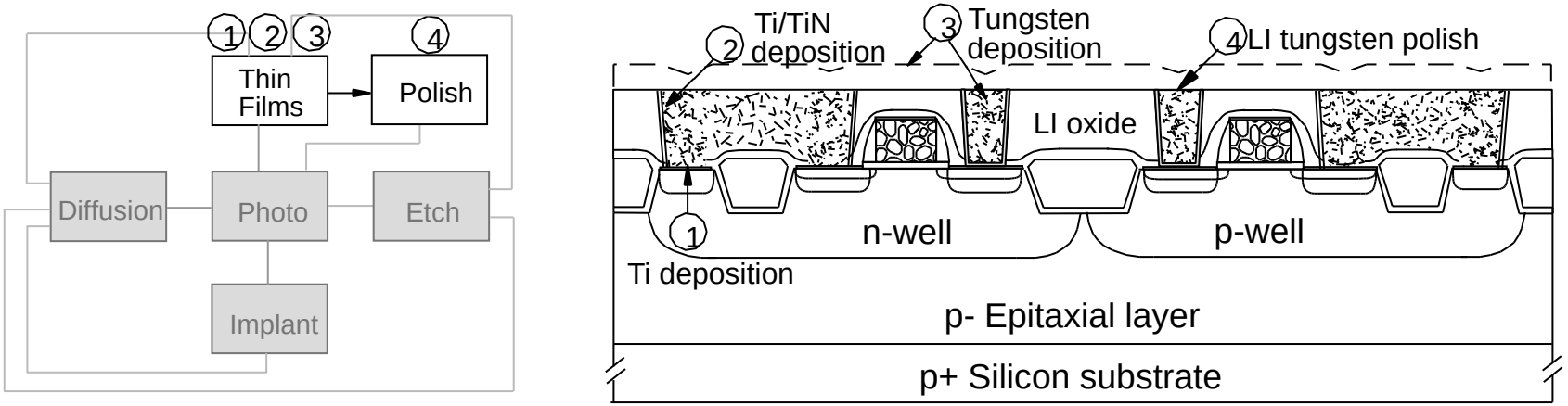


Figure 9.22

Via-1 Formation

- Interlayer dielectric (ILD): insulator between metal (800nm)
- Via: electrical pathway from one metal layer to adjacent metal layer
- 10th mask

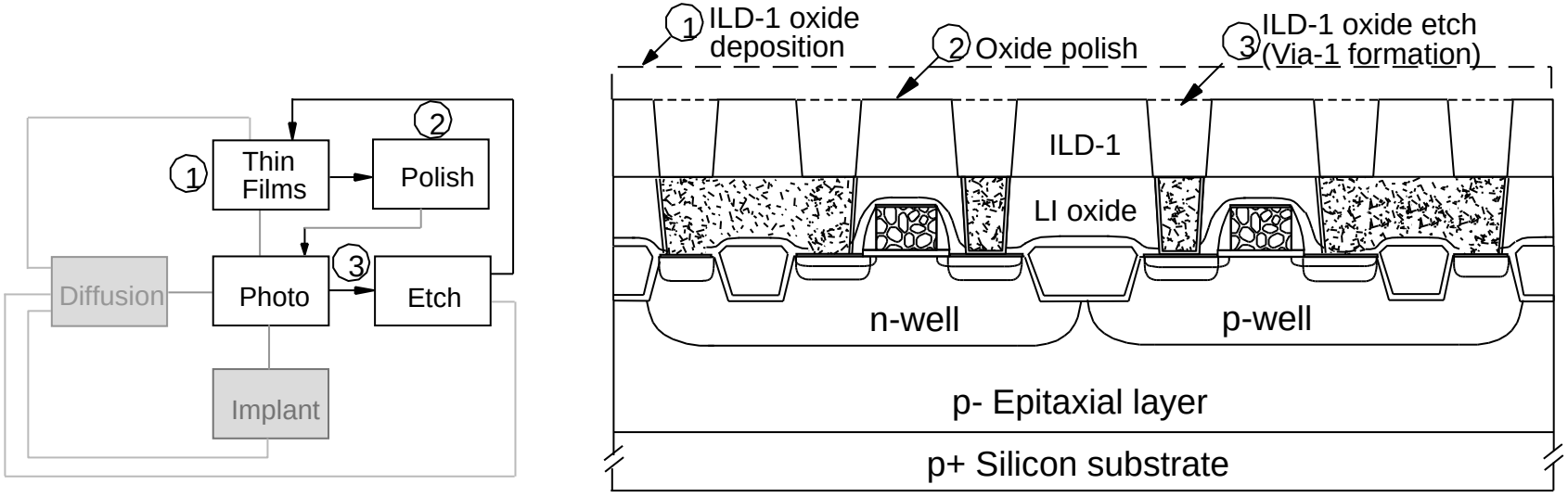
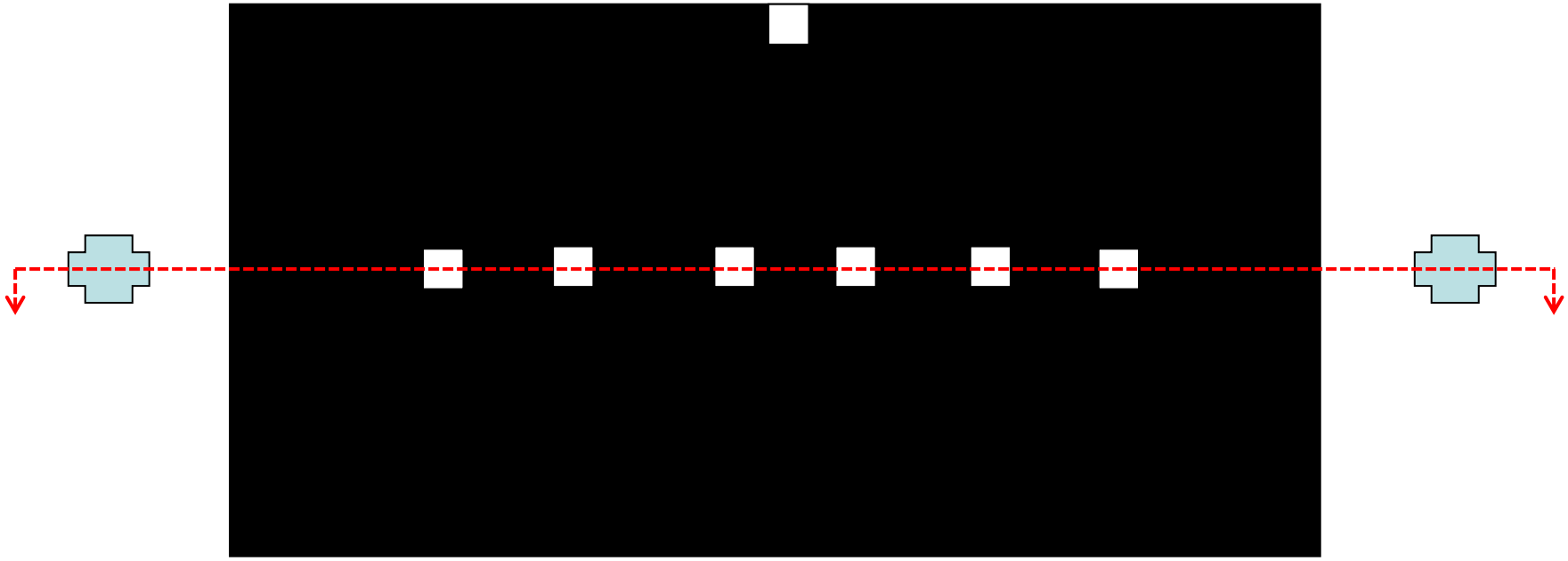


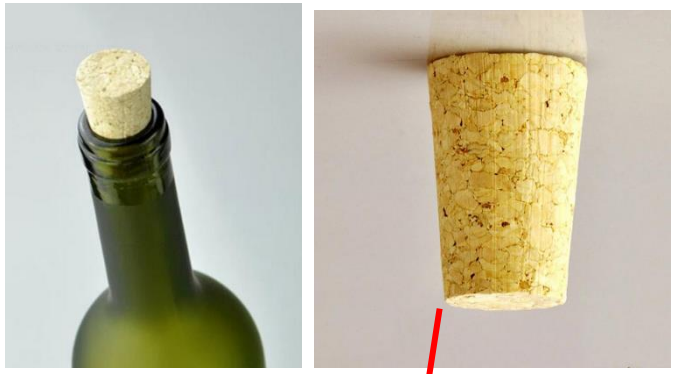
Figure 9.23

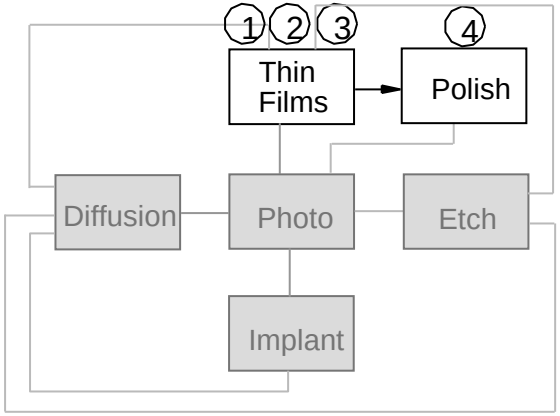


Mask # 10: Via-1 formation

Plug-1 Formation

- Ti layer as a glue layer to hold W
- TiN layer as the diffusion barrier
- Tungsten (W) as the via
- CMP W-polish





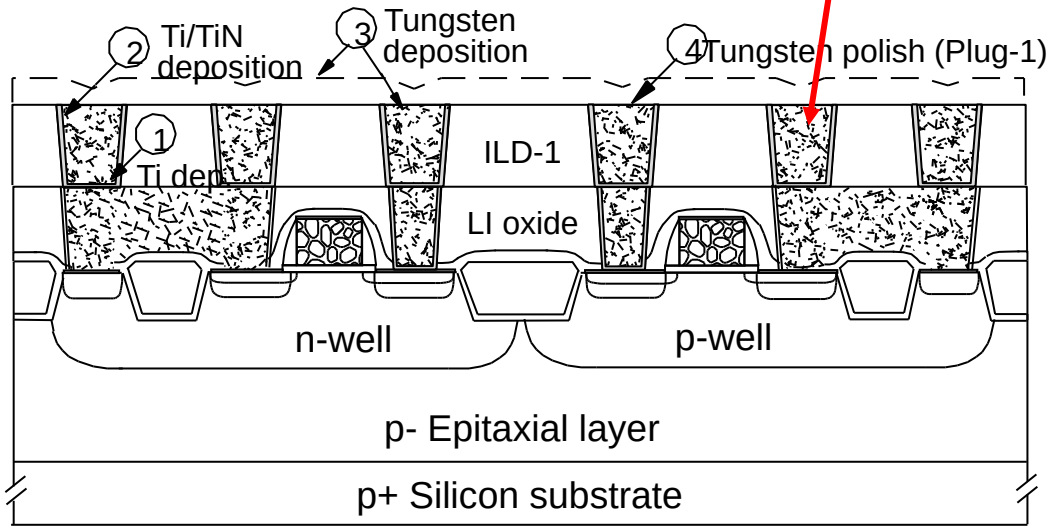
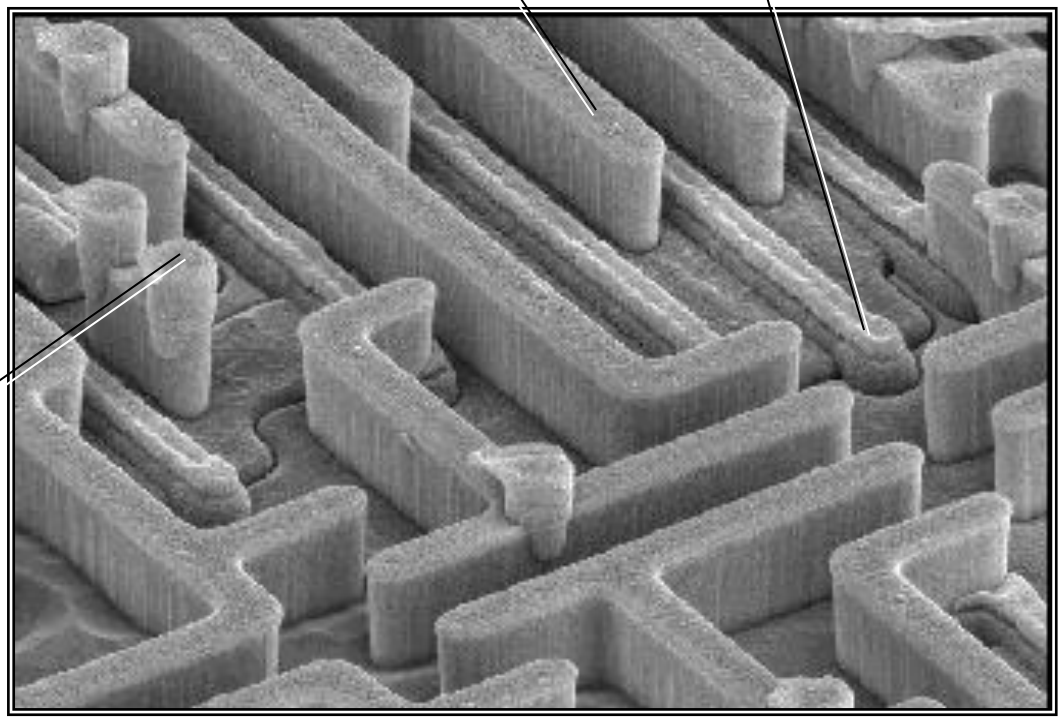


Figure 9.24

SEM Micrographs of Polysilicon, Tungsten LI and Tungsten Plugs



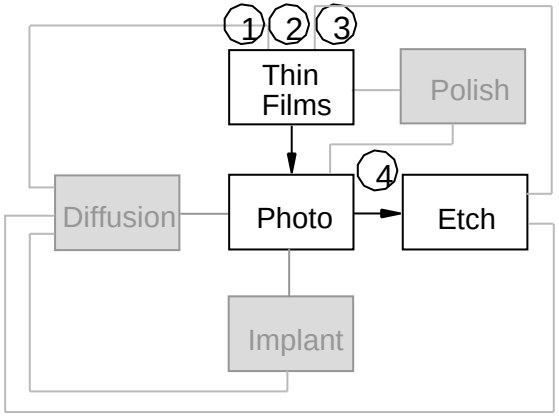
Mag. 17,000 X

Micrograph courtesy of Integrated Circuit Engineering

Photo 9.4

Metal-1 Interconnect Formation

- Metal stack: Ti/Al (or Cu)/TiN is used
- Al(99%) + Cu (1%) is used to improve reliability
- 11th mask



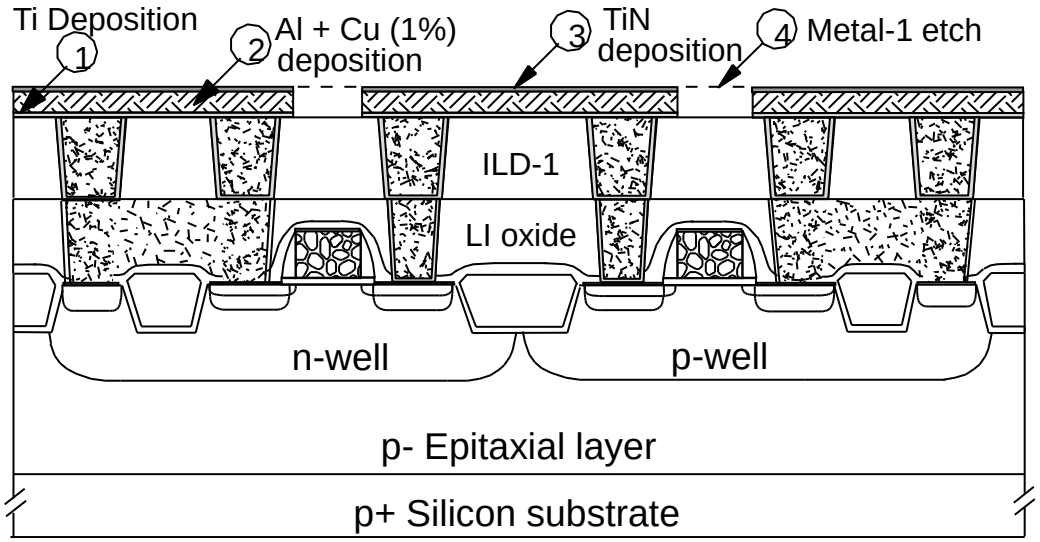
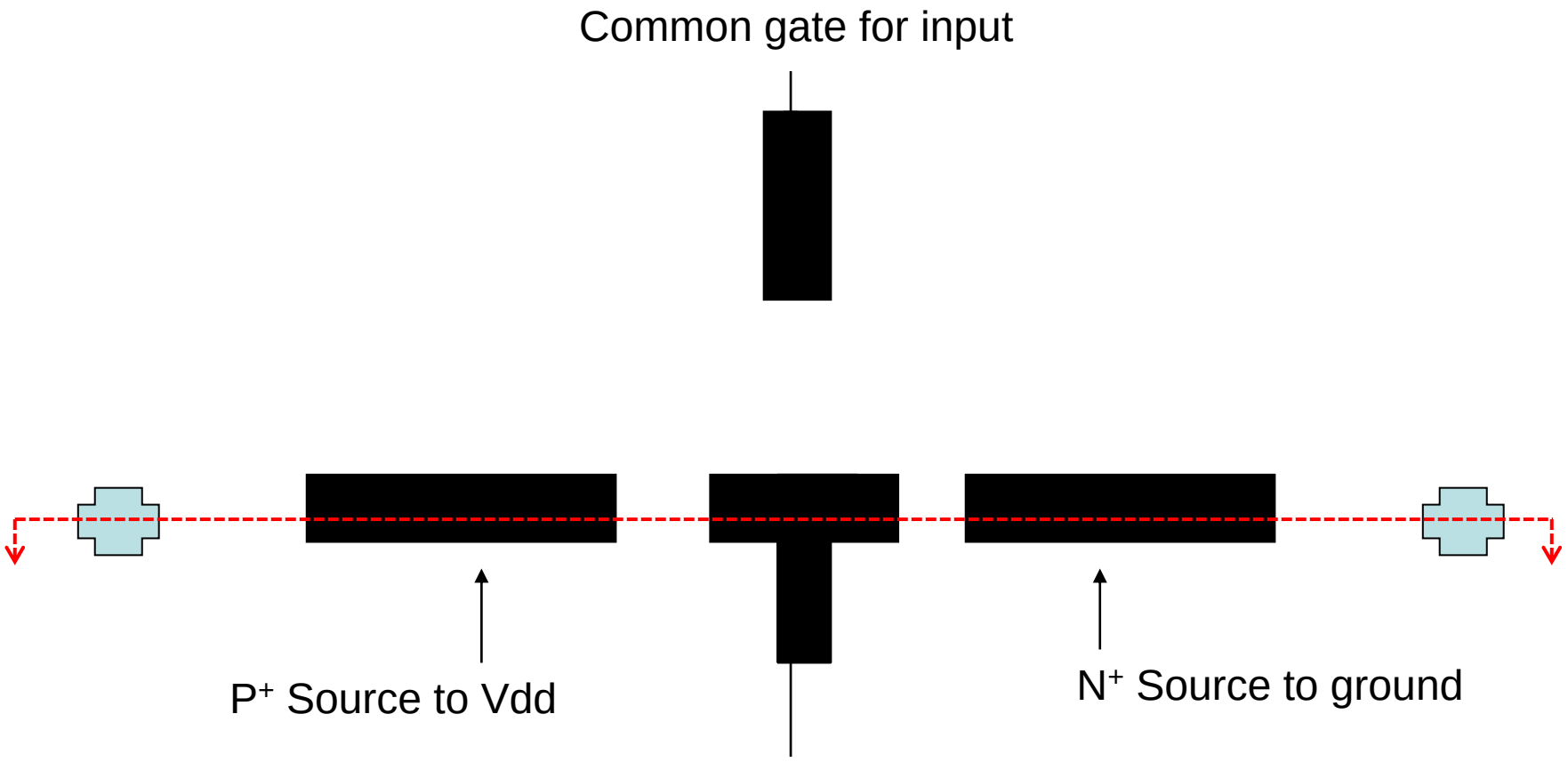
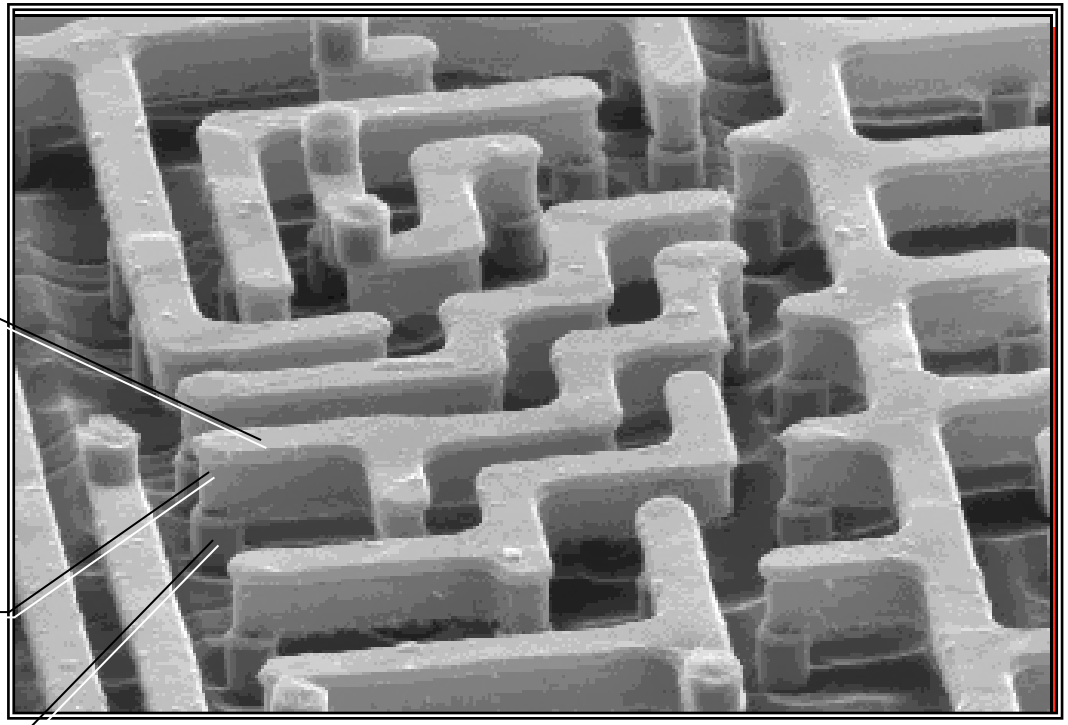


Figure 9.25



Mask # 11: Metal-1 formation

SEM Micrographs of First Metal Layer over First Set of Tungsten Vias



Micrograph courtesy of Integrated Circuit Engineering

Via-2 Formation

- Gap fill: fill the gap between metal
- Oxide deposition
- Oxide polish
- 12th mask

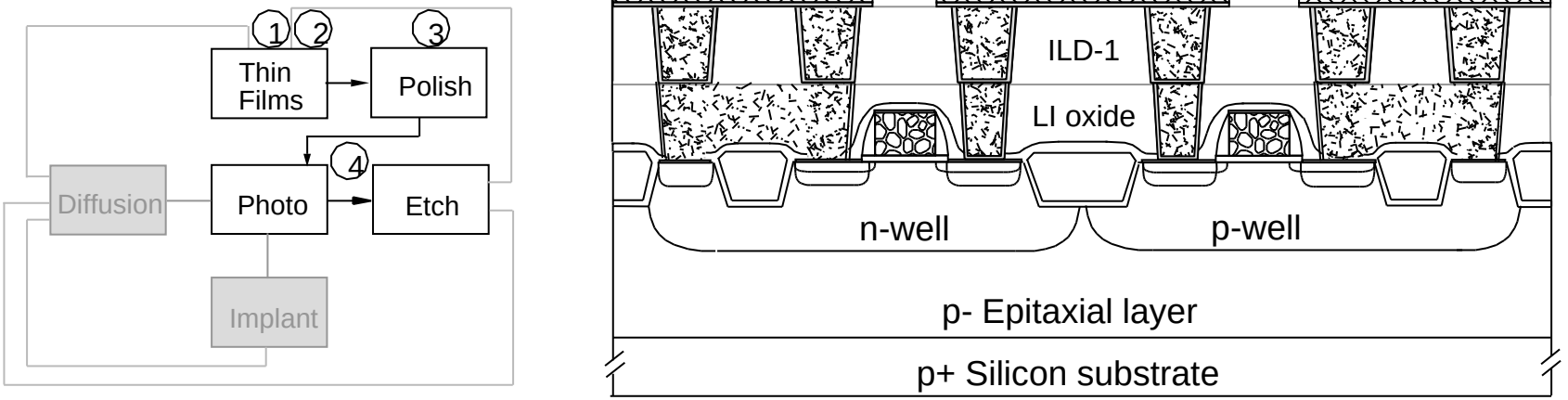
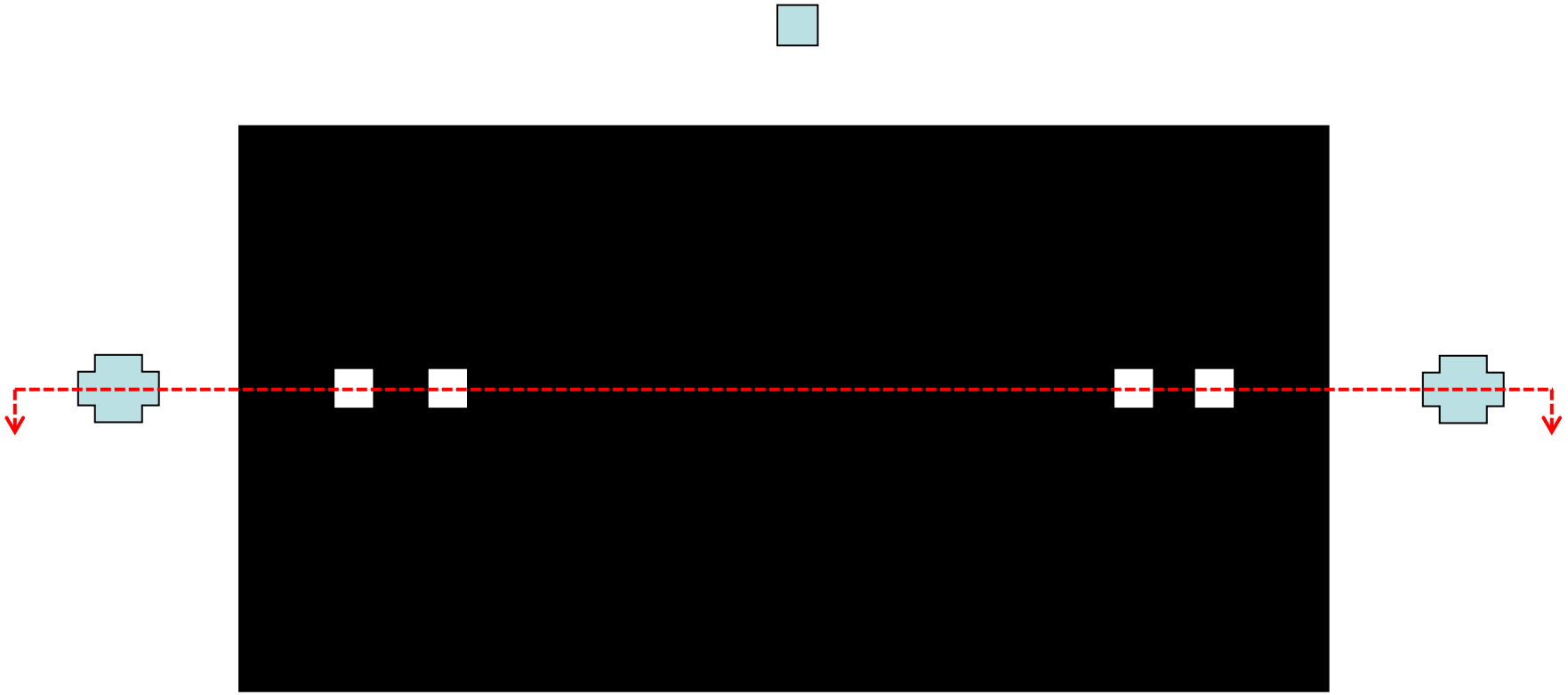


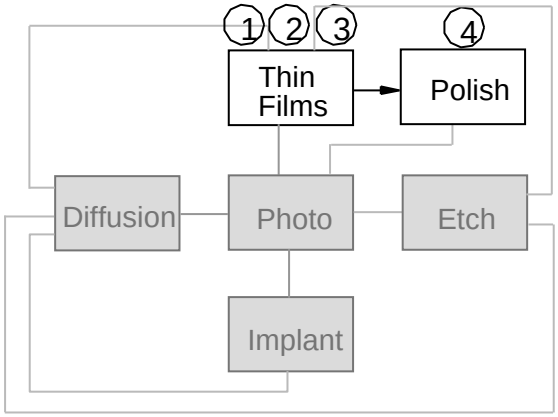
Figure 9.26



Mask # 12: Via-2 formation

Plug-2 Formation

- Ti/TiN/W
- CMP W polish



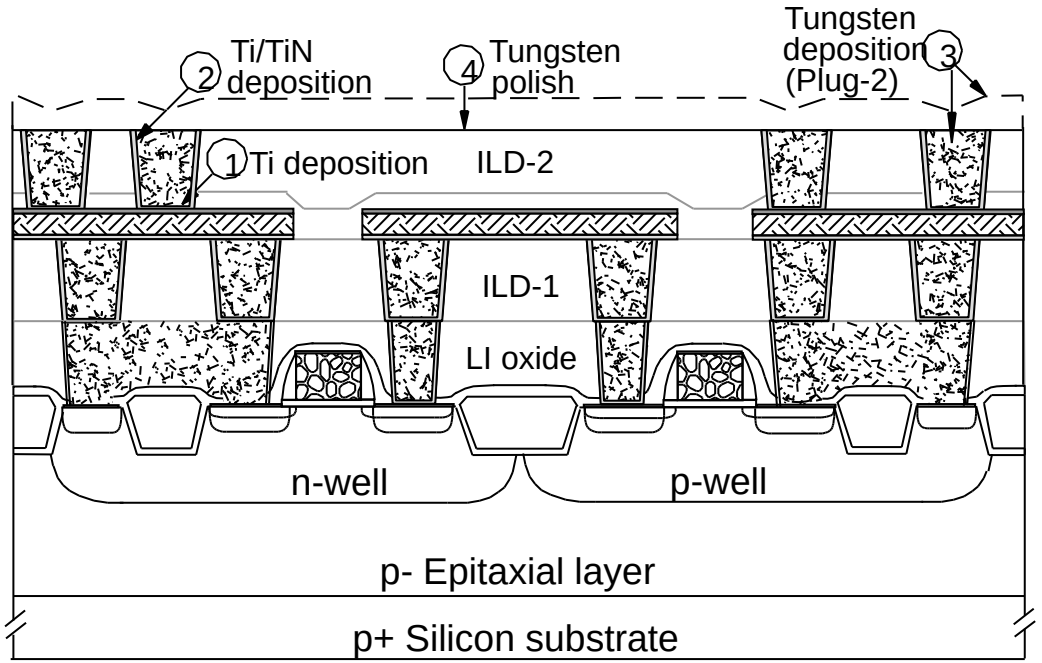


Figure 9.27

Metal-2 Interconnect Formation

- Metal 2: Ti/Al/TiN
- ILD-3 gap filling
- ILD-3
- ILD-polish
- Via-3 etch and via deposition, Ti/TiN/W

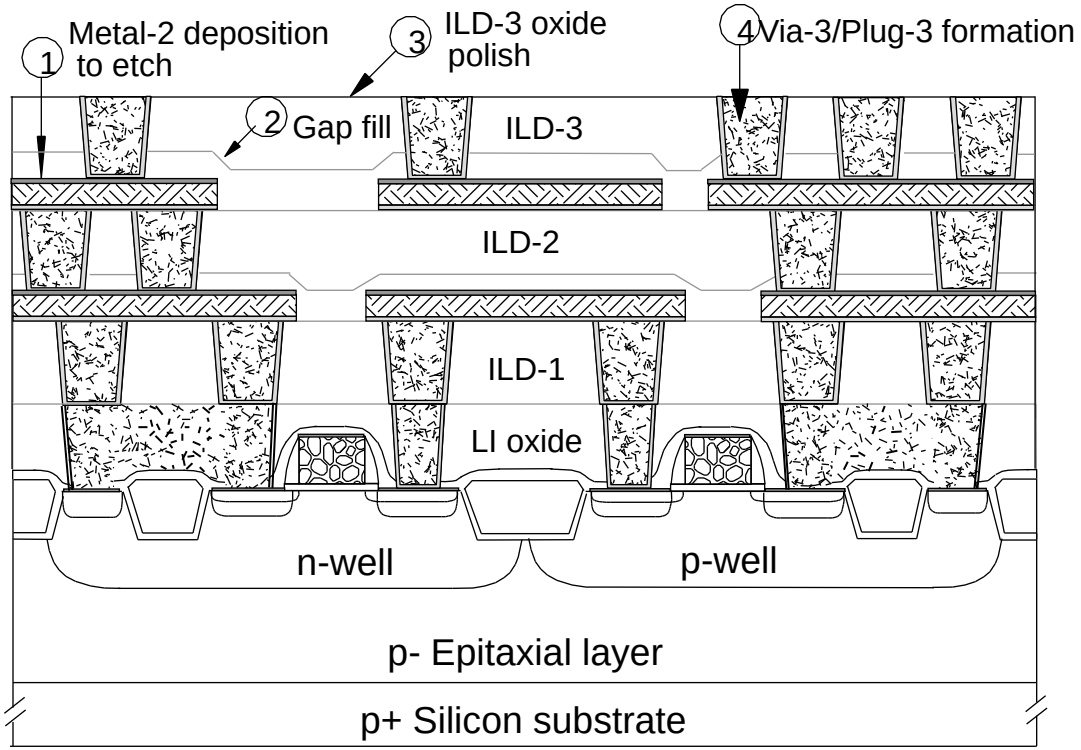
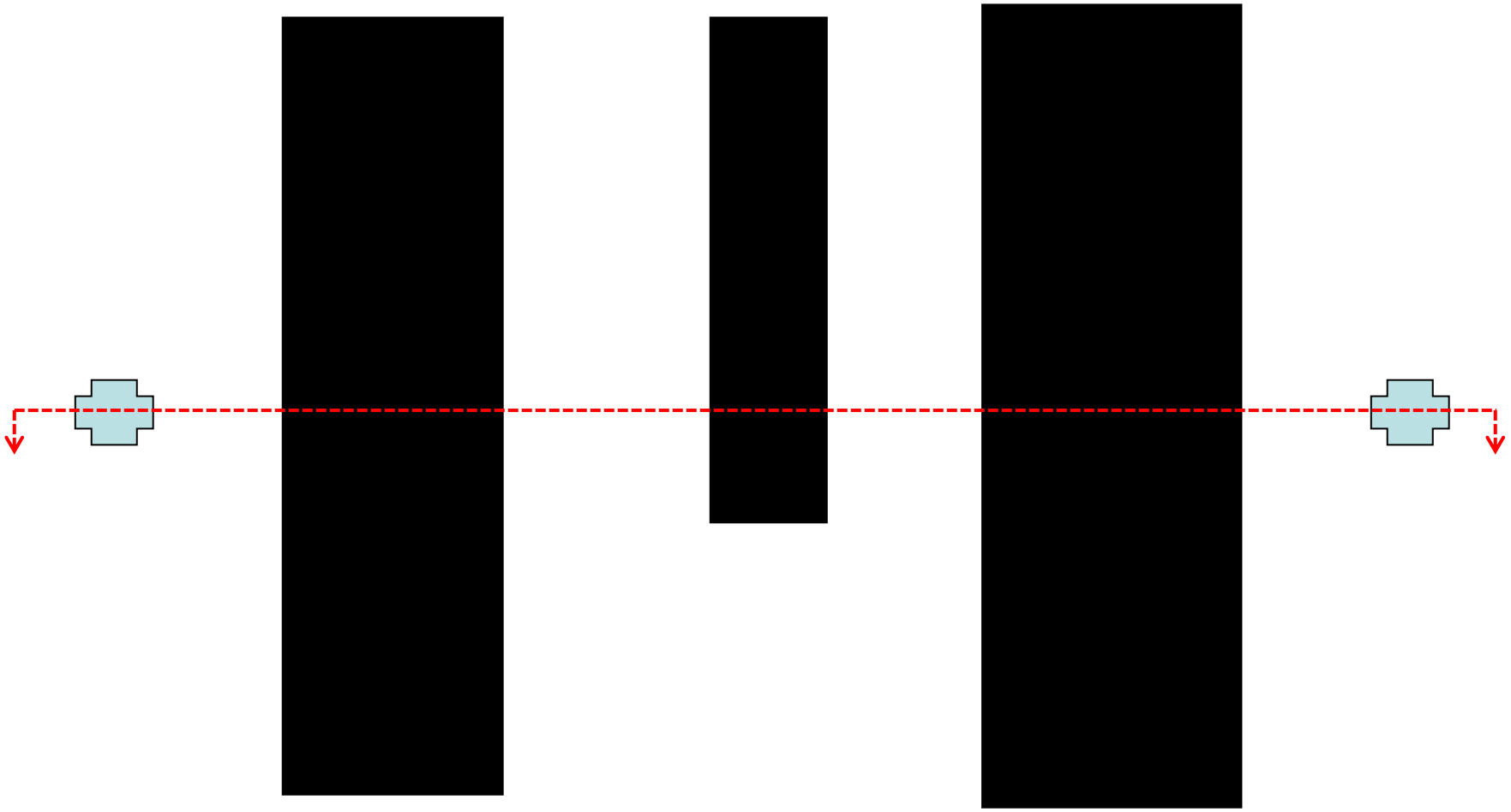
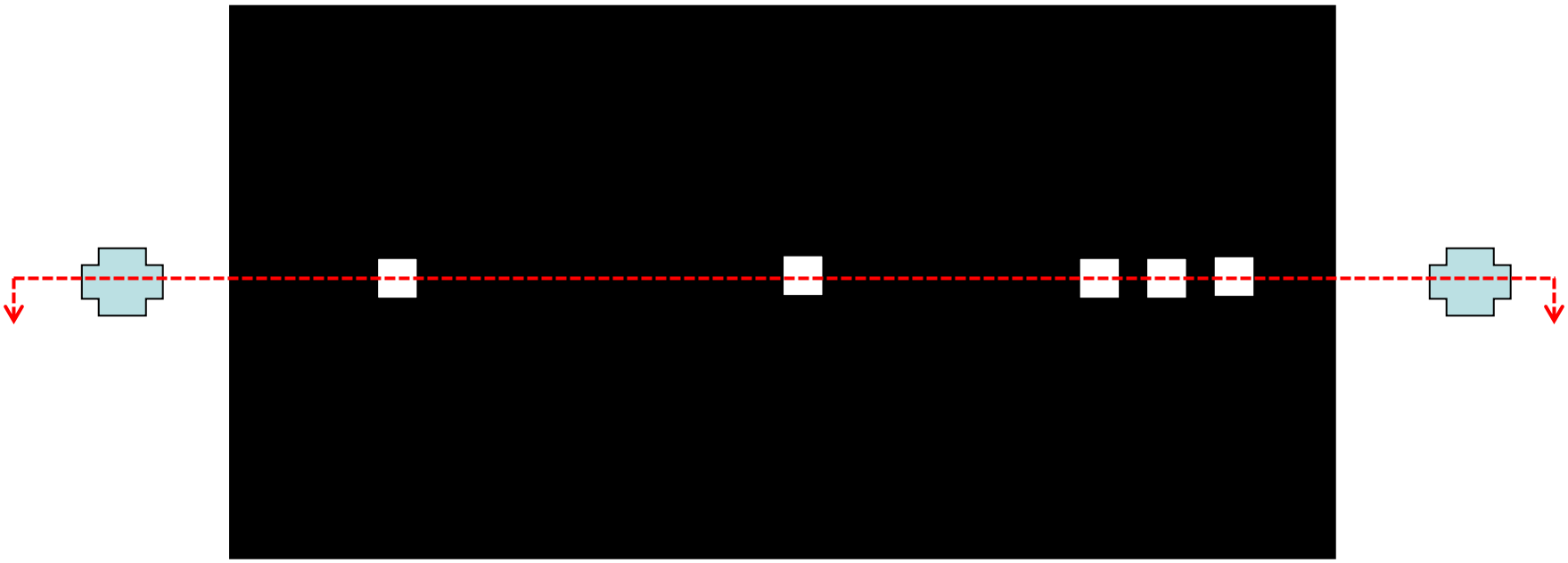


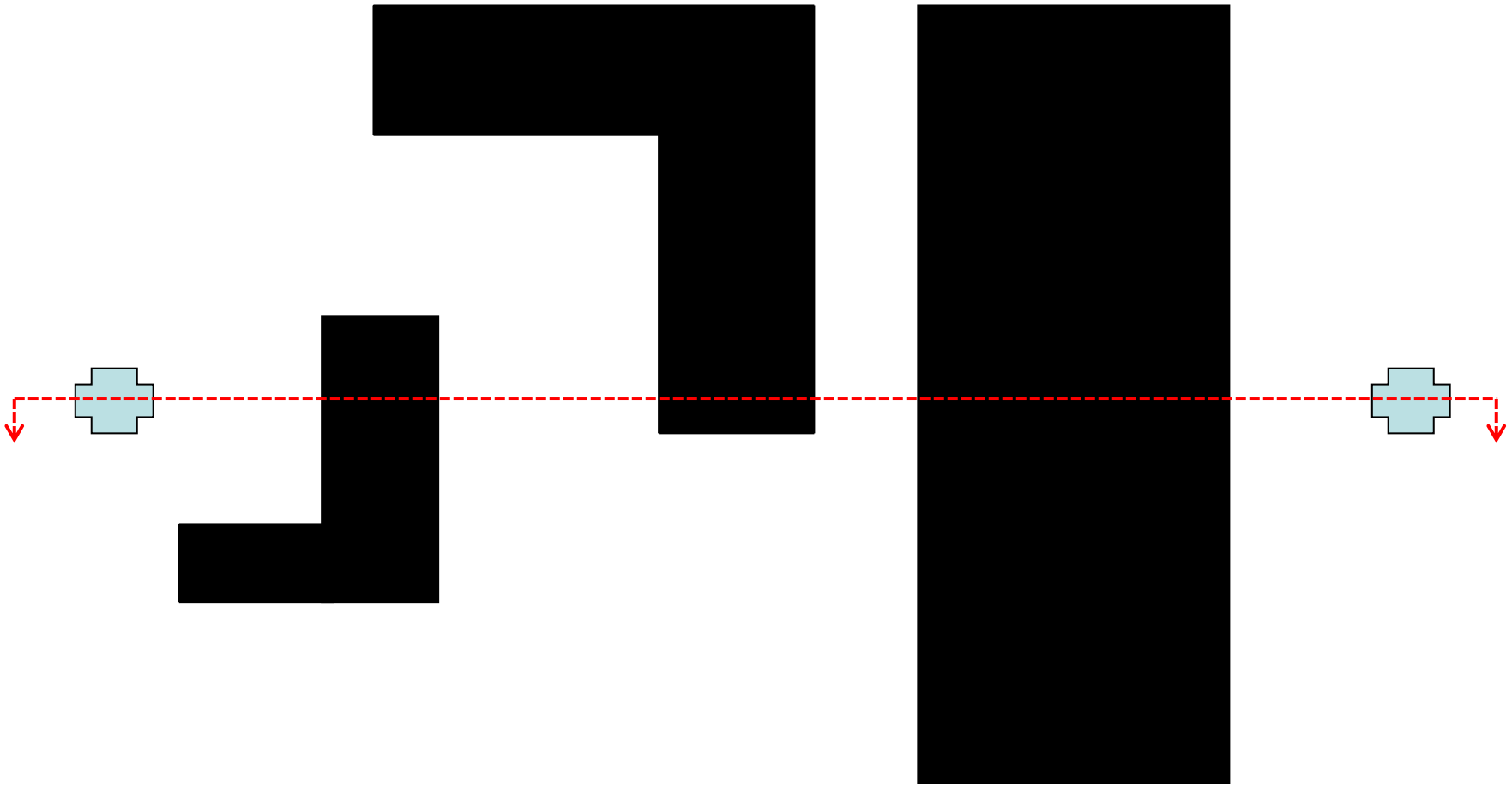
Figure 9.28



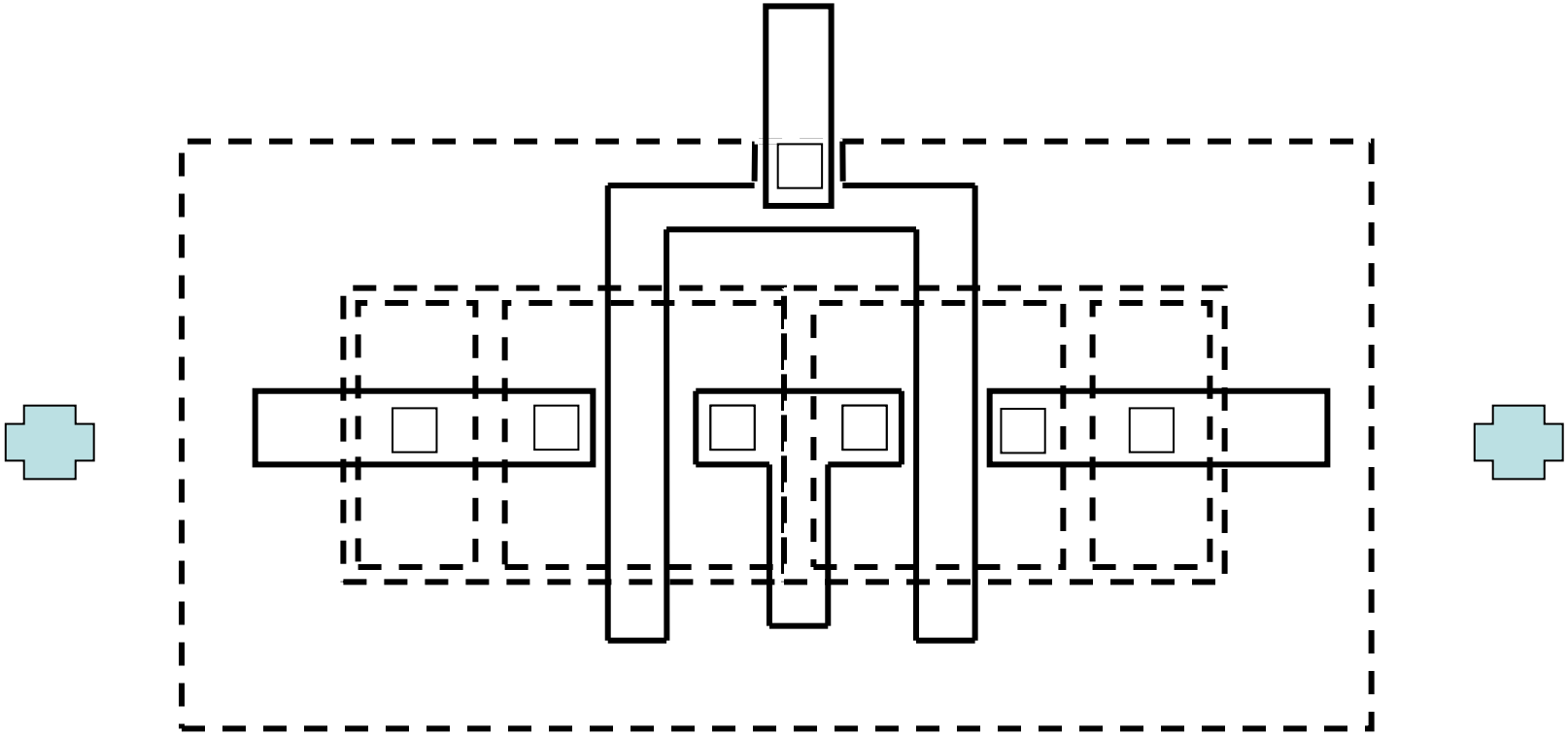
Mask # 13: Metal-2 formation



Mask # 14: Via-3 formation



Mask # 15: Metal-3 formation



CMOS layout (mask 1 to mask 12)

Full 0.18 μm CMOS Cross Section

- Passivation layer of **nitride** is used to protect from moisture, scratched, and contamination
- ILD-6 : **oxide**

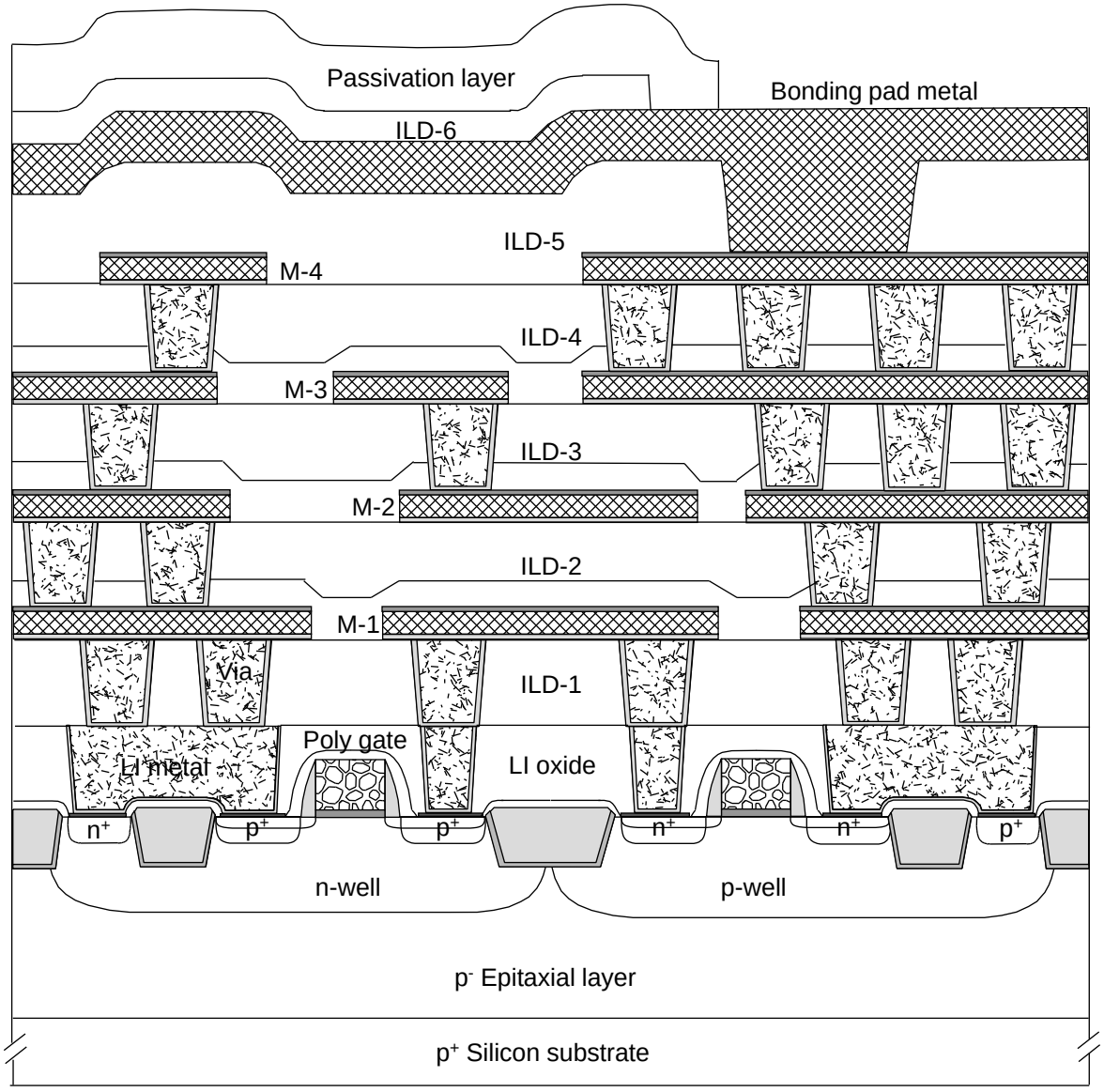
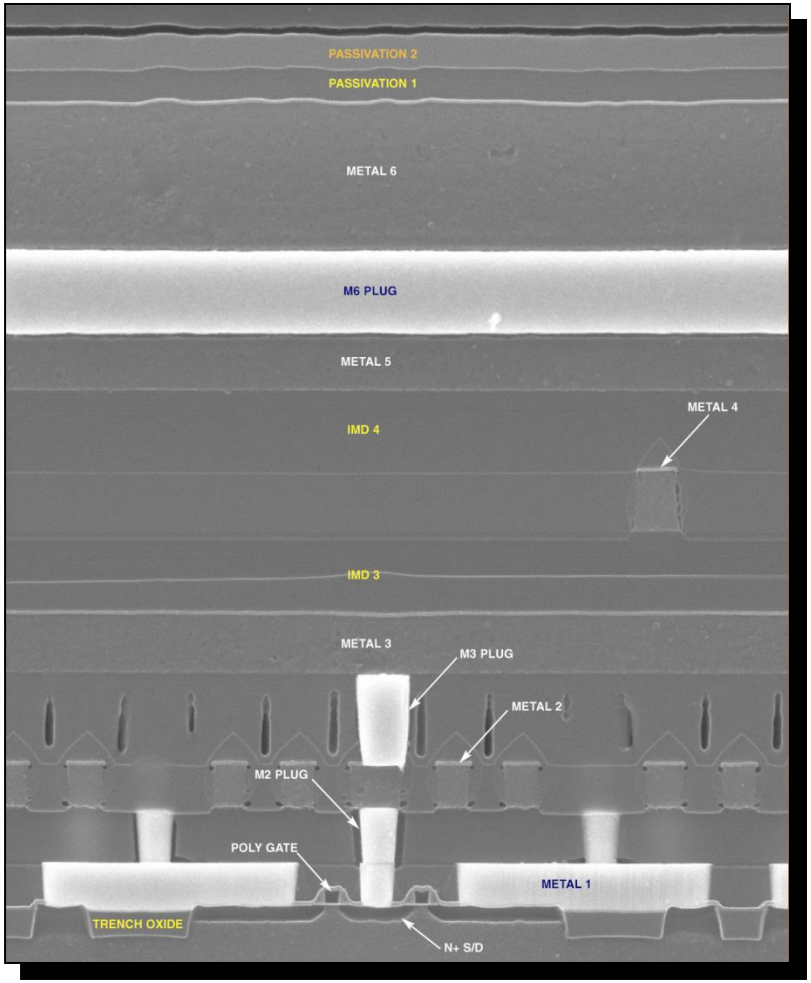


Figure 9.29

SEM Micrograph of Cross-section of AMD Microprocessor

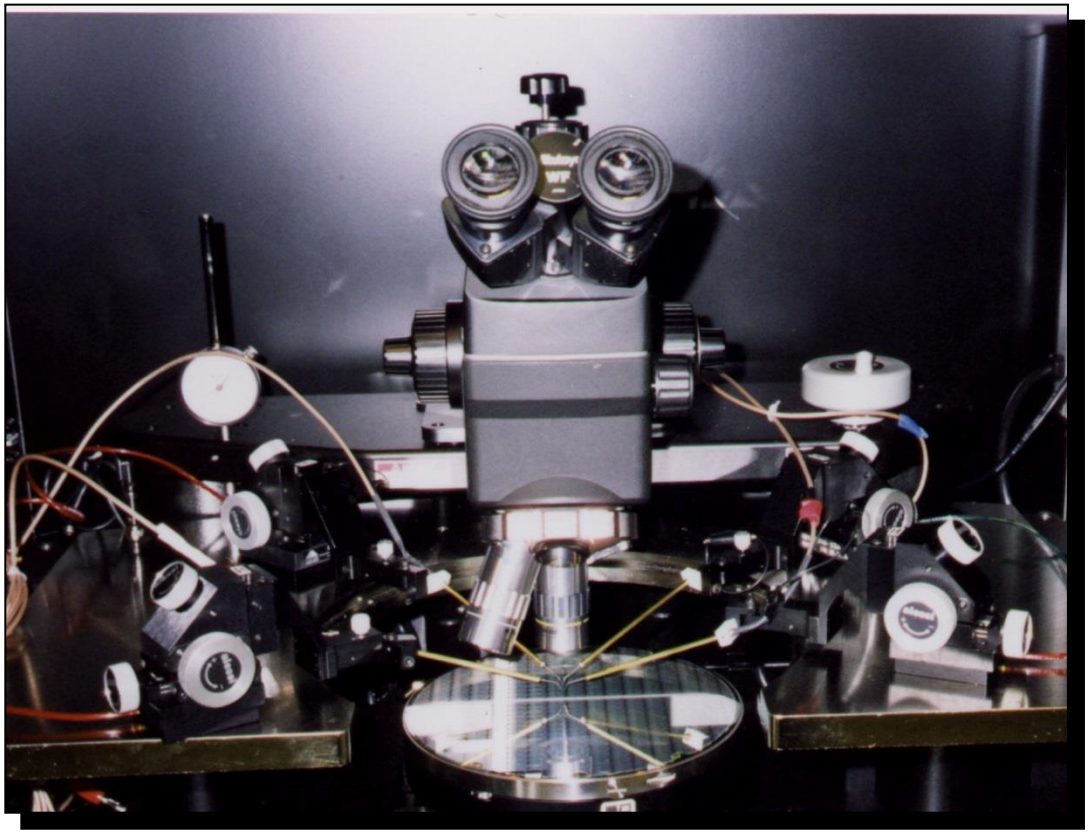


Mag. 18,250 X

Micrograph courtesy of Integrated Circuit Engineering

Photo 9.6

Wafer Electrical Test using a Micromanipulator Prober (Parametric Testing)



- After metal-1 etch, wafer is tested, and after passivation test again
- Automatically test on wafer, sort good die (X-Y position, previous marked with an red ink)
- Before package, wafer is backgrind to a thinner thickness for easier slice and heat dissipation

Photo courtesy of Advanced Micro Devices

Photo 9.7