Semiconductor Manufacturing Technology

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Chapter 10

Oxidation

Objectives

After studying the material in this chapter, you will be able to:

1. Describe an oxide film for semiconductor manufacturing, including its atomic structure, how it is used and its benefits.
2. State the chemical reaction for oxidation and describe how oxide grows on silicon.
3. Explain selective oxidation and give two examples.
4. State the three types of thermal processing equipment, describe the five parts of a vertical furnace, and give the attributes of a fast ramp vertical furnace.
5. Explain what is a rapid thermal processor, its usage and design.
6. Describe the critical aspects of the oxidation process, its quality measures and some common troubleshooting problems.

Diffusion Area of Wafer Fabrication

- **Grown** oxide: $Si + O_2 \rightarrow SiO_2$
- **Deposited** oxide: $SiH_4 + O_2 \rightarrow SiO_2 + 2H_2$
- The most **important** role for silicon technology
- **Thermal budget**: temp.x time must be reduced

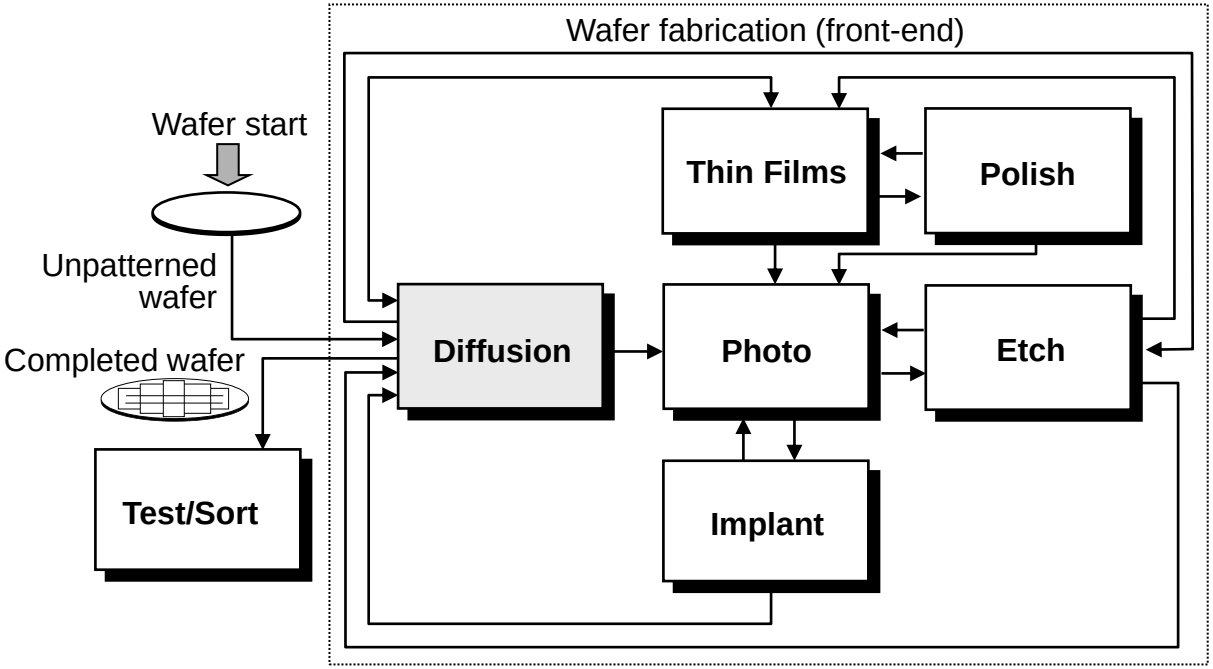
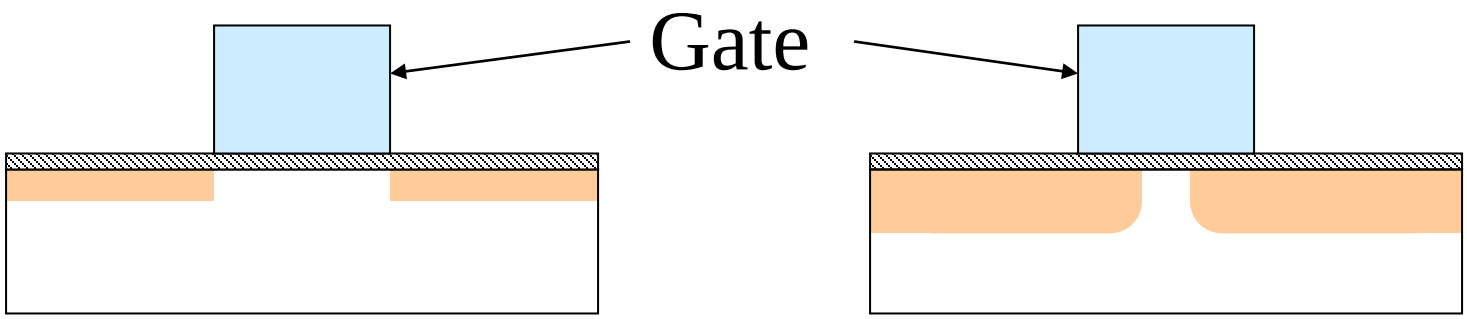


Figure 10.1

Illustration of Thermal Budget



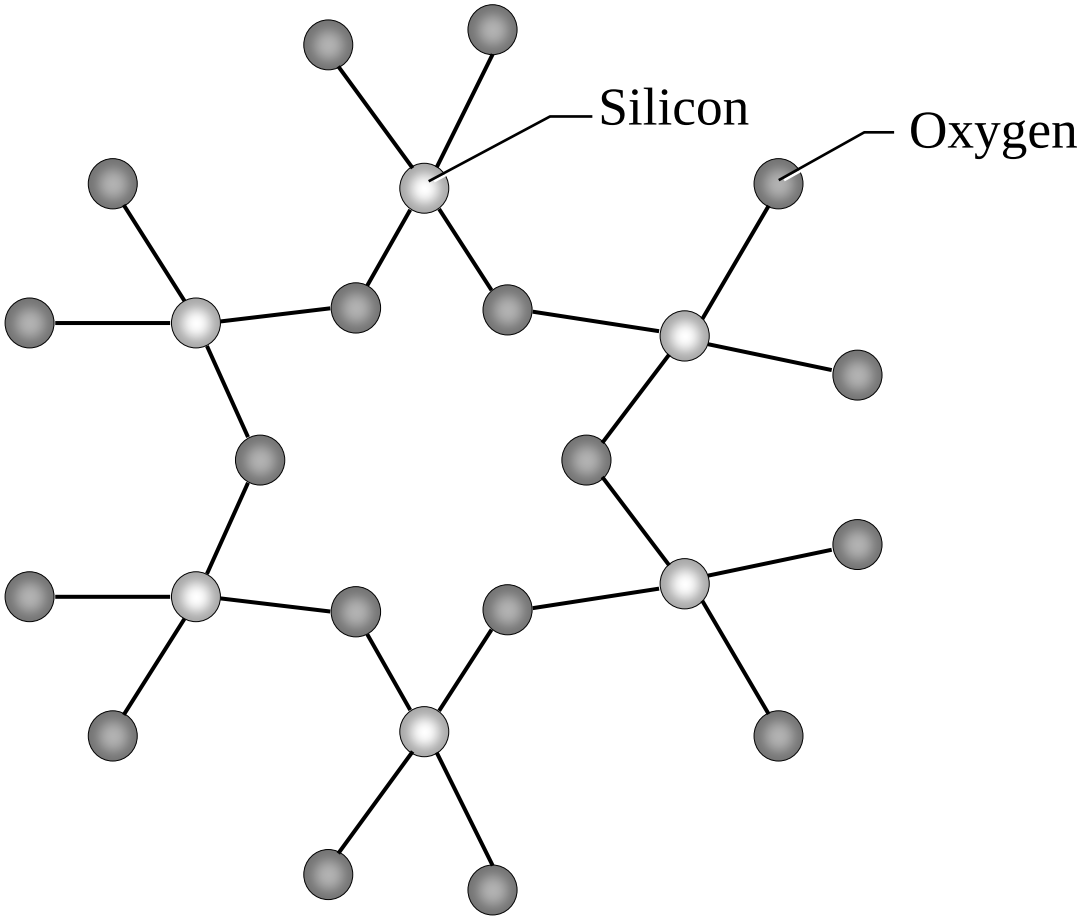
As S/D Implantation

Over Thermal Budget

Oxide Film

- Nature of Oxide Film
- Uses of Oxide Film (glass)
  - Device Protection and Isolation
  - Surface Passivation
  - Gate Oxide Dielectric
  - Dopant Barrier
  - Dielectric Between Metal Layers

Atomic Structure of Silicon Dioxide



- It is amorphous
- It is **tetrahedron** cell
- Strong adhesion to silicon and **good** electrical properties
- **Native** oxide grows at room temperature, non-uniform

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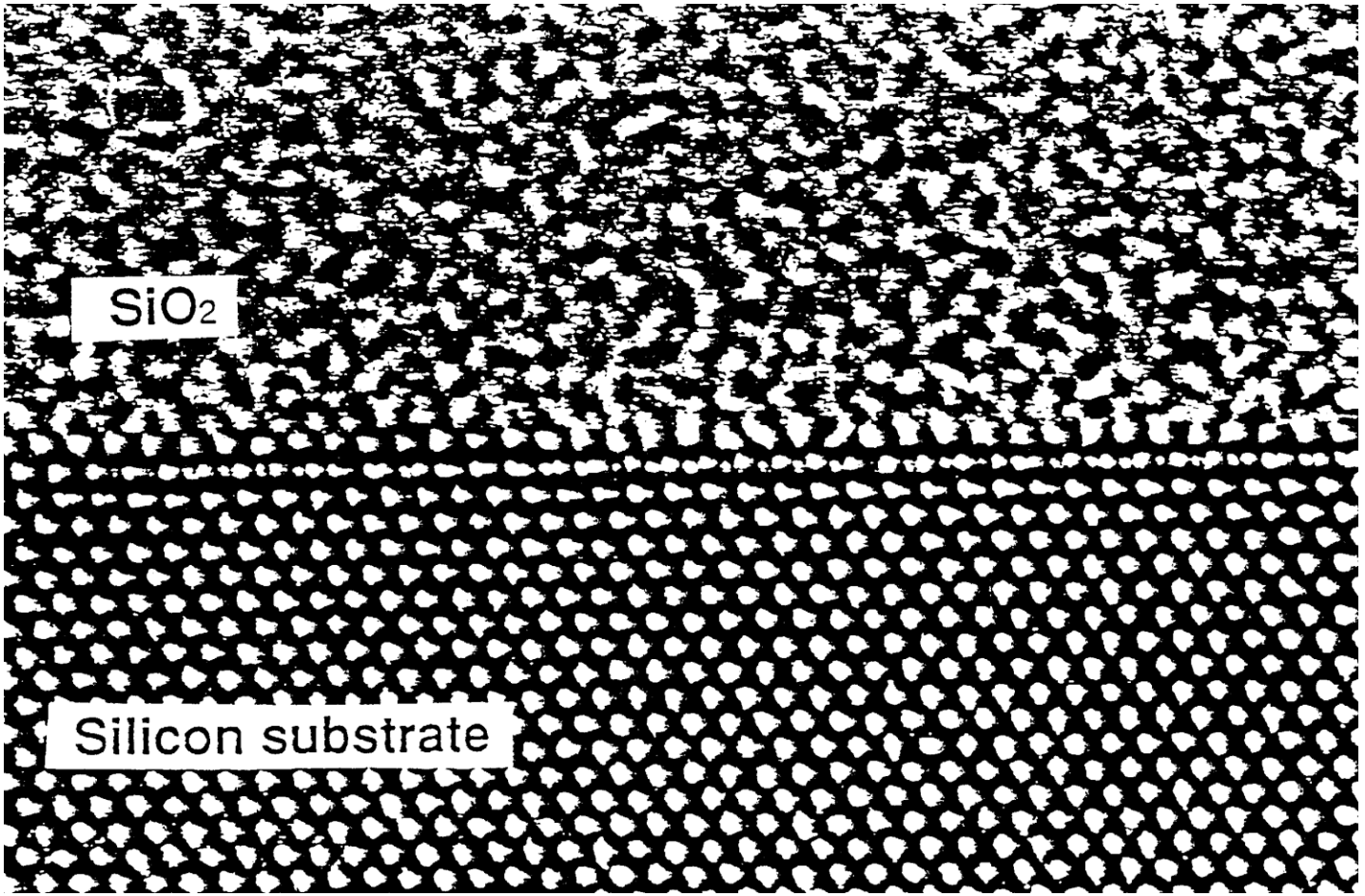
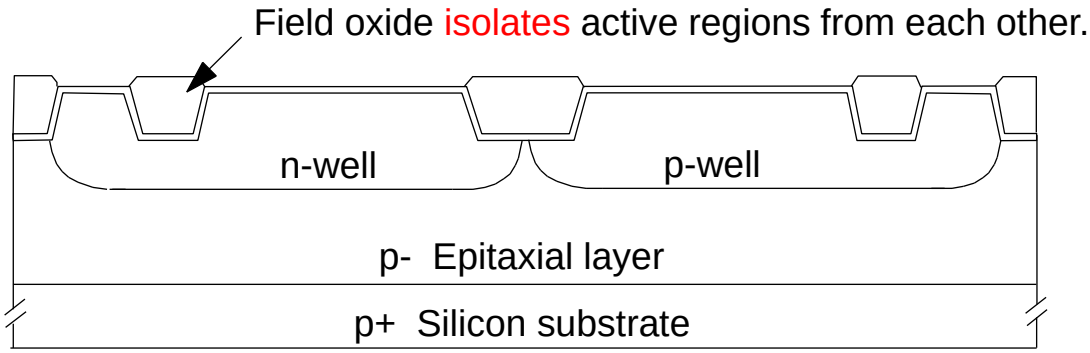
Figure 10.2

HRTEM of SiO_2/Silicon Interface



S. L. Wu

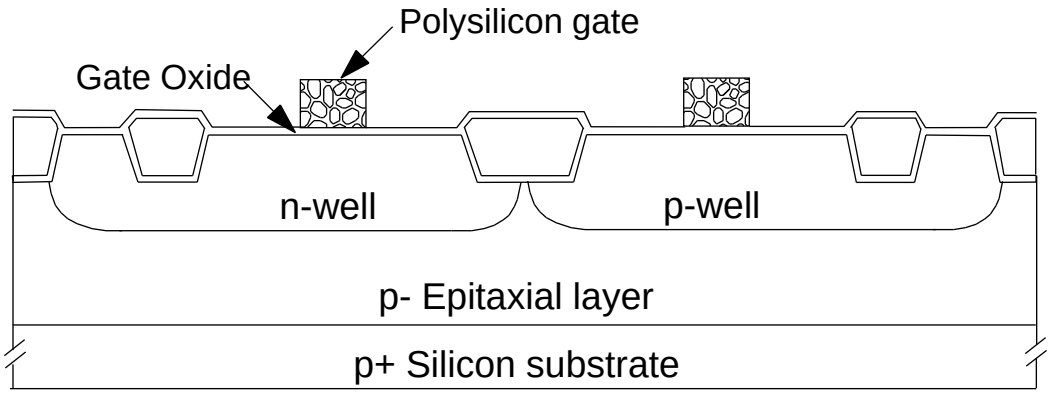
Applications: Field Oxide Layer



- SiO_2 (glass) physically protects devices because it is a very hard and nonporous material that effectively insulates active devices.
- Major benefit from thermal oxide is the reduction of surface state density (surface passivation)
- This passivation is important for controlling the leakage of the ***pn junction*** and a stable gate oxide.
- Field oxide makes IC possible
- SiO_2 has a coefficient of thermal expansion very similar to that of Silicon.

Figure 10.3

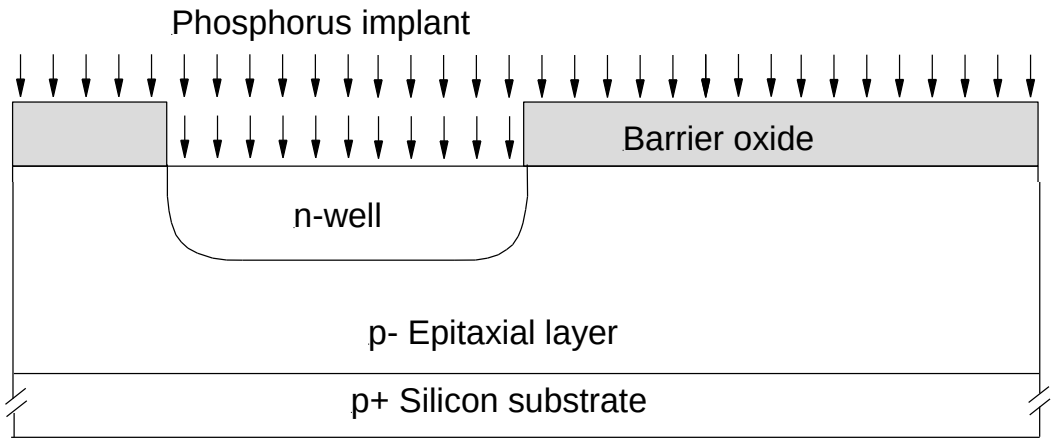
Gate Oxide Dielectric



- Oxide has dielectric strength of 10^7 V/cm and 10^{17} ohms-cm
- For 0.18 μm, Tox ~ 20 ± 1.5 Å
- Contaminations must be controlled for good gate oxide integrity (GOI)

Figure 10.4

Oxide Layer Dopant Barrier

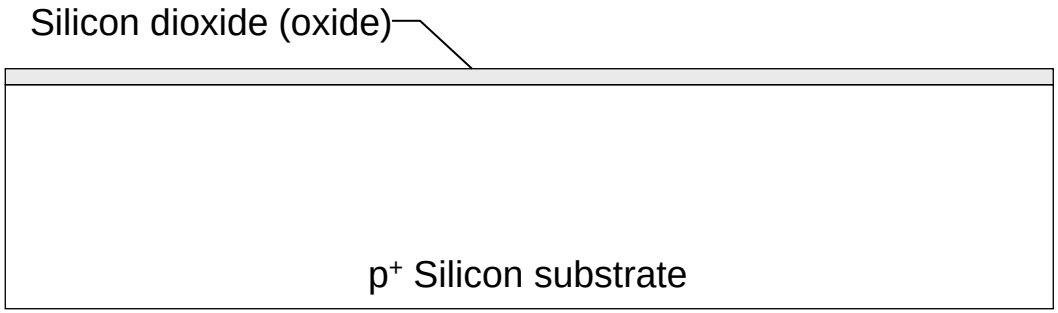


- To obtain a selective impurity doping
- Tox ~ 15 nm is grown to reduce damage of I/I, depth control, and reduce channel effect (Ch 9, 17) [p.17]

Figure 10.5

Table 10.1
Oxide Applications: Native Oxide

Purpose: This oxide is a contaminant and generally undesirable. Sometimes used in memory storage or film passivation.

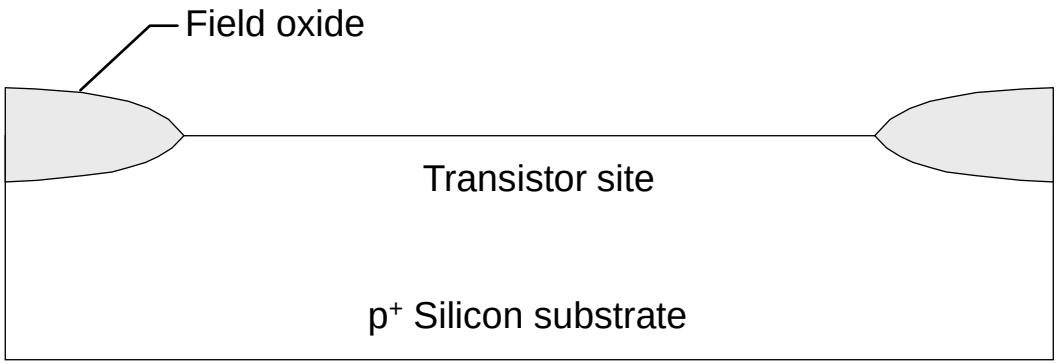


Comments: Growth rate at room temperature is 15 per hour up to about 40 Å.

Table 10.1A

Table 10.1
Oxide Applications: Field Oxide

Purpose: Serves as an isolation barrier between individual transistors to isolate them from each other.

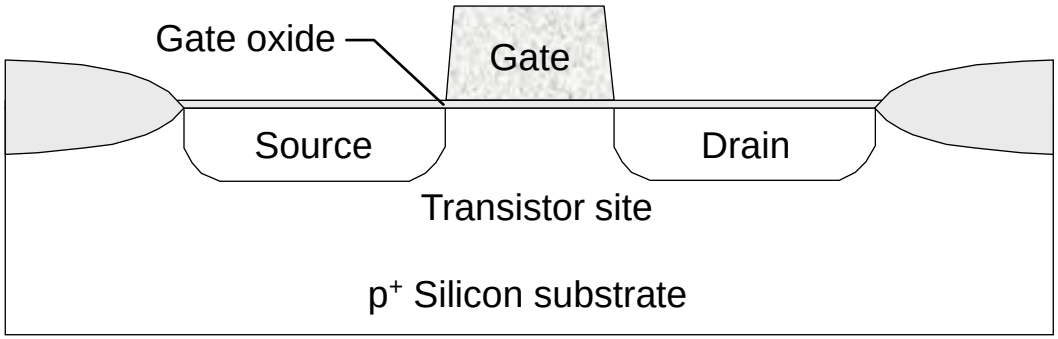


Comments: Common field oxide thickness range from 2,500 Å to 15,000 Å. Wet oxidation is the preferred method.

Table 10.1B

Table 10.1
Oxide Applications: Gate Oxide

Purpose: Serves as a dielectric between the gate and source-drain parts of MOS transistor.

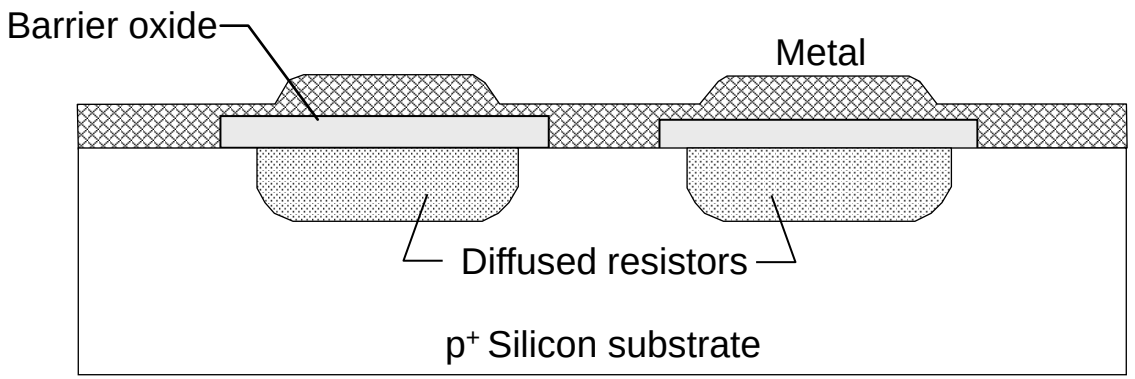


Comments: Growth rate at room temperature is 15 Å per hour up to about 40 Å. Common gate oxide film thickness range from about 30 Å to 500 Å. Dry oxidation is the preferred method.

Table 10.1C

Table 10.1
Oxide Applications: Barrier Oxide

Purpose: Protect active devices and silicon from follow-on processing.

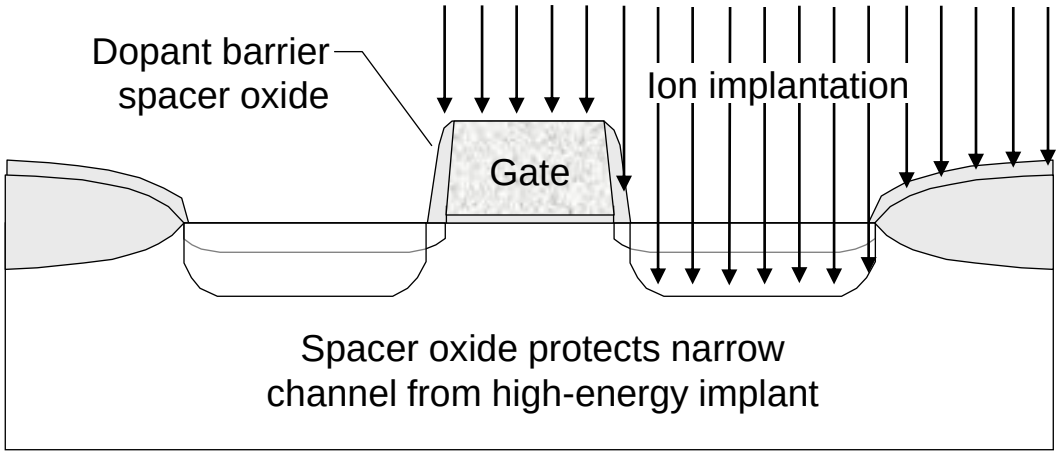


Comments: Thermally grown to several hundred Angstroms thickness.

Table 10.1D

Table 10.1
Oxide Applications: Dopant Barrier

Purpose: Masking material when implanting dopant into wafer. Example: Spacer oxide used during the implant of dopant into the source and drain regions.

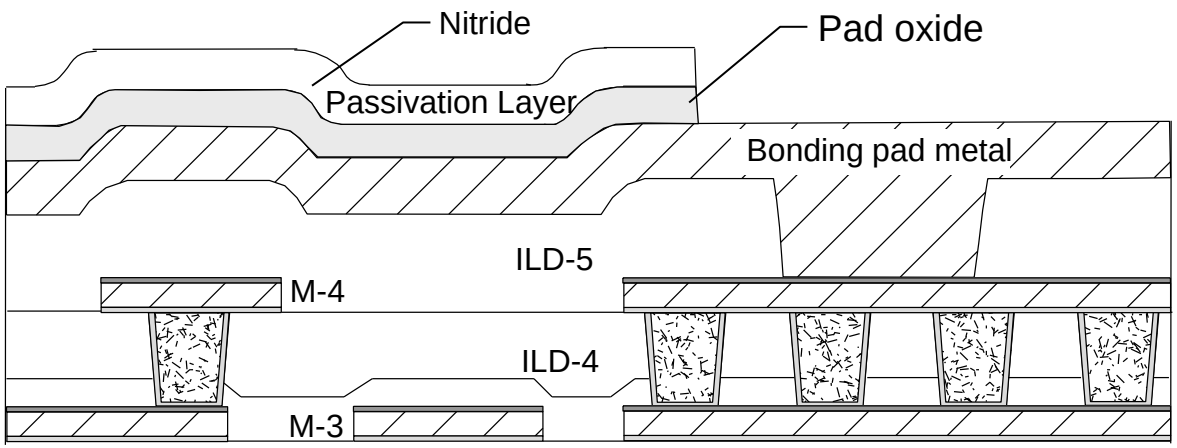


Comments: Dopants diffuse into unmasked areas of silicon by selective diffusion.

Table 10.1E

Table 10.1
Oxide Applications: Pad Oxide

Purpose: Provides stress reduction for Si_3N_4



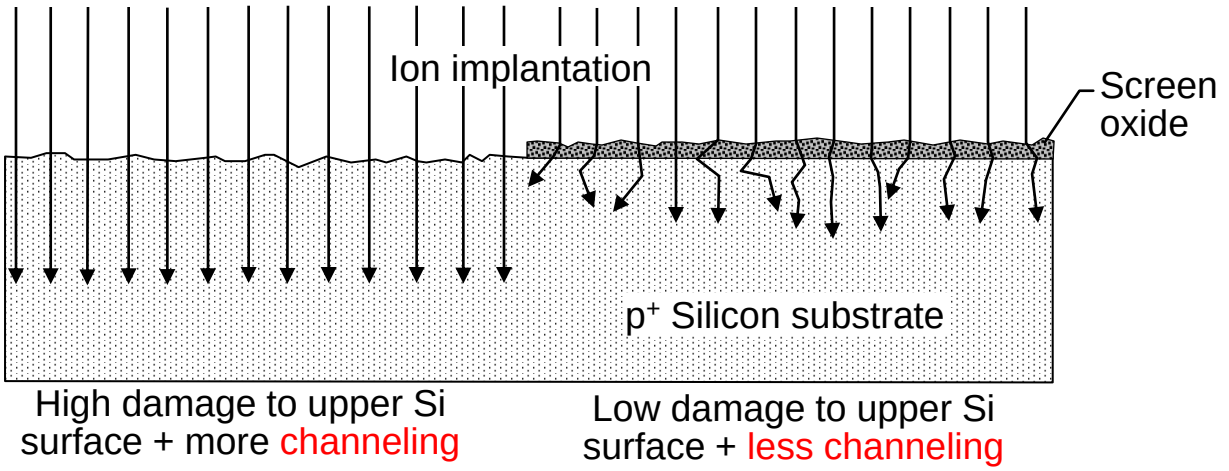
Comments: Thermally grown and very thin. [X]

CVD deposition, not thin

Table 10.1F

Table 10.1
Oxide Applications: Implant Screen Oxide

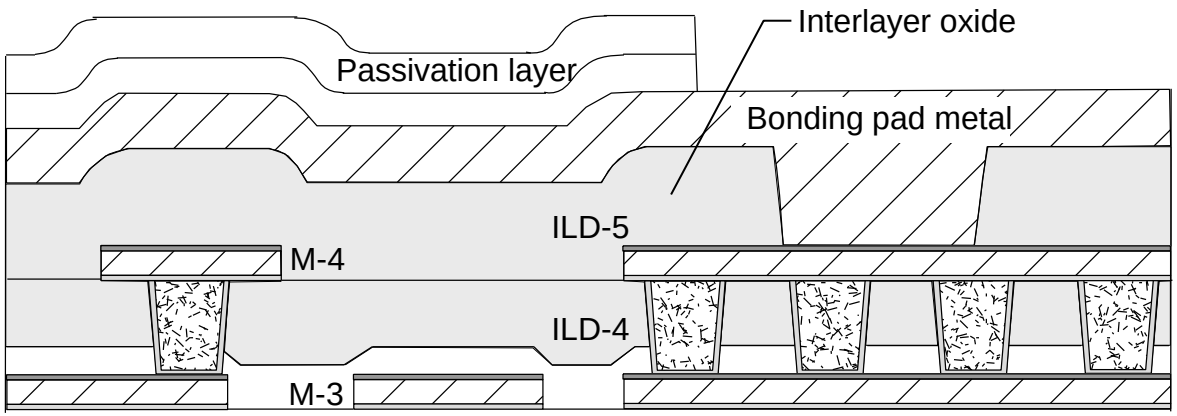
Purpose: Sometimes referred to as "sacrificial oxide", screen oxide, is used to reduce implant channeling and damage. Assists creation of shallow junctions.



Comments: Thermally grown

Table 10.1
Oxide Applications: Insulating Barrier between Metal Layers

Purpose: Serves as protective layer between metal lines.



Comments: This oxide is not thermally grown, but is deposited.

Table 10.1H

Thermal Oxidation Growth

- Chemical Reaction for Oxidation
  - Dry oxidation
  - Wet oxidation
- Oxidation Growth Model
  - Oxide silicon interface
    - Use of chlorinated agents in oxidation
  - Rate of oxide growth
  - Factors affecting oxide growth
  - Initial growth phase
  - Selective oxidation
    - LOCOS
    - STI

Oxide Thickness Ranges for Various Requirements

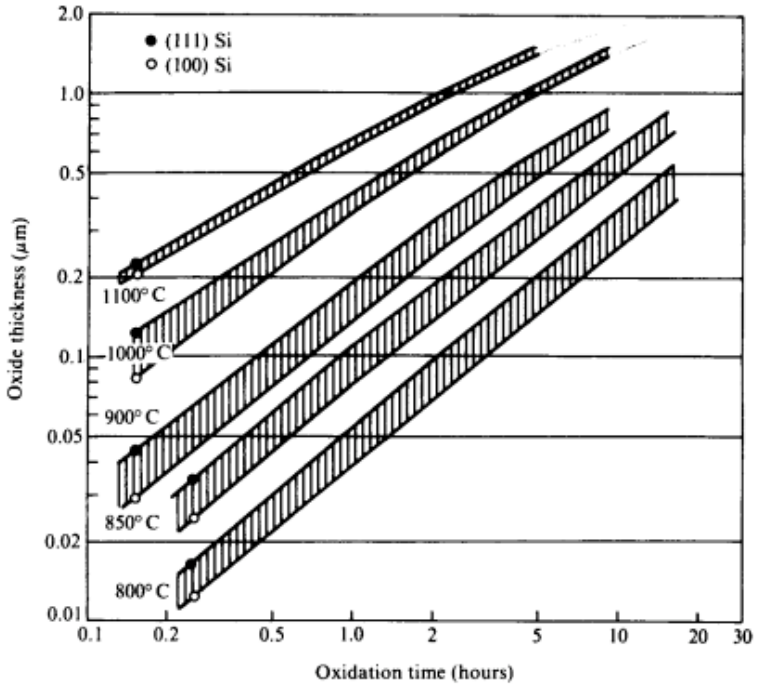
Semiconductor Application	Typical Oxide Thickness, Å
Gate oxide (0.18 μm generation)	20 – 60
Capacitor dielectrics	5 – 100
Dopant masking oxide	400 – 1,200 (Varies depending on dopant, implant energy, time & temperature)
STI Barrier Oxide	150
LOCOS Pad Oxide	200 – 500
Field oxide	2,500 – 15,000

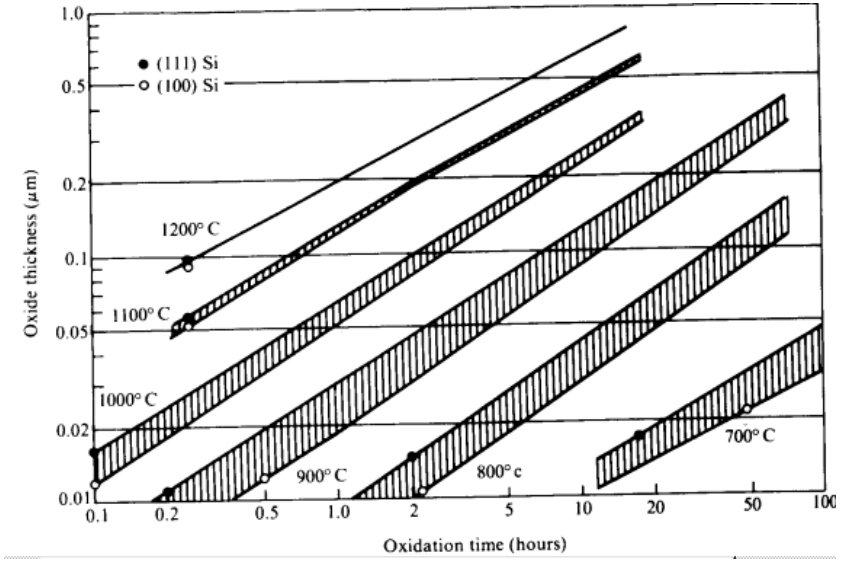
Table 10.2

Oxidation Thickness Vs. Oxidation Time in Dry and Wet Ambient

$Si\ (solid) + O_2\ (gas) \rightarrow SiO_2\ (solid)$

Dry oxidation ⟶

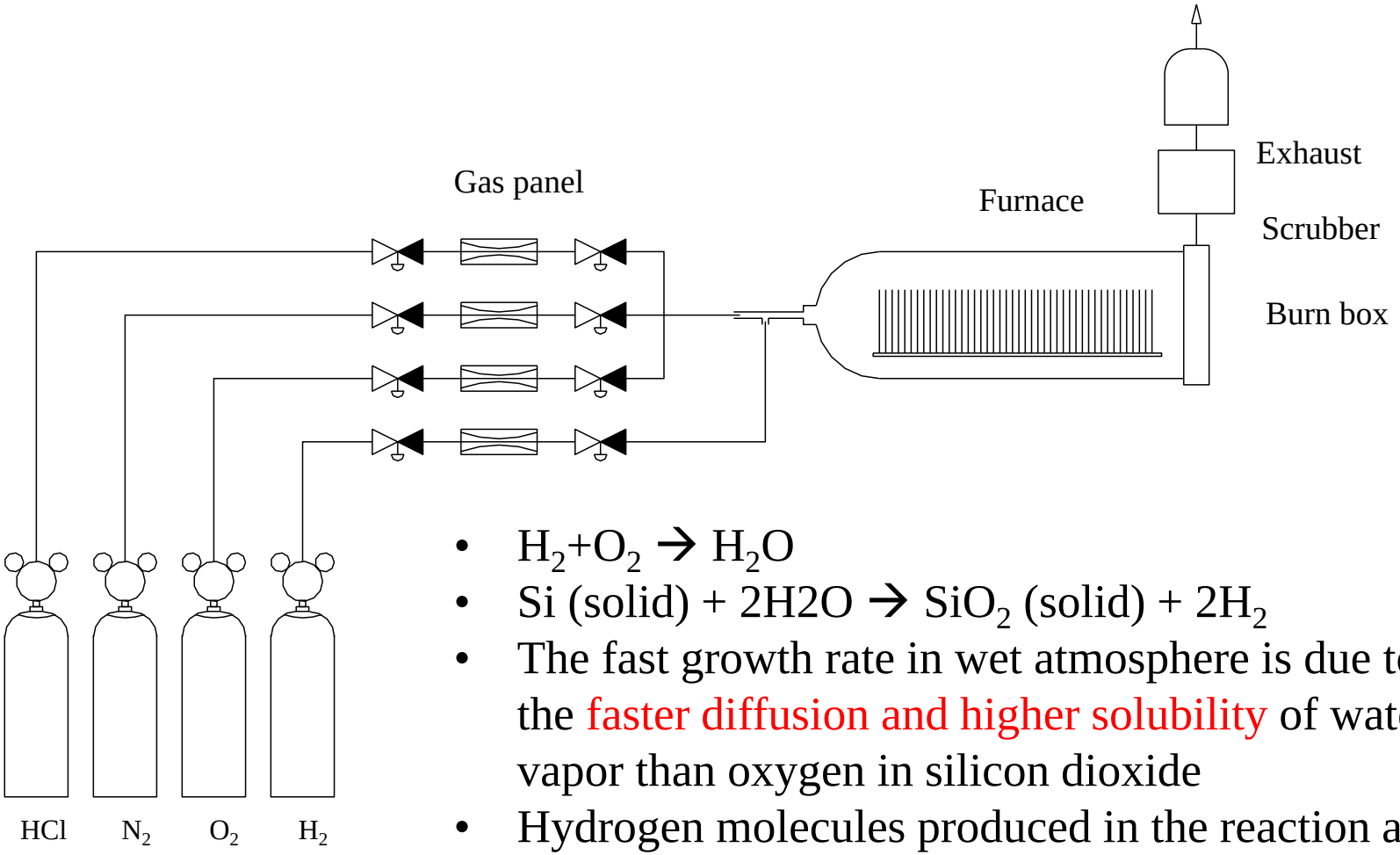




$Si\ (solid) + 2H2O \rightarrow SiO_2\ (solid) + 2H_2$

⟵ Wet oxidation

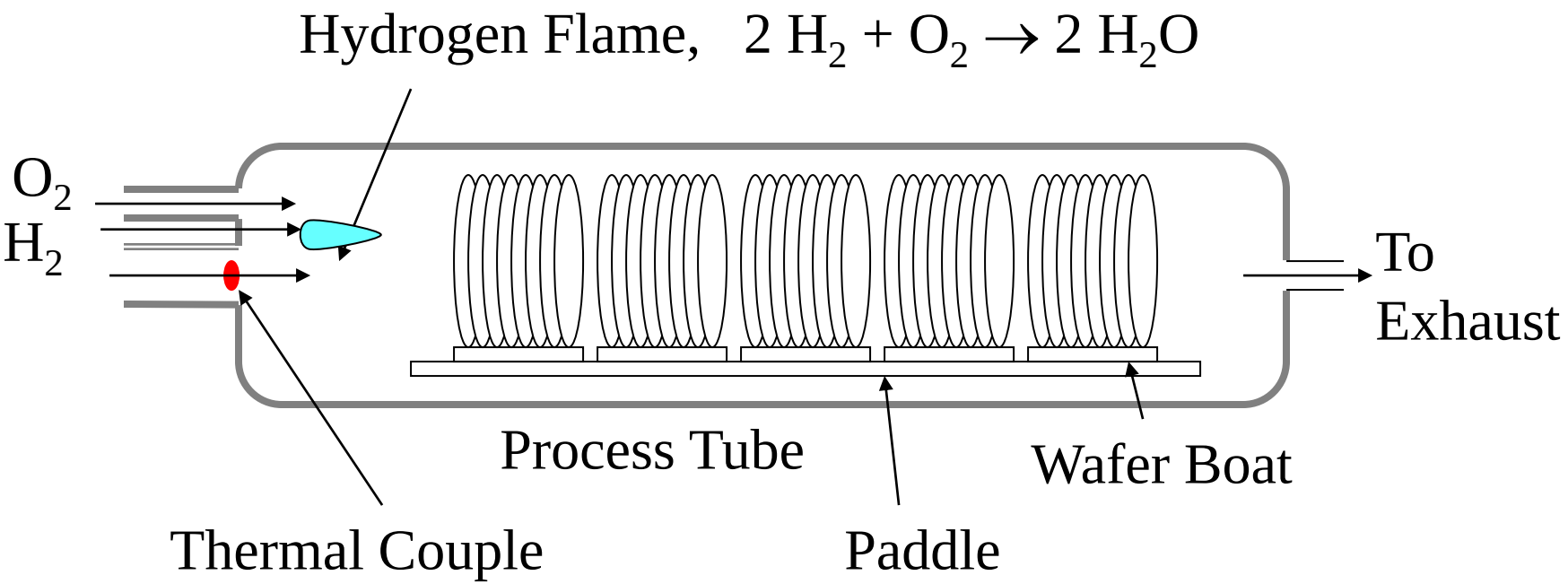
Wet Oxygen Oxidation



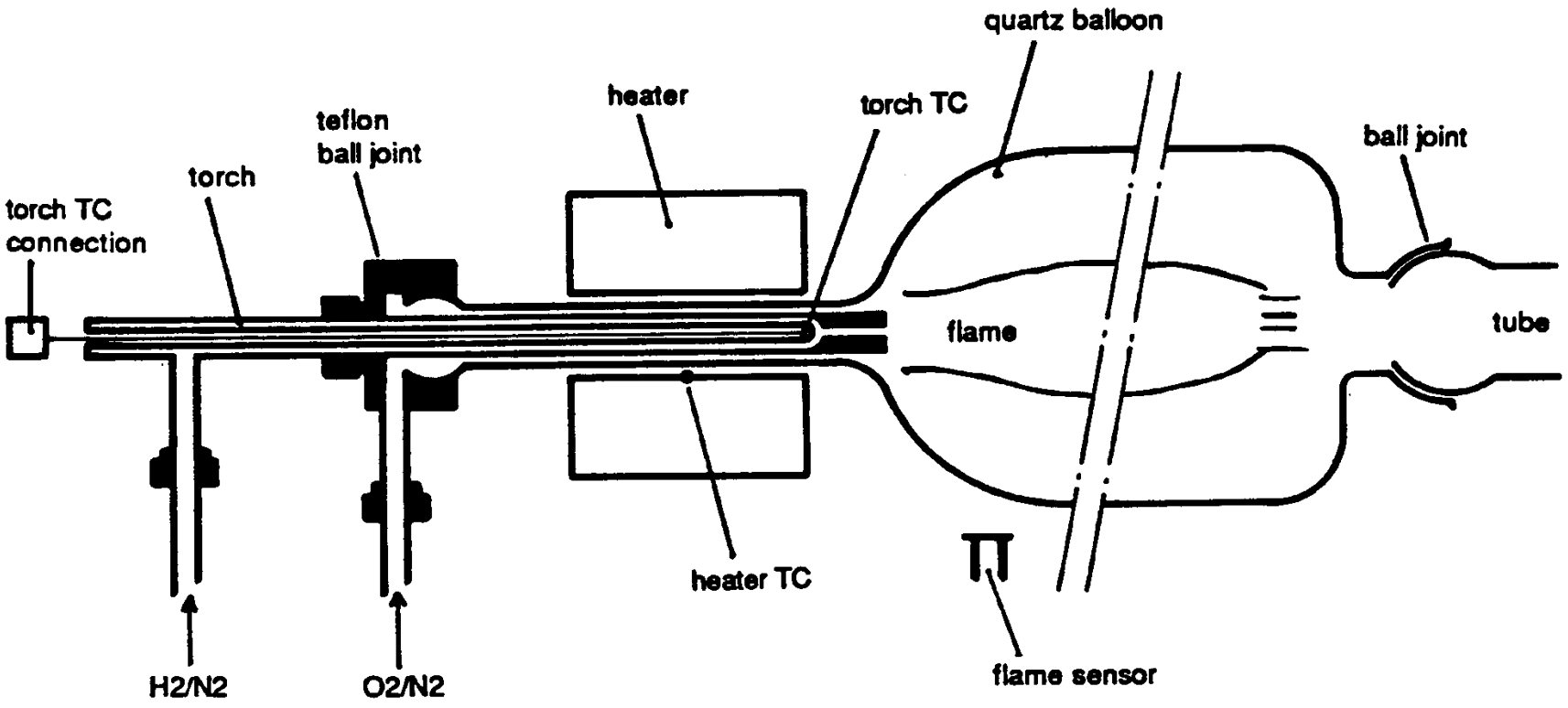
- $H_2+O_2 \rightarrow H_2O$
- Si (solid) + 2H2O → SiO_2 (solid) + $2H_2$
- The fast growth rate in wet atmosphere is due to the faster diffusion and higher solubility of water vapor than oxygen in silicon dioxide
- Hydrogen molecules produced in the reaction are trapped in oxide, less dense, using heating (annealing) to improve.

Figure 10.7

Pyrogenic Steam System

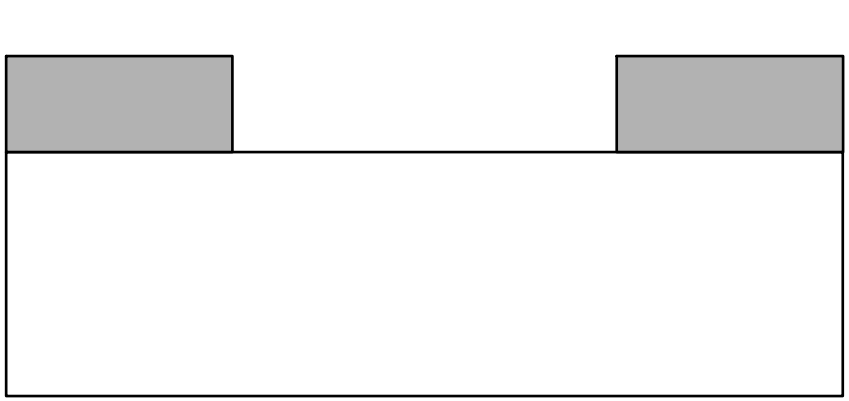


Outside Torch System
Wet oxidation: $H_2+O_2 \rightarrow H_2O$

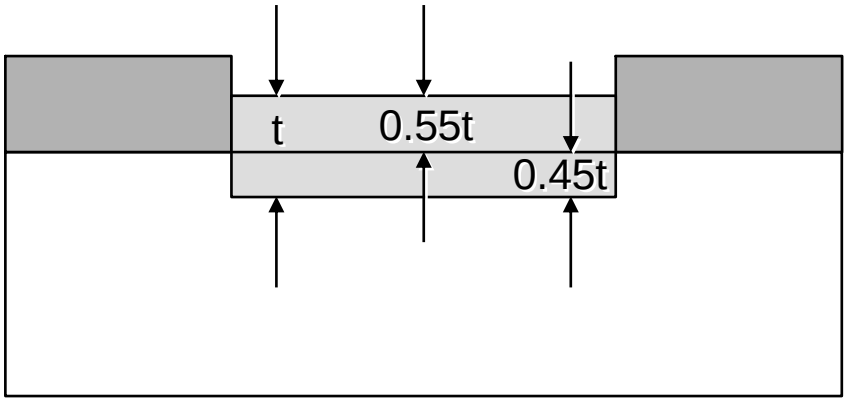


Consumption of Silicon during Oxidation

- For every 1000Å, 450Å of silicon is consumed
- Oxide growth occurs when the **oxygen** gas molecules move through the existing silicon oxide layer to the silicon wafer
- This process is called diffusion, high concentration to low



Before oxidation



After oxidation

Figure 10.8

Liquid-State Diffusion

Fick's law: $F = -D(\Delta n/\Delta x)$

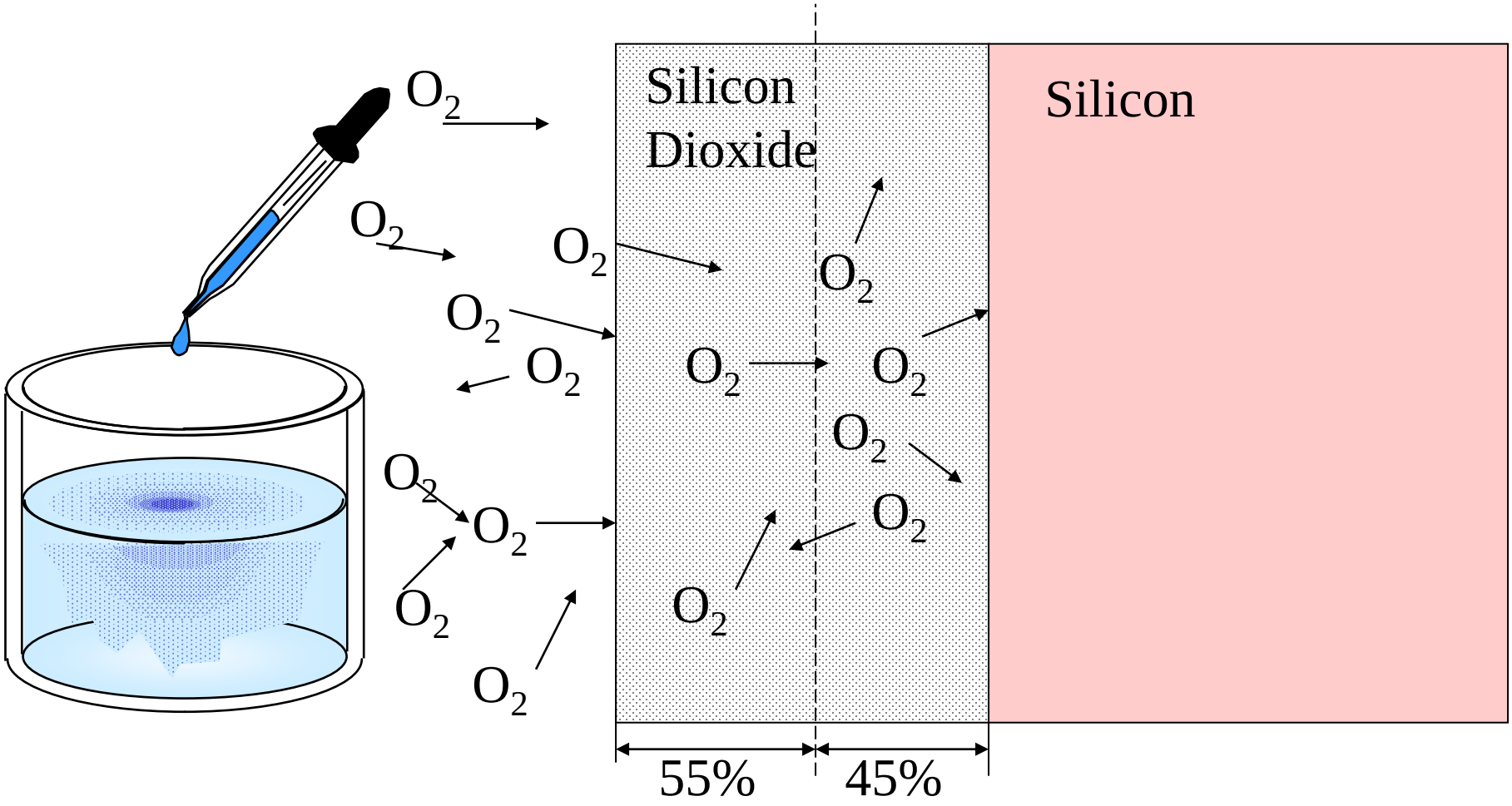
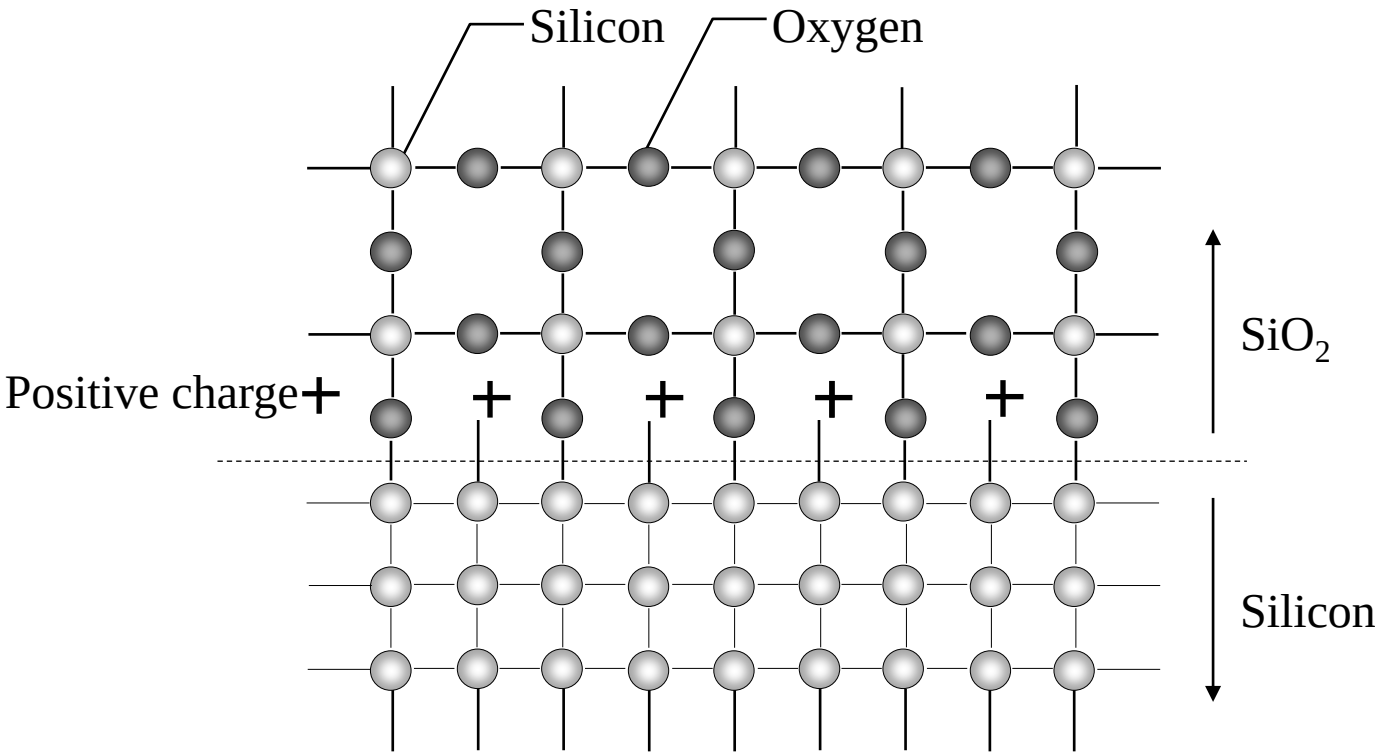


Figure 10.9

Charge Buildup at Si/SiO_2 Interface



- Positive charge is due to incomplete oxidation of Si
- Interface-trapped charge consisting positive or negative that result from structural defects, oxidation induced defects, or metal impurities, and a mobile oxide charge
- Dangling bond can be annealed out using forming gas (H_2/N_2)
- **Annealing to reduce positive fixed charges**.

Figure 10.10

Use of Chlorinated Agents in Oxidation

- Neutralize the charge at interface
- Normally, Cl (<3%), increases oxidation growth rate 10-15%
- Immobilize (gettering) mobile ionic
- Early work use HCl-gas (toxic and corrosive)
- TCA (trichloroethane, 三氯乙烷 $C_2H_3Cl_3$) was used but stop for ozone-depleting
- Trans-LC ($C_2H_2Cl_2$) is used

Diffusion of Oxygen Through Oxide Layer

The growth rate depends on: **temp**., **pressure**, **wet** or **dry**, silicon **orientation**, and **doping** level

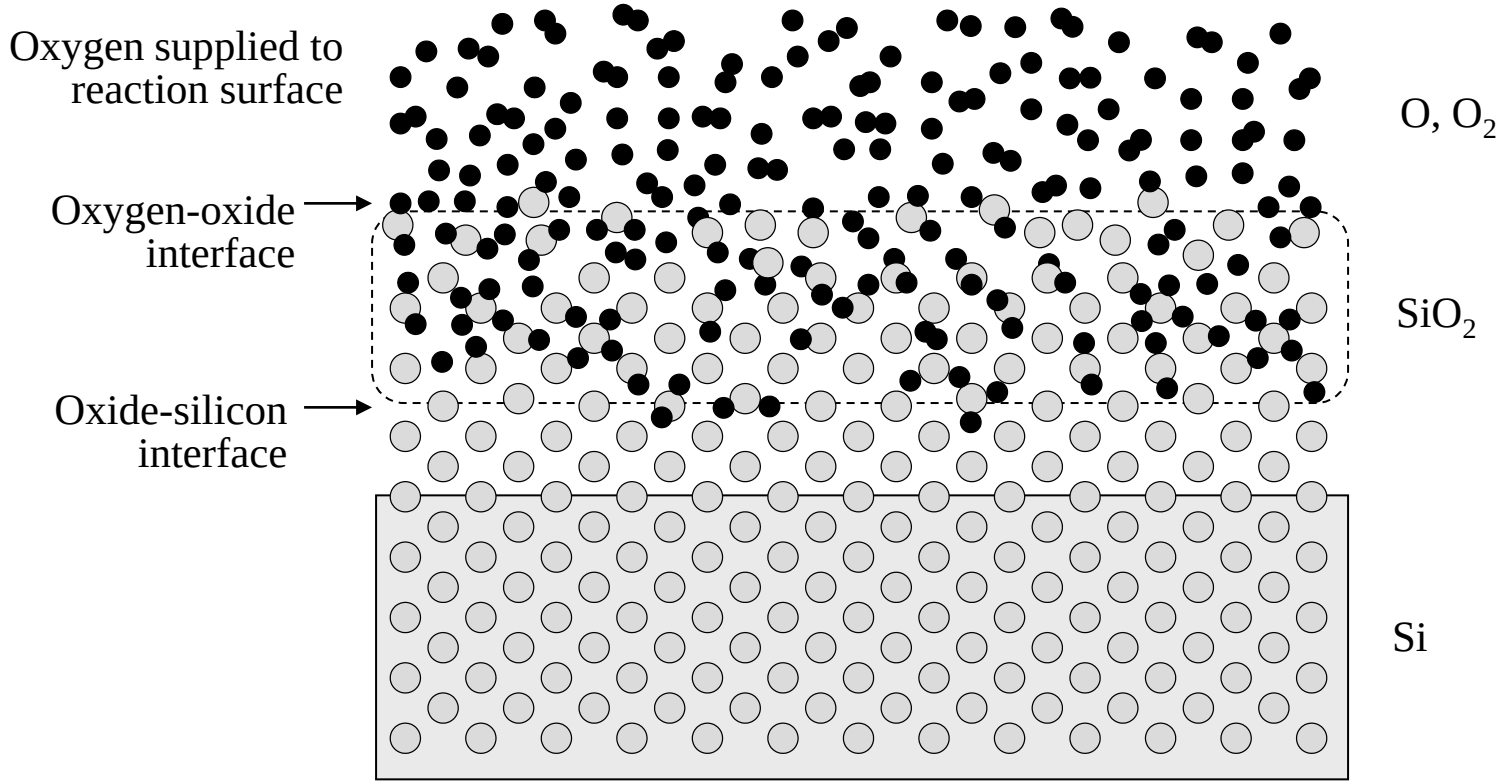


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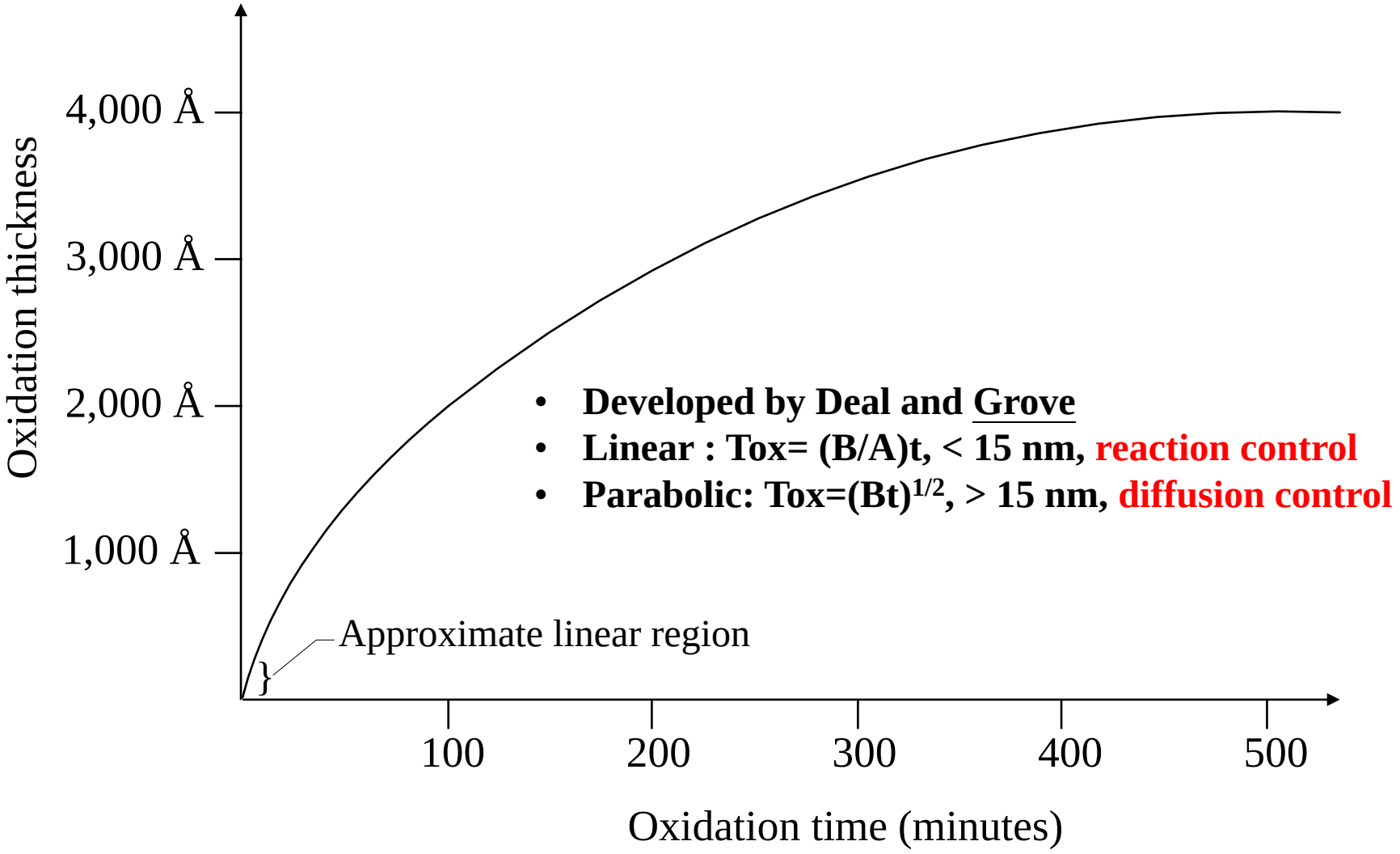
Figure 10.11

Linear & Parabolic Stages for Dry Oxidation Growth at 1100ºC



- **Developed by Deal and Grove**
- **Linear : Tox= (B/A)t, < 15 nm, reaction control**
- **Parabolic: Tox=$(Bt)^{1/2}$, > 15 nm, diffusion control**

Figure 10.12

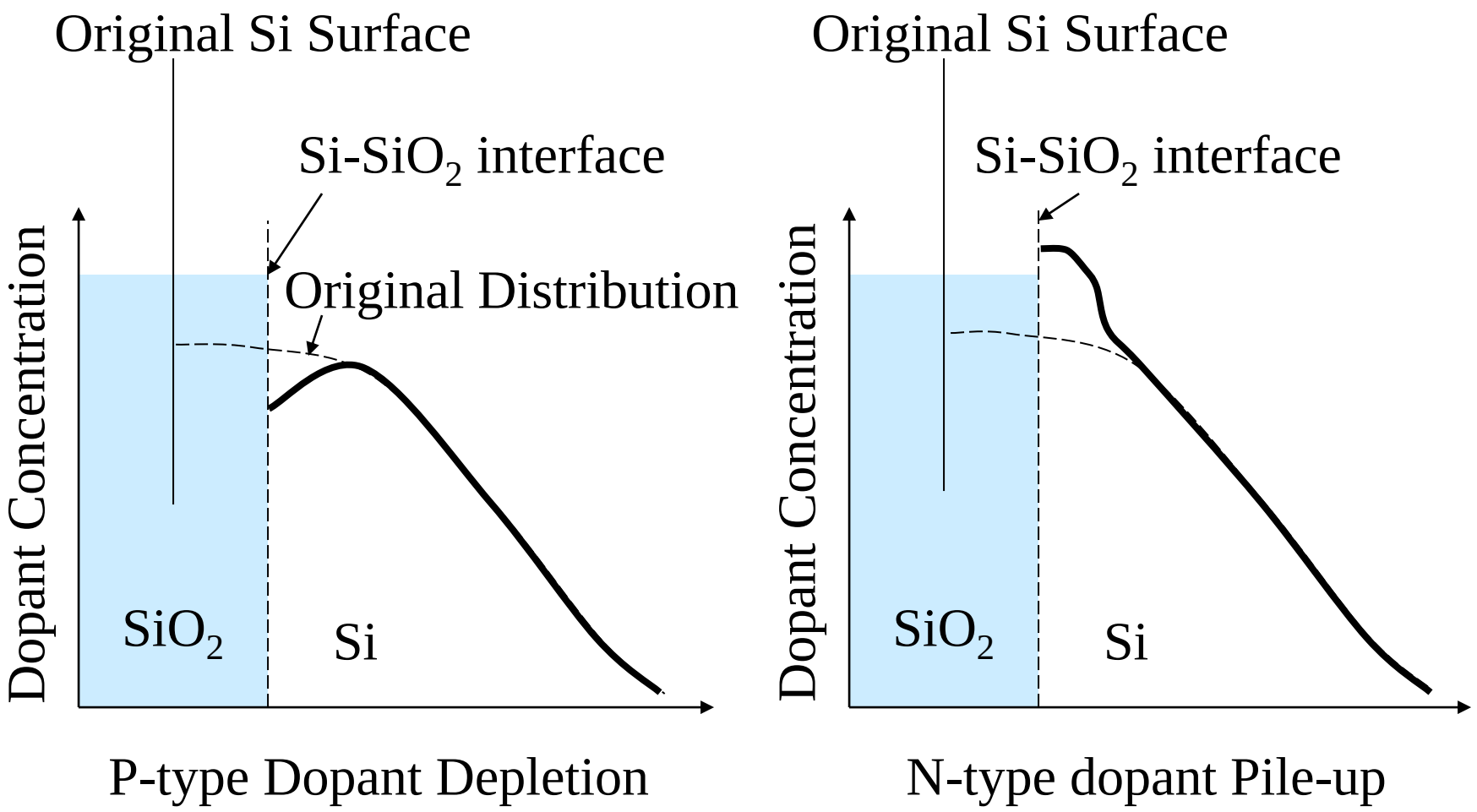
Factors Affecting Oxide Growth

- Dopant effect: heavily doped > lightly doped, Boron > P due to B incorporates into oxide (weakens bonds)
- Crystal orientation: (111) > (110) > (100) due to high density of (111), only in linear region (reaction control, not diffusion control)
- Pressure effect: high pressure increases rate, reduce thermal budget using high pressure (1 atm increase, 30°C reduced)
- Plasma enhancement: oxidation at low temperature, but with low quality
- Deal and Grove model can accurately predicts oxidation growth T_{ox}< 30 nm, no accurate model for T_{ox}< 6nm

Oxidation: Dopants
Pile-up and Depletion Effects

- N-type dopants (P, As, Sb) have higher solubility in Si than in SiO_2, when SiO_2 grow they move into silicon, it is call pile-up or snowplow effect.
- Boron tends to go to SiO_2, it is called depletion effect.

Depletion and Pile-up Effects



LOCOS Process (Selective Oxidation)

LOCOS: local oxidation of silicon [> 0.25 μm]

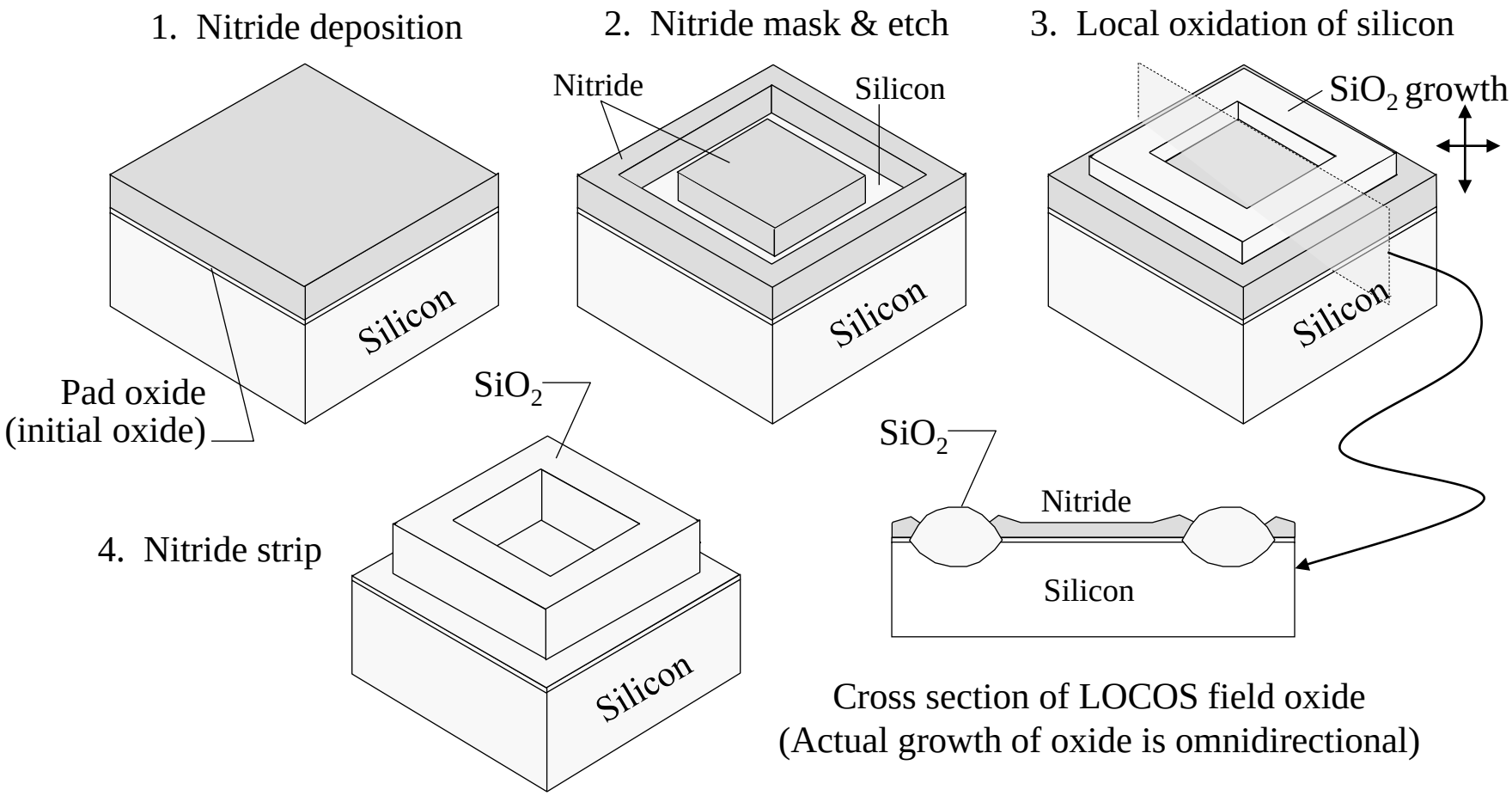


Figure 10.13

Selective Oxidation and Bird's Beak Effect

- **Compressive** stress due to different thermal expansion coefficient
- Oxidation-induced stacking fault (OISF): due to excess interstitial silicon

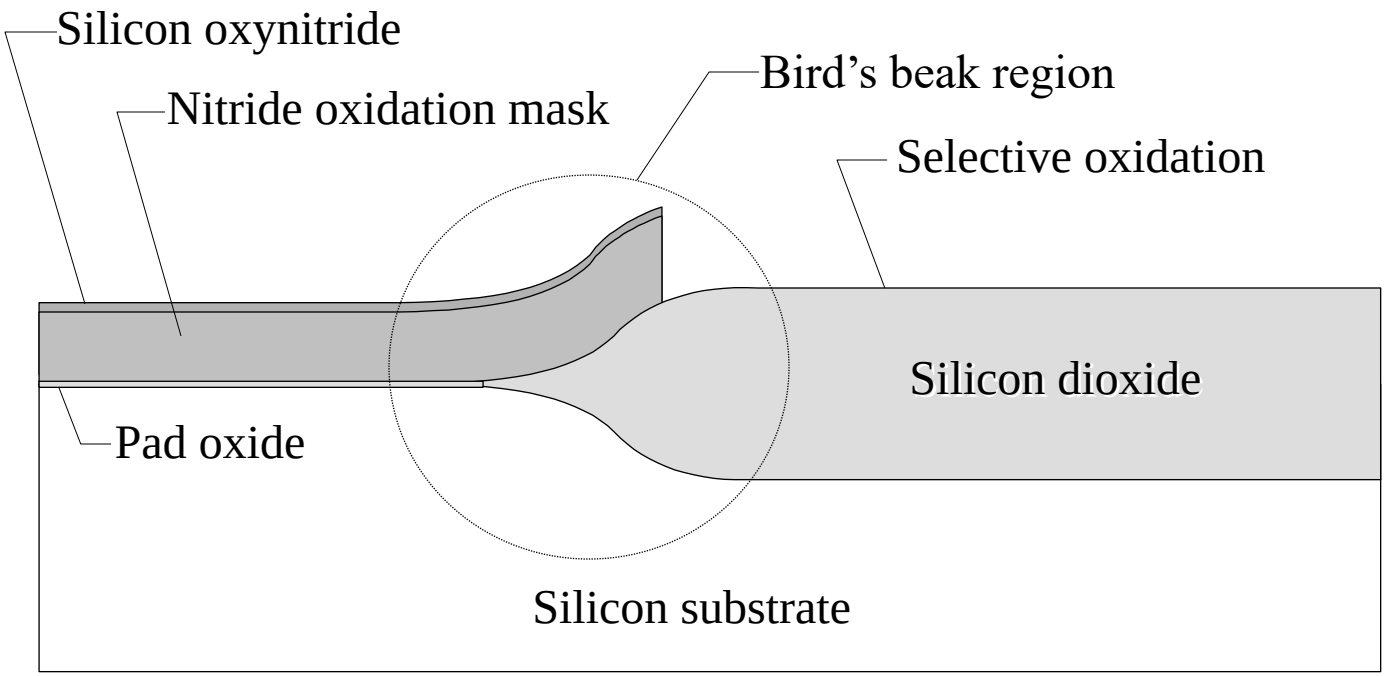


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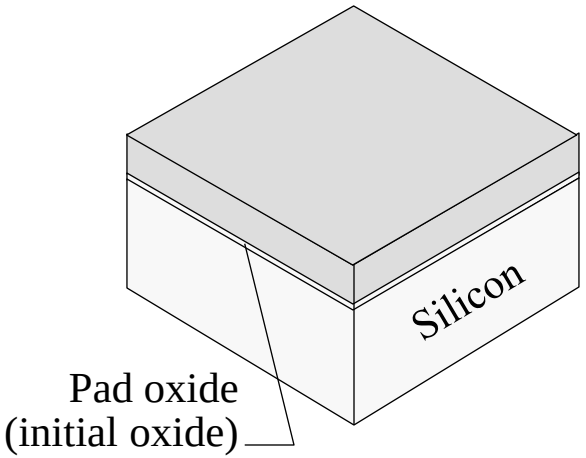
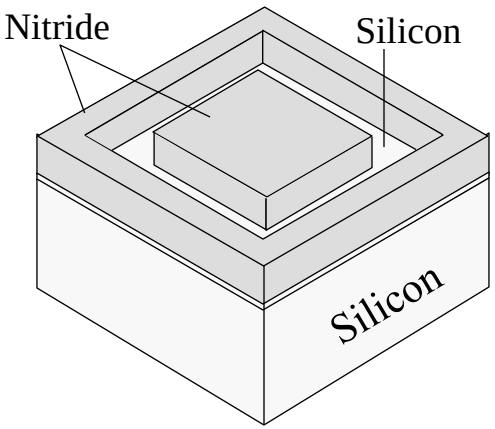
Figure 10.14

STI (shallow trench isolation) Oxide Liner

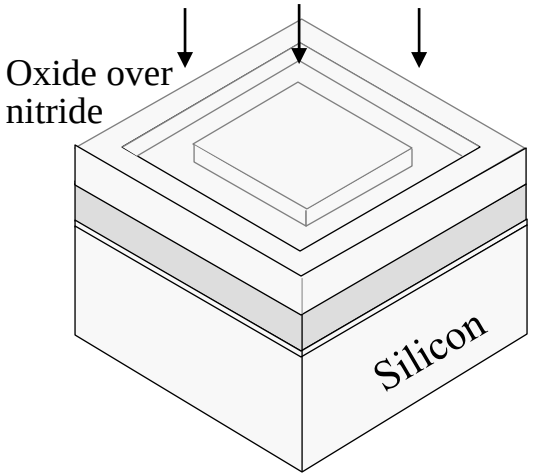
1. Nitride deposition



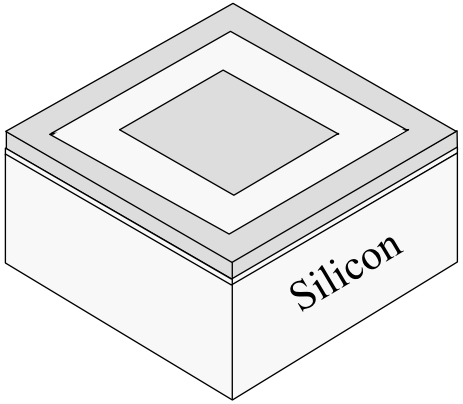
2. Trench mask and etch



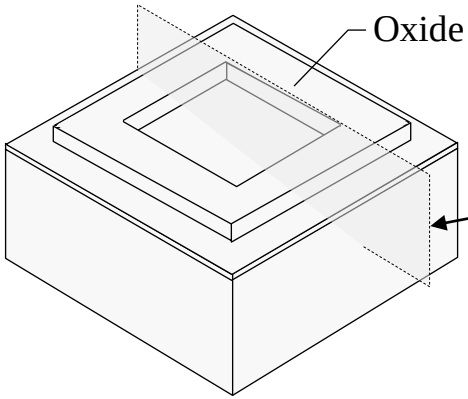
3. Sidewall oxidation and trench fill

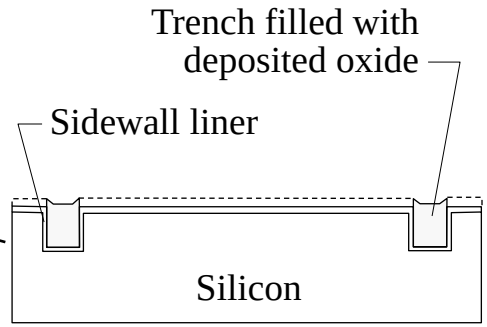


4. Oxide planarization (CMP)



5. Nitride strip





Cross section of shallow trench isolation (STI)

Figure 10.15

Furnace Equipment

- Horizontal Furnace (conventional)
- Vertical Furnace (early 1990s)
- Rapid Thermal Processor (RTP)

Horizontal and Vertical Furnaces

Performance Factor	Performance Objective	Horizontal Furnace	Vertical Furnace
Typical wafer loading size	Small, for process flexibility	200 wafers/batch	100 wafers/batch
Clean room footprint	Small, to use less space	Larger, but has 4 process tubes	Smaller (single process tube)
Parallel processing	Ideal for process flexibility	Not capable	Capable of loading/unloading wafers during process, which increases throughput
Gas flow dynamics (GFD)	Optimize for uniformity	Worse due to paddle and boat hardware. Bouyancy and gravity effects cause non-uniform radial gas distribution.	Superior GFD and symmetric/uniform gas distribution
Boat rotation for improved film uniformity	Ideal condition	Impossible to design	Easy to include
Temperature gradient across wafer	Ideally small	Large, due to radiant shadow of paddle	Small
Particle control during loading/unloading	Minimum particles	Relatively poor	Improved particle control from top-down loading scheme
Quartz change	Easily done in short time	More involved and slow	Easier and quicker, leading to reduced downtime
Wafer loading technique	Ideally automated	Difficult to automate in a successful fashion	Easily automated with robotics
Pre-and post-process control of furnace ambient	Control is desirable	Relatively difficult to control	Excellent control, with options of either vacuum or neutral ambient

Table 10.3

Horizontal Diffusion Furnace

Photograph courtesy of International SEMATECH

Photo 10.1

Vertical Diffusion Furnace

Host computer: recipe download, wafer tracking, automatic scheduling, data collection

Photo 10.2

Block Diagram of Vertical Furnace System

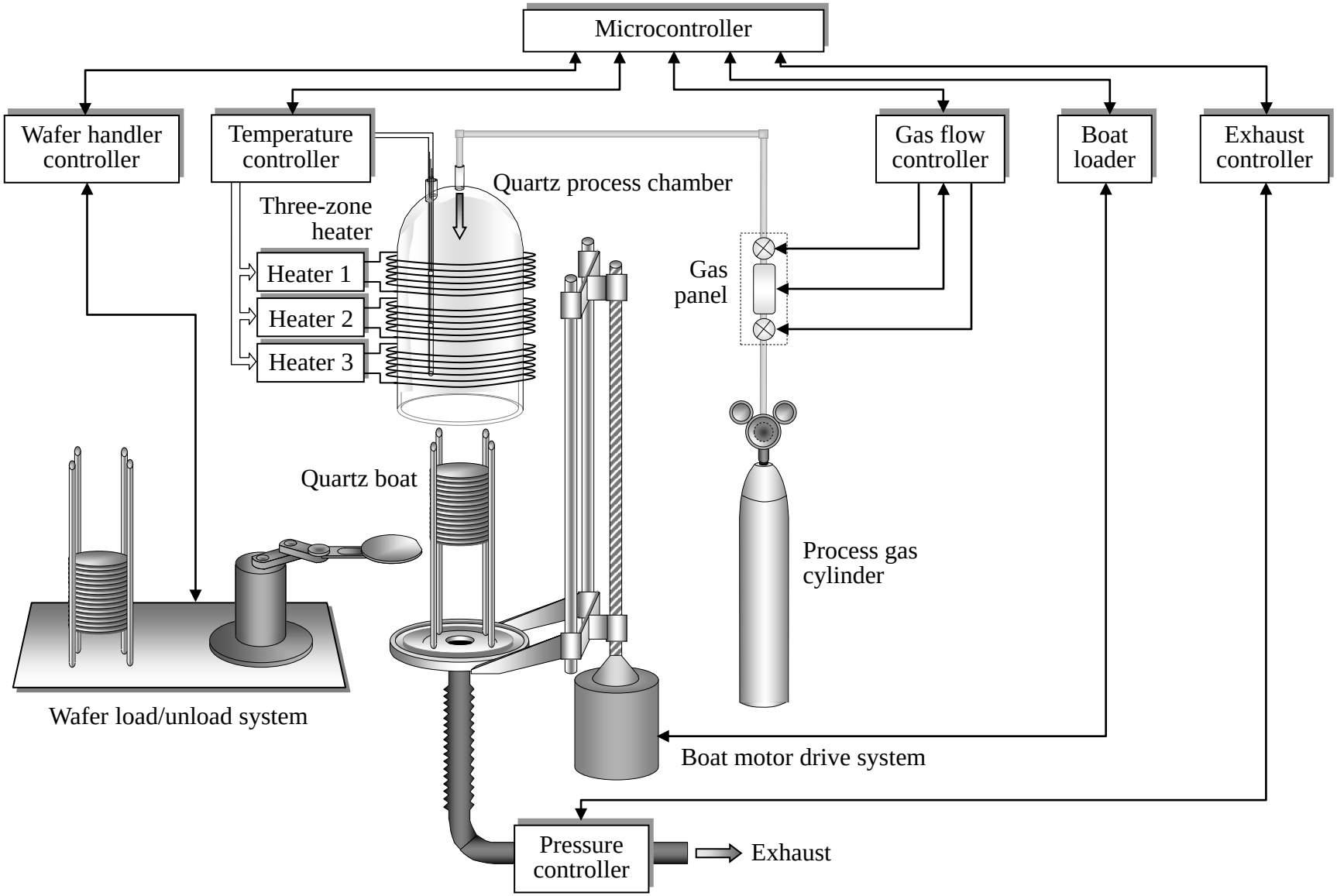
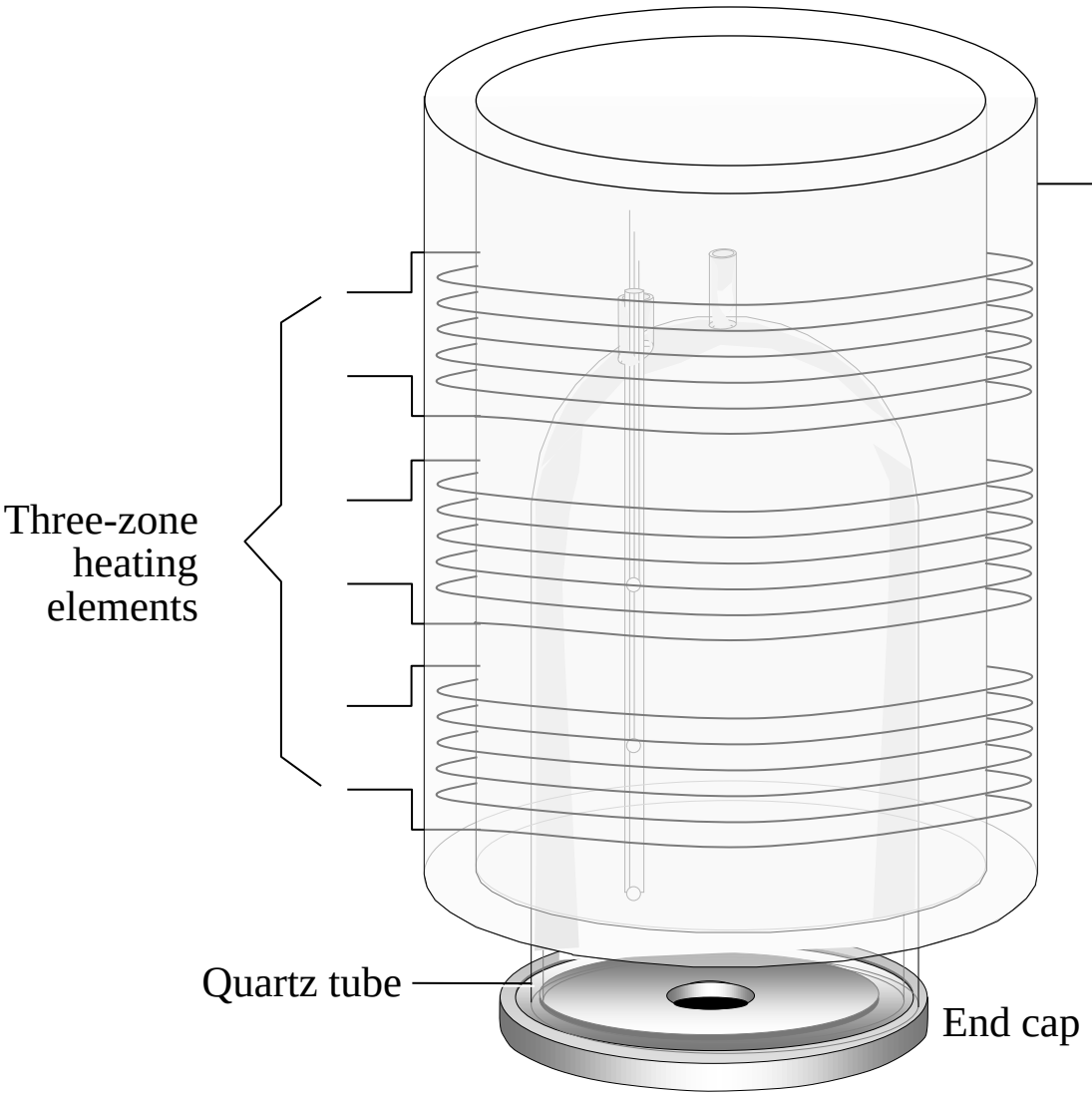


Figure 10.16

Vertical Furnace Process Tube



Quartz: single crystal SiO_2
Fused silica: amorphous quartz
SiC is popular now but expensive

Figure 10.17

Heater Element Power Distribution

- SCR: silicon control rectifier
- Switching to control power delivered to system, e.g., 50% on

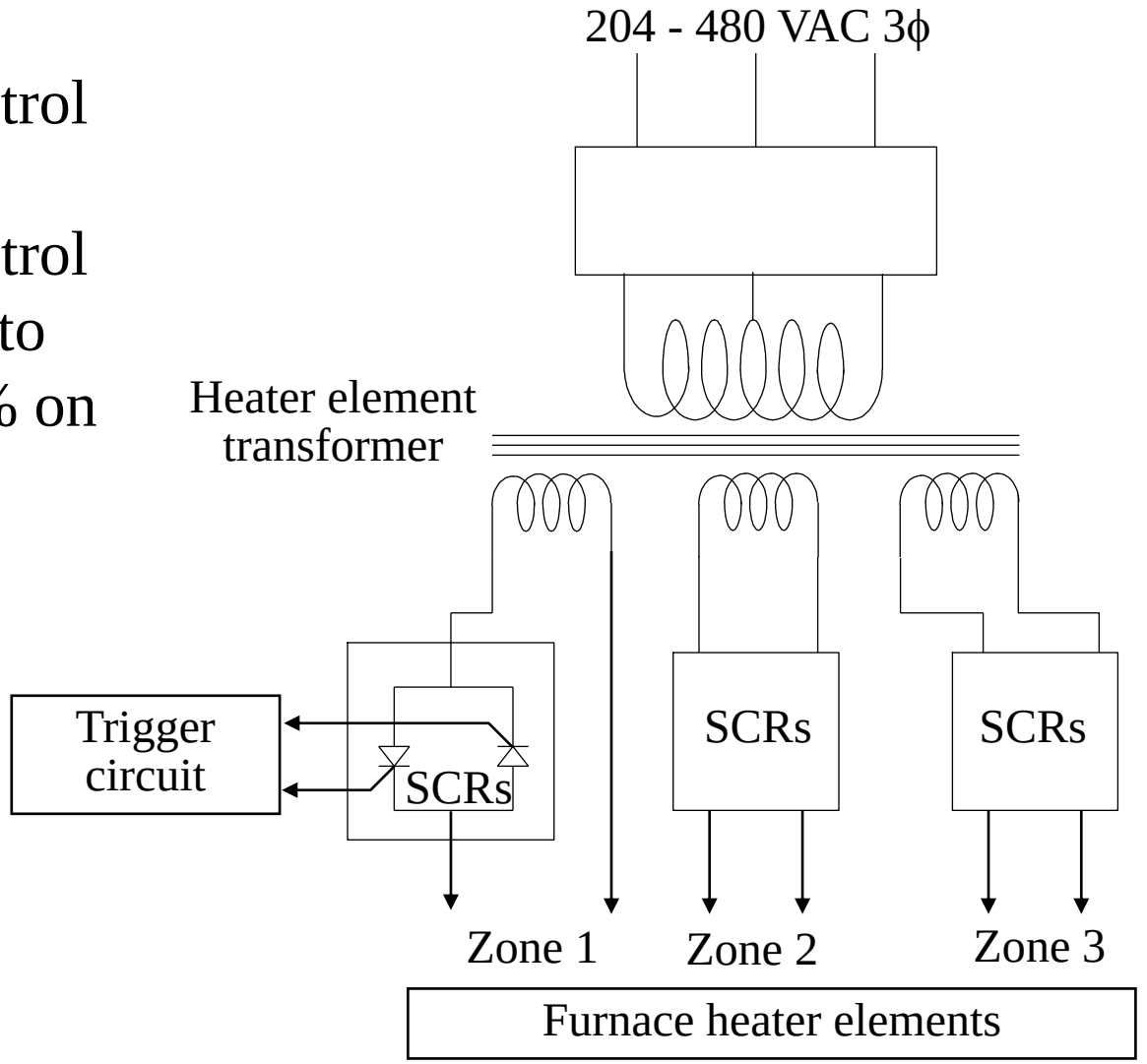


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Figure 10.18

Locations of **Thermocouples** in the Furnace Chamber

- To create a flat zone near the middle of tube ~ **0.25˚C**
- The atmosphere around the wafer is called **ambient**

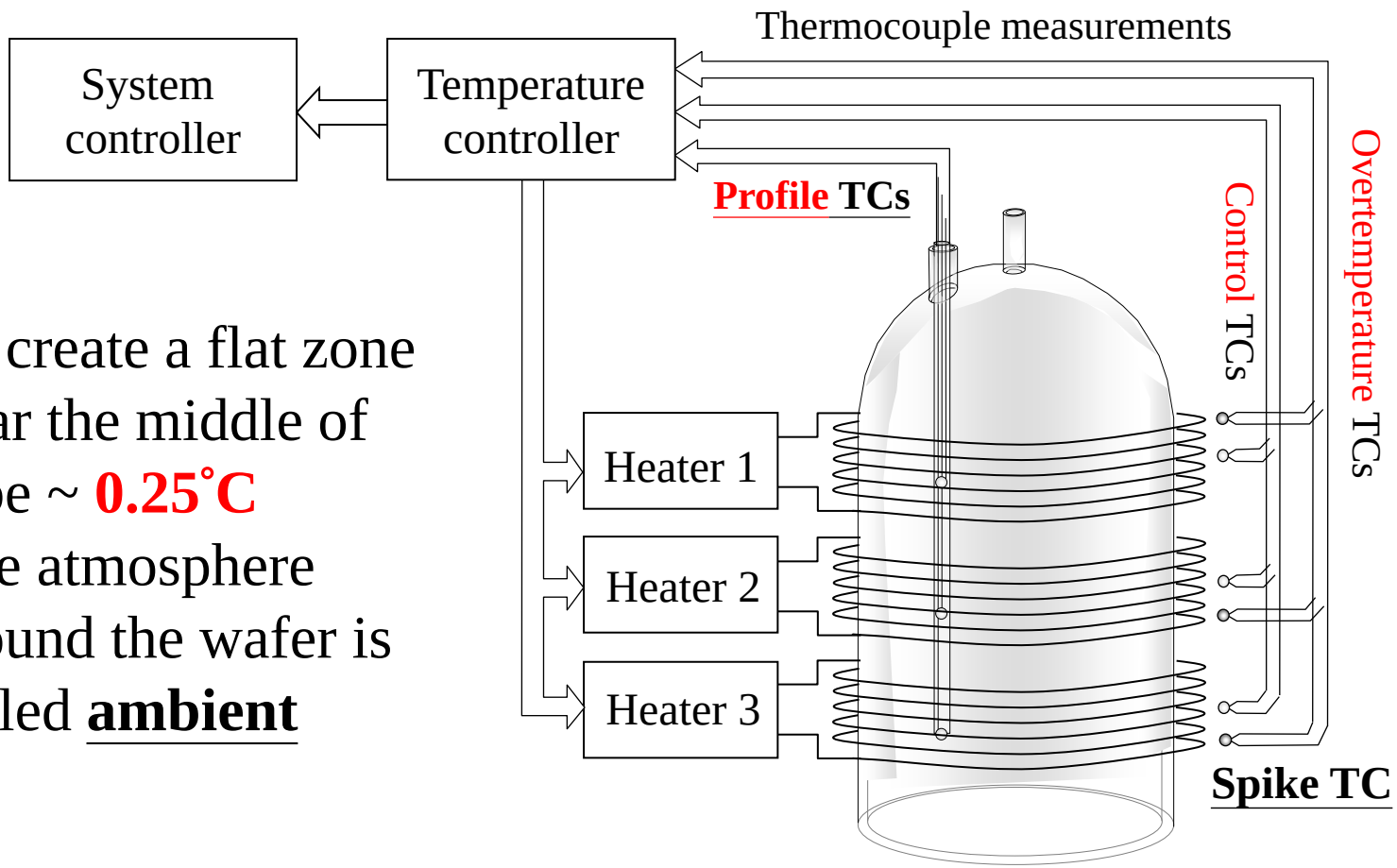

Figure 10.19

Common Gases used in Furnace Processes

Gases	Classifications	Examples
Bulk	Inert gas	Argon (Ar), Nitrogen (N_2)
	Reducing gas	Hydrogen (H_2)
	Oxidizing gas	Oxygen (O_2)
Specialty	Silicon-precursor gas	Silane (SiH_4), dichlorosilane (DCS) or (H_2SiCl_2)
	Dopant gas	Arsine (AsH_3), phosphine (PH_3) Diborane (B_2H_6)
	Reactant gas	Ammonia (NH_3), hydrogen chloride (HCl)
	Atmospheric/purge gas	Nitrogen (N_2), helium (He)
	Other specialty gases	Tungsten hexafluoride (WF_6)

Table 10.4

Burn Box to Combust Exhaust

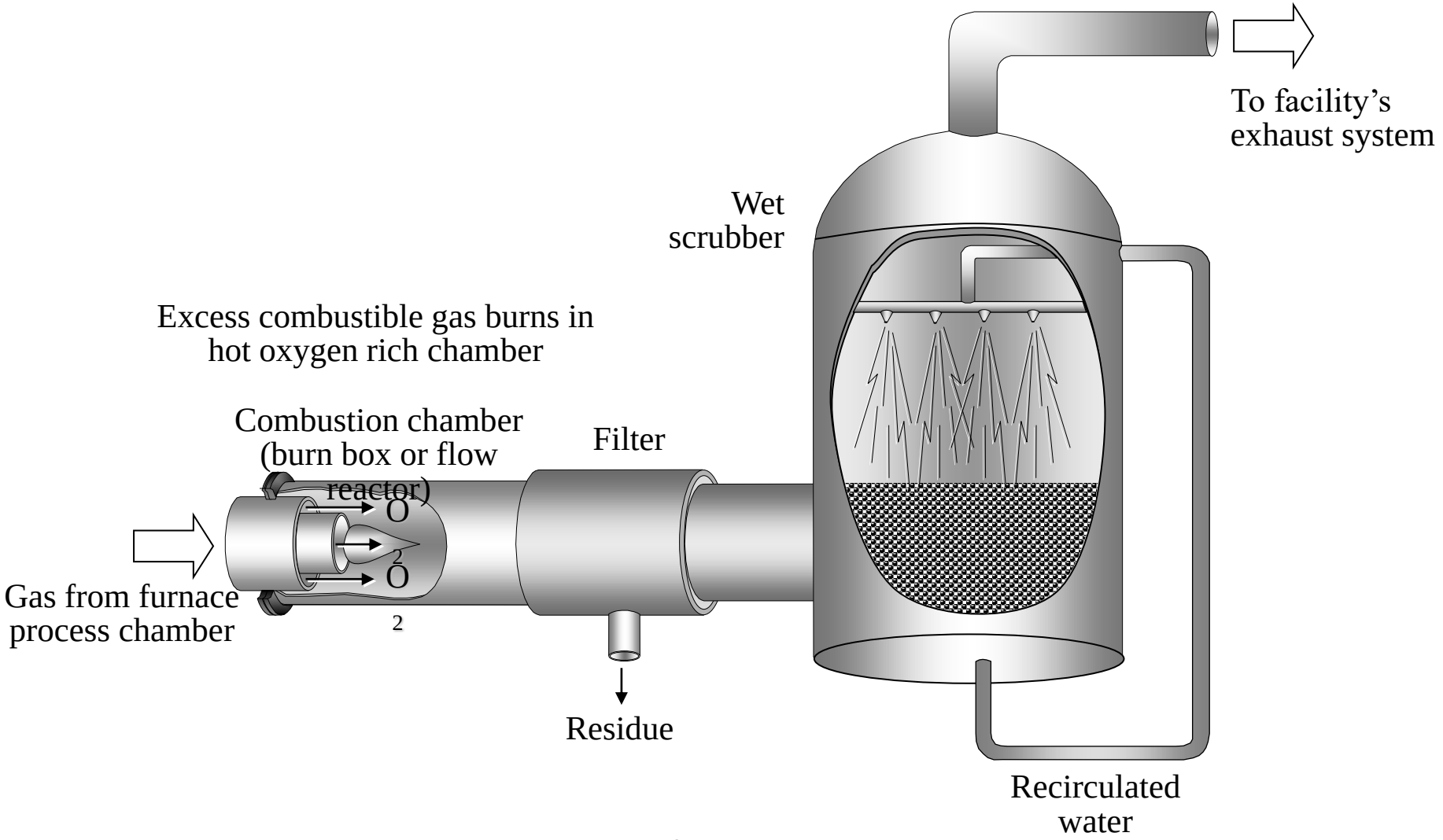

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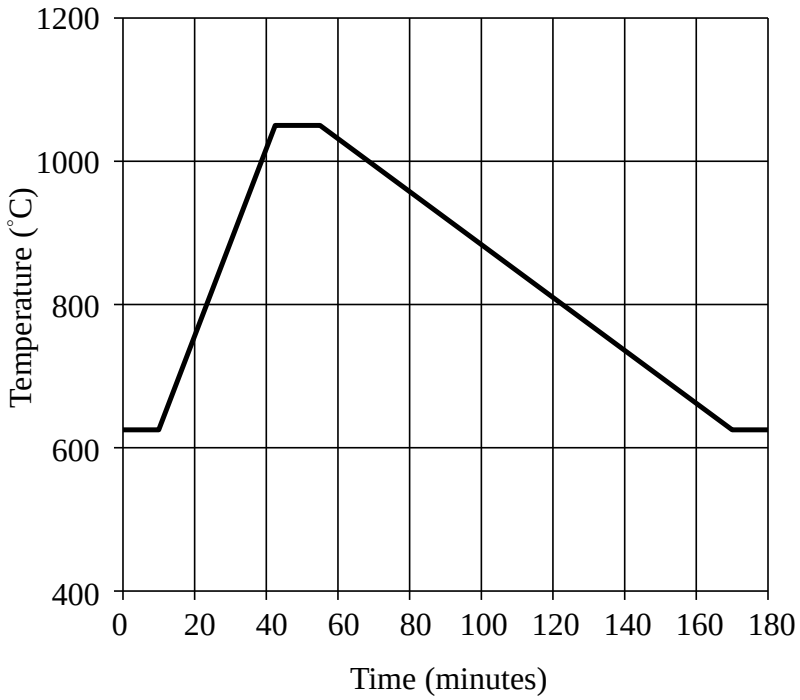
Figure 10.20

Thermal Profile of Conventional Versus Fast Ramp Vertical Furnace

Conventional: 5-10°C/min

Fast Ramp: 100°C/min up and 60°C down
To maintain uniform, using small batch 50-100 wafer



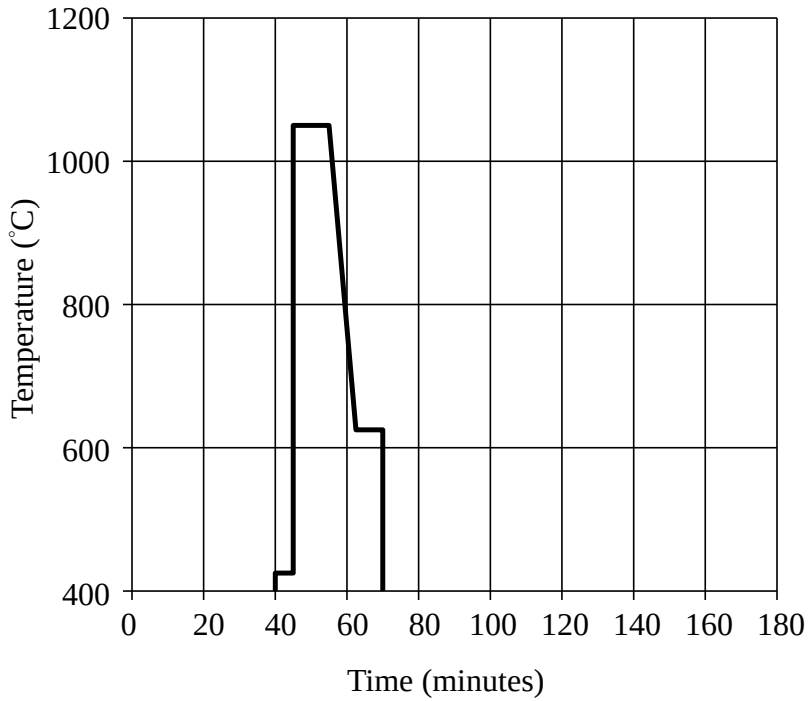


Figure 10.21

The Main Advantages of a Rapid Thermal Processor

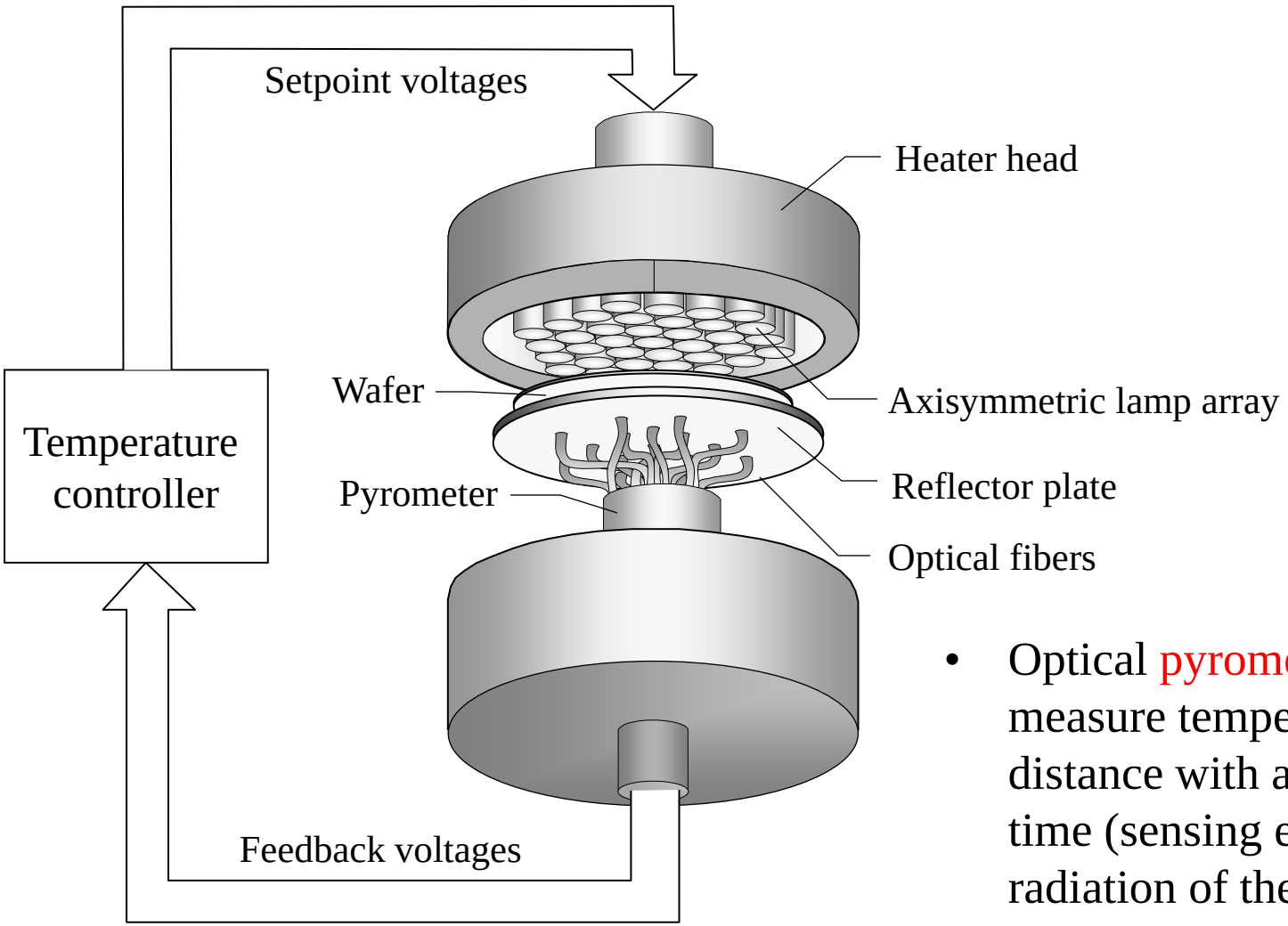
- Reduced **thermal budget**
- Minimized dopant movement in the silicon
- Ease of clustering multiple tools
- Reduced contamination due to cold wall heating
- Cleaner ambient because of the smaller chamber volume
- Shorter time to process a wafer (referred to as cycle time)

Comparison of Conventional Vertical Furnace and RTP

Vertical Furnace	RTP
Batch	Single-wafer
Hot wall	Cold wall
Long time to heat and cool batch	Short time to heat and cool wafer
Small thermal gradient across wafer	Large thermal gradient across wafer
Long cycle time	Short cycle time
Ambient temperature measurement	Wafer temperature measurement
Issues:	Issues:
Large thermal budget	Temperature uniformity
Particles	Minimize dopant movement
Ambient control	Repeatability from wafer to wafer
	Throughput
	Wafer stress due to rapid heating
	Absolute temperature measurement

Table 10.5

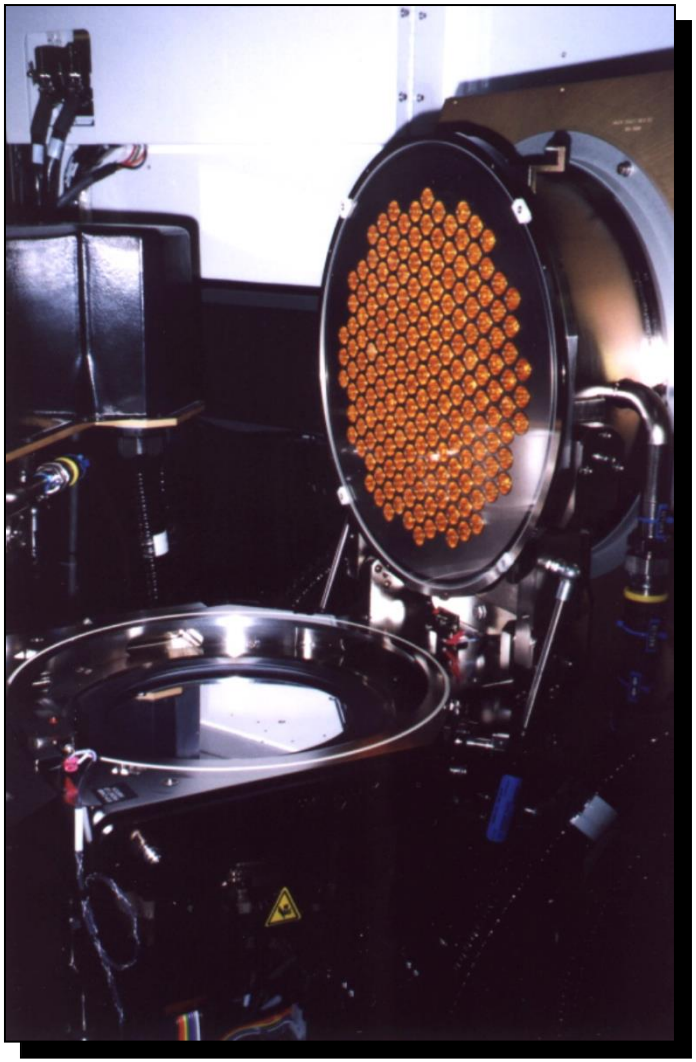
Rapid Thermal Processor **(cold wall)**



- Optical pyrometer can measure temperature from a distance with a fast response time (sensing emitted infrared radiation of the wafer)

Figure 10.22

Rapid Thermal Processor



- Tungsten halogen lamp
- Can be a cluster tool to reduce native oxide and contamination

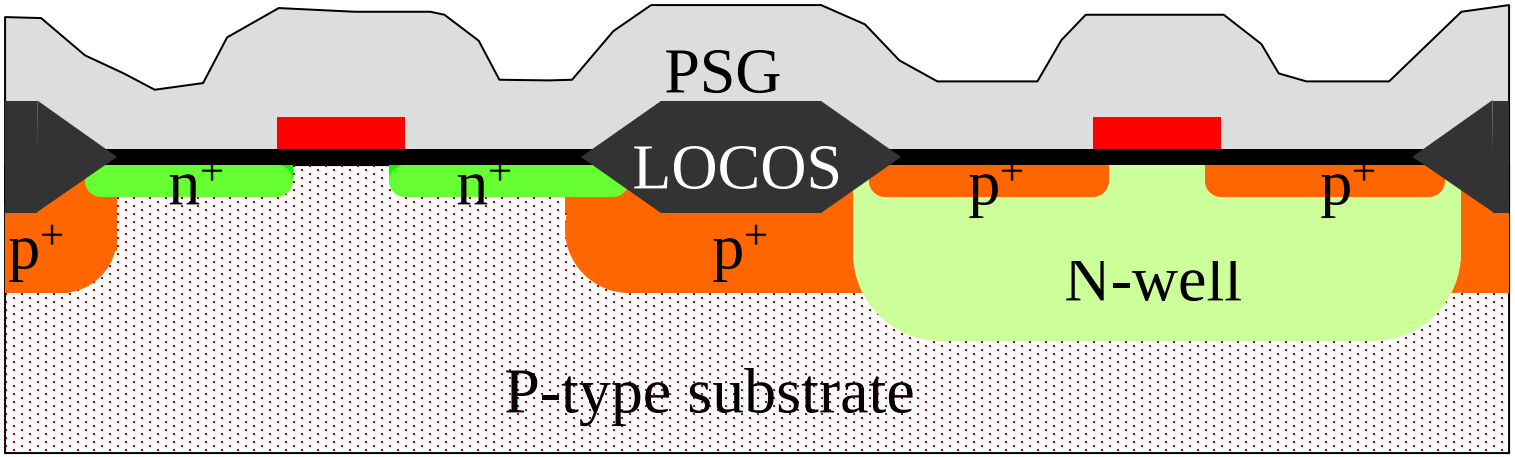
Photo 10.3

RTP Applications

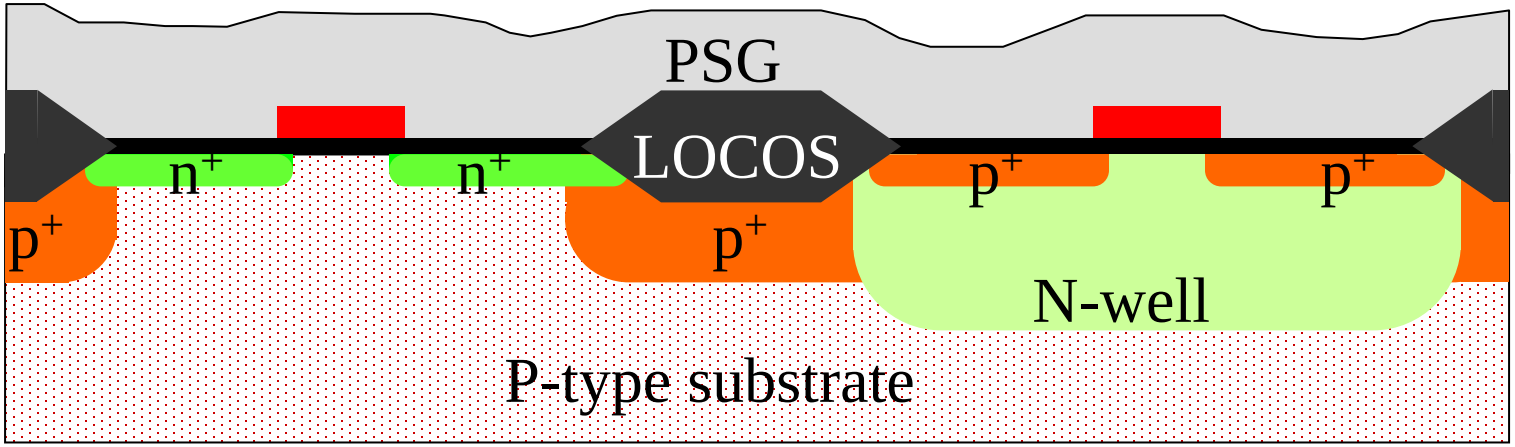
- Anneal of implants to remove defects and activate and diffuse dopants
- Densification of deposited films, such as deposited oxide layers
- Borophosphosilicate glass (BPSG) reflow
- Anneal of barrier layers, such as titanium nitride (TiN)
- Silicide formation, such as titanium silicide ($TiSi_2$)
- Contact alloying

Illustration of BPSG Reflow

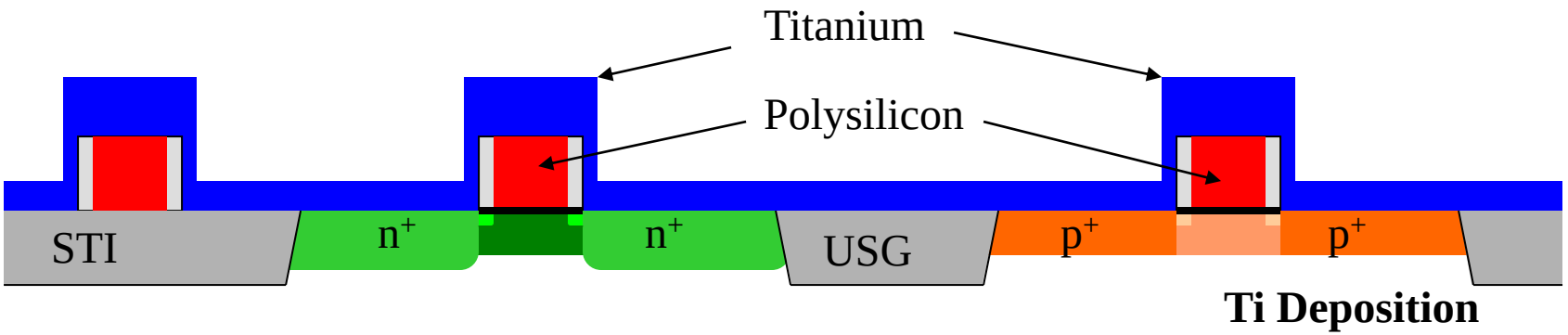
As Deposit



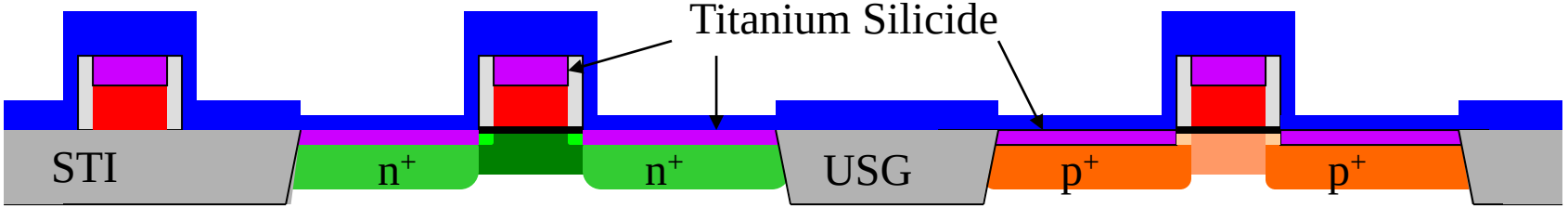
After Reflow



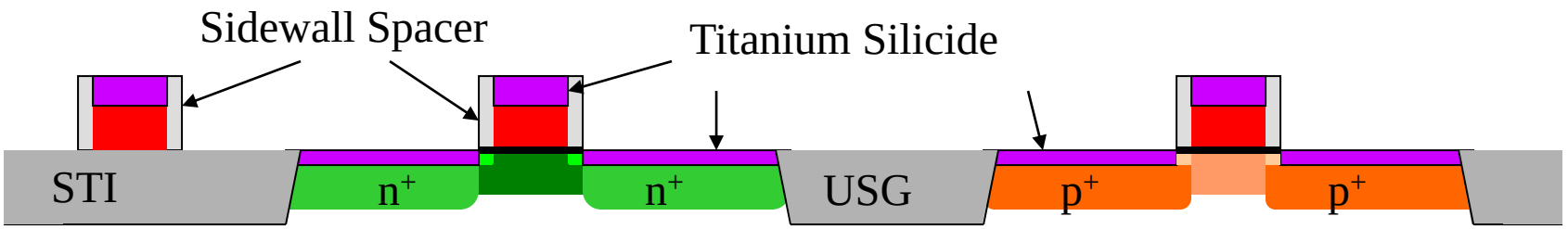
Titanium Silicide Process



Ti Deposition



Annealing



Ti Strip

Oxidation Process

- Pre Oxidation Cleaning
  - Oxidation process recipe
- Quality Measurements
- Oxidation Troubleshooting

Critical Issues for Minimizing Contamination

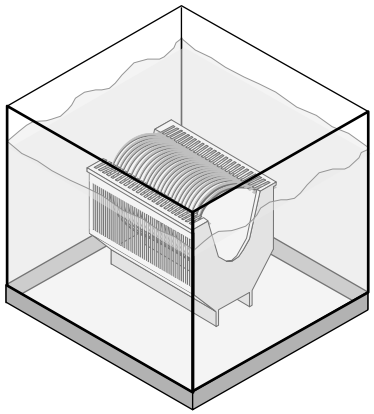
- Maintenance of the furnace and associated equipment (especially quartz components) for cleanliness
- Purity of processing chemicals
- Purity of oxidizing ambient (the source of oxygen in the furnace)
- Wafer cleaning and handling practices

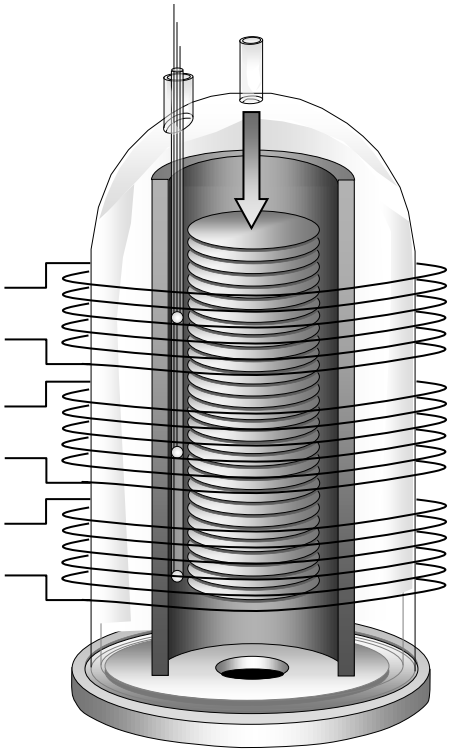
Thermal Oxidation Process Flow Chart

Wet Clean
- Chemicals
- % solution
- Temperature
- Time

Oxidation Furnace
- O_2, H_2 , N_2 , Cl
- Flow rate
- Exhaust
- Temperature
- Temperature profile
- Time

Inspection
- Film thickness
- Uniformity
- Particles
- Defects





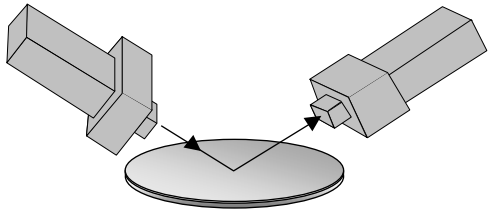


Figure 10.23

Process Recipe for Dry Oxidation Process

Step	Time (min)	Temp (°C)	N_2 Purge Gas (slm)	Process Gas N_2 (slm)	O_2 (slm)	HCl (sccm)	Comments
0		850	8.0	0	0	0	Idle condition
1	5	850		8.0	0	0	Load furnace tube
2	7.5	Ramp 20°C/min		8.0	0	0	Ramp temperature up
3	5	1000		8.0	0	0	Temperature stabilization
4	30	1000		0	2.5	67	Dry oxidation
5	30	1000		8.0	0	0	Anneal
6	30	Ramp -5°C/min		8.0	0	0	Ramp temperature down
7	5	850		8.0	0	0	Unload furnace tube
8		850	8.0	0	0	0	Idle

Note: gas flow units are slm (standard liters per minute) and sccm (standard cubic centimeters per minute)

Table 10.6

Wafer Loading Pattern in Vertical Furnace

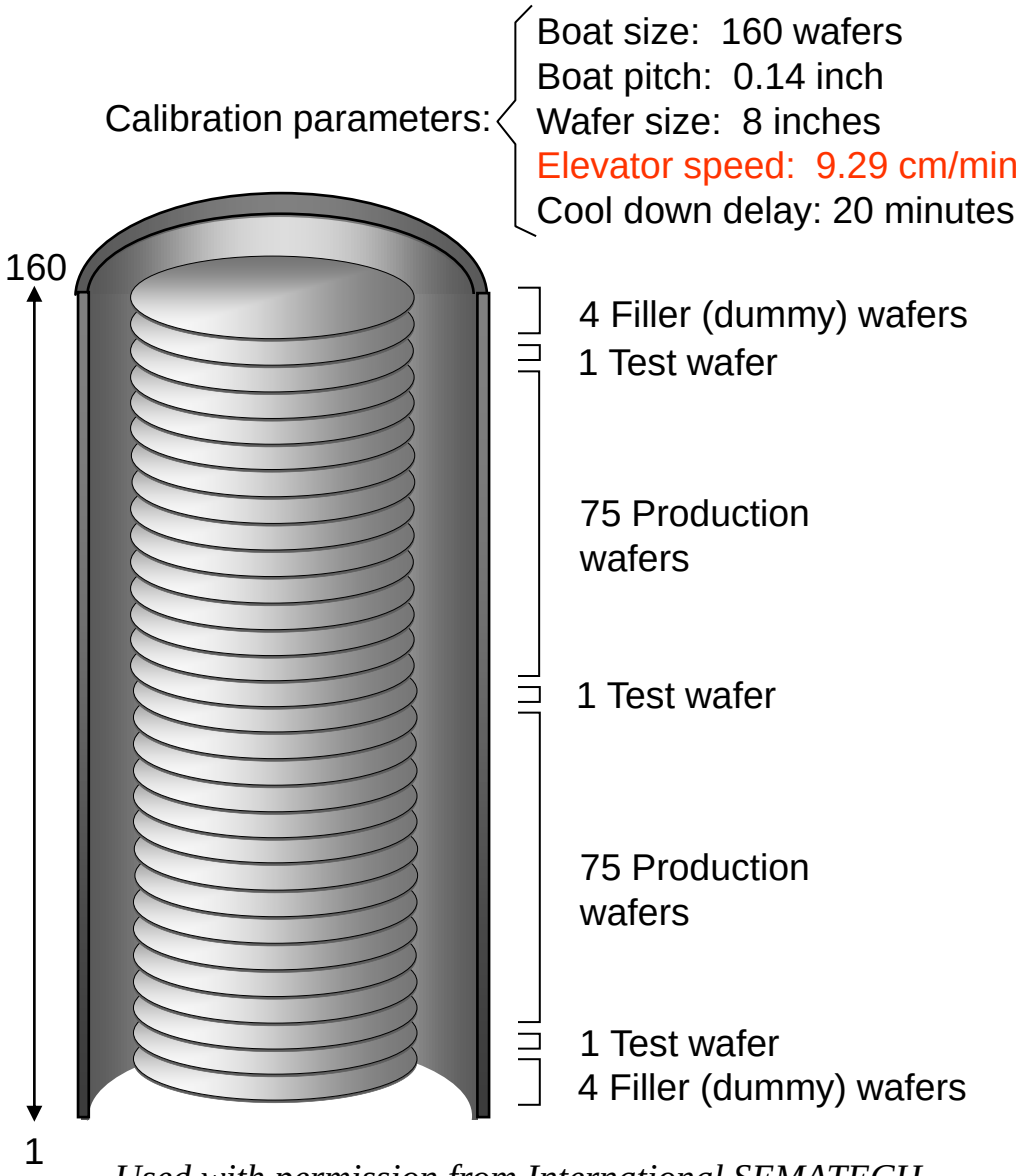


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Figure 10.24