1M ×4Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM44C1000C/CL/CSL-5	50ns	13ns	90ns
KM44C1000C/CL/CSL-6	60ns	15ns	110ns
KM44C1000C/CL/CSL-7	70ns	20ns	130ns
KM44C1000C/CL/CSL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and hidden refresh capability**
- **Fast parallel test mode capability**
- **TTL compatible inputs and outputs**
- **Early Write or output enable controlled write**
- **Single + 5V ±10% power supply**
- **Refresh Cycle**
  - **1024 cycle/16ms (Normal)**
  - **1024 cycle/128ms (L-version)**
  - **1024 cycle/256ms (SL-version)**
- **Power Dissipation**
  - **Standby: 5.5mW (Normal)**
    1.1mW (L-Ver.)
    0.55mW (SL-Ver.)
  - **Active (50/60/70/80): 470/415/360/305mW**
- **JEDEC standard pinout**
- **Available in plastic DIP,SOJ, ZIP and TSOP -II packages**

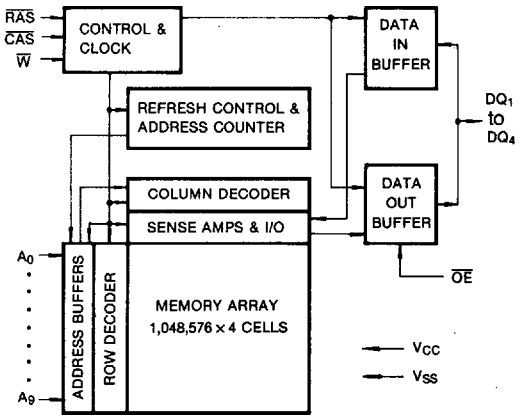
GENERAL DESCRIPTION

The Samsung KM44C1000C/CL/CSL is a high speed CMOS 1,048,576 × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM44C1000C/CL/CSL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alterntive to $\overline{RAS}$-only Refresh. All inputs and outputs are fully TTL compatible.

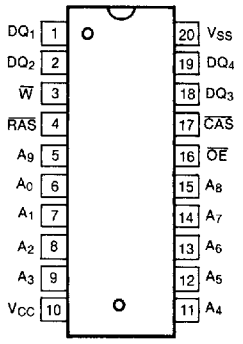
The KM44C1000C/CL/CSL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

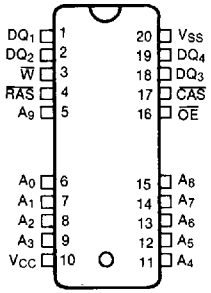


PIN CONFIGURATION (Top Views)

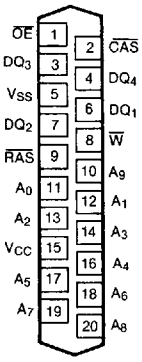
• KM44C1000CP/CLP/CSLP



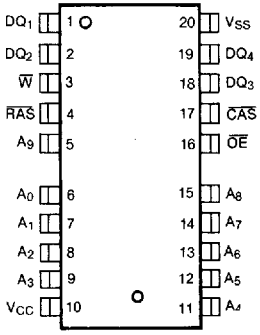
• KM44C1000CJ/CLJ/CSLJ



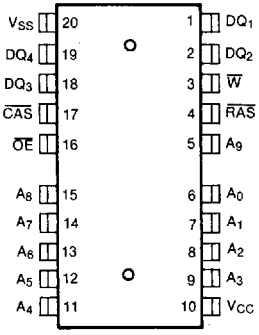
• KM44C1000CZ/CLZ/CSLZ



• KM44C1000CT/CLT/CSLT



• KM44C1000CTR/CLTR/CSLTR



Pin Names	Pin Function
A_0-A_9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
DQ_1~DQ_4	Data In/Data Out
V_{CC}	Power (+5V)
V_{SS}	Ground

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SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Units
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	℃
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	−	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	−	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C1000C/CL/CSL-5	I_{CC1}	-	85	mA
	KM44C1000C/CL/CSL-6		-	75	mA
	KM44C1000C/CL/CSL-7		-	65	mA
	KM44C1000C/CL/CSL-8		-	55	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})		I_{CC2}	-	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM44C1000C/CL/CSL-5	I_{CC3}	-	85	mA
	KM44C1000C/CL/CSL-6		-	75	mA
	KM44C1000C/CL/CSL-7		-	65	mA
	KM44C1000C/CL/CSL-8		-	55	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM44C1000C/CL/CSL-5	I_{CC4}	-	65	mA
	KM44C1000C/CL/CSL-6		-	55	mA
	KM44C1000C/CL/CSL-7		-	45	mA
	KM44C1000C/CL/CSL-8		-	35	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC} -0.2V)	KM44C1000C	I_{CC5}	-	1	mA
	KM44C1000CL		-	200	μA
	KM44C1000CSL		-	100	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C1000C/CL/CSL-5	I_{CC6}	-	85	mA
	KM44C1000C/CL/CSL-6		-	75	mA
	KM44C1000C/CL/CSL-7		-	65	mA
	KM44C1000C/CL/CSL-8		-	55	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V DQ_{1-4}=Don't Care, t_{RC}=125μs(L-Ver.) t_{RC}=250μs(SL-Ver.), t_{RAS}=t_{RAS} min~300ns	KM44C1000CL	I_{CC7}	-	300	μA
	KM44C1000CSL		-	150	μA

DC AND OPERATING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 < V_{IN} < V_{CC}+0.5V$ all other pins not under test=0 volts.)	$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

* Note: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. I_{CC4}, Address can be changed maximum once during a fast page Mode cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	–	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	–	7	pF
Output Capacitance (DQ_1-DQ_4)	C_{DQ}	–	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	133		155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	13	0	15	0	20	0	20	ns	7
Transition time(rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10,000	15	10,000	20	10,000	20	10.000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold time	t_{CAH}	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	40		45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		35		40		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		20		ns	
Data-in-set-up time	tDS	0		0		0		0		ns	10
Data-in hold time	tDH	10		10		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	6
Refresh period (Normal)	tREF		16		16		16		16	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
Refresh period (SL-ver)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		110		ns	8
Column address to $\overline{W}$ delay time	tAWD	48		55		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Fast page mode cycle time	tPC	35		40		45		50		ns	
Fast page mode read-modify-write cycle time	tPRWC	76		85		100		105		ns	
$\overline{RAS}$ pulse width(Fast Page Mode)	tRASP	50	200,000	60	200,000	70	200,000	80	200,000	ns	
$\overline{CAS}$ precharge time(Fast page mode)	tCP	10		10		10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	0	13	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Write command hold time (test mode in)	tWTH	10		10		10		10		ns	
Write command gold time (test mode in)	tWPH	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ rcycle)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ rcycle)	tWRH	10		10		10		10		ns	

TEST MODE CYCLE

(Note. 12)

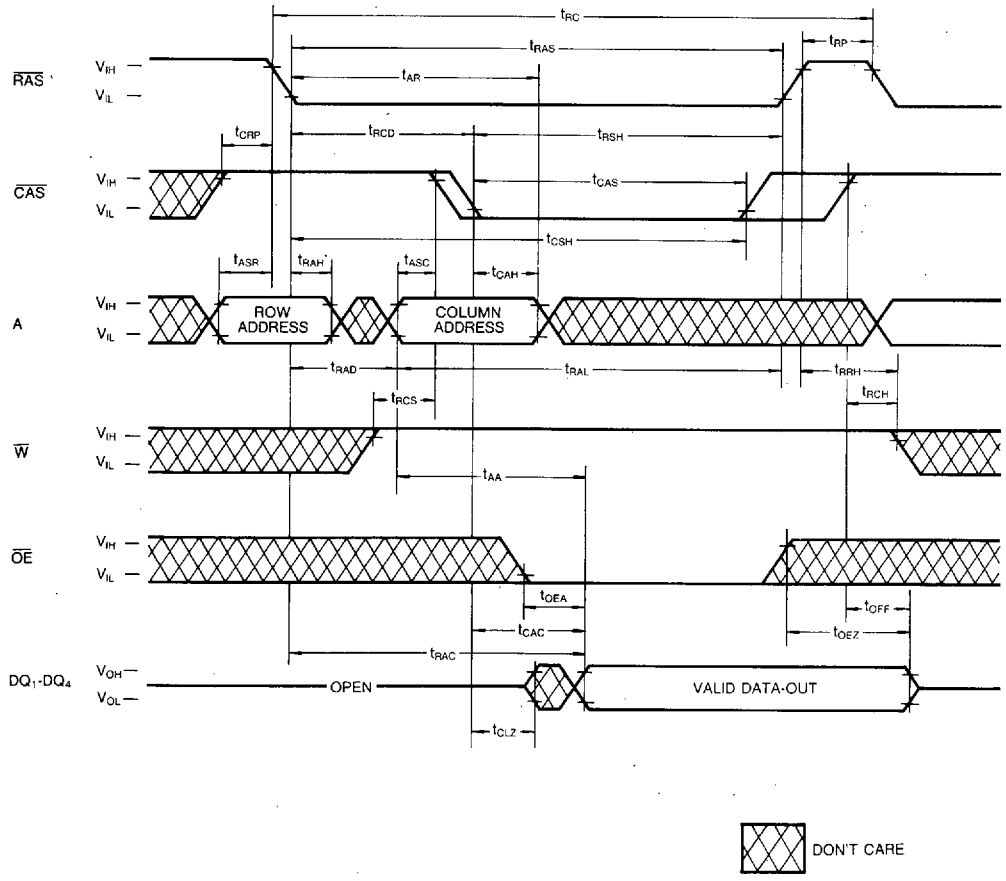
Parameter	Symbol	-5		-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	95		115		135		155		ns	
Read-modify-write cycle time	t_{RWC}	138		160		190		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		55		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		18		20		25		25	ns	3,4,5
Access time from column address	t_{AA}		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		25		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		45		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	41		45		55		55		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	78		90		105		115		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	53		60		70		75		ns	8
Fast mode cycle time	t_{PC}	40		45		50		55		ns	
Fast page mode read-modefy-write	t_{PRWC}	81		85		100		105		ns	
$\overline{RAS}$ pulse width(Fast page mode)	t_{RASP}	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45		50	ns	3
$\overline{OE}$ access time	t_{OEA}		20		20		25		25	ns	
$\overline{OE}$ to data delay	t_{OED}	18		20		25		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	18		20		25		25		ns	

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only Refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If $t_{RCD(max)}$ is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-modify-write cycle and the data our will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF(max)}$ and $t_{OEZ(max)}$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

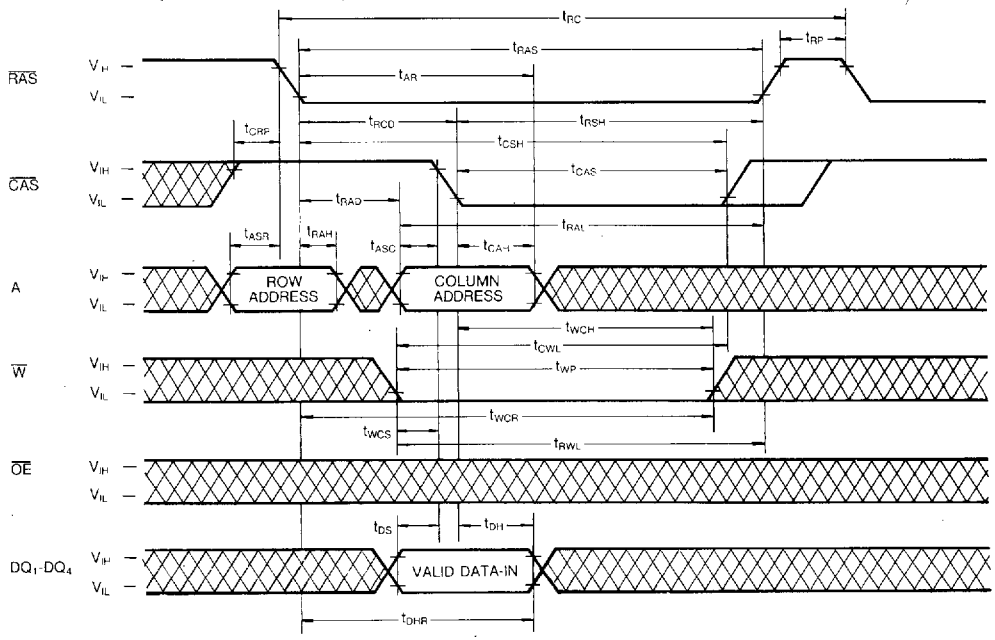
TIMING DIAGRAMS

READ CYCLE

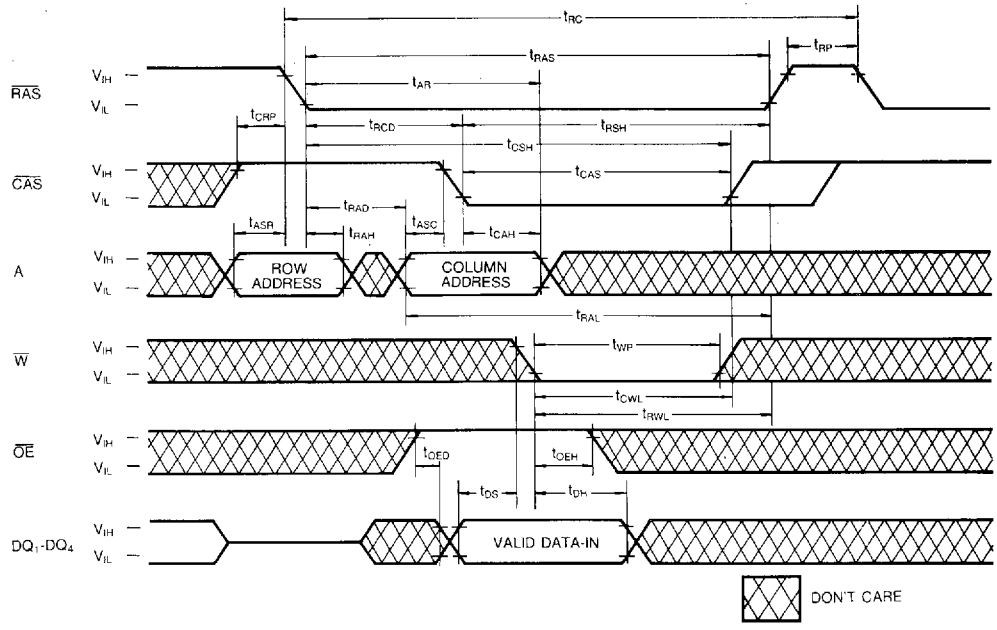


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)



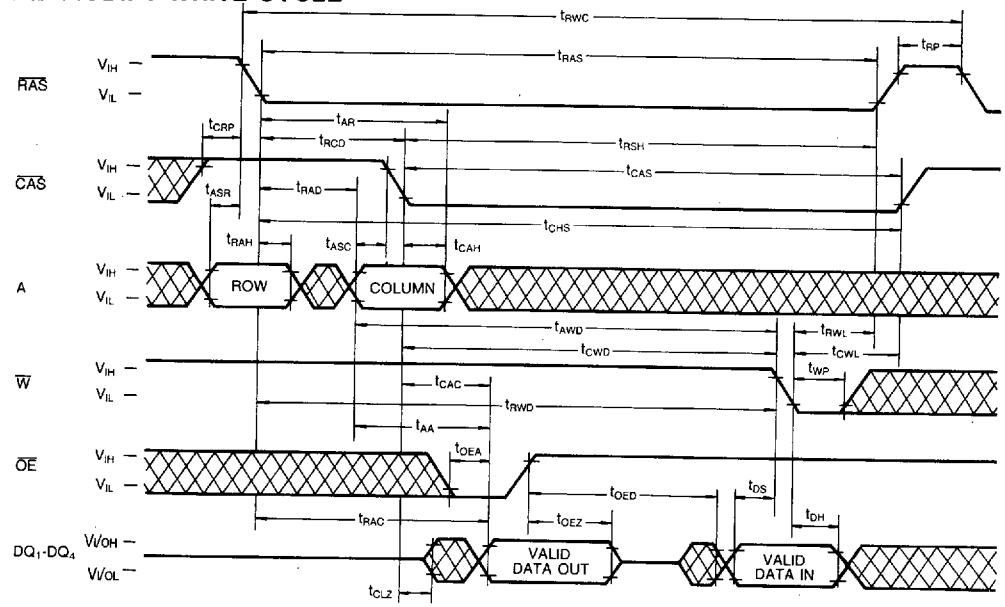
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



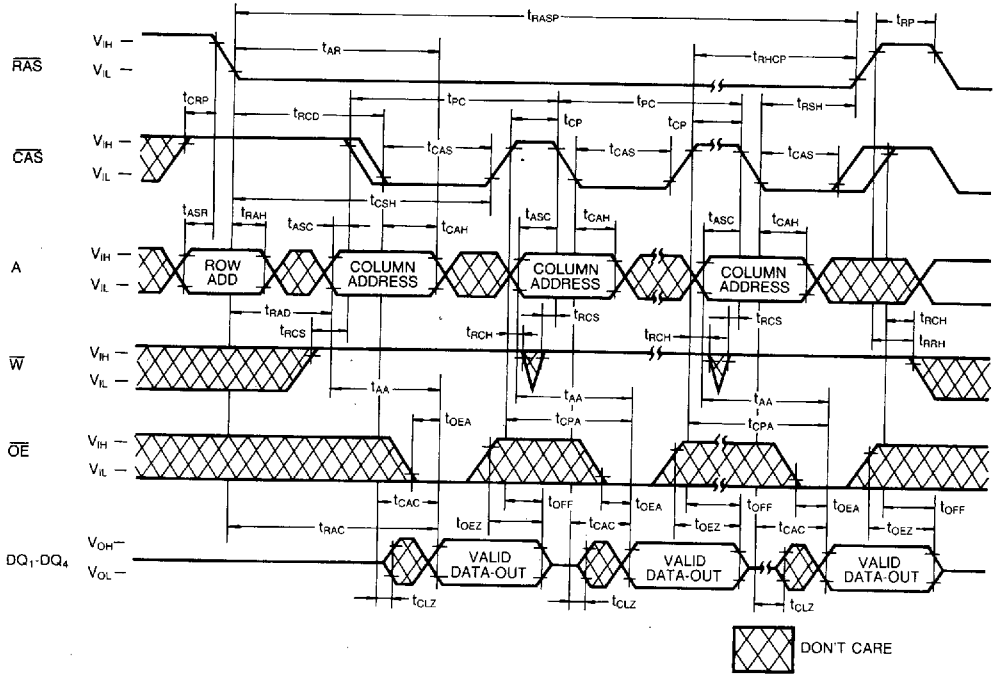
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



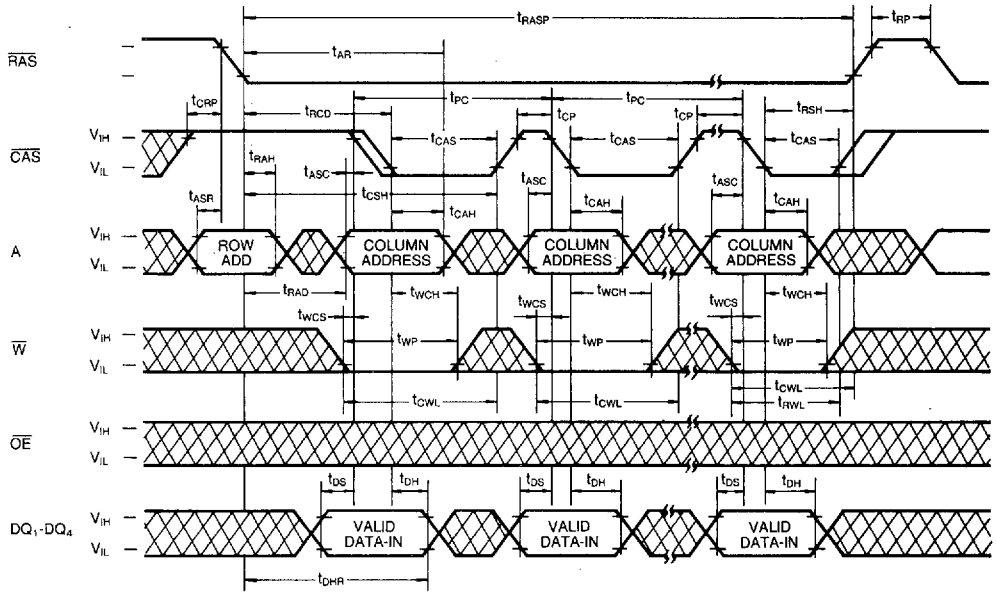
FAST PAGE MODE READ CYCLE



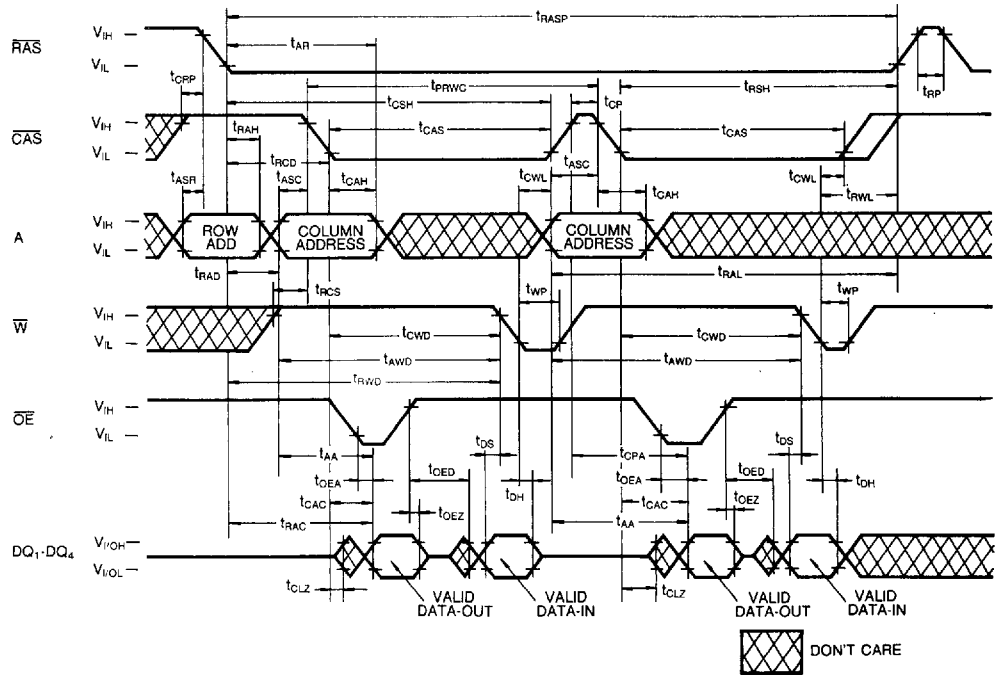
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

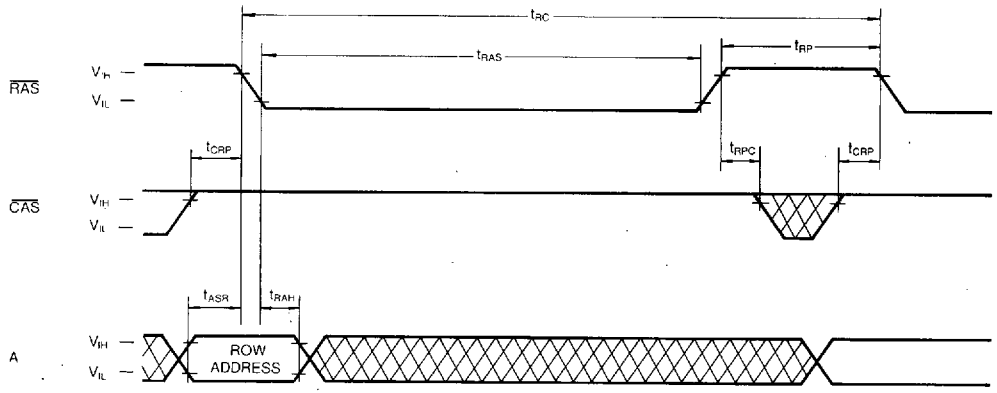


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

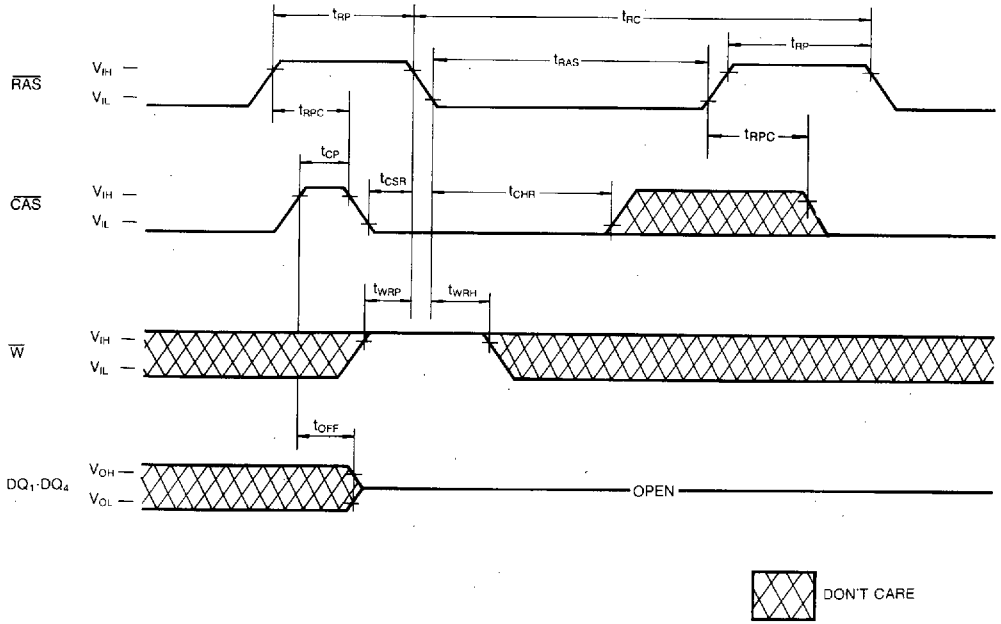
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$=Don't Care



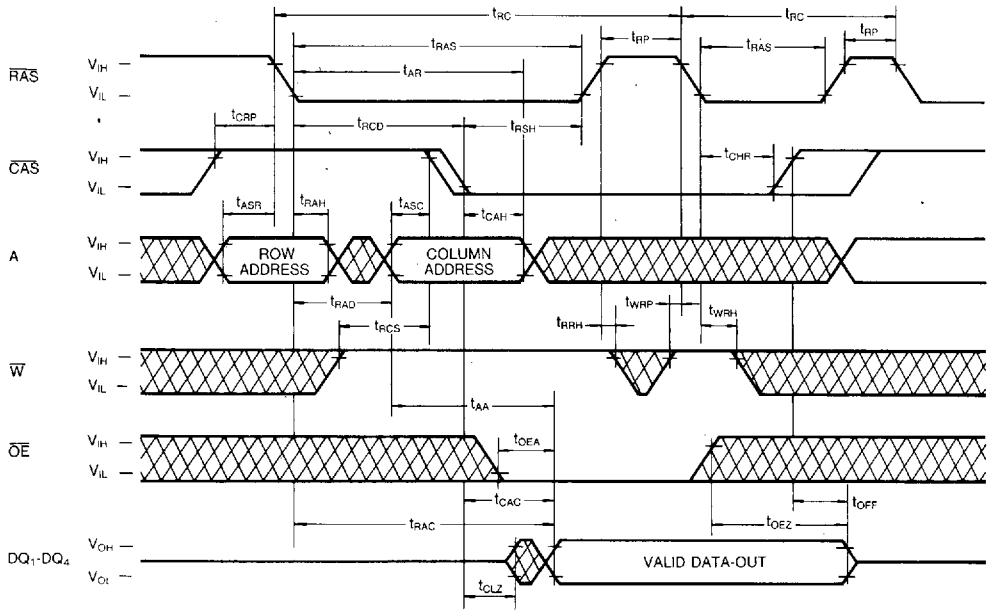
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

Note: $\overline{OE}$, Address=Don't Care

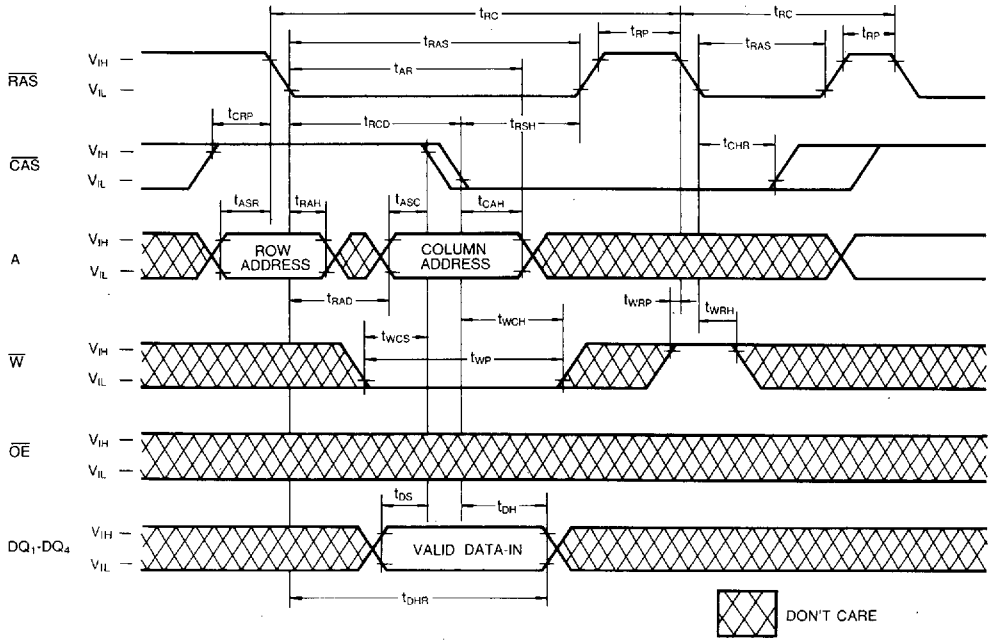


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

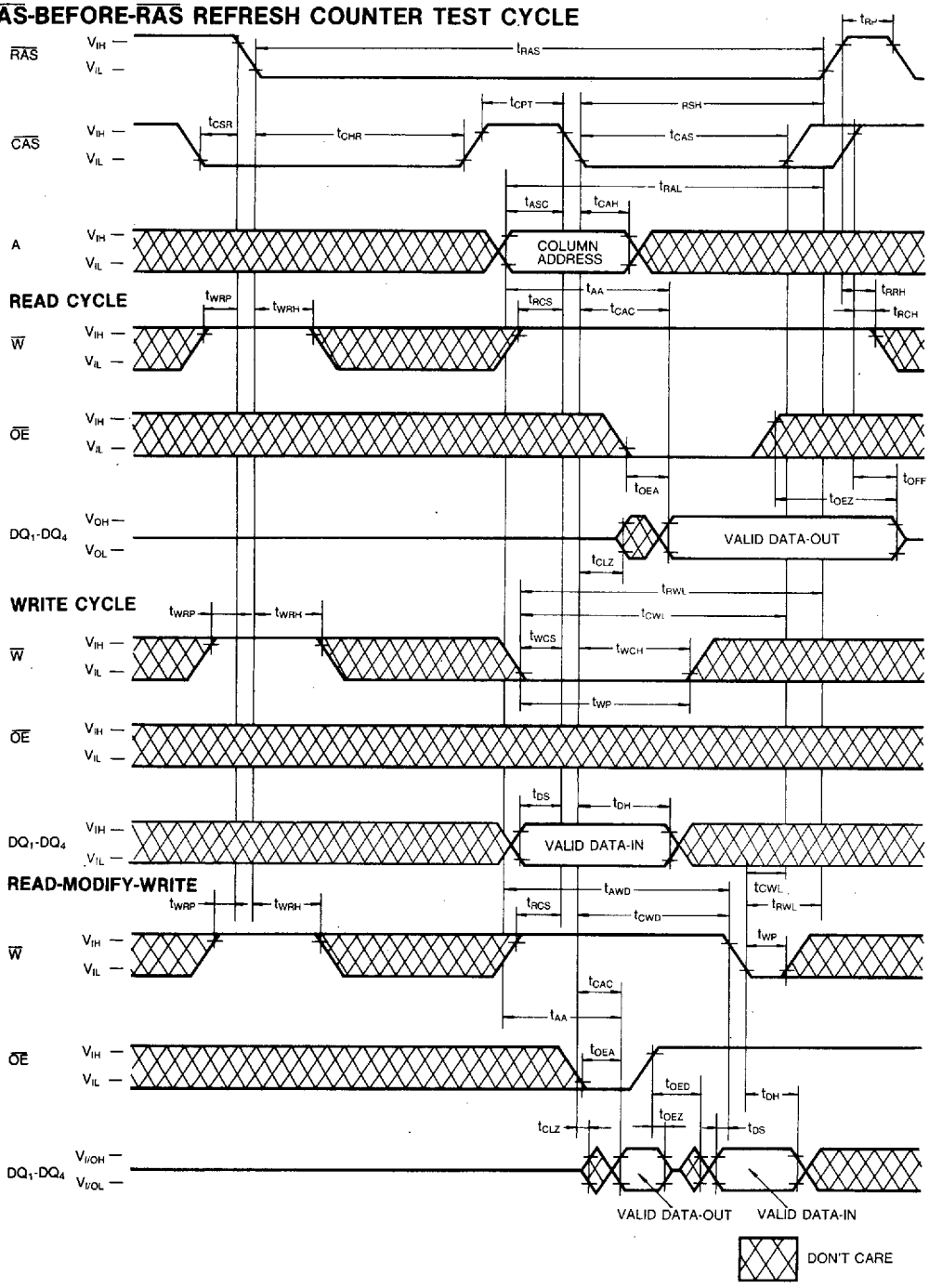


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

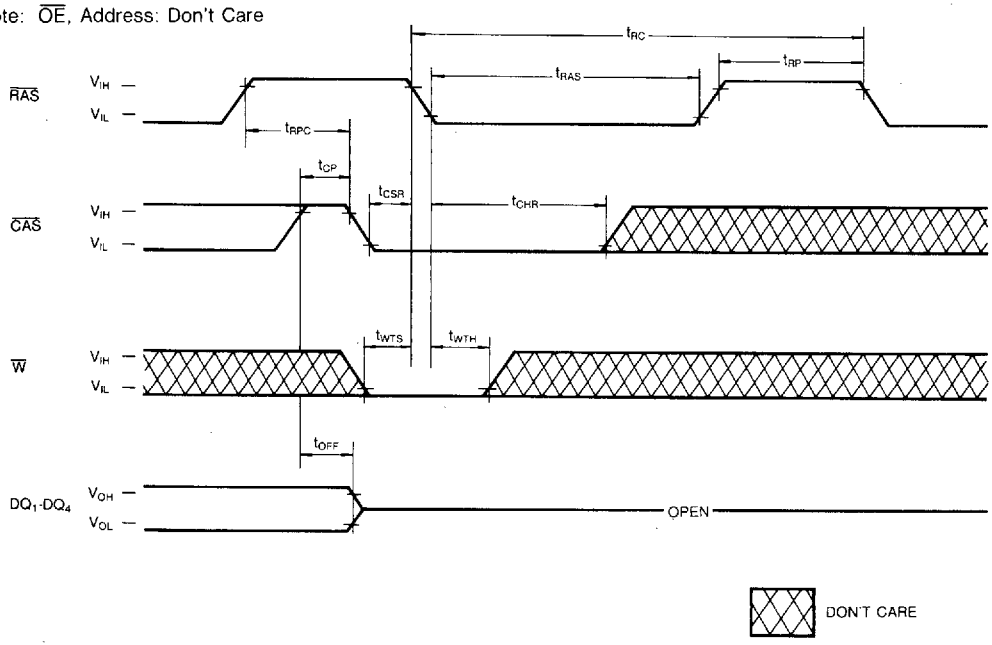


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: $\overline{OE}$, Address: Don't Care



TEST MODE DESCRIPTION

The KM44C1000C/CL/CSL is the RAM organized 1, 048,576 words by 4 bit internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A_0 is not used. If, upon reading, two bits on one I/O pin are equal (all "1" or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 1M x 4 DRAM can be tested as if it were a 512K x 4DRAM. $\overline{W}$, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode", And "$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE" or "$\overline{RAS}$-only-Refresh Cycle" puts it back into "Normal Mode". During the test mode operation, a WCBR cycle is used to perform refresh. The "Test Mode" function reduces test time(1/2 in cases of N test pattern.)

DEVICE OPERATION

The KM44C1000C/CL/CSL contains 4,194,304 memory locations. Twenty address bit are required to address a particular 4-bit word in the memory array. Since the KM44C1000C/CL/CSL has only 10 address input pins, time multiplexed addressing is used to input 10 row (A_0-A_9) and 10 column (A_0-A_9) address. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column adress strobe($\overline{CAS}$), and the valid row and column address inputs.

Operating of the KM44C1000C/CL/CSL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins (A_0-A_9) is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM44C1000C/CL/CSL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C1000C/CL/CSL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid befor t_{RCD}(max), the access time to valid data is specified by t_{RAC}(min). However if $\overline{CAS}$ goes low after t_{RCD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC} (min), it is necessary to meet both t_{RCD}(max) and t_{RAD} (max). The KM44C1000C/CL/CSL has common data I/O pins

The this reason an output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the output, $\overline{OE}$ must be low for the period of time defined by t_{OEA} and t_{OEZ}.

Write

The KM44C1000C/CL/CSL can perform eary write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the three state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing W low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur, The late write cycle is very simiar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterninate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM44C1000C/CL/CSL has a three-state output buffer which is controlled by $\overline{CAS}$ and $\overline{OE}$. Whenever $\overline{CAS}$ and $\overline{OE}$ are high(V_{IH}), the outputs are in the high impedance state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output untill $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C1000C/CL/CSL operating cycles is listed below after the corresponding output state produced by the cycle.

DEVICE OPERATION (Continued)

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{OE}$ controlled write.

Indeterminate Output State: Delayed Write(t_{CWD} or t_{RWD} are not met)

Refresh

The data in the KM44C1000C/CL/CSL is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16/128/256ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM44C1000C/CL/CSL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is vheld low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM44C1000C/CL/CSL hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C1000C/CL/CSL by using read, write or read-modify write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order.

A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time requried to set up and strobe sequential row addresses for the same page

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, is $\overline{CAS}$ goes high and then low again while RAS is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell be addressed with 10 row address bits and 10 column address bits defined as follows

Row Address- Bits A_0 through A_9 are supplied by the on-chip refresh counter.

Column Address-Bits A_0 through A_9 are supplied by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row address (The row addresses are supplied by the on-chip refresh counter)
3. Using read-modify-write cycle, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

If $\overline{RAS}$=V_{SS} during power-up, the KM44C1000C/CL/CSL cold possibly begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current. An initial pause of 200 μsec is required after

DEVICE OPERATION (Continued)

power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 16(L-ver:128, SL-ver:256) msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM44C1000C/CL/CSL inputs act like unteminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terrminate the input lines and to keep them as short as possible. Although eiter series or parallel temination may be used,series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44C1000C/CL/CSL input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is importnat to lay out the power and ground lines on memory boards in such a way that switching transinent effects are mimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS.

The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the Vcc line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the Vcc to Vss voltage (measured at the device pins) should not exceed 500mV

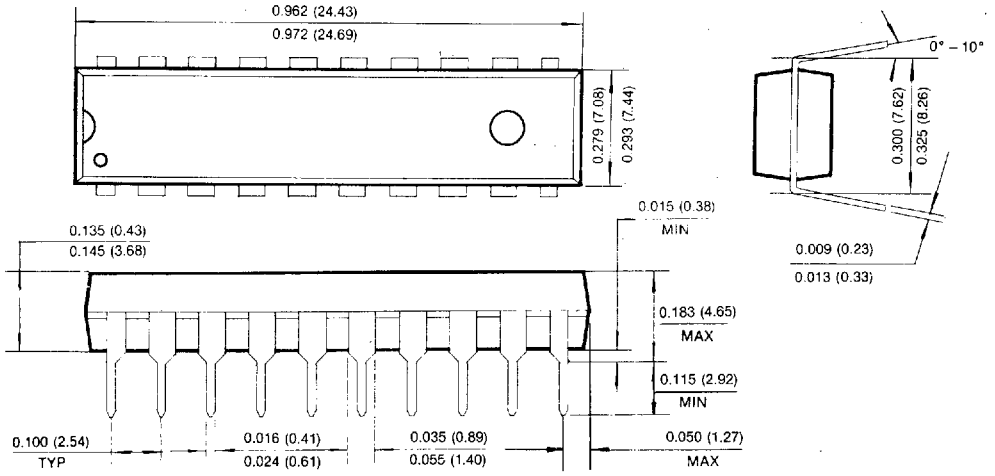
A high frequency 0.1 μF ceramic decoupling capacitor should be connected between the Vcc and ground pins of each KM44C1000C/CL/CSL using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44C1000C/CL/CSL and they supply much of the current used by the KM44C1000C/CL/CSL during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

Units: Inches (Millimeters)

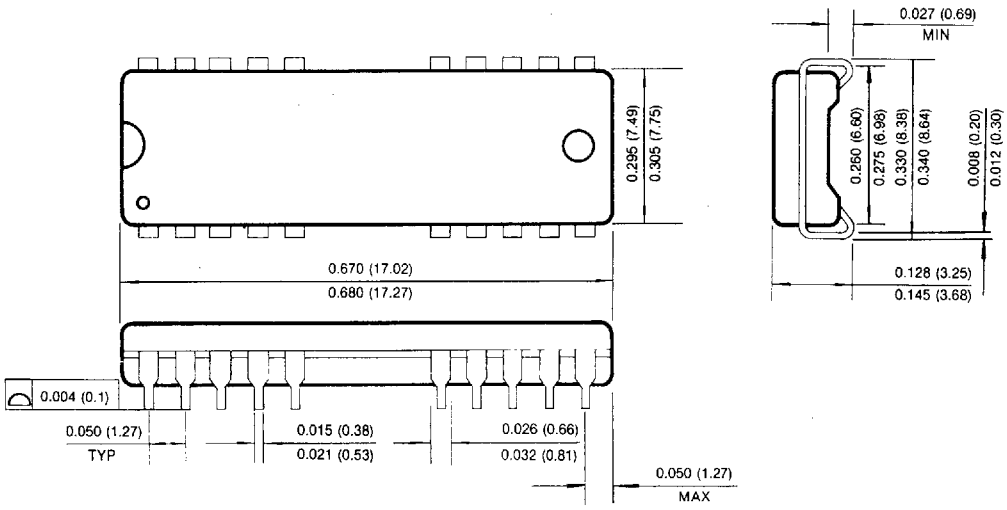
20-LEAD PLASTIC DUAL IN-LINE PACKAGE



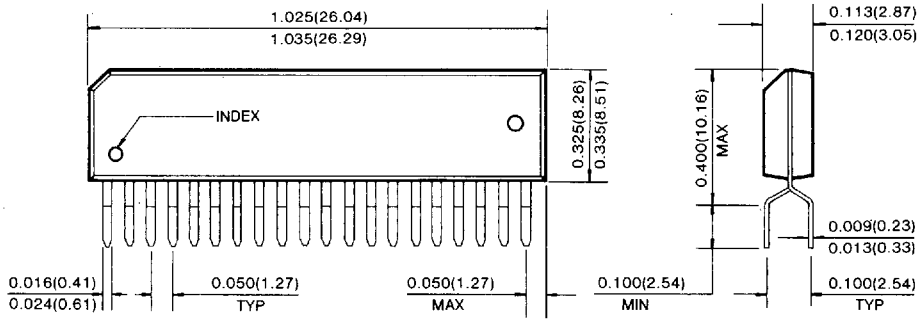
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



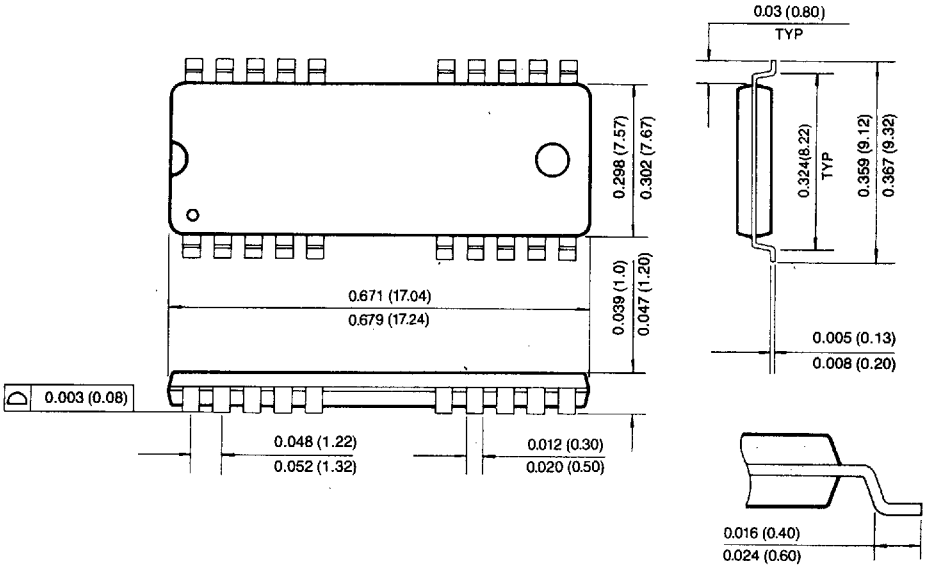
20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)



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